chapter 6

SERIAL, IR SERIAL, PARALLEL, AND USB INTERFACES

Serial Interface

The serial interface in the SMC FDC37C95x FR Ultra I/O (MSIO) is equipped with two Universal Asynchronous Receiver/Transmitter (UART) controllers functionally equivalent to the 16550A. UART 1 may be I/O-mapped to addresses 3F8h..3FFh (COM1), 2F8h..2FFh (COM2), 3E8h..3EFh (COM3), or 2E8h ..2EFh (COM4) through the setup utilities. The UART input, output, and handshake pins are connected to the serial connector through a MAX213 RS232 transceiver. A detailed description of the device registers follows.

Device Registers

The following is a detailed description of the serial interface device registers. Note that the first two I/O addresses have different registers and bit definitions depending on state of the line control register (base address + 3). The scratch pad register is a general purpose register used to store temporary data at the programmer's discretion.

Receiver Buffer/Transmitter Holding Register (Base Address)

This register contains the byte just received or the next byte to be transmitted by the serial controller.

Baud Rate Divisor Latch (Base Address)

This register is enabled when bit <7> of the line control register = 1. The serial controller contains a built-in baud rate generator that divides the input clock (1.8432 MHz) by a divisor to create a desired baud rate or serial transmission frequency.

The divisor is found according to the formula:

Divisor = 1843200 / (desired baud rate × 16)

Interrupt Enable (Base Address + 1)

The bits of this register enable up to four interrupt sources. The register format is described in the following chart.

Address. Offset = 1h, DLAB = 0, R/W

BIT	FUNCTION
7..4	Reserved
3	1 = Modem Status interrupt enabled
2	1 = Receiver Line Status interrupt enabled
1	1 = Transmitter Holding register empty, interrupt enabled
0	1 = Baud Rate Divisor interrupt enabled

Interrupt ID (Base Address + 2)

This register contains one bit that flags the serial controller as the source of the interrupt and three bits that specify the reason for the interrupt. The serial controller interrupts are prioritized and are listed below with the lowest-priority interrupt first. To clear the interrupt, read the contents of the register.

Address Offset = 2h, DLAB = 0, RO

BIT	FUNCTION
7,6	00 = FIFO disabled 11 = FIFO enabled
5,4	Reserved
3..1	000 = Modem Status (Clear to Send, Data Set Ready, Ring Indicator, or Carrier Detect) 001 = Transmitter Holding register empty 010 = Received Data Available 011 = Receiver Line Status register (Overrun Error, Parity Error Framing Error, or Break) 100 = Reserved 101 = Reserved 110 = Character timeout 111 = Reserved
0	0 = Interrupt is pending (this device sent interrupt)

FIFO Control Register (Base Address + 2)

This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level, and select DMA mode.

Address Offset = 2h, DLAB = x, WO

BIT	FUNCTION
7, 6	Sets the RCVR trigger level 00 = 1 byte 01 = 4 bytes 10 = 8 bytes 11 = 14 bytes
5, 4	Reserved
3	Reserved
2	0 = XMIT FIFO not reset 1 = Clears and resets the XMIT FIFO
1	0 = RCVR FIFO not reset 1 = Clears and resets the RCVR FIFO
0	0 = Disables and clears the FIFOs 1 = Enables both the XMIT and RCVR FIFOs

Line Control (Base Address + 3)

This register specifies the serial data transmission format.

Address Offset = 3h, DLAB = 0, R/W

BIT	FUNCTION
7	0 = Enable Receiver Buffer/Transmitter Holding registers and Interrupt Enable register Access 1 = Enable Divisor Latch Access to write Baud Rate Divisor
6	1 = Break control bit # forces SOUT signal low
5	1 = Stick Parity # with even parity enabled, the parity bit becomes logic 0; with odd parity enabled, the parity bit becomes logic 1.
4	0 = Odd Parity 1 = Even parity
3	1 = Parity bit enabled
2	0 = 1 Stop bit 1 = 2 Stop bits (1.5 for 5-bit words)
1, 0	00 = 5-bit word 01 = 6-bit word 10 = 7-bit word 11 = 8-bit word

Modem Control (Base Address + 4)

This register controls the modem interface lines.

Address Offset = 4h, DLAB = x, R/W

BIT	FUNCTION
7..5	Reserved
4	1 = Enable Internal Loopback (processor verification of Tx/Rx)
3	1 = Enable Serial Port Interrupts (Out2)
2	1 = Output 1 (Out1) control. R/W by CPU only
1	1 = RTS_ signal active
0	1 = DTR_ signal active

Line Status (Base Address + 5)

This register contains the status of the current data transfer. Bits <2..0> are cleared on a read of this port.

Address Offset = 5h, DLAB = x, R/W

BIT	FUNCTION
7	1 = At least one parity error, framing error, or break indication in the RCVR FIFO
6	1 = Transmitter Holding register and Transmitter Shift register are empty
5	1 = Transmitter Holding register is empty, ready for character
4	1 = When a Break Interrupt has occurred
3	1 = Framing Error
2	1 = Parity Error
1	1 = Overrun Error - data lost
0	1 = A character is in the Data register to be read

Modem Status (Base Address + 6)

This register contains the status of the interface lines.

Address Offset = 6h, DLAB = x, R/W

| BIT	FUNCTION
7	1 = DCD_ signal active
6	1 = RI_ signal active
5	1 = DSR_ signal active
4	1 = CTS_ signal active
3	1 = DCD_ has changed state since last read by the system
2	1 = RI_ has changed from a low to a high state since last read
1	1 = DSR_ has changed state since last read by the system
0	1 = CTS_ has changed state since last read by the system

Infrared Serial Interface

The infrared serial interface of the computer is composed of two parts. The first part is the Infrared Data Association (IrDA) compliant transceiver module. This module meets the IrDA specifications[1] for Fast IR (4-MB) communication with infrared (IR) driven devices. The transceiver is designed to operate from a distance of from 1 cm to 1 m between the computer and the external IR device. The IR communication data rate can be as high as 4 Mb/s at viewing angles up to 15 degrees.

The transceiver module consists of a high-speed IR photo diode receiver and an IR LED transmitter. The input and output of this module are connected directly to the output and input pins of the MSIO Super I/O device. The choice of input and output pins may be selected through the SCE Configuration Register A, bit <7>.

The second part of the IR interface is the second UART in the MSIO Super I/O device. This section of the device is fully compliant to the IrDA Version 1.1 specification. IrDA-SIRA, IrDA-SIRB, IrDA-HDLC and IrDA-FIR modes at up to 4 Mb/s are supported. The Infrared Communications Controller (IrCC) also provides support for ASK-IR, Consumer (TV remote) IR, and RAW-IR.

The host controller has direct access to the IR bit stream from/to the transceiver in RAW mode. The IrCC block is a superset of UART2, comprising a UART2 Asynchronous Communications Engine (ACE) and a separate Synchronous Communications Engine. These provide the full set of IR modes, as well as the standard UART COM mode. This device is more fully described in the IrCC Specification referenced in Chapter 1, "Introduction.". This document is available from the SMC Web site, http:\\www.smc.com.

Figure 6-1 is a block diagram of the infrared serial interface.
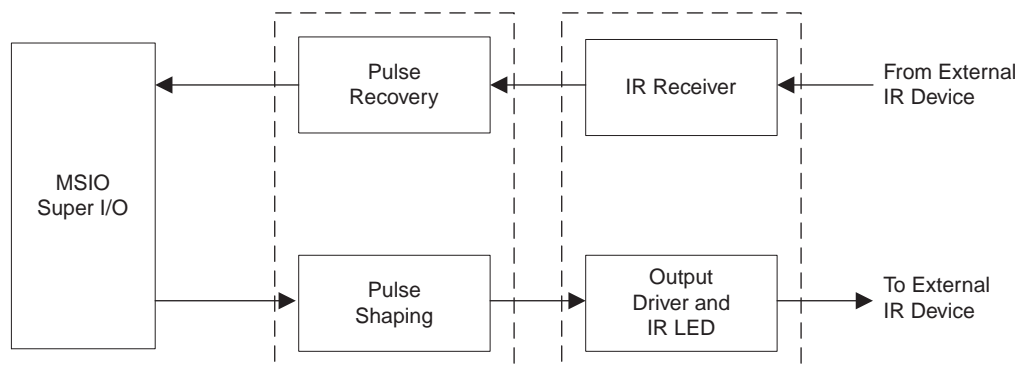
Figure 6-1. Infrared Serial Interface, Block Diagram

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[1] IrDA 4MB compliant. IR performance may vary depending on performance of IR peripherals, distance between IR devices, and applications used.

IR Registers

Configuration Registers Overview

To support the IrCC, four configuration registers are added to UART2. These registers consist of the Fast IR Base I/O address registers (0x62h and 0x63h), an IrCC DMA channel select register (0x74h), and an IR Half Duplex timeout register (0xF2h).

Base I/O Addresses

Asynchronous Communications Engine (UART) Registers

Register Index	Base I/O Range	Fixed Base Offsets
0x60h, 0x61h (0x60h = MSB 0x61h = LSB of UART 16 bit Base address)	0x100h : 0xFF8h On 8 byte boundaries	+0 : RR/TB | LSB divisor +1 : IER | MSB divisor +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR

Fast IR/USRT

Synchronous Communications (SCE) Registers

Register Index	Base I/O Range	Fixed Register Base Offset
0x62h, 0x63h (0x62h = MSB 0x63h = LSB of UART 16 bit Base address)	0x100h : 0xFF8h On 8 byte boundaries	+0 : Register Block N, Address 0 +1 : Register Block N, Address 0 +2 : Register Block N, Address 0 +3 : Register Block N, Address 0 +4 : Register Block N, Address 0 +5 : Register Block N, Address 0 +6 : Register Block N, Address 0 +7 : USRT Master Control Register

IR DMA Channels

DMA channel 0, 1, 2, or 3 may be selected for use with the IR logic through the configuration registers of logical device 5. The DMA channel for IR is routed from channel 2 on the MSIO to the General Purpose DRQ (GPDRQ) #4 on the Southbridge. BIOS maps this register during POST to DMA channel 5, as seen in Device Manager.

IR IRQ

The interrupt IRQ for the IR logic is selectable through the configuration registers for logical device 5. Refer to the SMC publications referenced in Chapter 1, "Additional Information Sources," of this document.

Parallel Interface

The parallel port interface is integrated in the MSIO Super I/O device. The parallel port supports three standard modes of operation: standard parallel port (SPP), enhanced parallel port (EPP), and extended capabilities port (ECP). The parallel port pins are accessible by the 8051, which allows the 8051 to perform flash recovery through this port.

Printer functions are controlled by writing to, or reading from I/O ports. The printer access I/O ports are given in Table 6-1.

Table 6-1
Parallel Port I/O Addresses

Primary Port	Secondary Port	Read/Write	Function
378h	278h	R/W	Printer data register
379h	279h	R	Printer status register
37Ah	27Ah	R/W	Printer control register
37Bh	27Bh	Reserved	

Standard Parallel Port

The SPP is fully compatible with ISA, EISA, and Micro Channel parallel ports. The parallel port uses a software based protocol and can transfer data up to 150 Kb/s.

A write operation causes data to be sent to pins PD [0:7]. With the extended SPP mode, a write operation to the data register causes data to be latched in the data register. If the data port direction bit CTR <5> is 0, the latched data is also sent to pins PD [0:7]. Otherwise, the data is only latched.

In a read operation of the data register, the register contains the last data written to it by the CPU. With the extended SPP mode, when the CTR <5> is 0, a read operation from the data register allows the CPU to read the last data it wrote to the port. When CTR <5> is 1, a read operation to the data register causes the port to present the latched data on pins PD [0:7].

Enhanced Parallel Port

The EPP mode provides better parallel port throughput and allows the CPU to address the peripheral device registers directly. Faster data transfers are achieved by automatically generating the address and data strobes. The EPP mode uses 8 single byte registers with a base address of 278h or 378h.

The four EPP transfer operations are address write, address read, data write, and data read. An EPP transfer operation consists of a CPU read or write cycle (from or to an EPP register) and an EPP read or write cycle (from a peripheral device to an EPP register or from an EPP register to a peripheral device).

Extended Capabilities Port

The ECP mode is a hardware protocol that provides data transfer rates up to 2 MB/s. The ECP has DMA support and FIFO buffers for receive/transmit capability to reduce the load on the CPU. The FIFO buffers are 16 bytes each and can be configured for either transmit or receive. In addition, the FIFO buffers provide threshold interrupt for both directions.

The ECP is enabled when printer control register PCR <2> is 1. Once enabled, its mode is controlled through ECR[5:7]. The ECP has a total of 10 registers.

Registers

The parallel ports are controlled by several mapped registers: data, control, status, and configuration. The following paragraphs and charts describe the important registers in detail.

Data Register (378h, or 278h)

Each byte written to the data register (read or write) is latched into a loopback register and is output to the printer. The register contents can be read back (for test purposes). When the parallel port is in input mode, data is read from this register.

Status Register (379h, or 279h Read Only)

This register contains the current printer status. Reading this register clears the interrupt condition from the parallel port.

BIT	FUNCTION
7	0 = Printer busy
6	0 = Printer acknowledges correct receipt of data byte
5	1 = Out of paper
4	1 = Printer selected (on line)
3	0 = Printer error
2	Reserved
1	Reserved
0	1 = In EPP mode, time-out occurred in EPP cycle

Control Register (37Ah or 27Ah)

This register provides the printer control functions described below.

BIT	FUNCTION
7,6	Reserved
5	Direction control in PS/2 and ECP modes 1 = Tristates drivers on data lines and data is read from peripheral. 0 = Drivers enabled, Port writes to peripheral (Default)
4	Acknowledge Interrupt Enable 1 = Enables an interrupt on the rising edge of nACK 0 = Disables the nACK interrupt (Default)
3	0 = Printer select
2	1 = Initialize
1	0 = Auto line feed
0	0 = Strobe