chapter **8**

GRAPHICS/VIDEO SUBSYSTEM

The standard graphics subsystem consists of a graphics controller, frame buffer memory, and a Liquid Crystal Display (LCD). The graphics/video subsystem can alternately drive an external Compaq VGA monitor by switching between the internal display and the external VGA monitor.

Multimedia capabilities are provided by Motion Video Acceleration (MVA) for playback of video data. The Zoomed Video (ZV) port provides video capabilities through optional PC Card multimedia hardware decoder cards (MPEG or Video Capture) for full-screen, full-motion viewing of TV/VCR video files stored in hard disk or CD-ROM drives. Stored video clips can also be displayed without hardware decoders through the preinstalled Mediamatics MPEG decoder software.

NOTE: This chapter describes general subsystem architecture, focusing largely on aspects unique to this system's graphics and video subsystem. For detailed information regarding BIOS and register programming for standard VGA modes, refer to the *Compaq QVision Video Graphics System Technical Reference Guide* P/N 073A/0693.

For detailed information regarding components used in this subsystem refer to the particular component's data sheet.

Subsystem Overview

A general block diagram of the graphics/video subsystem is shown in Figure 8-1 and described in the following paragraphs.

Master Clock—Provides dot clock source at a frequency specified by the Miscellaneous Output Register. An external clock may be substituted through the video feature connector. In QVision modes a separate clock is generated for memory for optimum performance.

Graphics/Video ASIC—The Chips 69000™ graphics/video component provides most of the graphics/video subsystem's functionality. The video BIOS code is contained within the 48-KB system BIOS ROM, video drivers are supplied with the system.

Frame Buffer—2-MB SDRAM imbedded inside graphics controller (C & T 69000).

ZV Port—Provides direct connection between the VGA controller and external PC Card host adapter. The ZV port allows the PC Cards that are plugged into the host adapter to write video data directly into the video frame buffer.

CRT Monitor I. D. (DDC-2) —Provides a standard for the CPU to determine the type of VGA monitor that is connected to the system. DDC-2 is unidirectional and only allows reading of monitor information.
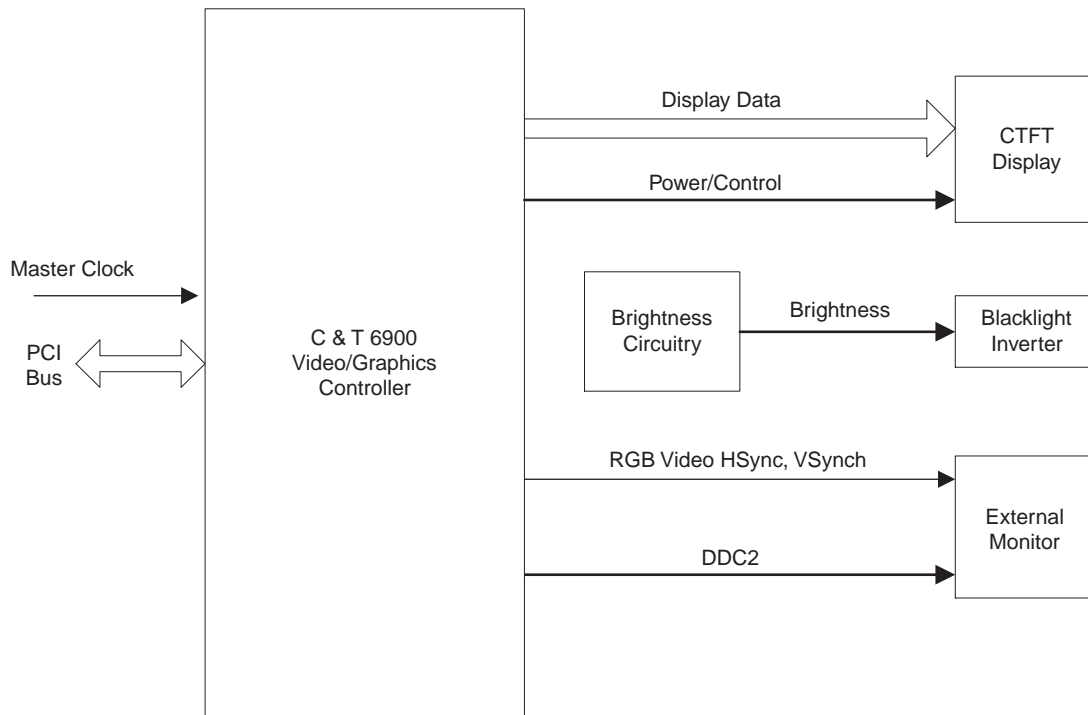

Figure 8-1. Graphics/Video Subsystem, Block Diagram

Graphics ASIC

The Chips 69000™ graphics ASIC contains most of the functionality the graphics/video subsystem. The CHIPS 69000™ graphics ASIC features a Motion Video Accelerator (MVA) that provides hardware support of video decompression and a ZV port. Other features include imbedded 2-MB SDRAM support, multi-format frame buffering, YCrCb-to-RGB color space conversion, enhanced frame-rate buffering, and comprehensive resolution-compensation. The following paragraphs describe key functions of the 69000.

Local Bus Interface

The 69000 is configured for PCI local bus operation. Memory and I/O accesses utilize a 64-bit bandwidth at up to 33 MHz, including burst cycle support. The 69000 is register-level compatible with software applications written for standard VGA, EGA, and CGA operation. Extended VGA modes and special features are supported through the video BIOS and supplied drivers.

Table 8-1 lists the I/O addresses used in the graphics subsection.

Table 8-1
69000™ Video/Graphics Controller Registers

Address	Function
03B4h-03B5h	CRT Controller (monochrome)
03Bah	EGA Compatibility
03C0h-03C1h	Attribute Controller
03C2h	Miscellaneous Control (Write)/Input Status (Read)
03C3h	Controller Enable
03C4h-03C5h	Sequencer
03C6h-03C9h	VGA Color Palette
03Cah	Feature Control (Read)
03CCh	Miscellaneous Control Read)
03CEh-03CFh	Graphics Controller/Extended Mode Functions *
03D0h- 03D1h	Flat Panel Control
03D2h-3D3h	Multimedia Controller
03D4h-03D5h	CRT Controller (color)/Extended Mode Functions
03D6h-03D7h	Extended Mode Functions*
03D8h-03DBh	Compatibility
0E2.92h-0E2.93h	Contrast and Brightness (data R/W @ 0E3h)

* Extended Mode Functions use indexed addressing to access extended (super) VGA functions such as the BitBLT engine as well as LCD control and Motion Video Accelerator control functions. For detailed register descriptions refer to the data sheet for the Chips 69000™ video/graphics controller.

Memory Interface

The memory interface to the frame buffer handles the data transfers to and from the frame buffer in both text and graphics modes. This function provides formatting and manipulation operations that may be required of display data. The memory interface is also responsible for taking the output of the master clock and generating timing and control signals used by all other graphics subsystem functions.

Attribute Controller

The attribute controller processes the data from the frame buffer and provide text blinking, highlighting, underlining, and reverse. A 16-of-64 color palette is included for EGA compatibility.

BitBLT Engine

The Bit Block Transfer (BitBLT) engine is activated in S and/or extended VGA modes and provides hardware support for moving blocks of data from one area of the frame buffer to another with minimum CPU intervention. The BitBLT engine can also provide pattern fills, raster ops, and color expansion or transparency. These operations enhance the performance of graphics user interface (GUI) such as Windows that typically call for high-resolution packed-pixel graphics modes.

Screen-to-Screen BitBLT

This function copies a rectangular bitmap from one section of the frame buffer to another. The memory addresses are generated by the BitBLT engine without CPU intervention. The graphics subsystem is programmed with the bitmap width, height, source address, destination offset address, an increment/decrement selection for the copy direction, and the pitch between scan lines. The registers allow the flexibility to move non-byte aligned and overlapping blocks.
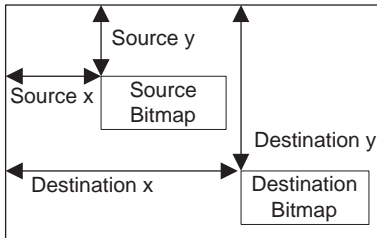

Figure 8-2. *Screen-to-Screen BitBLT*

CPU-To Screen BitBLT

This function facilitates the transfer of data from the microprocessor to the screen. Both planar (color-expand) and packed pixel views are supported. In planar modes, the data is transferred from the microprocessor as bytes, words, or dwords.

Pattern-to-Screen BitBLT

Pattern-to-Screen BitBLTs are useful for filling portions of the frame buffer with a repetitive pattern that may be as complex as a multi-color bitmap or as simple as a solid color. Simple patterns can be transferred to the screen in a single packed-pixel or color-expand BitBLT. More complex patterns may require multiple BitBLTs.

Color Expansion

Color expansion is the automatic conversion of a monochrome bitmap (which typically defines a character, icon, or pattern) into foreground and background values. These values are written to memory and also held in registers. Write performance of the CPU is improved by optimizing Host bus bandwidth since single bits are expanded across the bus into 8- or 16-bit pixels.

Cursor Engine

The cursor engine provides hardware support of the cursor indicator and replaces the need for software to continually save and restore cursor draw data as the pointing device position is changed. Once the software has initiated the cursor engine, only x-y data needs to be updated, allowing much smoother cursor operation. The cursor is overlaid on top of graphics and/or video information and can be either a 64 x 64 bit pattern (8 pattern choices) or a 32 x 32 bit pattern (with up to 32 pattern choices). Each pixel in the pattern can be transparent or one of two colors from the extended palette.

Video Playback

Full-screen video playback of software-decompressed DCI-compatible video clips (MPEG files) from a HDD/CD-ROM. Decoding and playback of MPEG video from files stored in the HDD or CD-ROM is provided through the CPU under Mediamatics software control without additional hardware decoders. Optional MPEG and Video Capture PC Card multimedia cards are also available to provide hardware decoding of video input signals.

RAMDAC

The RAMDAC contains the color palette (also known as the color look up table (CLUT)) that is used for color processing of the graphics data for some modes. An extended palette is also provided for color support for the cursor engine and border functions. The DAC portion provides the digital-to-analog conversion for an external color monitor. Color-processed data is also distributed to the LCD controller. The RAMDAC also provides the overlaying of motion video data.
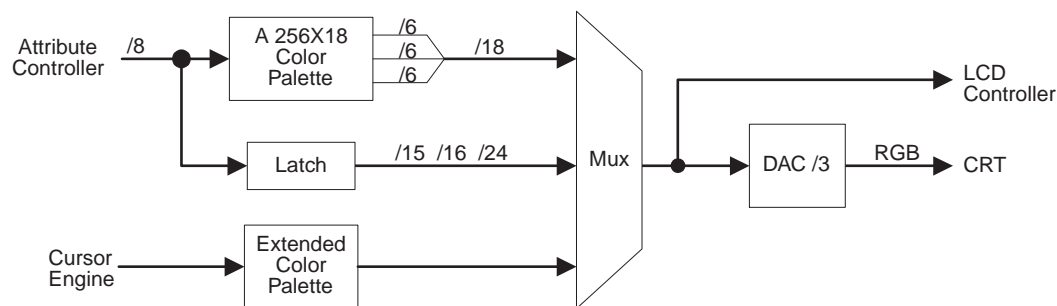

Figure 8-3. RAMDAC Block Diagram.

Color Processing With Palette

The color palette consists of a 256 x 18-bit color lookup table (CLUT) that provides three 6-bit values (an 18-bit word) to determine the hue from the primary colors of red, green, and blue. Using an 8-bit color code input, the CLUT can support a simultaneous display of up to 256 out of 262,144 ("256K") colors. For VGA modes using up to 256 colors at a time, the color palette provides very fast color processing.

Direct-/True-Color Processing

The color palette (CLUT) is bypassed in direct- and true-color VGA modes, which allow 32K, 64K, and 16 million colors to be displayed simultaneously. In these modes, pixel color data is received from the attribute controller, selected by the mux and applied to the DAC. More data is required from the frame buffer but of course more colors are available. Performance is maintained by using a higher video clock frequency in these modes.

Digital-To-Analog Converter

The DAC converts digital video data to three analog signals (Red, Green, and Blue) for routing to a CRT monitor. The output voltage is based on the .7 volt standard for a white pixel.

Dithering Engine

The dithering engine intermingles pixels of available colors together to produce a perceived color that is otherwise unavailable. This technique increases the number of colors in a given display mode relative to what the display is capable of without dithering. A pattern is used to add as many as six bits of resolution per primary color. Dithering can be applied to both the main graphics display as well as the motion video window. The amount of dithering can be set for automatic or can be programmed.

CRT Controller

The CRT controller generates horizontal and vertical blanking and synchronization signals required by an external CRT monitor. Simultaneous LCD/CRT display capability is possible depending on the display mode, the LCD panel type, and CRT type used.

LCD Controller

The LCD controller processes the video data for display on the LCD and provides power sequencer and screen save functions. A dithering engine uses a pattern and frame rate modulation to produce grey shades with a minimum of flicker on the LCD screen.

Power Management

The 69000 includes controls and features that support the system's power management functions to maximize battery life. The following subsections describe the Local Standby and Global Standby (Suspend) modes of the 69000 during the system unit's power conservation states.

Local Standby Mode

In Local Standby, the unit's applications are active (microprocessor is still processing data) and the 69000 continues to process display data. The Local Standby mode is entered through software control after a predetermined period of subsystem inactivity time has elapsed.

For software initialization of Standby, the 69000 power management register CR20 (3D5.20h) bit <4> is set. Standby is entered upon timeout if no hardware activity has occurred.

The following states occur in the 69000 during Standby:

- LCD and LCD controller are powered down.

- CRT controller is powered down.

- VCLK is stopped.

- RAMDAC is in low power mode.

- Frame buffer memory is refreshed at a slower rate.

- Microprocessor can still access the graphics subsystem for memory/palette updates.

Suspend Mode

The 69000 enters its Suspend mode when system unit enters Global Standby, which occurs either as a software- or hardware-initiated function. When Suspend mode is initiated, the 69000 Software Configuration register SR23 (3C5.23h) bit <5> is cleared and the SUSPI pin (87) is pulled active, resulting in the additional situations:

■ MCLK is stopped

■ CPU cannot access 69000 registers or frame buffer

■ Frame buffer contents are preserved

CRT Monitor Control

The 69000 supports Display Power Management Signaling (DPMS) criteria specified by the EPA Energy Star Computer Program and by VESA for controlling an external CRT monitor that is DPMS-compatible.

Table 8-2 describes the CRT monitor control register settings and the resulting sync and CRT monitor status.

Table 8-2
DPMS-Compliant CRT Monitor Control

GRE Reg. Bits <2,1>	VSYNC	HSYNC	CRT Monitor Status
00	active	active	On. Full power consumption
01	active	inactive	Standby. Nominal power, short recovery time to On.
10	inactive	active	Suspend. Significant power reduction, long recovery to On.
11	inactive	inactive	Off. Minimum power consumption, long recovery to On.

For more information on power management refer to "Power Conservation" in "Appendix B" of this manual.

Zoomed Video Port

The ZV port is a point to point, unidirectional, video bus that allows video data from a PC Card device to be transferred directly into the VGA frame buffer over a dedicated bus in real time without extra data buffering or bus arbitration logic. Either a composite or S-video signal can be received with automatic input signal detection provided. The PC Card hardware performs decoding/digitizing and routes the video signal in YUV 4:2:2 format to the ZV port. The ZV interface performs video processing, and routes the 16-/32-bit video data (along with the 3-bit audio data) to the 69000 over the zoom video bus for on-screen viewing.

Video capturing to disk is done by the CPU through the ZV port. The CPU takes the video data out of the display frame buffer and sends it to the mass storage device directly, thus allowing the stored data to be viewed as it is being stored.

When the optional video PC Card is installed, and the PC Card host adapter is switched to the ZV multimedia mode, the bussing is as shown in Figure 8-4. In this special mode the CPU control and data will follow the same data path to the card as it would for any standard PC Card device, but the addressing range is restricted to 32, sixteen-bit I/O ports. The unused address range is used to define the 19-pin ZV data bus and as control for a four-channel digital audio. The multimedia PC Card does not support memory mapped addressing.
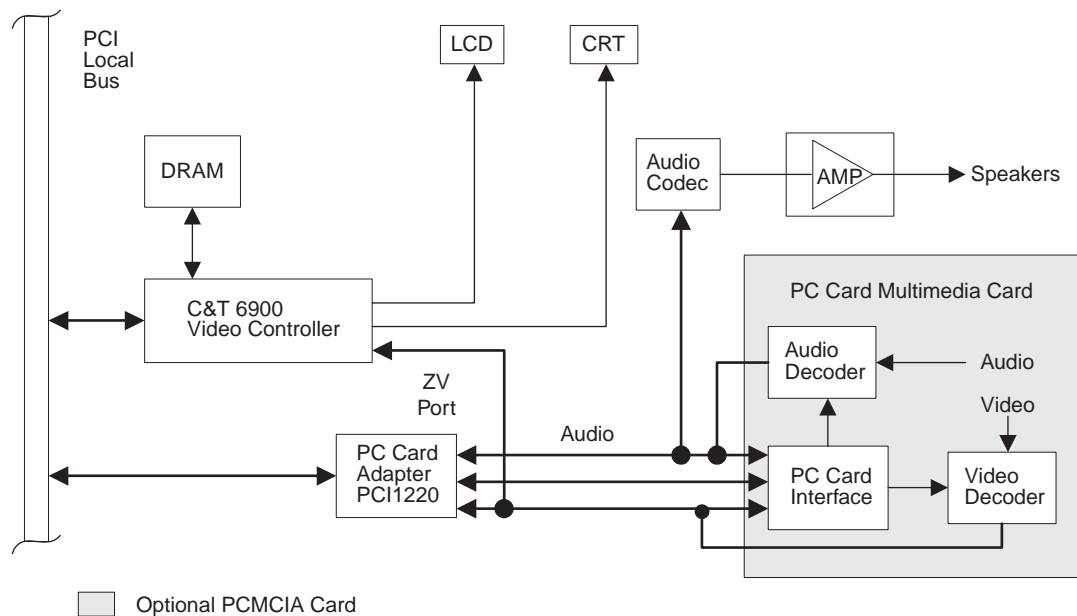

Figure 8-4. *Zoomed Video Multimedia Port Block Diagram*

Zoomed Video/LPB Signals

The PC Card, ZV, and LPB signals and their functions are given in Table 8-3.

<div align="center">

Table 8-3
PC Card Port

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PC Card Signal Name	PC Card Pin Number	Zoomed Video	LPB Signals	Function
IOIS16_	33	PCLK	LCLK	Pixel Clock to ZV Port
A10	8	HREF	~VREQ/HS	Horz. Sync to ZV Port
A11	10	VS	~CREQ/VS	Vert. Sync to ZV Port
A9	11	Y0	LD0	Video Data to ZV Port (YUV:4:2:2)
A17	46	Y1	LD1	Video Data to ZV Port (YUV:4:2:2)
A8	12	Y2	LD2	Video Data to ZV Port (YUV:4:2:2)
A18	47	Y3	LD3	Video Data to ZV Port (YUV:4:2:2)
A13	13	Y4	LD4	Video Data to ZV Port (YUV:4:2:2)
A19	48	Y5	LD5	Video Data to ZV Port (YUV:4:2:2)
A14	14	Y6	LD6	Video Data to ZV Port (YUV:4:2:2)
A20	49	Y7	LD7	Video Data to ZV Port (YUV:4:2:2)
A21	50	UV0	LD8	Video Data to ZV Port (YUV:4:2:2)
A22	53	UV1	LD9	Video Data to ZV Port (YUV:4:2:2)
A16	19	UV2	LD10	Video Data to ZV Port (YUV:4:2:2)
A23	54	UV3	LD11	Video Data to ZV Port (YUV:4:2:2)
A15	20	UV4	LD12	Video Data to ZV Port (YUV:4:2:2)
A24	55	UV5	LD13	Video Data to ZV Port (YUV:4:2:2)
A12	21	UV6	LD14	Video Data to ZV Port (YUV:4:2:2)
A25	56	UV7	LD15	Video Data to ZV Port (YUV:4:2:2)
INPACK_	60	I^2S _LRCLK	I^2S _LRCLK	I^2S Audio L/R Select PCM
BVD2/SPKR_	62	I^2S _DATA	I^2S _DATA	I^2S Audio PCM Data
A7	22	I^2S _SCLK	I^2S _SCLK	I^2S Data Clock
A6	23	I^2S _MCLK	I^2S _MCLK	I^2S Master Clock
A5	24	RESERVED	RESERVED	N/C in PC Card. (3 state)
A4	25	RESERVED	RESERVED	N/C in PC Card. (3 state)
A[3:0]	26:29	ADD[3:0]	ADD[3:0]	Used for accessing PC Card

MPEG-1

The MPEG software decoder decompresses MPEG-1 stream data, which includes video and audio information. The decompressed video data is distributed in 4:2:2 YUV format back to the 64V+ controller, which transfers the video data to the video memory. The MPEG audio data stream, which contains left and right channel information, is converted into separate left and right digital I^2S signals that are routed to the audio subsystem.

MPEG-1 Video Data Structure

Video information is contained in a portion of the stream called a video sequence. A video sequence (Figure 8-5) starts with a sequence header, followed by one or more picture groups, and ending with a sequence end code.
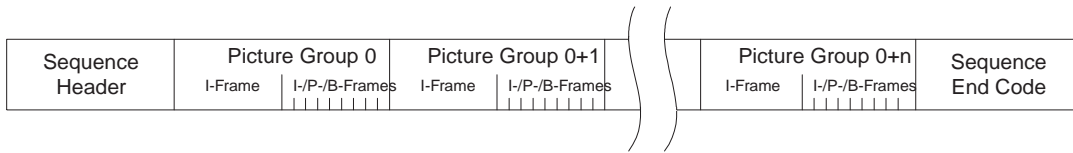

Sequence Header	Picture Group 0		Picture Group 0+1		Picture Group 0+n		Sequence End Code
	I-Frame	I-/P-/B-Frames	I-Frame	I-/P-/B-Frames	I-Frame	I-/P-/B-Frames	

Figure 8-5. *MPEG-1 Video Sequence*

Each picture group contains a set of frames. Video data compression is based on the fact that there is a large amount of redundancy (little change) from moment to moment on a video display. In a given video sequence and within picture groups, video information can be more efficiently coded based on differences (changes in the picture) from frame to frame than on the picture itself. Three types of frames are used:

■ Intra (I-) Frames: I-Frames are coded using Joint Photographic Experts Group (JPEG) compression and contain only picture data. These frames provide the basis for Predicted and Bidirectional Interpolated Frame production and are also used as reference points for MPEG file scanning. I-Frames offer the least amount of data compression, but are used at a much lower rate than Predicted or Bidirectional Interpolated Frames, typically no more than twice a second. A picture group always starts with an I-Frame.

■ Predicted (P-) Frames: P-Frames are coded by predicting image redundancy with respect to the preceding I- or P-Frame. Motion compensation is utilized in coding to allow more data compression.

■ Bidirectional Interpolated (B-) Frames: B-Frames are coded using predicted redundancy data from both preceding and succeeding I- and P-Frames, providing a higher degree of both accuracy and data compression. This third frame type distinguishes the MPEG system from the .AVI type of coding, which uses two frame types for video data compression.

Each frame can be further broken down into sub-units identified as slices, macroblocks, and, finally, blocks (Figure 8-6).

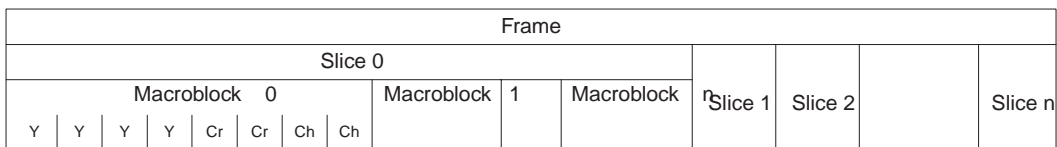| Frame											
Slice 0							Slice 1	Slice 2		Slice n	
Macroblock 0							Macroblock 1	Macroblock n			
Y	Y	Y	Y	Cr	Cr	Ch	Ch				

Figure 8-6. Video Frame Format

The block holds the values based on the CCIR 601 standard for color sub-sampling. Each block represents an 8-pixel $\times$ 8-line set of values for a luminance (Y) or chrominance (Cr or Cb) component. Upon decoding, the video data is output in a 4:2:2 format, meaning that for every 4 luminance (Y) samples there are 2 chrominance samples for CR (red minus Y) and 2 chrominance samples for Cb (blue minus Y).

MPEG-1 Audio Data Structure

The MPEG-1 includes audio information that is decoded into a serial bit stream. This stream is routed along with a clock signal and a signal that identifies the left and right channel information (Figure 8-7) to the MPEG audio DAC. The sampling rates are programmable for 32, 44.1, or 48 kHz.
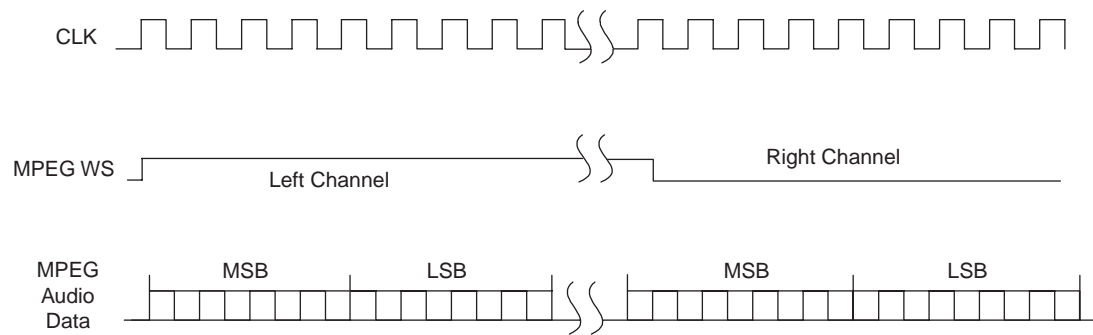

Figure 8-7. Decoded MPEG-1 Audio Stream

The MPEG DAC provides digital-to-analog conversion of the audio data and provides two signals (left/right) to the audio subsystem.

Liquid Crystal Display (LCD)

Table 8-4 and Table 8-5 list the key parameters of the active TFT matrix display.

Table 8-4
12.1-Inch CTFT, SVGA Display

	U.S.	Metric
Dimensions		
Height	7.24 in	18.4 cm
Width	9.7 in	24.6 cm
Number of Colors	64K	
Contrast Ratio	100:1 minimum	
Pixel Resolution		
Pitch	0.30 × 0.30 mm	
Format	800 × 600	
Configuration	RGB Stripe	
Backlight	Edge Lit	
Character Display	80 × 25	

Table 8-5
13.3-Inch CTFT, XGA Display

	U.S.	Metric
Dimensions		
Height	7.9 in	20.1 cm
Width	10.6 in	26.9 cm
Number of Colors	64K	
Contrast Ratio	100: 1 minimum	
Pixel Resolution		
Pitch	0.29 x 0.29 mm	
Format	1024 x 768	
Configuration	RGB Stripe	
Backlight	Edge Lit	
Character Display	80 × 25	

Brightness Control

The brightness of the TFT LCD display is controlled by a hotkey (**F10**) that affects a signal applied to the backlight inverter board. Keyboard inputs used to adjust the brightness are handled by system management (SM) firmware.

A 2-MHz pulse width modulator (PWM) timer is used to establish the brightness signal output duty cycle from 0% (min. brightness) to 100% (max. brightness). Brightness duty cycles are adjusted at a resolution of 1/128 (00h) for 0% duty cycle up to a value of 127/128 (FFh) at 100% duty cycle. The brightness control register (PWM0) used to configure the PWM clocking and output polarity is located in the 37C951 at address E2h (E3h data) index 92h.

Display Modes

The graphics subsystem provides one of two types of displays: text or graphics.

Text Modes

The text display uses a multiplane (MP) configuration where a character, its attributes, and fonts are stored in the separate memory planes. Table 8-6 lists the text configurations provided by the video system. Note that the text configurations for CGA/MDA, EGA, and VGA share common video BIOS modes that result in the same format but provide different pixel resolutions.

Table 8-6
Text Display Modes

Software Interface				Video BIOS Mode	Format	Pixel Resolution	Number of Colors	Display
SVGA	VGA	EGA	CGA	0	40 x 25 Text	320 x 200	16	LCD/CRT
			CGA	1	40 x 25 Text	320 x 200	16	LCD/CRT
				2	80 x 25 Text	640 x 200	16	LCD/CRT
				3	80 x 25 Text	640 x 200	16	LCD/CRT
			MDA	7	80 x 25 Text	720 x 350	Mono	LCD/CRT
				0	40 x 25 Text	320 x 350	16	LCD/CRT
				1	40 x 25 Text	320 x 350	16	LCD/CRT
				2	80 x 25 Text	640 x 350	16	LCD/CRT
				3	80 x 25 Text	640 x 350	16	LCD/CRT
				0	40 x 25 Text	360 x 400	16	LCD/CRT
				1	40 x 25 Text	360 x 400	16	LCD/CRT
				2	80 x 25 Text	720 x 400	16	LCD/CRT
				3	80 x 25 Text	720 x 400	16	LCD/CRT
				7	80 x 25 Text	720 x 400	Mono	LCD/CRT
				14	132 x 25	1056 x 400	16	CRT
				54	132 x 43	1056 x 350	16	CRT
				55	132 x 25	1056 x 350	16	CRT

Graphics Modes

The graphics subsystem can operate in either of two fundamental graphics modes: MP or packed pixel. The MP mode provides four graphics planes in memory, each plane simultaneously supplying one bit of the 4-bit code that defines a particular color. The packed-pixel (pp) mode allows software to use as many as 16 bits to determine a particular color. The graphics modes are listed in Table 8-7.

Table 8-7
Graphics Display Modes

Software Interface	Video BIOS Mode	Pixel Resolution	Number of Colors	Display Compatibility	
				LCD Panel	Ext. CRT Monitor *
CGA	4	320 x 200 @ 2 bpp	4	VGA, SVGA	VGA, SVGA
	5	320 x 200 @ 2 bpp	4	VGA, SVGA	VGA, SVGA
	6	640 x 200 @ 1 bpp	2	VGA, SVGA	VGA, SVGA
EGA	D	320 x 200 (MP)	16	VGA, SVGA	VGA, SVGA
	E	640 x 200 (MP)	16	VGA, SVGA	VGA, SVGA
	F	640 x 350 (MP)	Mono	VGA, SVGA	VGA, SVGA
	10	640 x 350 (MP)	16	VGA, SVGA	VGA, SVGA
VGA	11	640 x 480 (MP)	2	VGA, SVGA	VGA, SVGA
	12	640 x 480 (MP)	16	VGA, SVGA	VGA, SVGA
	13	320 x 200 @ 8 bpp	256	VGA, SVGA	VGA, SVGA
SVGA	16	640 x 480 (MP)	16	VGA, SVGA	VGA, SVGA
	17	800 x 600 (MP)	16	SVGA	SVGA
	18	1024 x 768 @ 4 bpp	16	---	SVGA
	58,6A	800 x 600 @ 4 bpp	16	SVGA	SVGA
	5C	800 x 600 @ 8 bpp	256	SVGA	SVGA
	5D	1024 x 768 @ 4 bpp	16	---	SVGA
	5E	640 x 400 @ 8 bpp	256	VGA, SVGA	VGA, SVGA
	5F	640 x 480 @ 8 bpp	256	VGA, SVGA	VGA, SVGA
	60	1024 x 768 @ 8 bpp	256	---	SVGA
	64	640 x 480 @ 16 bpp	64K	VGA, SVGA	VGA, SVGA
	65	800 x 600 @ 16 bpp	64K	SVGA	SVGA
	66	640 x 480 @ 15 bpp	32K	VGA, SVGA	VGA, SVGA
	67	800 x 600 @ 15 bpp	32K	SVGA	SVGA
SXGA		1024 x 768 @ 16 bpp	256	---	VGA, SVGA, XGA
		1280 x 1024 @ 8 bpp	256	---	VGA, SVGA, XGA
* Optional					

The 69000 provides resolution compensation for display modes that have a lower than maximum resolution than LCD panel is capable of. This compensation provides a full LCD screen display for lower resolution display modes.

Status Indication

The LCD pop-up status indicators provide system status that is displayed on the LCD display panel after any one of the hotkeys on the internal keyboard are depressed.

The displayed system status information includes the following:

- Popup Icon Location (**F1**)

- Firmware Version (**F2**)

- Speaker audio volume (**F5**)

- QuickLock (**F6**)

- Power Management Mode (**F7**)

- Display brightness (**F10**)