SM30 Block Diagram

Project code: 91.4BT01.001
PCB P/N : 48.4BT01.001
Revision : 08239-SA

Crystal 14.318MHz
CLK GEN. ICS 9LPRS929 3
Mobile CPU Penryn 4, 5
SMSC EMC2103 29
HOST BUS 667/800/1066MHz@1.05V
DDR3 800/1033 MHz 12,13
DDR3 800/1033 MHz 12,13
Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
6,7,8,9,10,11
LCD 15
CRT 17
X4 DMI 400MHz
C-Link0
Crystal 32.768KHz
Crystal 25MHz
LAN Giga LAN BCM5764
TXFM
RJ45
Mini Card (Robson2/3G)
Mini Card Kedron a/b/g/n 28 (WLAN)
PCIe
Int MIC 15
MIC In 32
32 Line Out (SPDIF)
Codec ALC272 30
AZALIA
ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
18,19,20,21
LPC BUS
Crystal 32.768KHz
KBC Winbond WPCE773LA0DG 33
SPI
BIOS (2MB) 34
Launch Buttom 35
LPC DEBUG CONN. 34
Daughter Board
Touch Pad 33
INT. KB 33
32 INT.SPKR 1.5W
OP AMP G1454 31
SATA
USB
HDD SATA 23
ODD SATA 22
Mini USB Blue Tooth 24
Finger Printer 26
USB 2 Port
Camera
USB 1 Port
CardReader Realtek RTS5159 27
MS/MS Pro/xD /MMC/SD 5 in 1 27

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC TPS51125 50	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 51	
INPUTS	OUTPUTS
DCBATOUT	1D05V_M(16A) 1D5V_S3(12A)

RT9026 52	
1.5V_S3	DDR_VREF_S3 (1.2A)

G9131 52	
3D3V_S0	2D5V_S0 (300mA)

TPS51117 54	
DCBATOUT	1D8V_S0 (9.4A)

CHARGER BQ24750 55	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ISL6266A 49	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 38A

GFX DC/DC ISL6263 53	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0~1.3V 6.5A

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Title: BLOCK DIAGRAM
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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

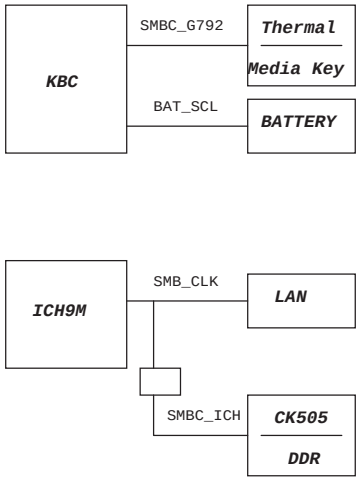
SIGNAL	Resistor Type/Value
CL_RST0#	
	PULL-DOWN 20K
HDA_BIT_CLK	
	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9		0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[13:12]		00 = Reserve **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	
CFG20		**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:

SMBus



USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	NC
3	MINIC2(WLAN)
4	CAMERA
5	NC
6	FingerPrint
7	BLUETOOTH
8	
9	USB1(IO board)
	CARD READER

PCIE Routing

LANE1	LAN BCM5764
LANE2	MiniCard WLAN
LANE3	MiniCard(Robson2G/3G)

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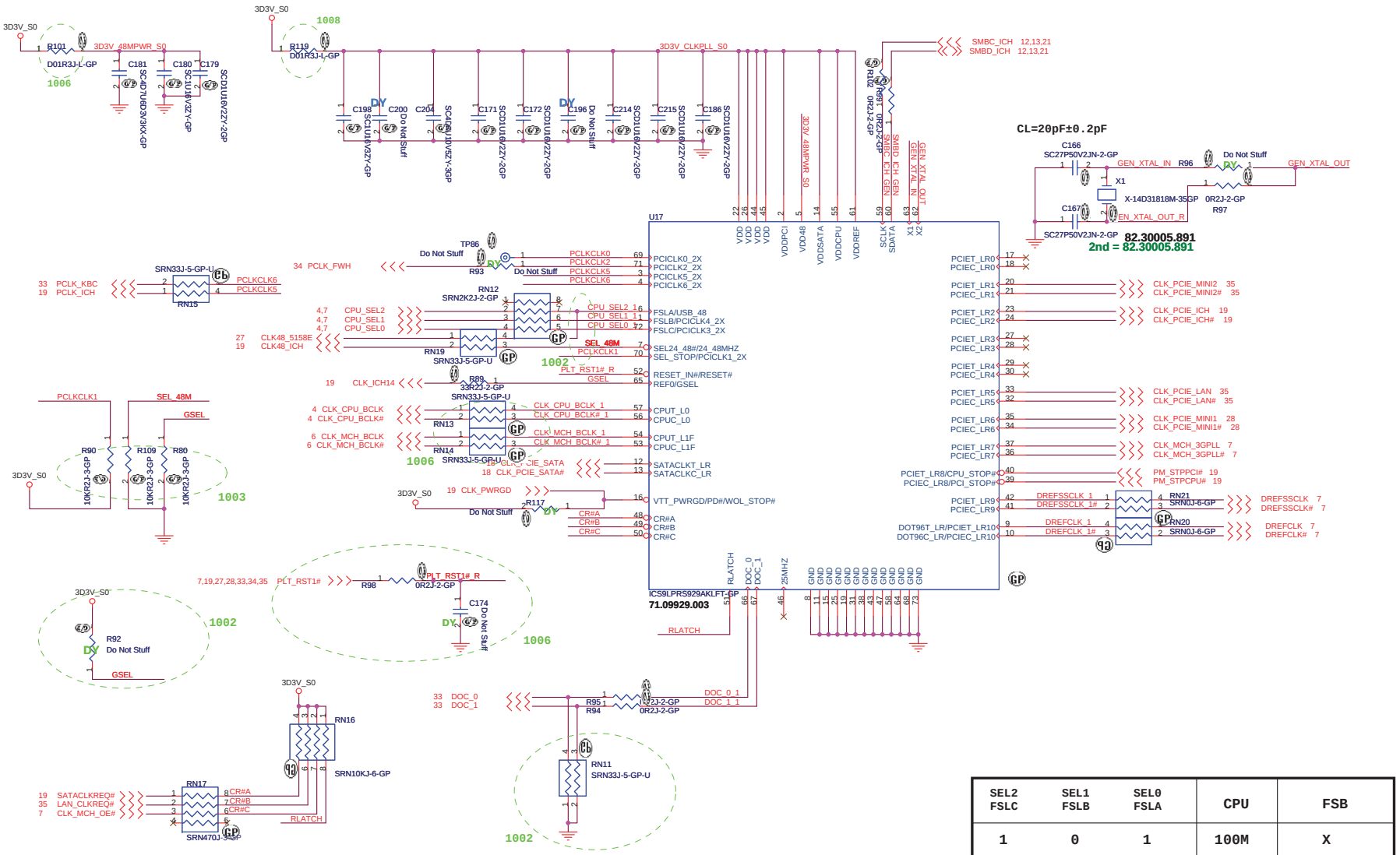

SEL2 FSLC	SEL1 FSLB	SEL0 FSLA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

GSEL	DOT Freq
0	100MHZ
1	96MHZ

SEL_STOP	Selects pin 39/40
0	PCI_STOP#/CPU_STOP#
1	PCIEX outputs

SEL24_48#/24_48MHZ	OUTPUT
0	24MHZ
1	48MHZ

DOC_0	Real Time Frequency
0	Normal
1	Frequency will transition to a preprogrammed value in the I2C

DOC_1	Real Time Frequency
0	Normal
1	Frequency will transition to a preprogrammed value in the I2C

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Title: Clock Generator

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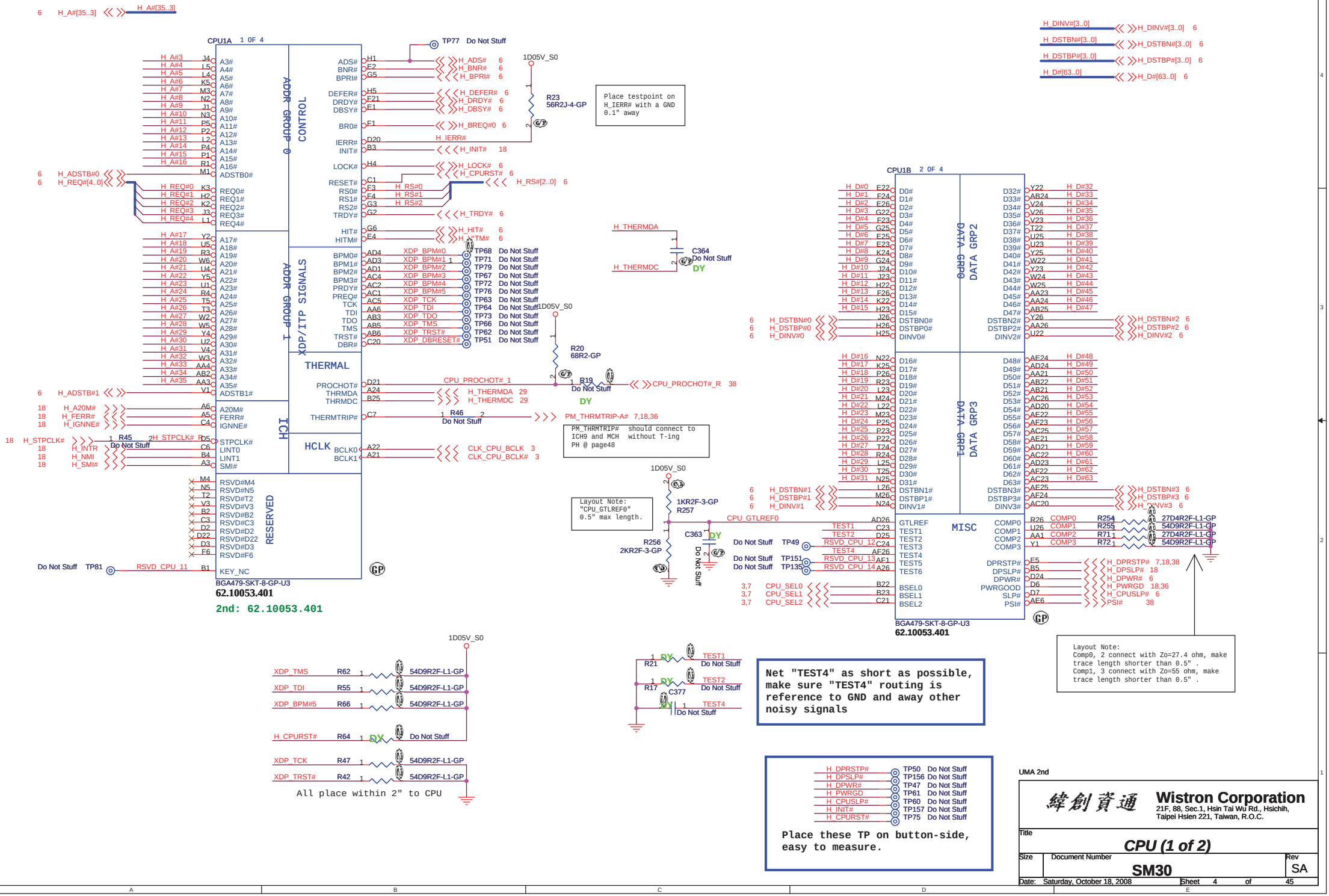
CPU1A 1 0F 4
ADDR GROUP 0
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
HCLK
RESERVED
ICH
BGA479-SKT-8-GP-U3
62.10053.401
2nd: 62.10053.401
CPU1B 2 0F 4
DATA GRP2
DATA GRP0
DATA GRP3
DATA GRP1
MISC
BGA479-SKT-8-GP-U3
62.10053.401
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing PH @ page48
Layout Note: "CPU_GTLREF0" 0.5" max length.
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
All place within 2" to CPU
Place these TP on button-side, easy to measure.
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Title
CPU (1 of 2)
Size
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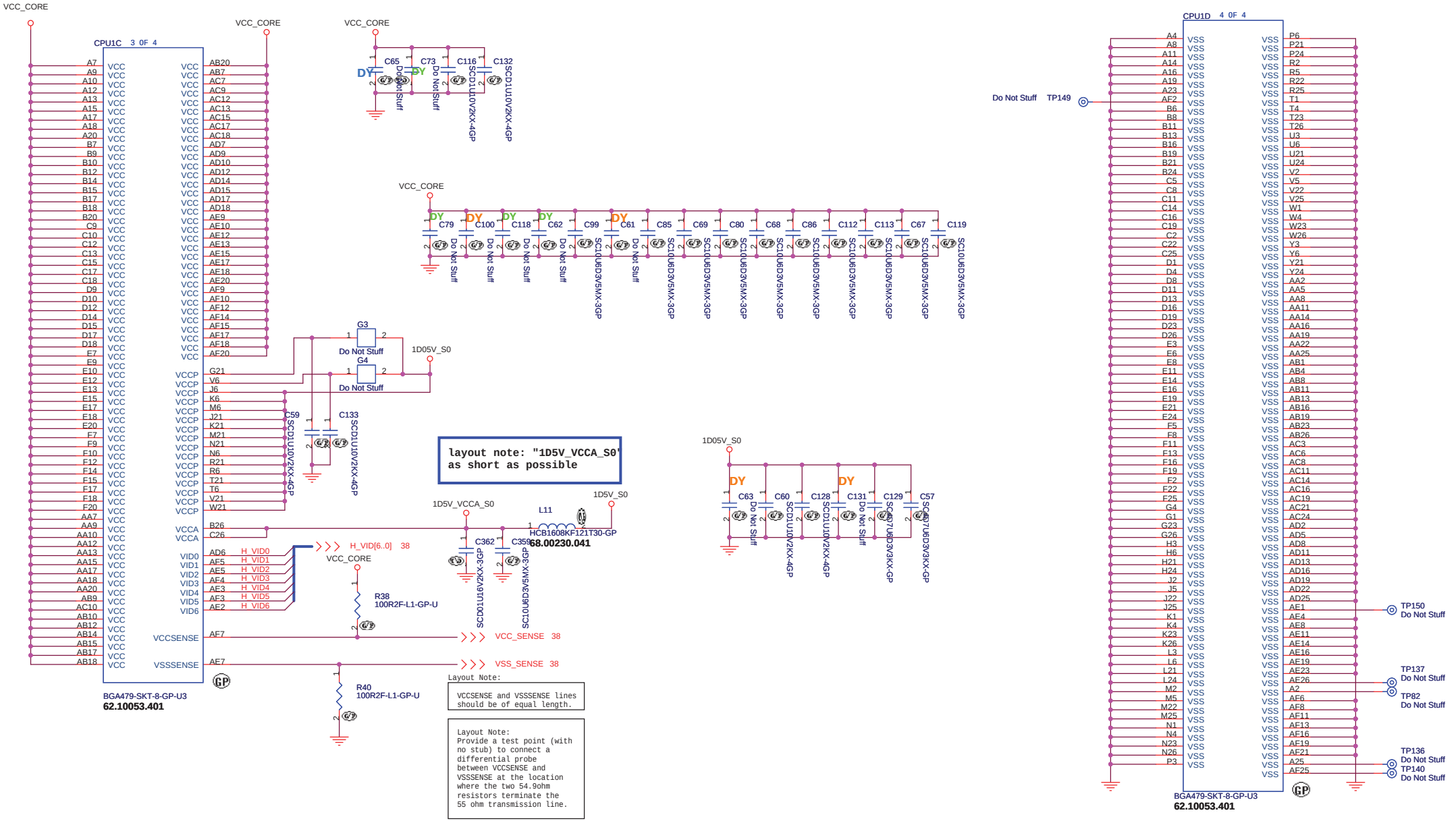

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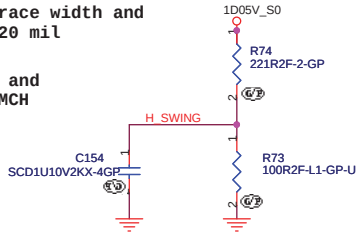
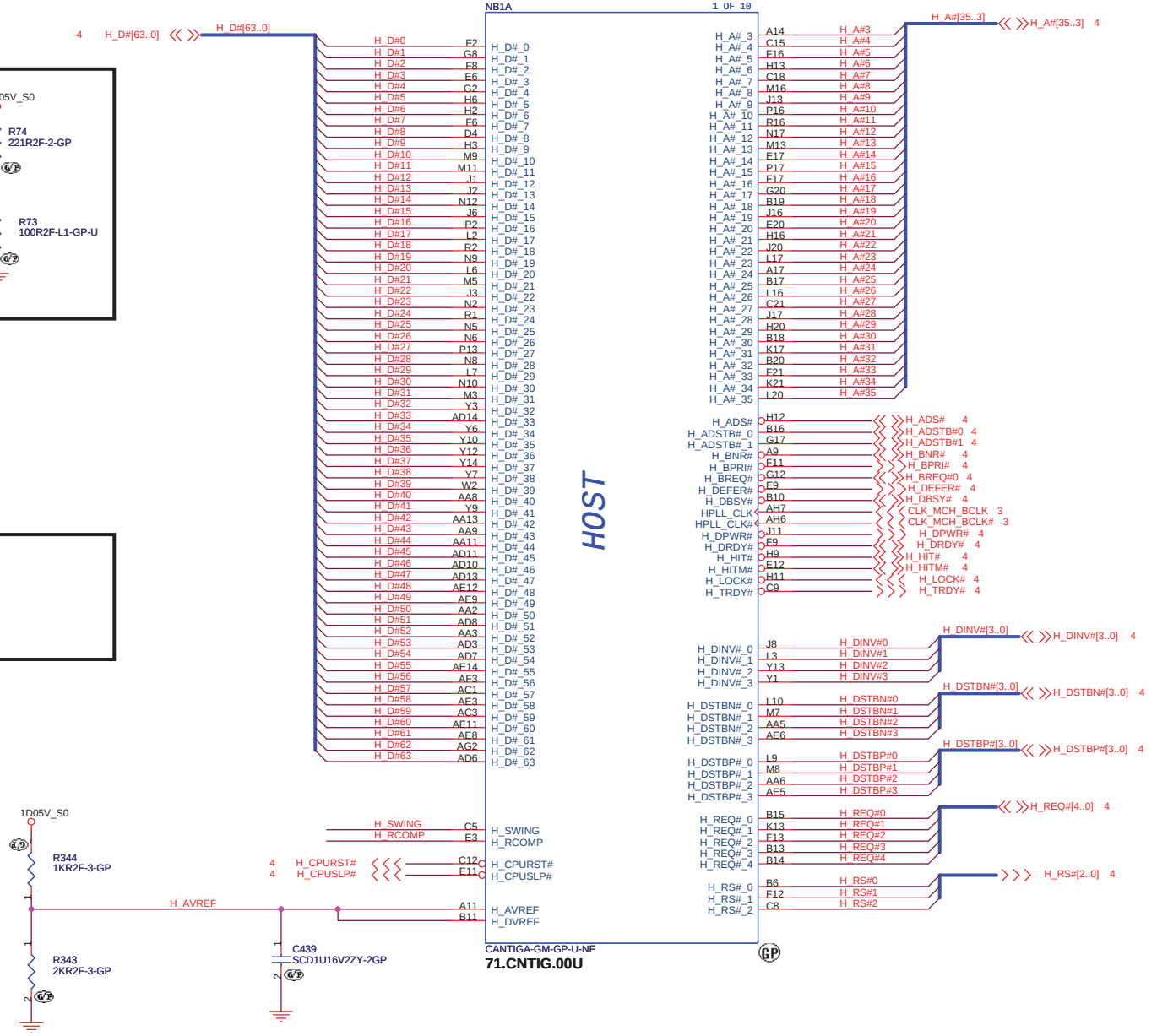
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

Place them near to the chip (< 0.5")



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Title	Cantiga (1 of 6)	
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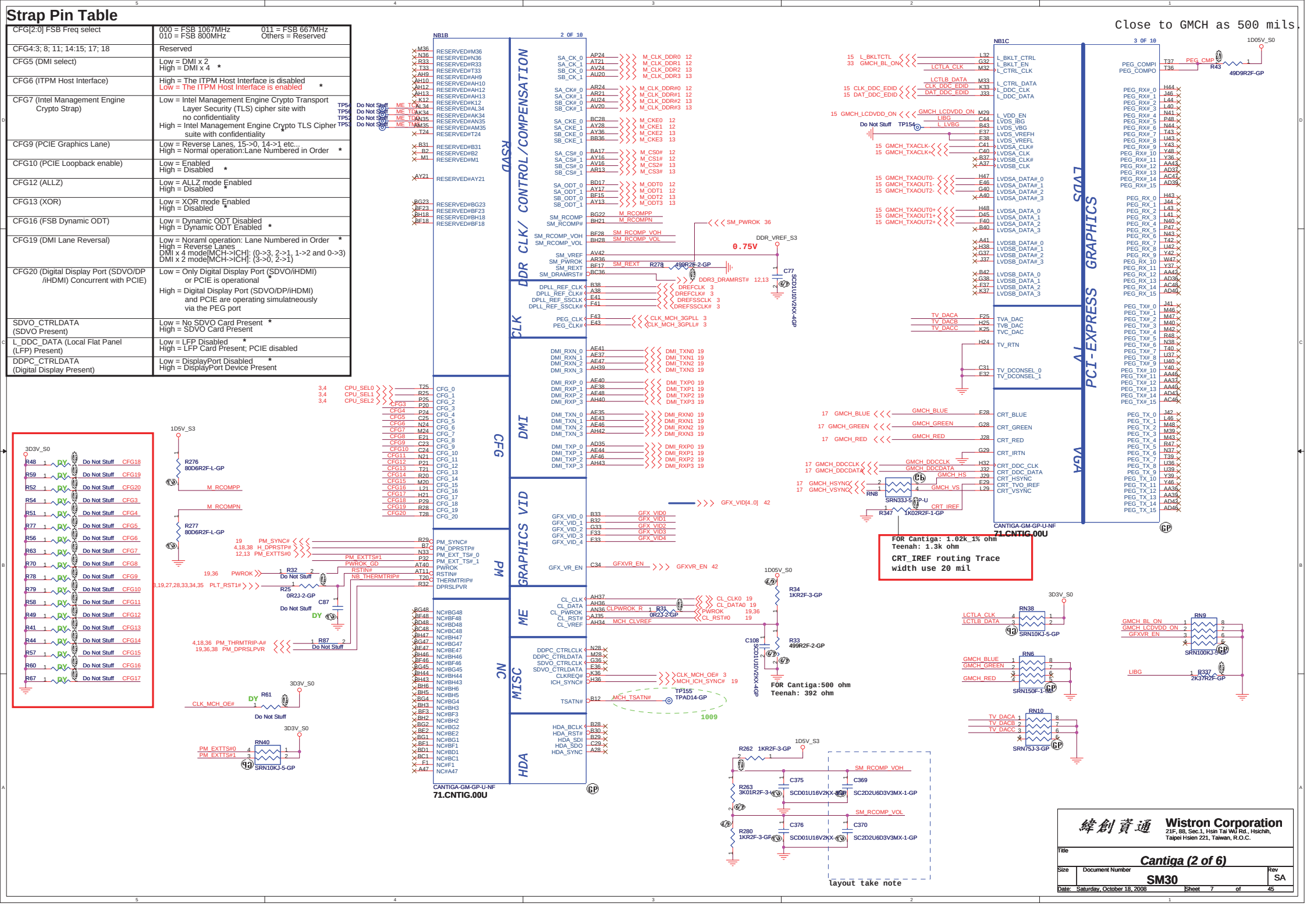
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1067MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG4:3; 8; 11; 14:15; 17; 18	Reserved
CFG5 (DMI select)	Low = DMI x 2 High = DMI x 4 *
CFG6 (ITPM Host Interface)	High = The ITPM Host Interface is disabled Low = The ITPM Host Interface is enabled *
CFG7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher site with no confidentiality High = Intel Management Engine Crypto TLS Cipher suite with confidentiality *
CFG9 (PCIE Graphics Lane)	Low = Reverse Lanes, 15->0, 14->1 etc... High = Normal operation:Lane Numbered in Order *
CFG10 (PCIE Loopback enable)	Low = Enabled High = Disabled *
CFG12 (ALLZ)	Low = ALLZ mode Enabled High = Disabled *
CFG13 (XOR)	Low = XOR mode Enabled High = Disabled *
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled *
CFG19 (DMI Lane Reversal)	Low = Noraml operation: Lane Numbered in Order * High = Reverse Lanes DMI x 4 mode[MCH->ICH]: (0->3, 2->1, 1->2 and 0->3) DMI x 2 mode[MCH->ICH]: (3->0, 2->1)
CFG20 (Digital Display Port (SDVO/DP /iHDMI) Concurrent with PCIE)	Low = Only Digital Display Port (SDVO/iHDMI) or PCIE is operational * High = Digital Display Port (SDVO/DP/iHDMI) and PCIE are operating simulatneously via the PEG port
SDVO_CTRLDATA (SDVO Present)	Low = No SDVO Card Present * High = SDVO Card Present
L_DDC_DATA (Local Flat Panel (LFP) Present)	Low = LFP Disabled * High = LFP Card Present; PCIE disabled
DDPC_CTRLDATA (Digital Display Present)	Low = DisplayPort Disabled * High = DisplayPort Device Present

Close to GMCH as 500 mils.



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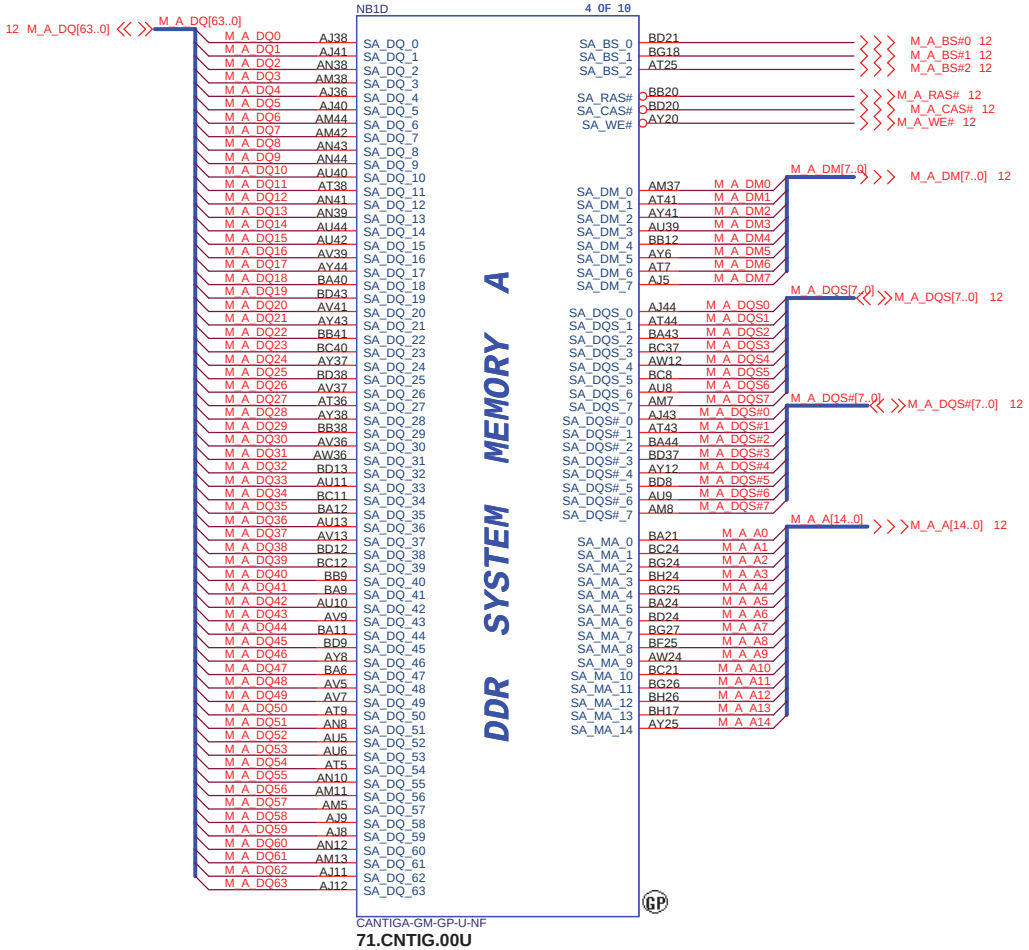

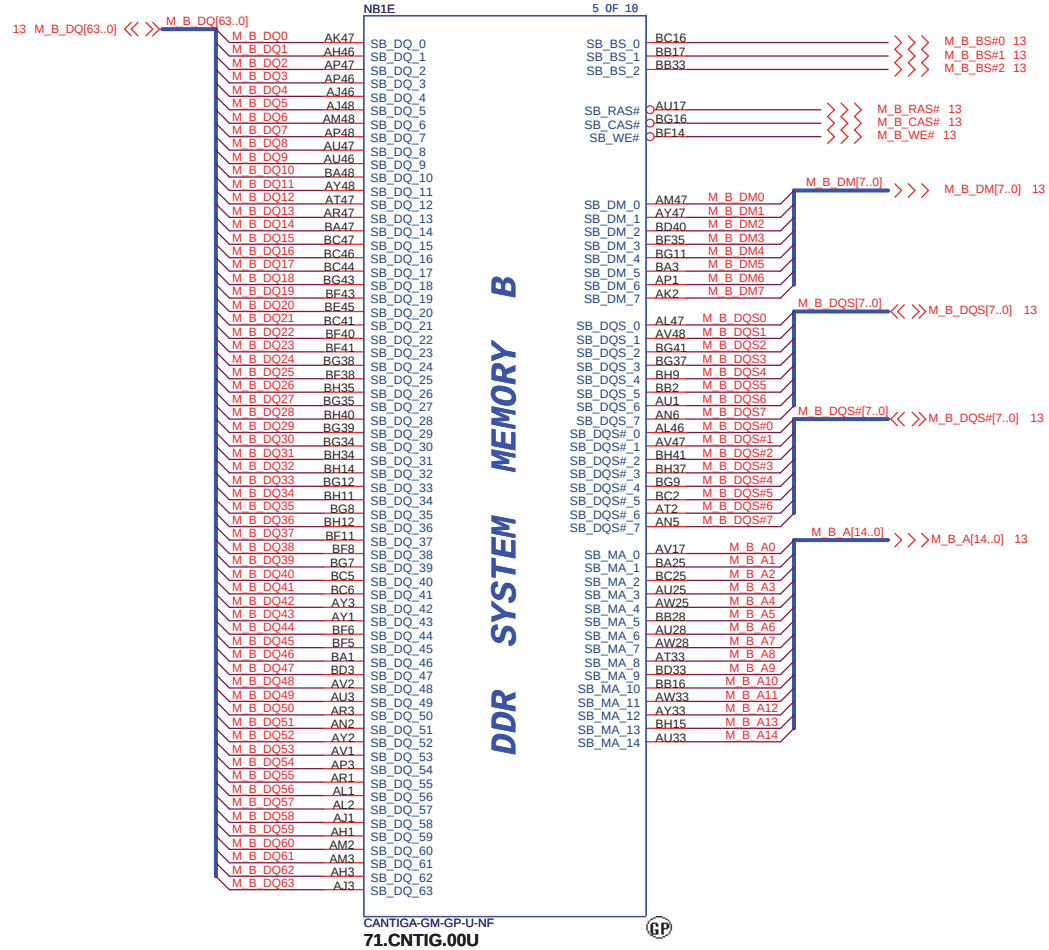

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Title: Cantiga (3 of 6)

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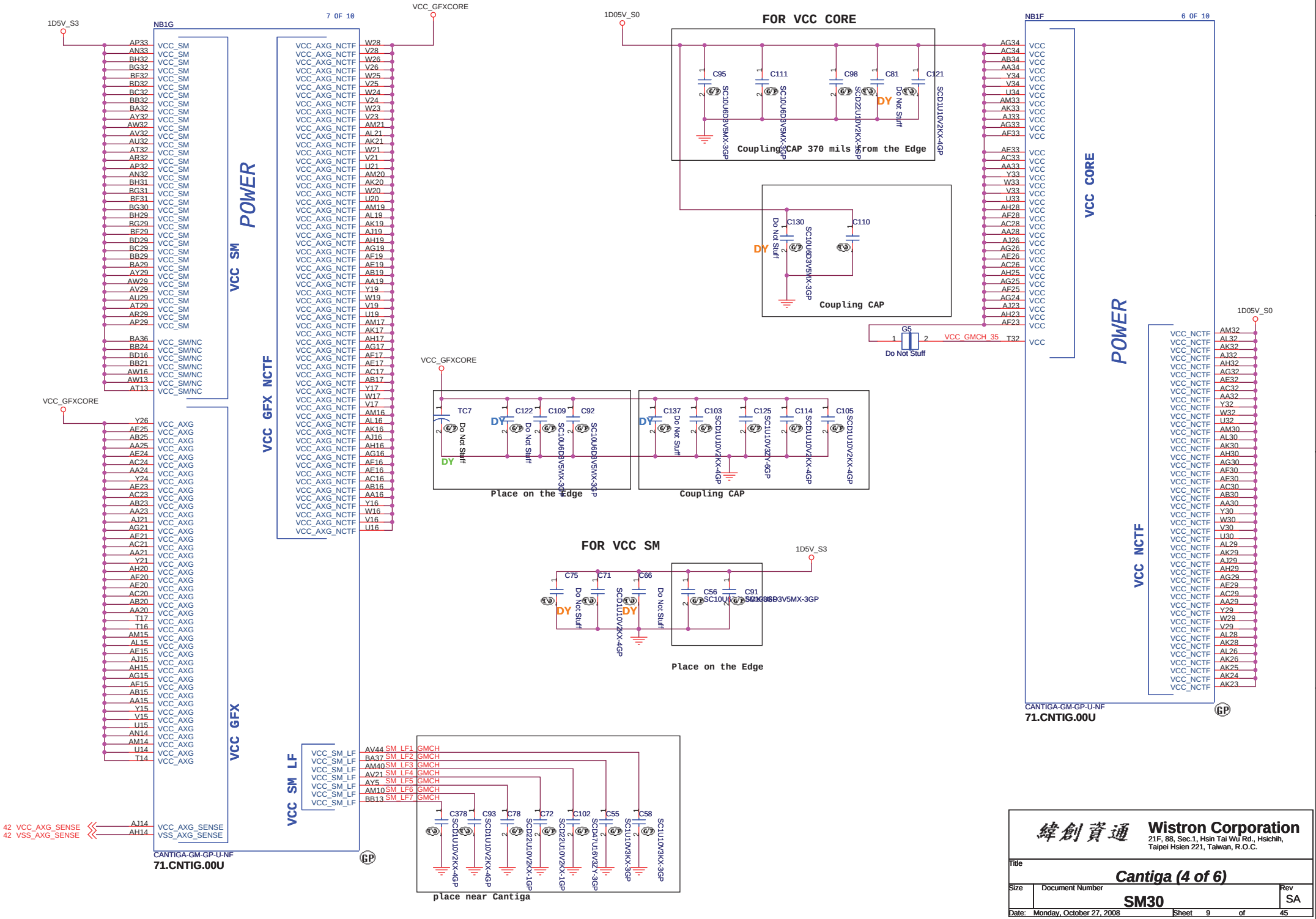
1D5V_S3
NB1G
7 OF 10
VCC_GFXCORE
POWER
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
VCC_GFXCORE
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
1D05V_S0
FOR VCC CORE
Coupling CAP 370 mils from the Edge
Coupling CAP
Do Not Stuff
VCC_GMCH_35
NB1F
6 OF 10
VCC CORE
VCC NCTF
Place on the Edge
Coupling CAP
FOR VCC SM
Place on the Edge
place near Cantiga
42 VCC_AXG_SENSE
42 VSS_AXG_SENSE
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Title
Cantiga (4 of 6)
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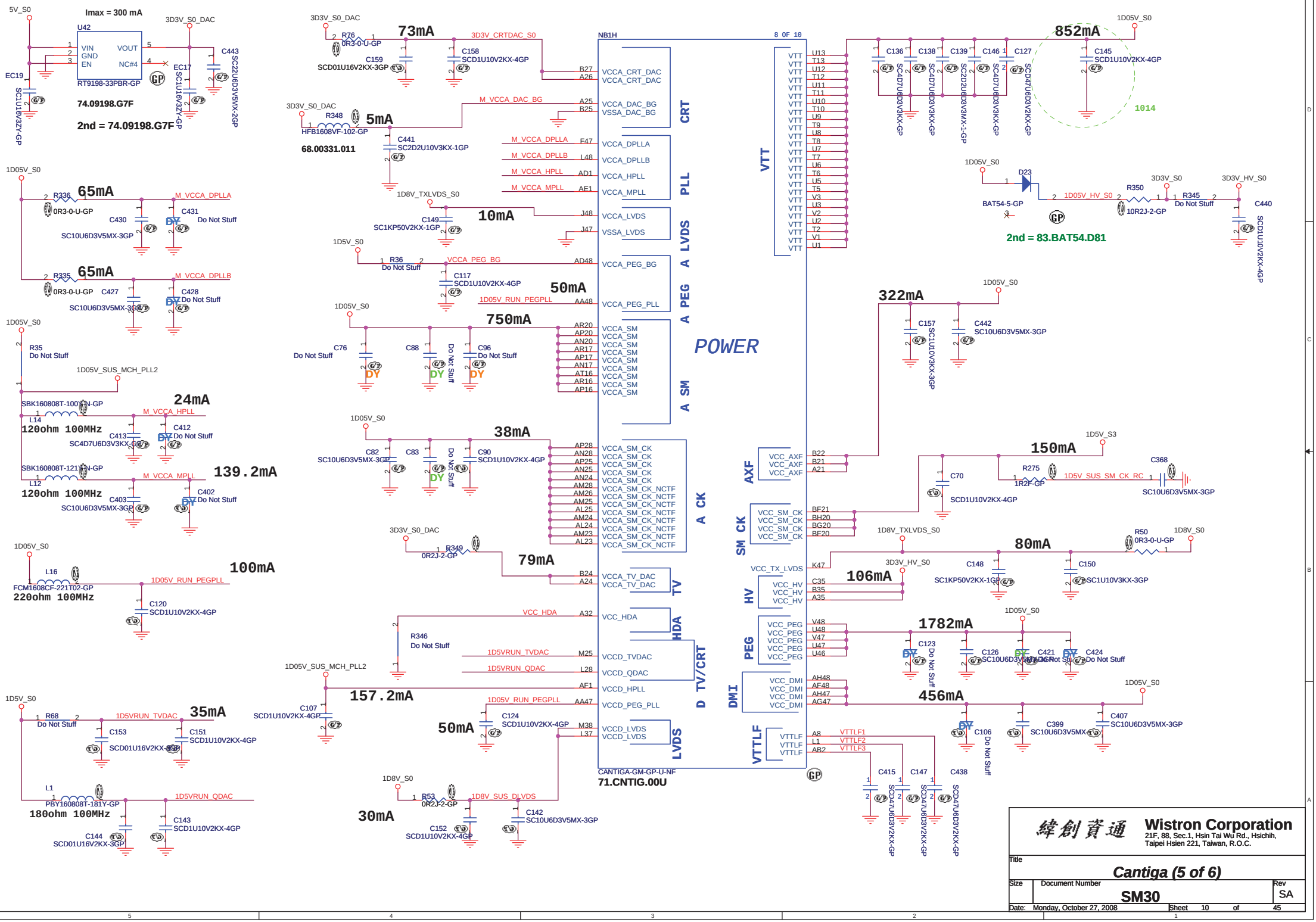

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Title: Cantiga (5 of 6)	
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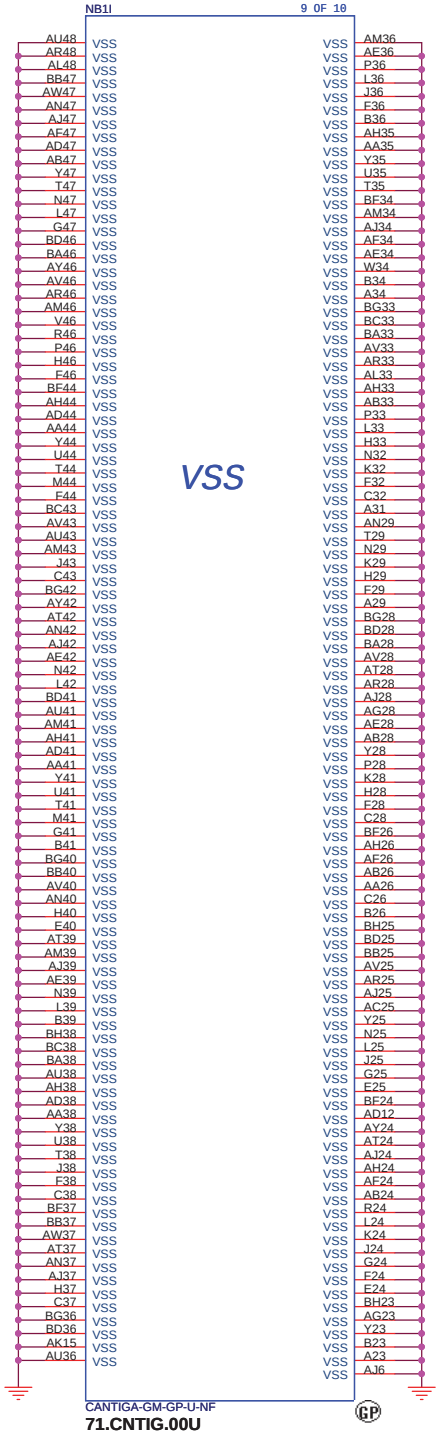

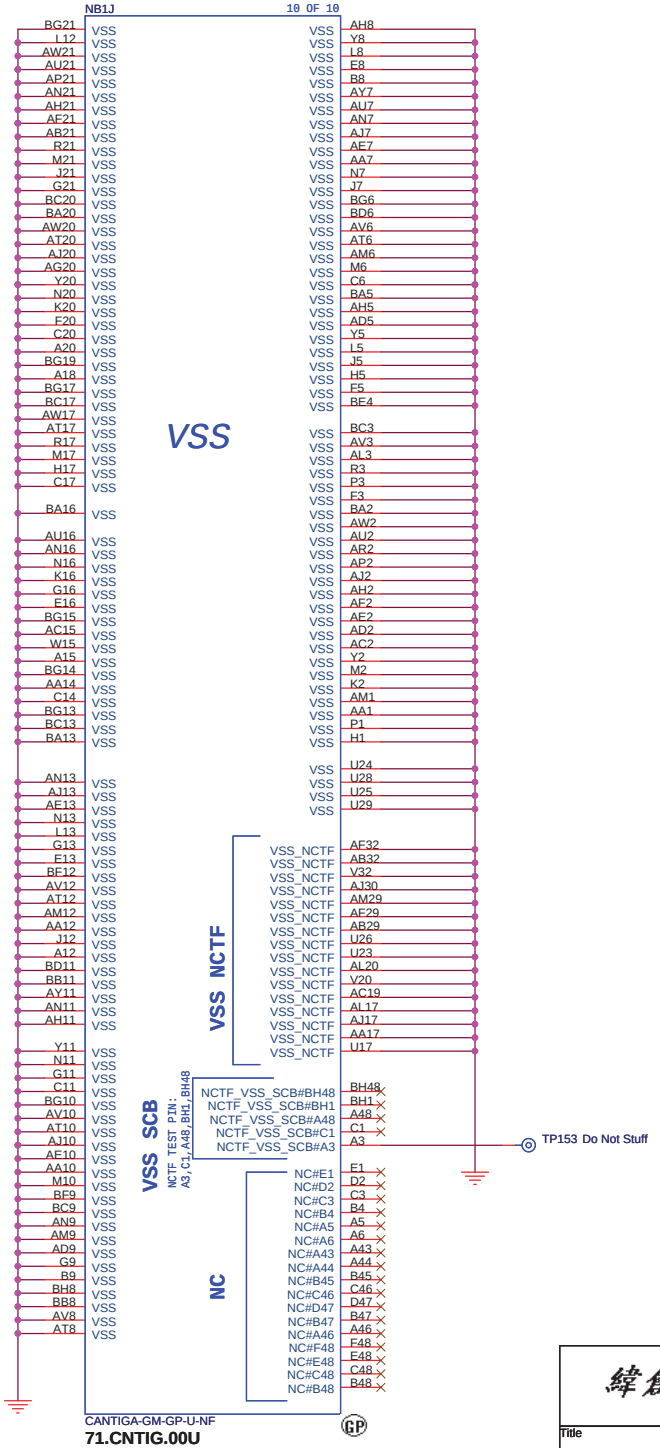

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Title	*Cantiga (6 of 6)*	
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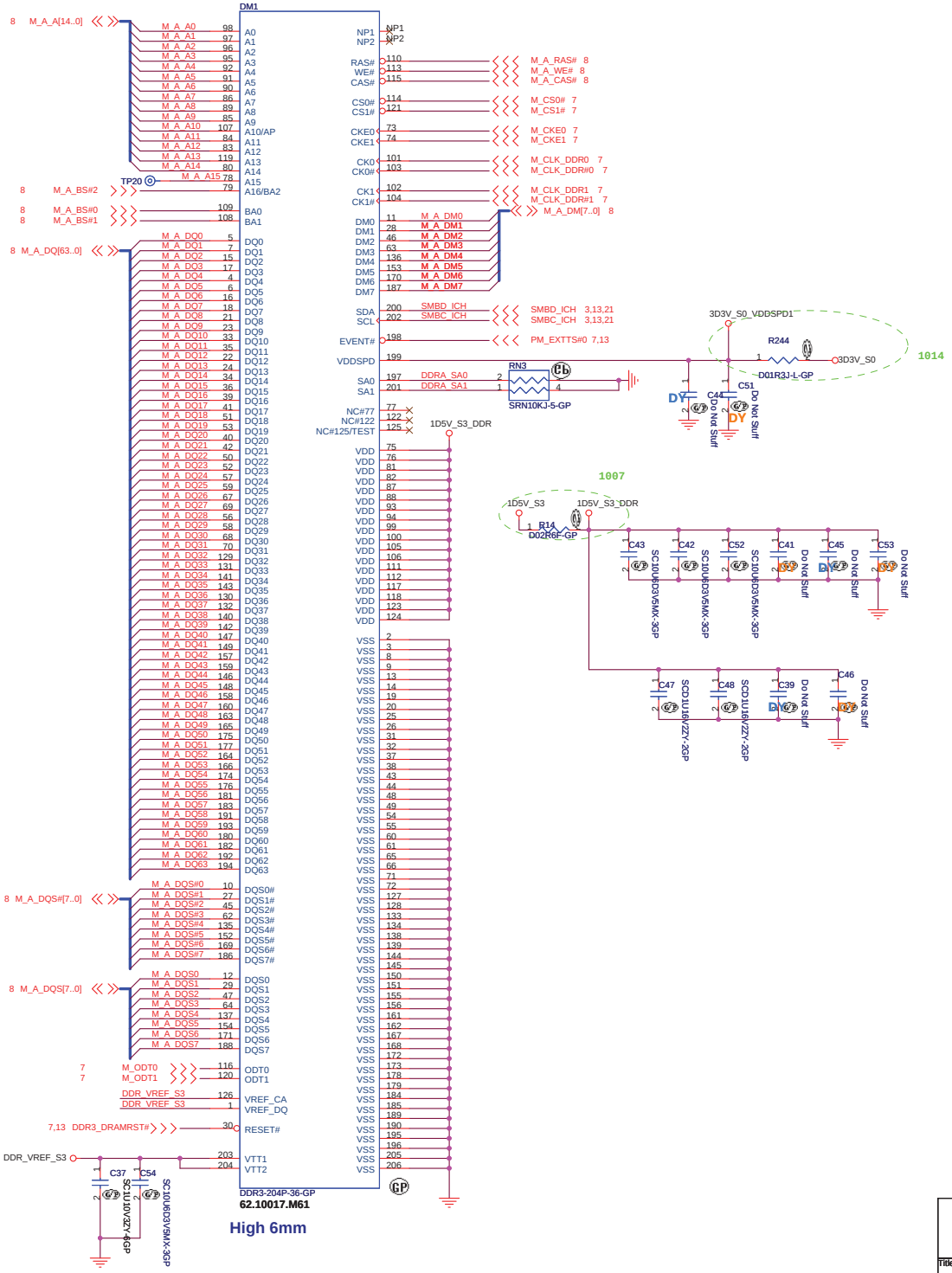
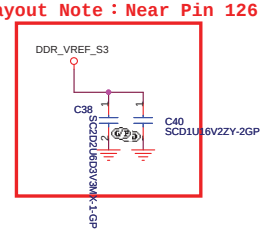
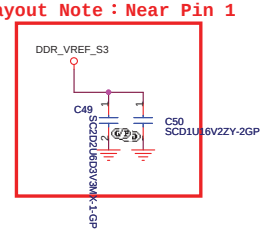
DDR3 SOCKET_1



Layout Note：Near Pin 126



Layout Note：Near Pin 1



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Title: DDR3 Socket			
Size	Document Number: SM30	Rev: SA	
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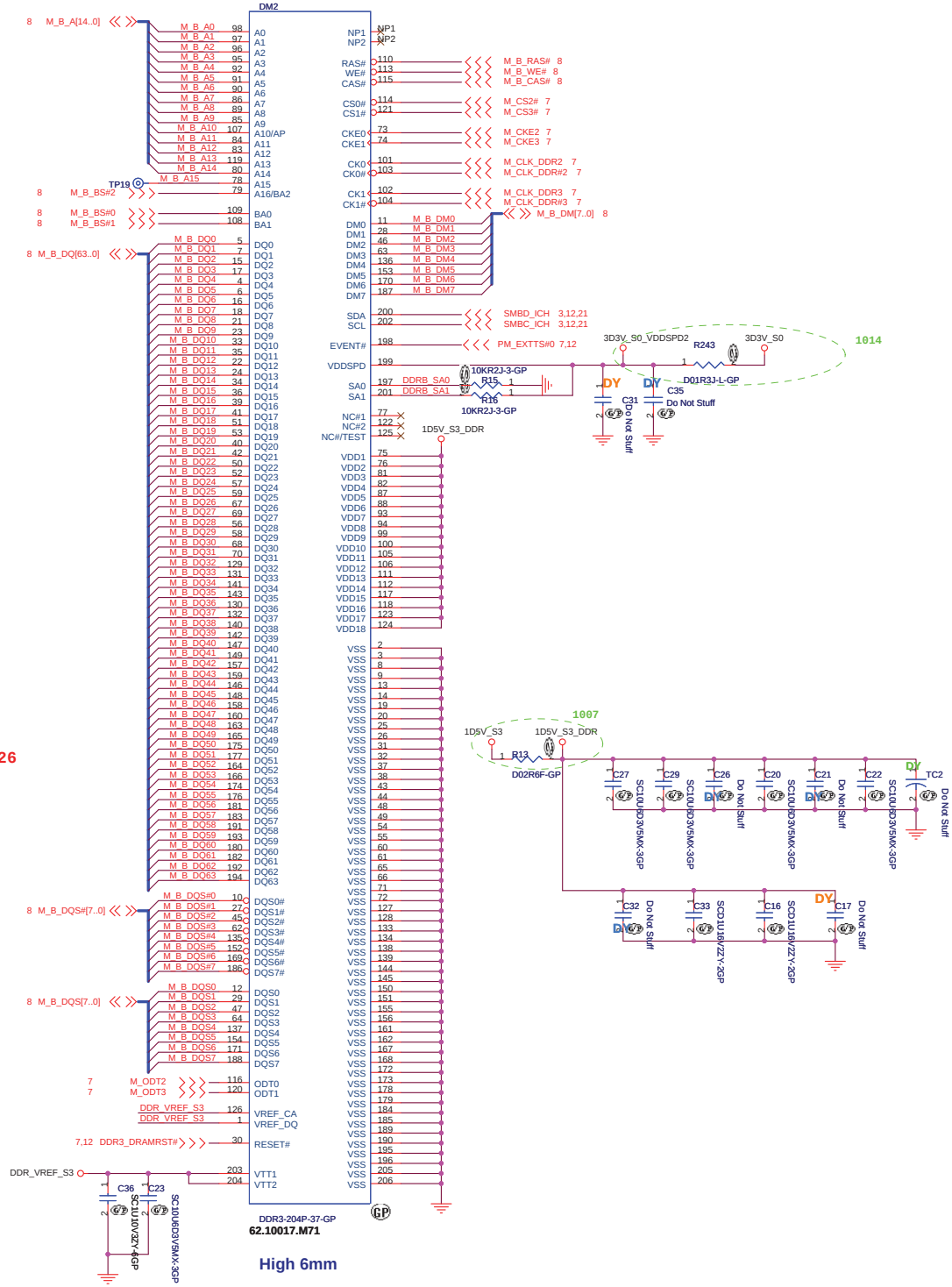
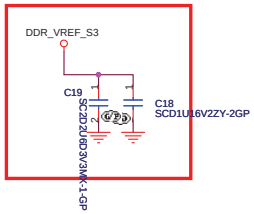
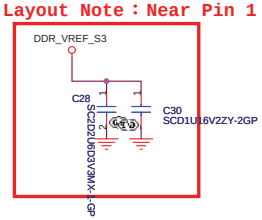
DDR3 SOCKET_2



Layout Note：Near Pin 126



Layout Note：Near Pin 1



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Title: DDR3 Termination Resistor		
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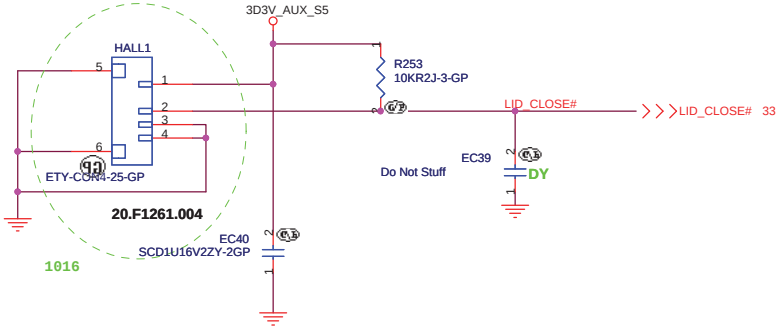
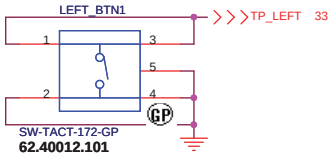
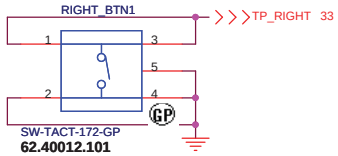
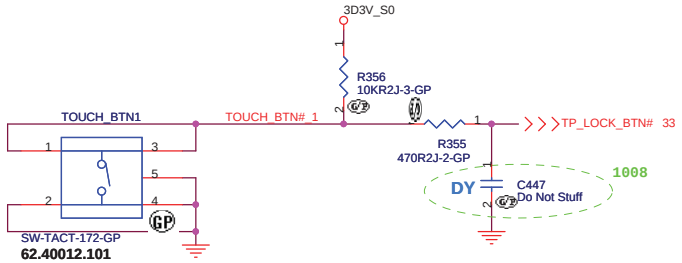
Cover Up Switch

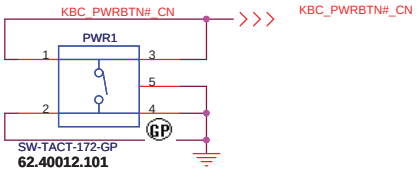


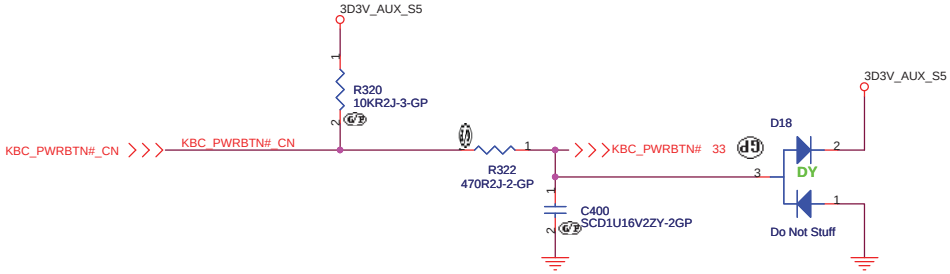
74.00268.A7B
74.00268.C7B











UMA 2nd

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SWITCH / Button***

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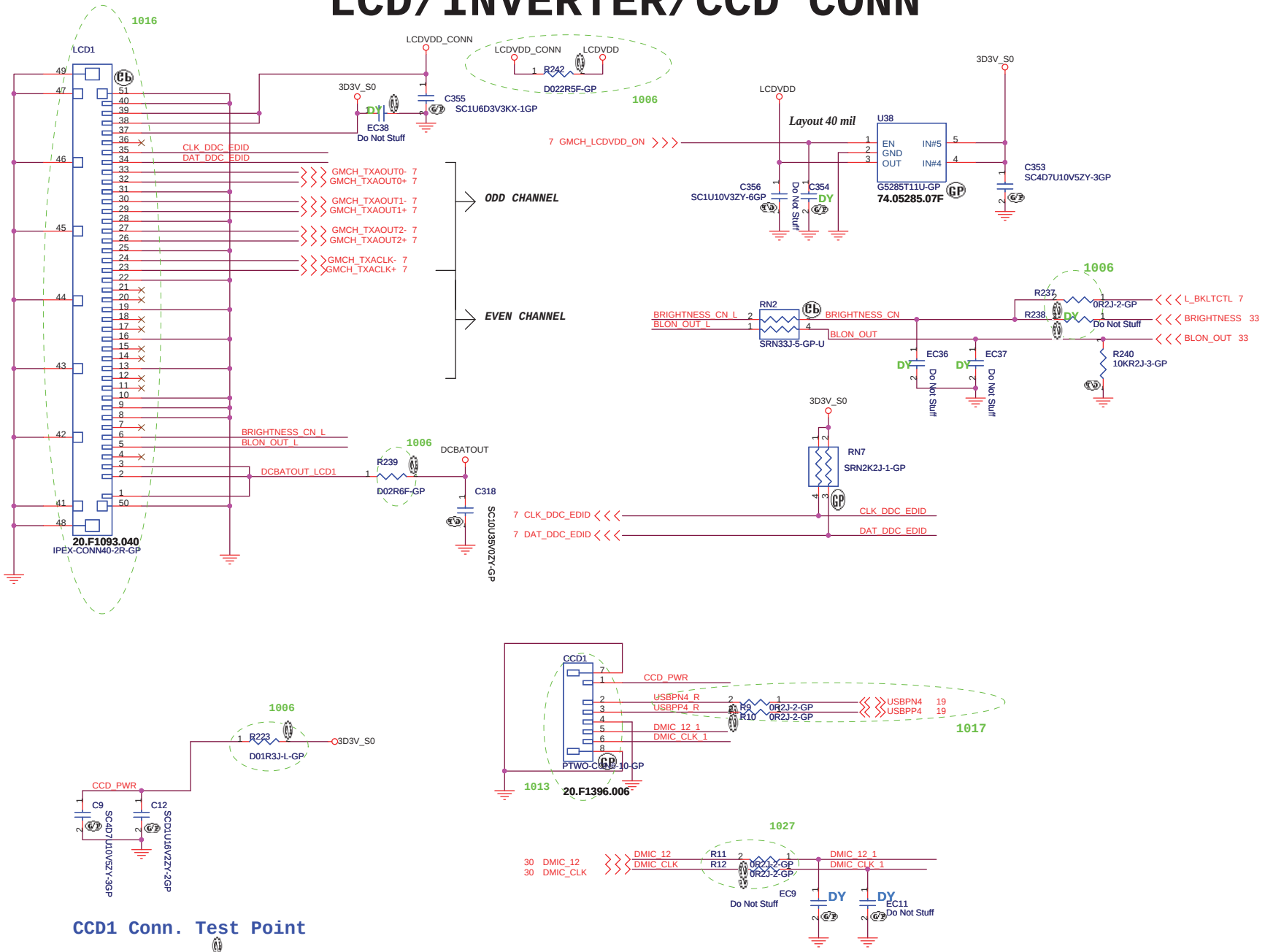
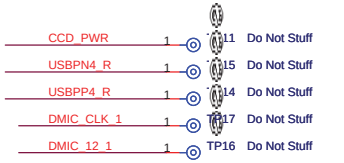
LCD/INVERTER/CCD CONN



CCD1 Conn. Test Point



UMA 2nd

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LCD CONN
Size	Document Number: SM30 — Rev: SA
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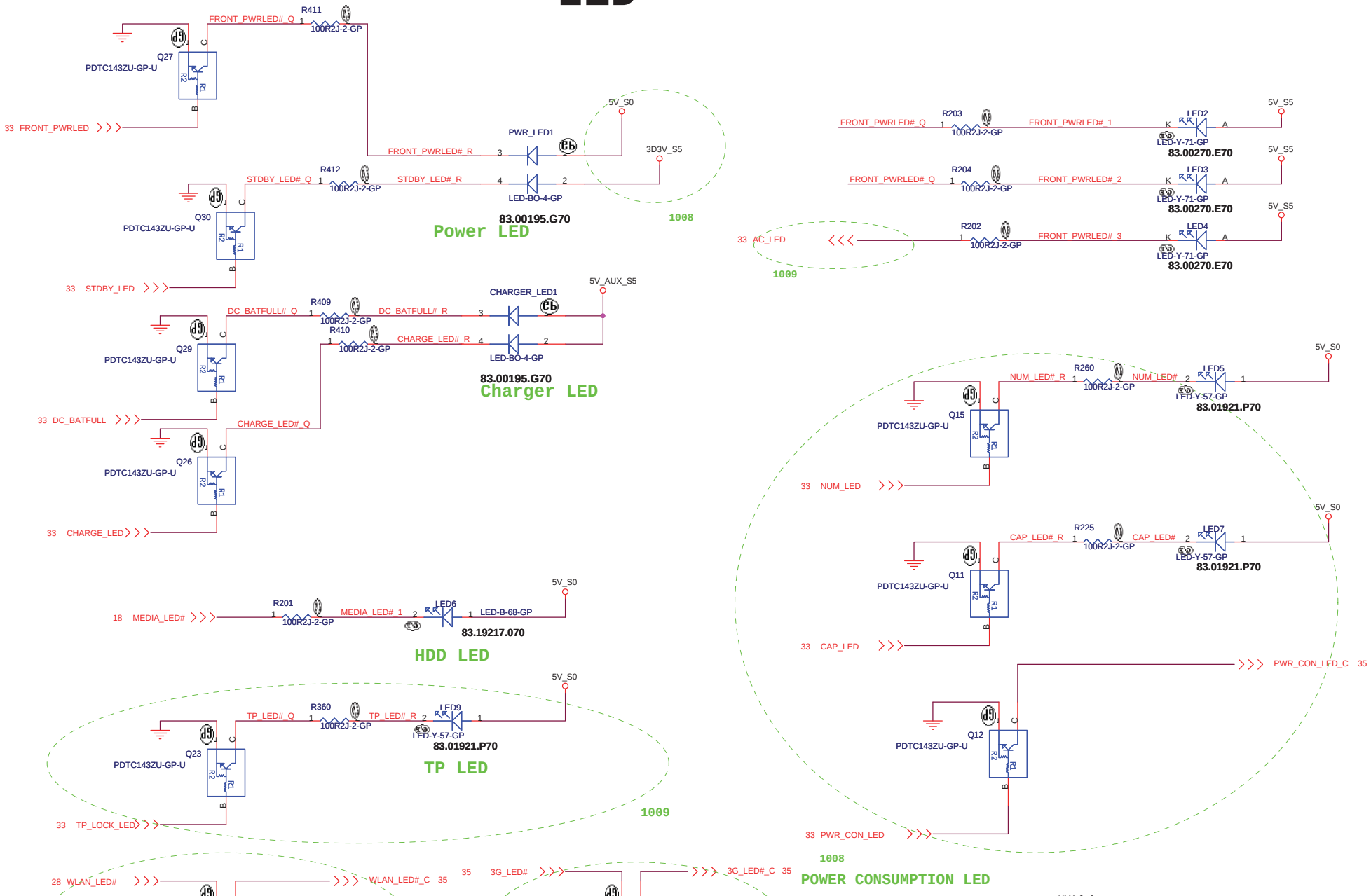
LED



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Title	***LED***	
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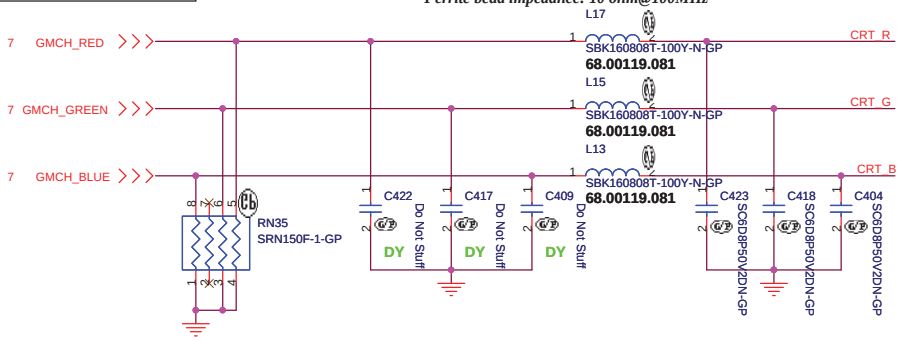
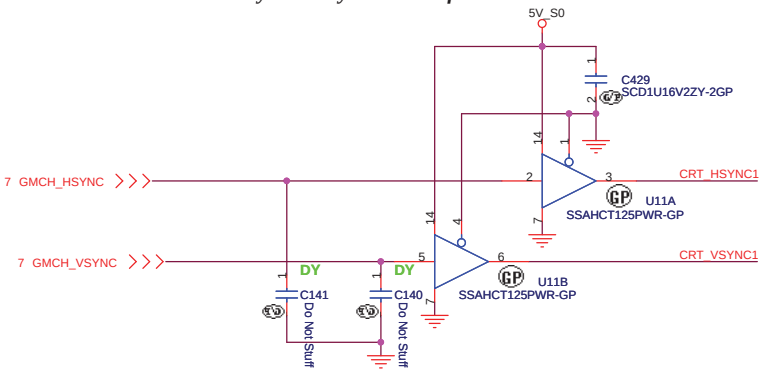
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

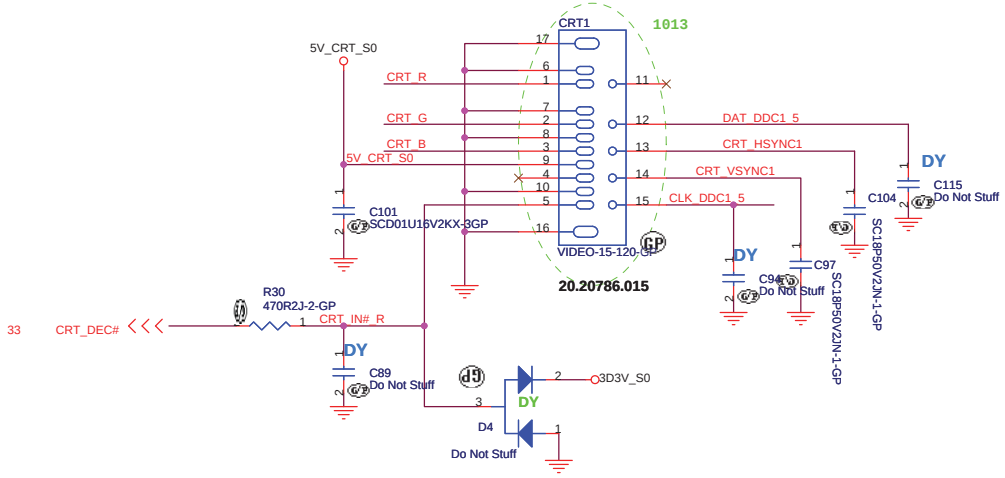


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

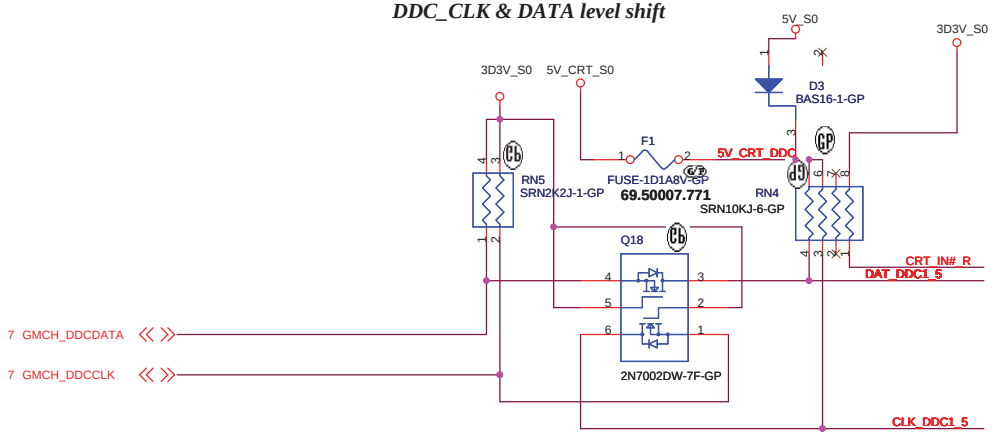
Hsync & Vsync level shift



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



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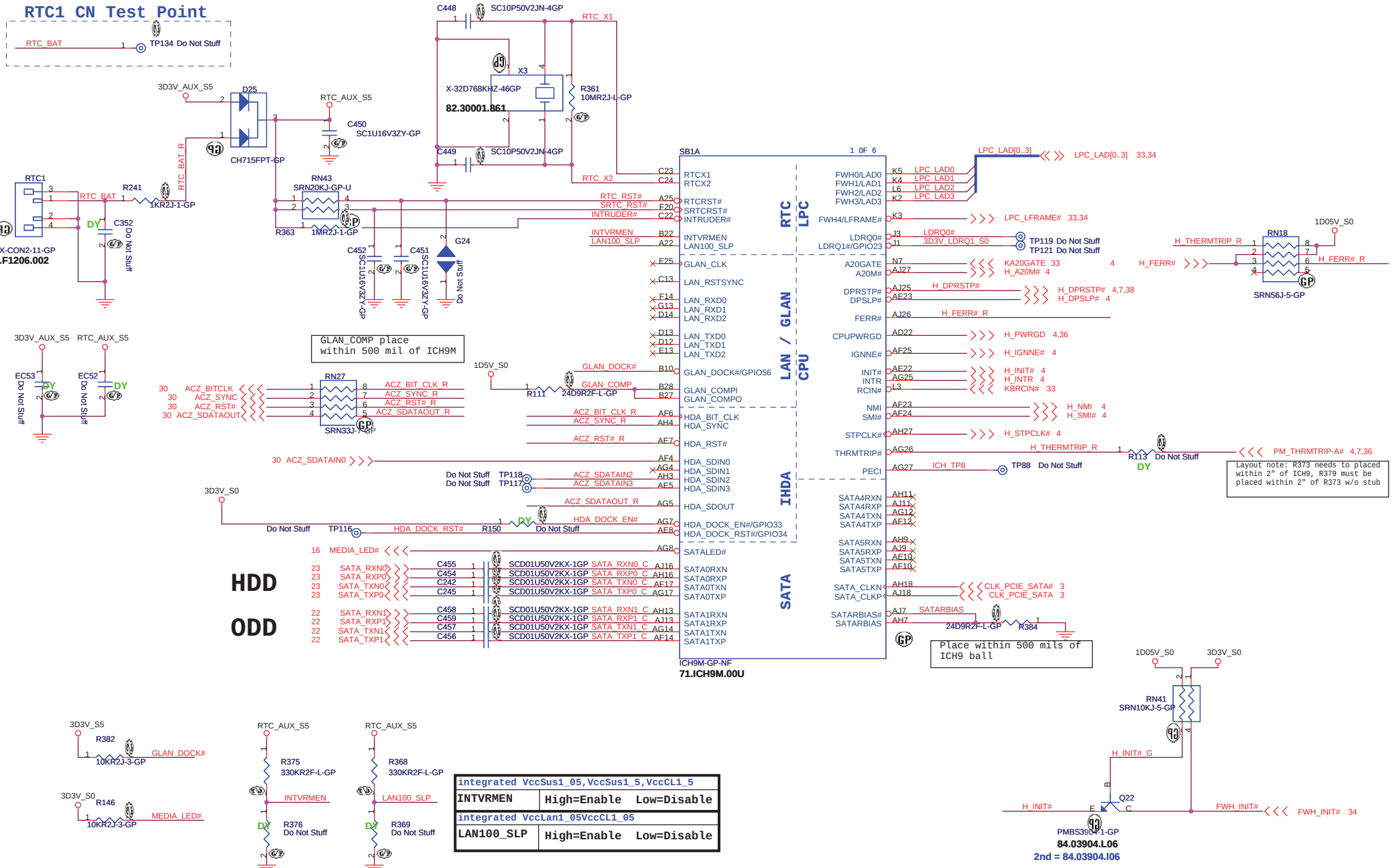
Title	***CRT CONN***	
Size	Document Number **SM30**	Rev SA
Date: Monday, October 27, 2008	Sheet 17 of 45	



UMA 2nd

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Title	*ICH9-M (1 of 4)*
Size	Document Number: SM30
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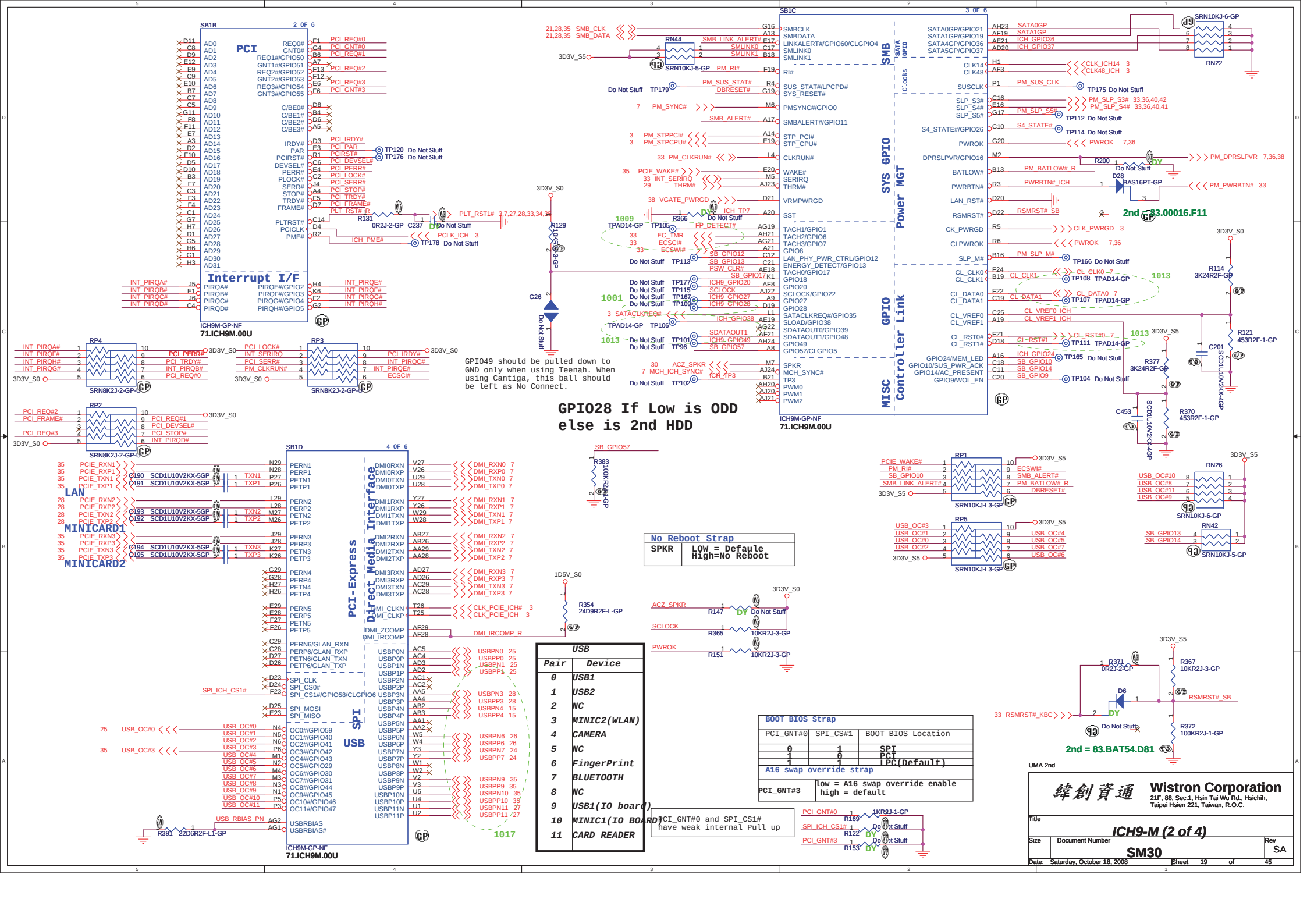
SB1B
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
SB1C
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
71.ICH9M.00U
GPIO049 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
GPIO28 If Low is ODD else is 2nd HDD
SB1D
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
71.ICH9M.00U
LAN
MINICARD1
MINICARD2
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
USB
Pair
Device
0
USB1
1
USB2
2
NC
3
MINIC2(WLAN)
4
CAMERA
5
NC
6
FingerPrint
7
BLUETOOTH
8
NC
9
USB1(IO board)
10
MINIC1(IO BOARD)
11
CARD READER
PCI_GNT#0 and SPI_CS1# have weak internal Pull up
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC(Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
2nd = 83.00016.F11
2nd = 83.BAT54.D81
UMA 2nd
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size
Document Number
SM30
Rev
SA
Date: Saturday, October 18, 2008
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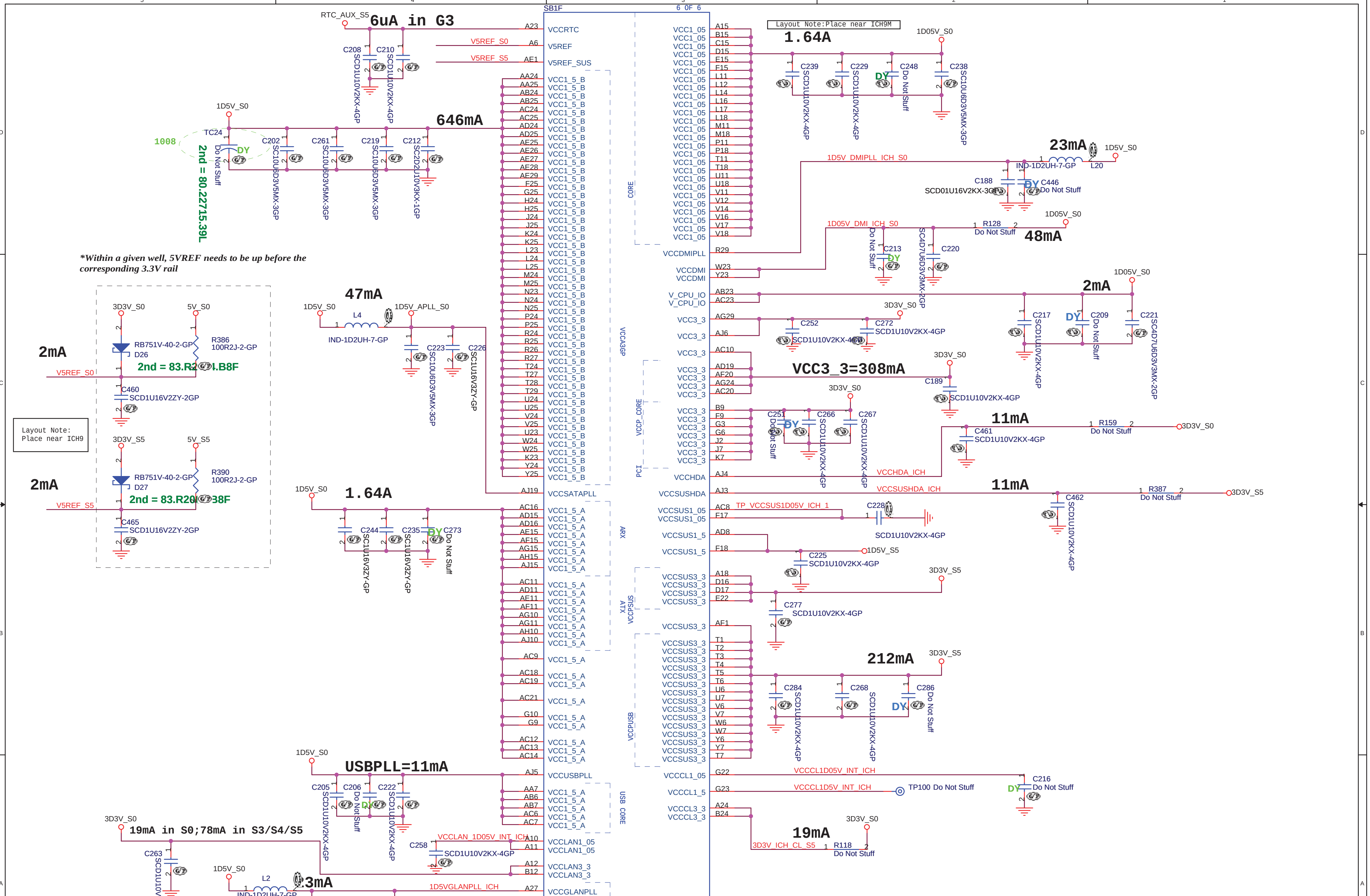

RTC_AUX_S5
6uA in G3
V5REF_S0
V5REF_S5
VCCRTC
V5REF
V5REF_SUS
SB1F
6 OF 6
1D5V_S0
646mA
1008
2nd = 80.22715.39L
TC24
Do Not Stuff
DY
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
3D3V_S0
5V_S0
RB751V-40-2-GP
D26
R386
100R2J-2-GP
2mA
2nd = 83.R2004.B8F
C460
SCD1U16V2ZY-2GP
Layout Note:
Place near ICH9
3D3V_S5
5V_S5
RB751V-40-2-GP
D27
R390
100R2J-2-GP
2nd = 83.R2004.B8F
C465
SCD1U16V2ZY-2GP
47mA
1D5V_APLL_S0
L4
IND-1D2UH-7-GP
1.64A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
VCCLAN_1D05V_INT_ICH
C258
SCD1U10V2KX-4GP
L2
IND-1D2UH-7-GP
3mA
1D5VGLANPLL_ICH
C187
Do Not Stuff
80mA
C218
SC4D7U6D3V3KX-GP
C199
Do Not Stuff
1mA
VCCSATAPLL
VCCUSBPLL
VCCLAN1_05
VCCLAN3_3
VCCGLANPLL
VCCGLAN1_5
VCCGLAN3_3
ICH9M-GP-NF
71.ICH9M.00U
CORE
VCCA3GP
VCCP_CORE
PCI
ARX
ATX
VCCPSUS
VCCPUSB
USB CORE
GLAN POWER
VCC1_05
VCCDMIPLL
VCCDMI
V_CPU_IO
VCC3_3
VCCHDA
VCCSUSHDA
VCCSUS1_05
VCCSUS1_5
VCCSUS3_3
VCCCL1_05
VCCCL1_5
VCCCL3_3
Layout Note:Place near ICH9M
1.64A
1D05V_S0
C239
SCD1U10V2KX-4GP
C229
SCD1U10V2KX-4GP
C248
Do Not Stuff
C238
SC10U6D3V5MX-3GP
23mA
1D5V_DMIPLL_ICH_S0
IND-1D2UH-7-GP
L20
C188
SCD01U16V2KX-3GP
C446
Do Not Stuff
1D5V_DMI_ICH_S0
R128
Do Not Stuff
48mA
C213
C220
SC4D7U6D3V3MX-2GP
2mA
C217
SCD1U10V2KX-4GP
C209
Do Not Stuff
C221
SC4D7U6D3V3MX-2GP
C252
SCD1U10V2KX-4GP
C272
SCD1U10V2KX-4GP
VCC3_3=308mA
C189
SCD1U10V2KX-4GP
C251
C266
C267
11mA
C461
SCD1U10V2KX-4GP
R159
Do Not Stuff
VCCHDA_ICH
VCCSUSHDA_ICH
11mA
R387
Do Not Stuff
C462
SCD1U10V2KX-4GP
TP_VCCSUS1D05V_ICH_1
C228
SCD1U10V2KX-4GP
C225
SCD1U10V2KX-4GP
C277
SCD1U10V2KX-4GP
212mA
C284
C268
C286
SCD1U10V2KX-4GP
Do Not Stuff
VCCCL1D05V_INT_ICH
VCCCL1D5V_INT_ICH
TP100 Do Not Stuff
C216
Do Not Stuff
19mA
3D3V_ICH_CL_S5
R118
Do Not Stuff

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
ICH9-M (3 of 4)		
Size	Document Number	Rev
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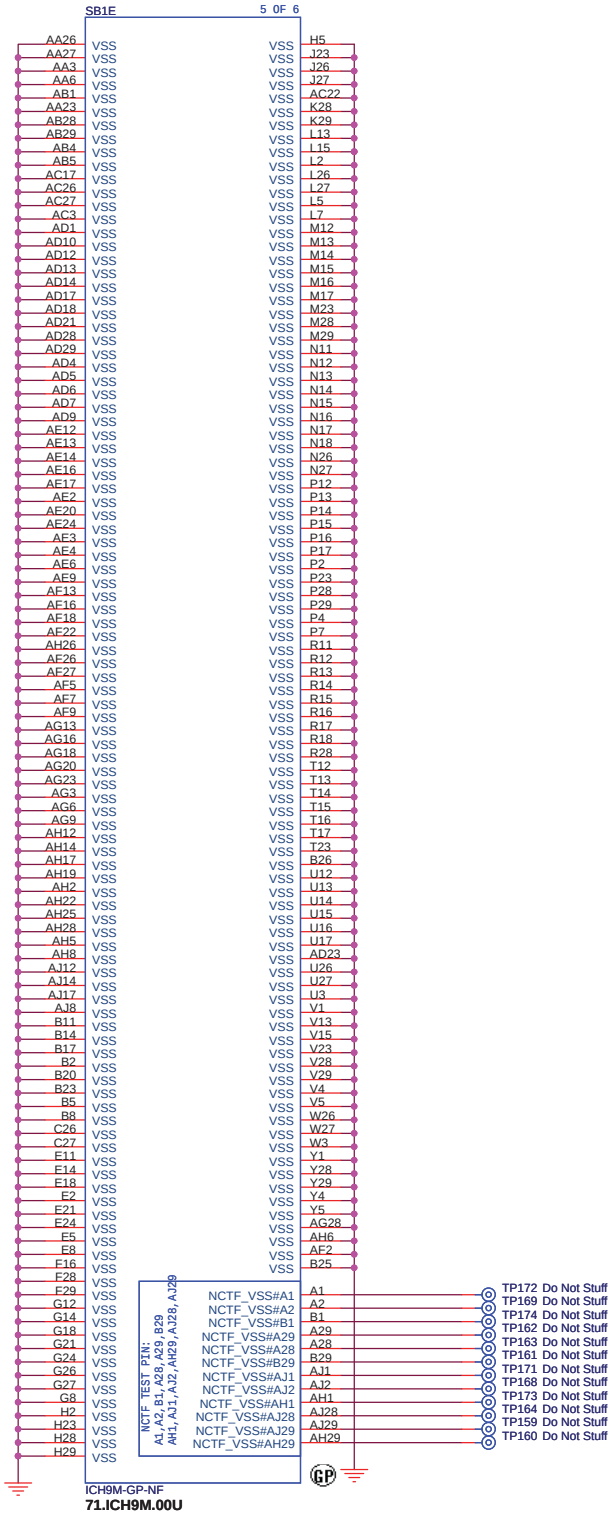

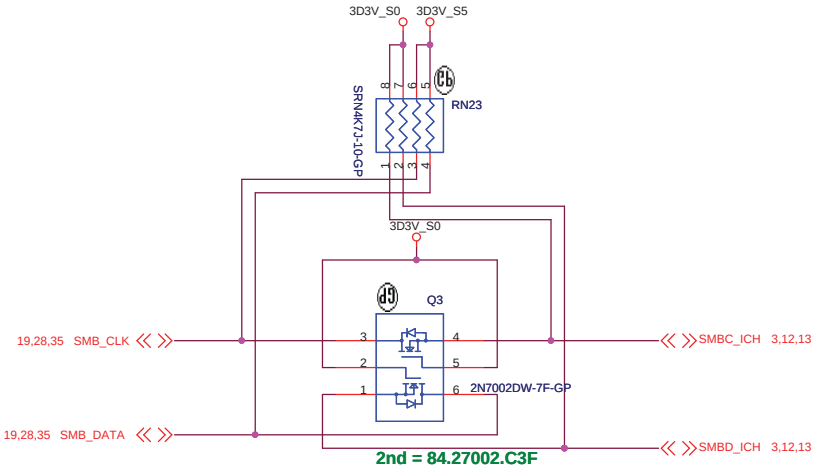

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *ICH9-M (4 of 4)*		
Size	Document Number: SM30	Rev: SA
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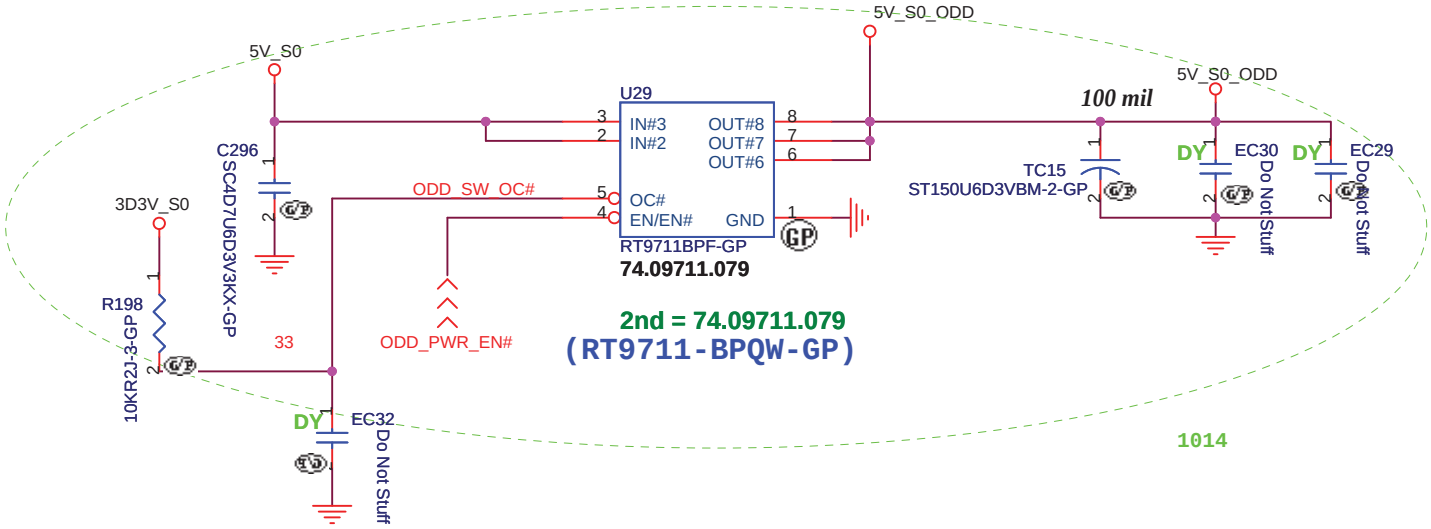
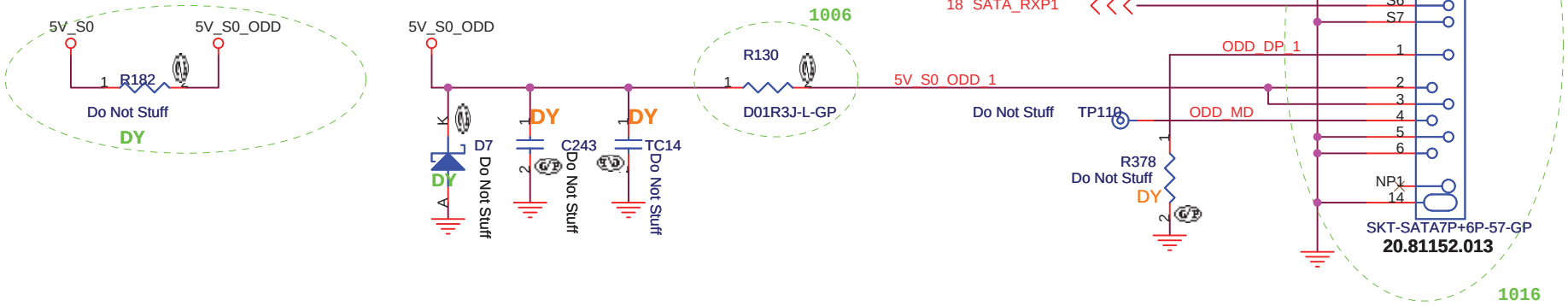
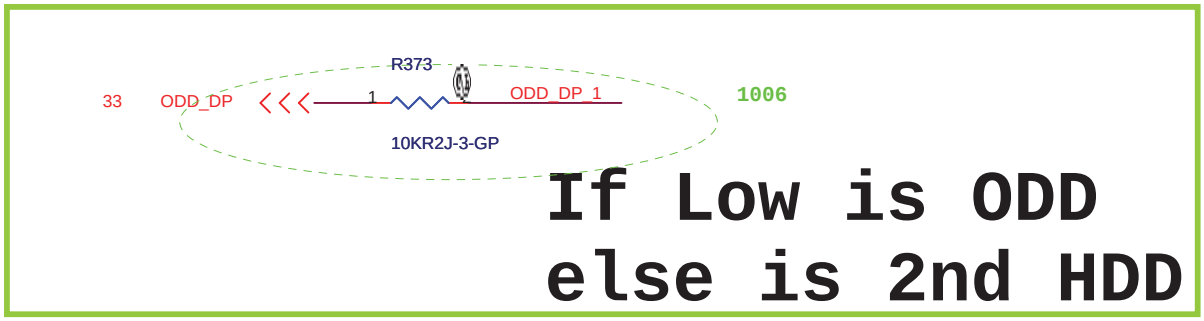
ODD Connector







UMA 2nd

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Title: ODD		
Size	Document Number: SM30	Rev: SA
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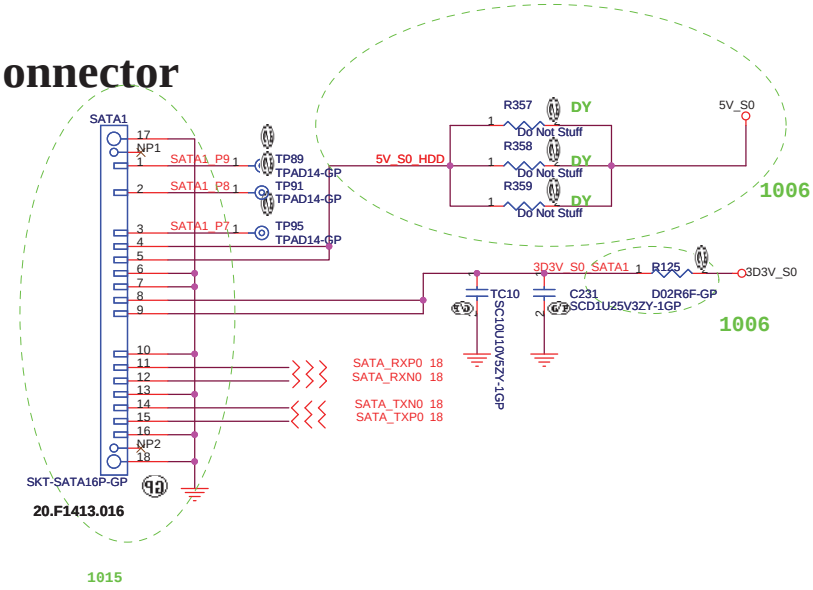
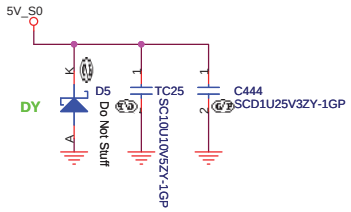
SATA Connector





UMA 2nd

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Title: HDD CONN		
Size	Document Number: SM30	Rev: SA
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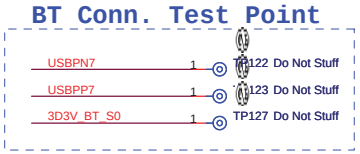
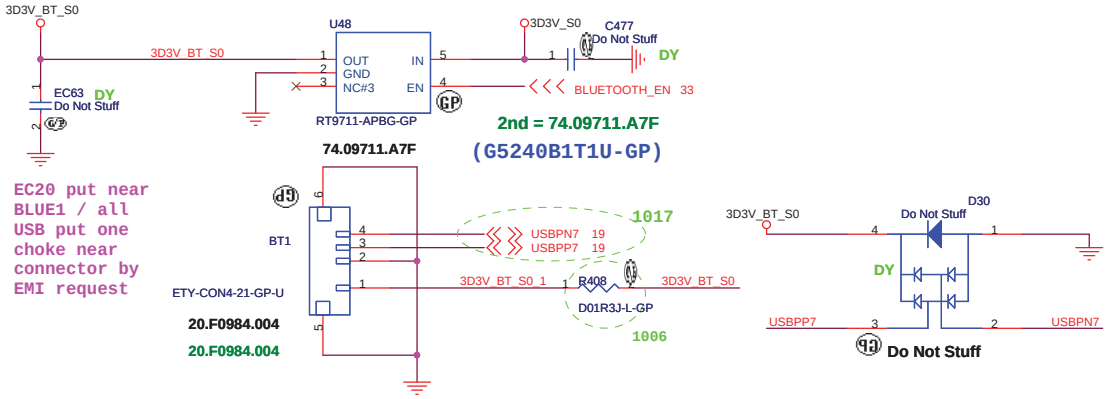
BLUETOOTH MODULE





Need check conn.

UMA 2nd

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Title: BLUETOOTH		
Size	Document Number: SM30	Rev: SA
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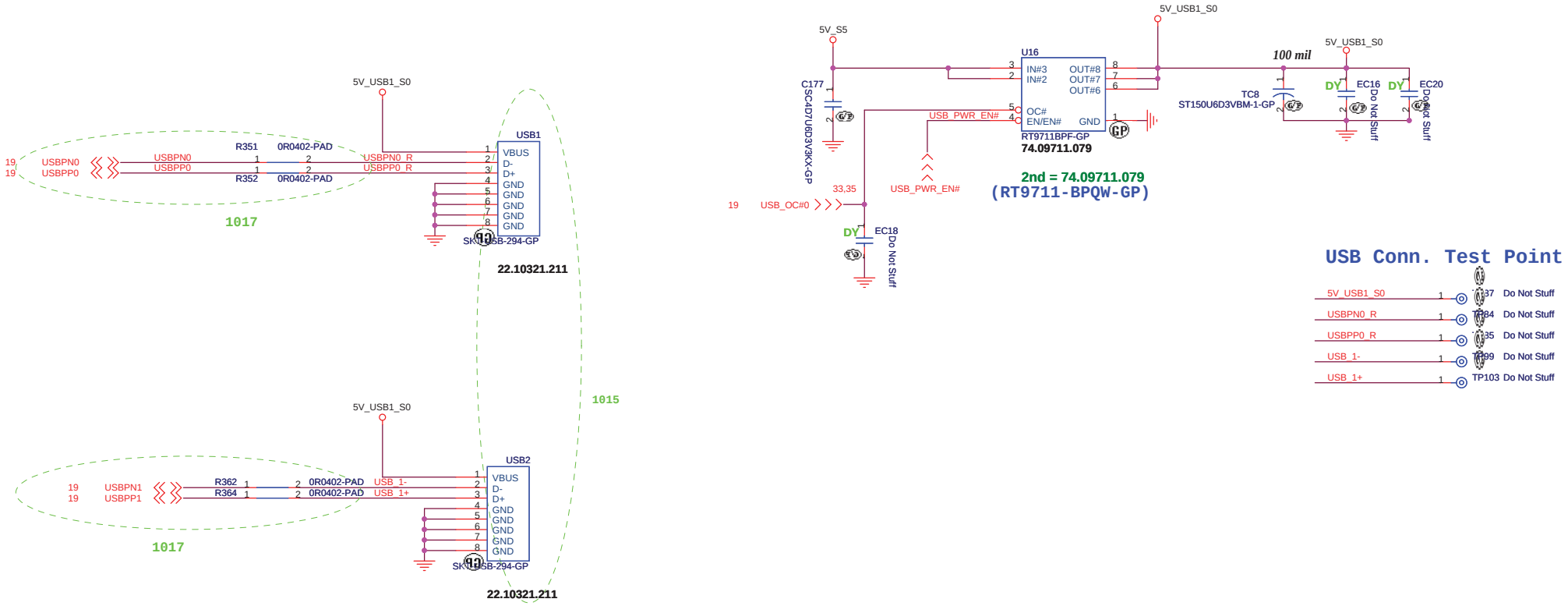

UMA 2nd

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Title: USB		
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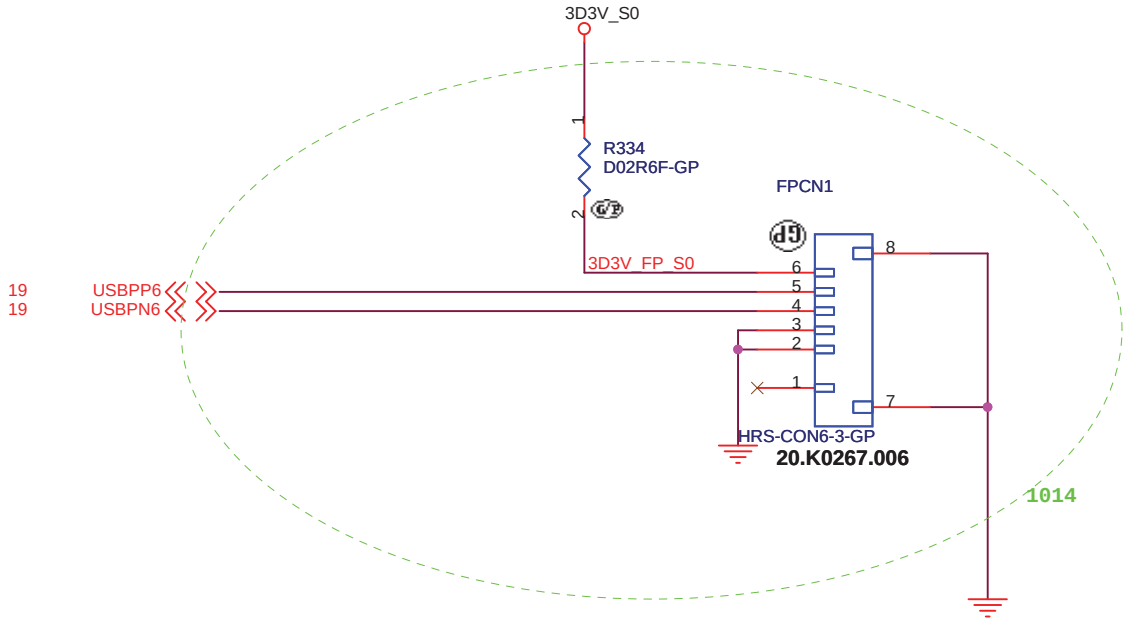
Finger printer

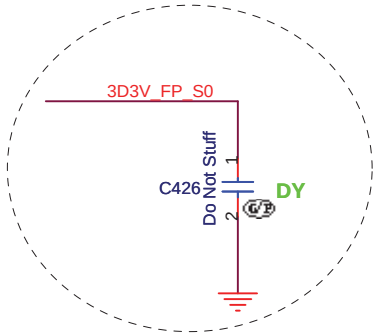
FP Conn. Test Point

3D3V_FP_S0 — 1 — TP148 Do Not Stuff

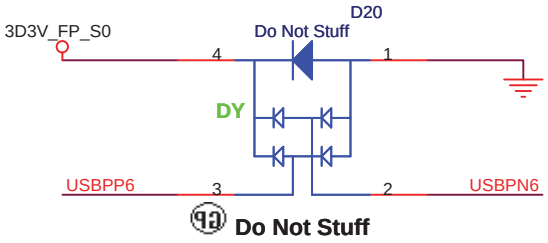
USBPP6 — 1 — TP146 Do Not Stuff

USBPN6 — 1 — TP145 Do Not Stuff





For EMI



Do Not Stuff

UMA 2nd

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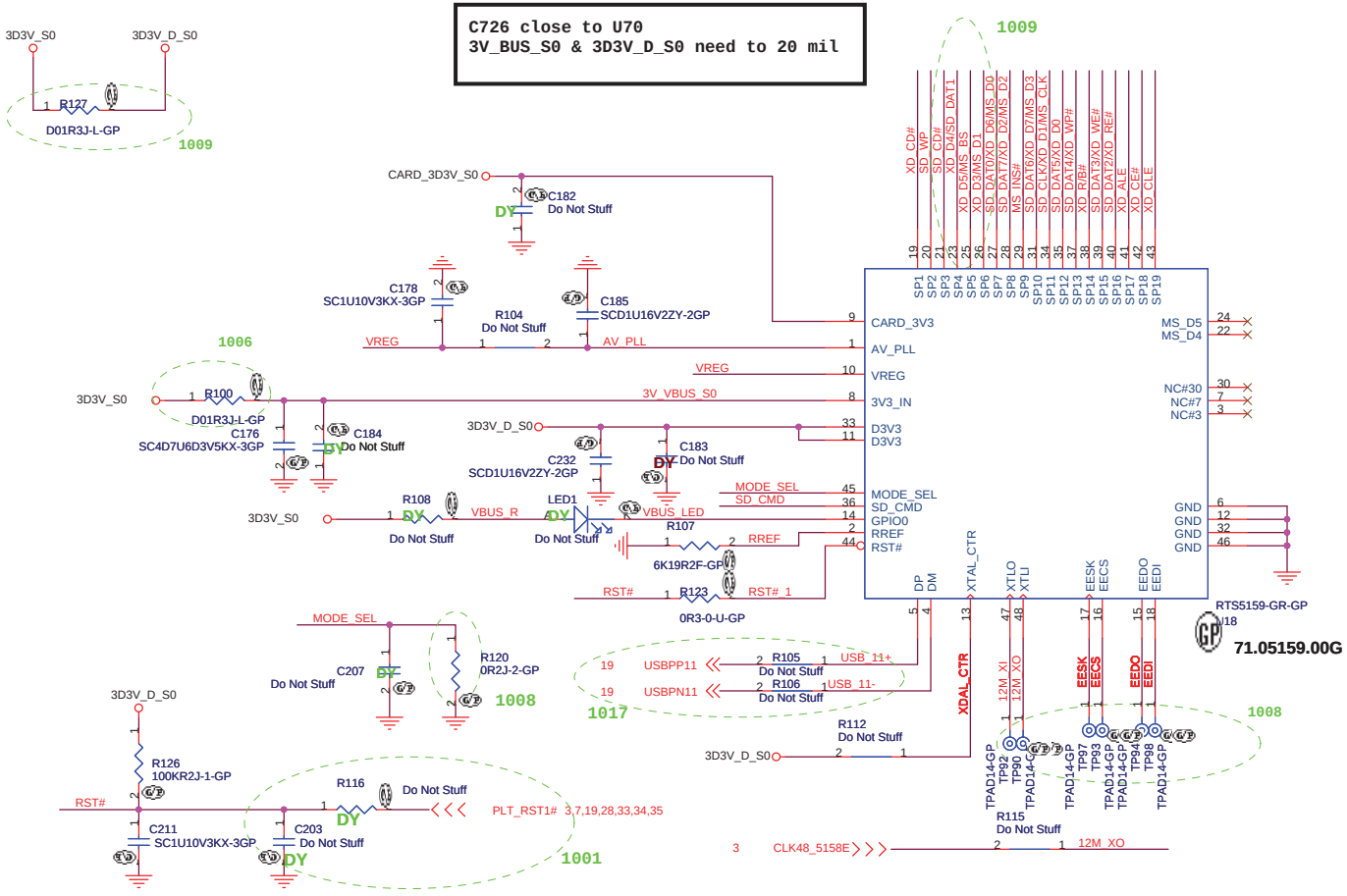
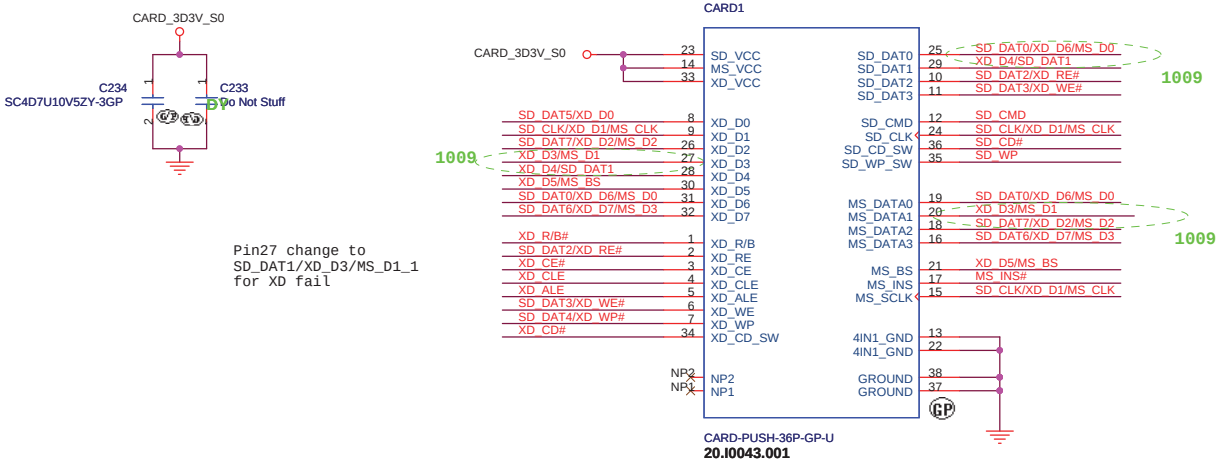
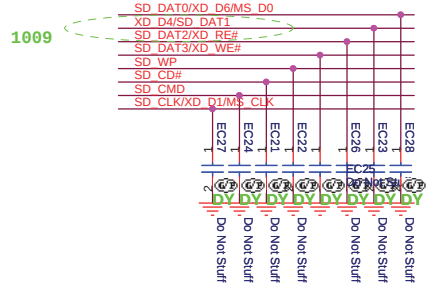
Title: *Finger Printer*		
Size	Document Number: SM30	Rev: SA
Date: Saturday, October 18, 2008	Sheet 26 of 45	

C726 close to U70
3V_BUS_S0 & 3D3V_D_S0 need to 20 mil



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)





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Title: CARDREADER- RTS5158E

Size	Document Number	Rev
	SM30	SA

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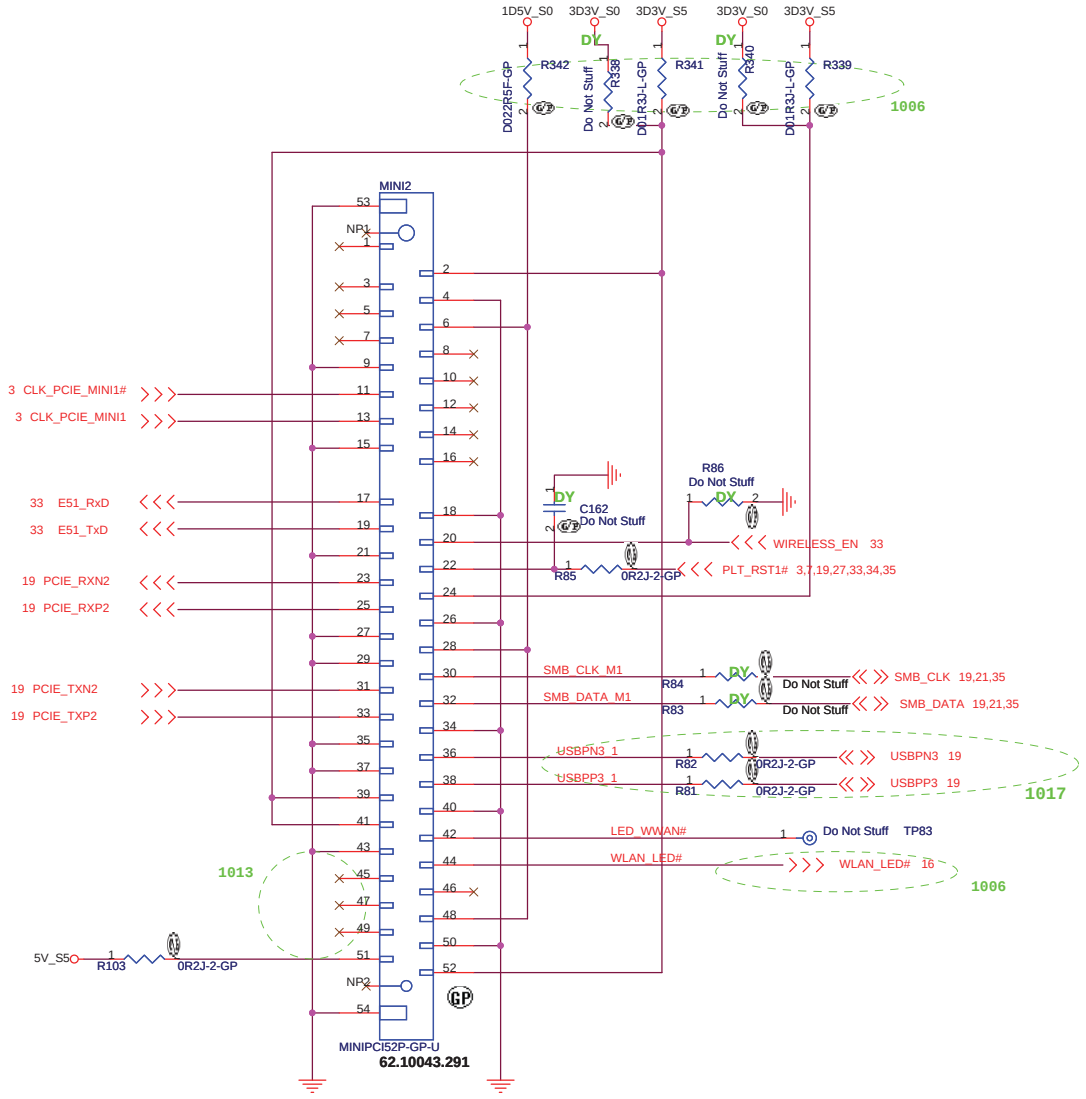
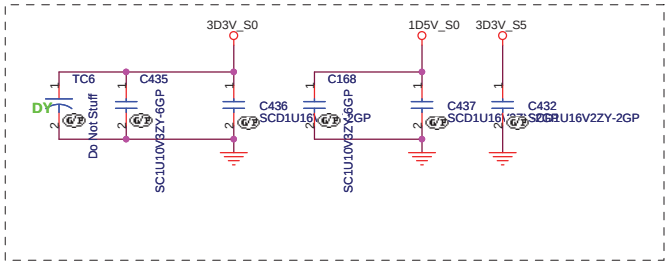
Mini Card Connector(WLAN)



Place near MINIC1



UMA 2nd

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
MINI CARD		
Size A3	Document Number SM30	Rev SA
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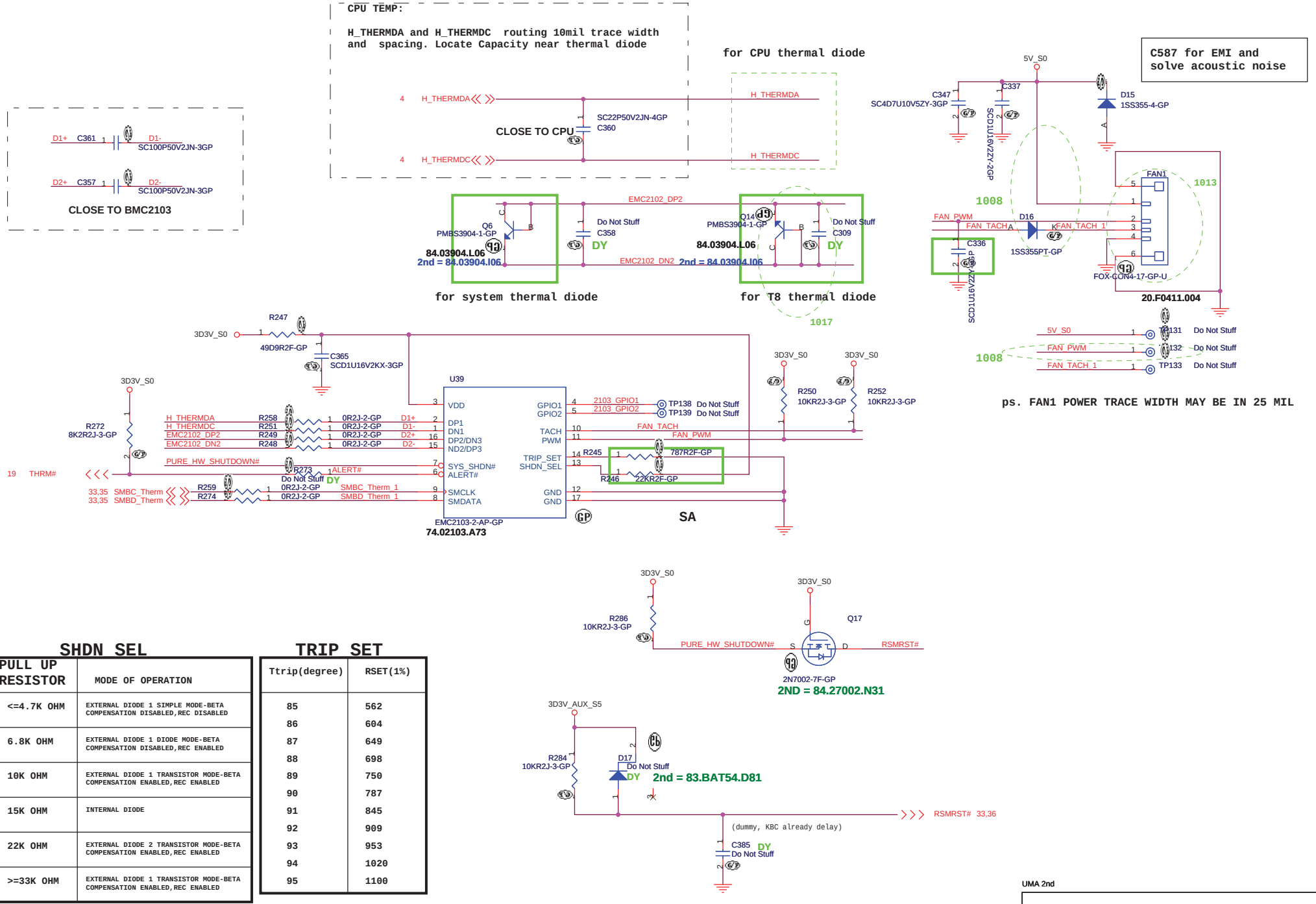


SHDN SEL

PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED,REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED,REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED

TRIP SET

Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100

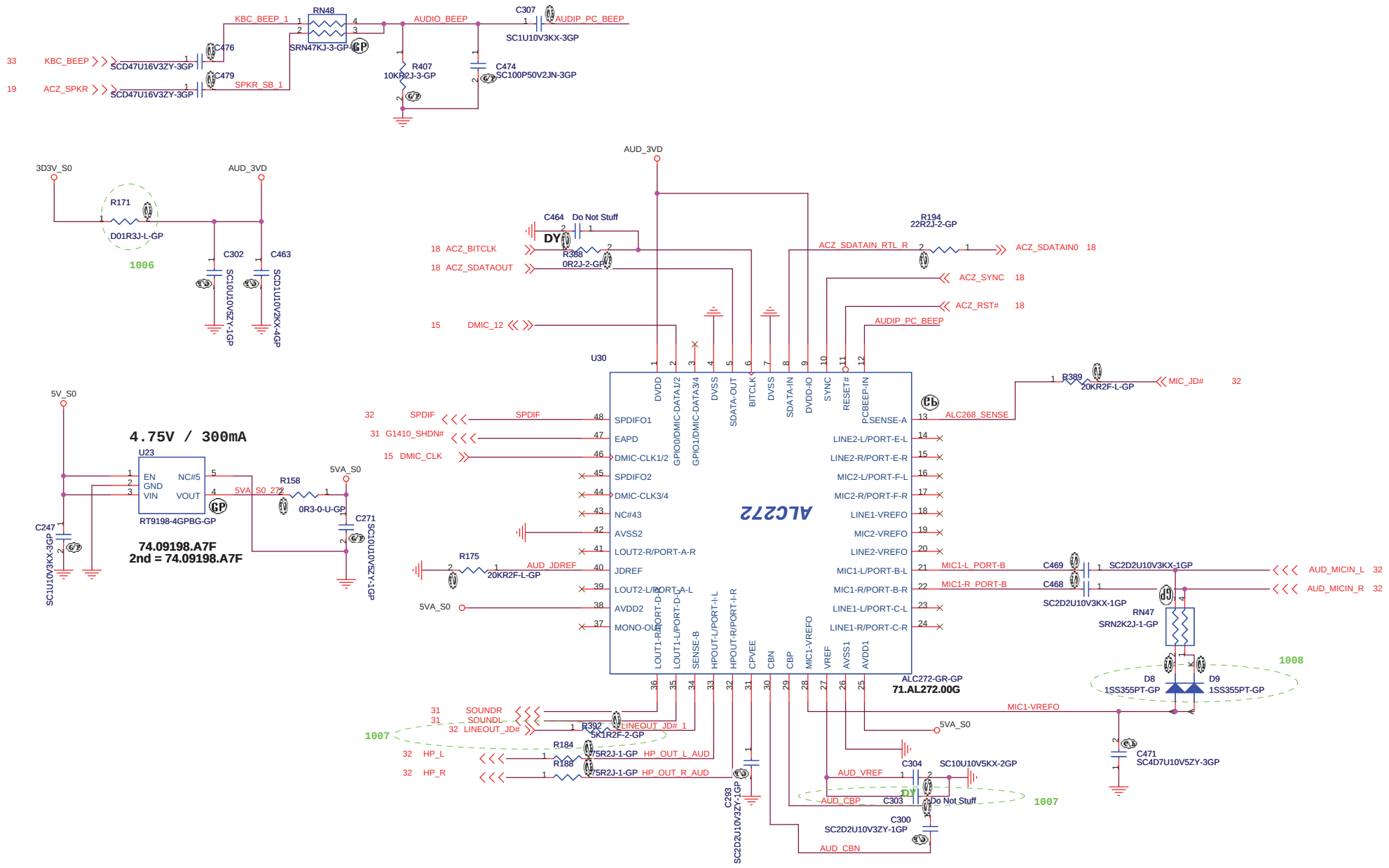
UMA 2nd

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

Size | Document Number: SM30 | Rev: SA

Date: Saturday, October 18, 2008 | Sheet 29 of 45



UMA 2nd

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Azalia codec ALC268***

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A3	SM30	SA

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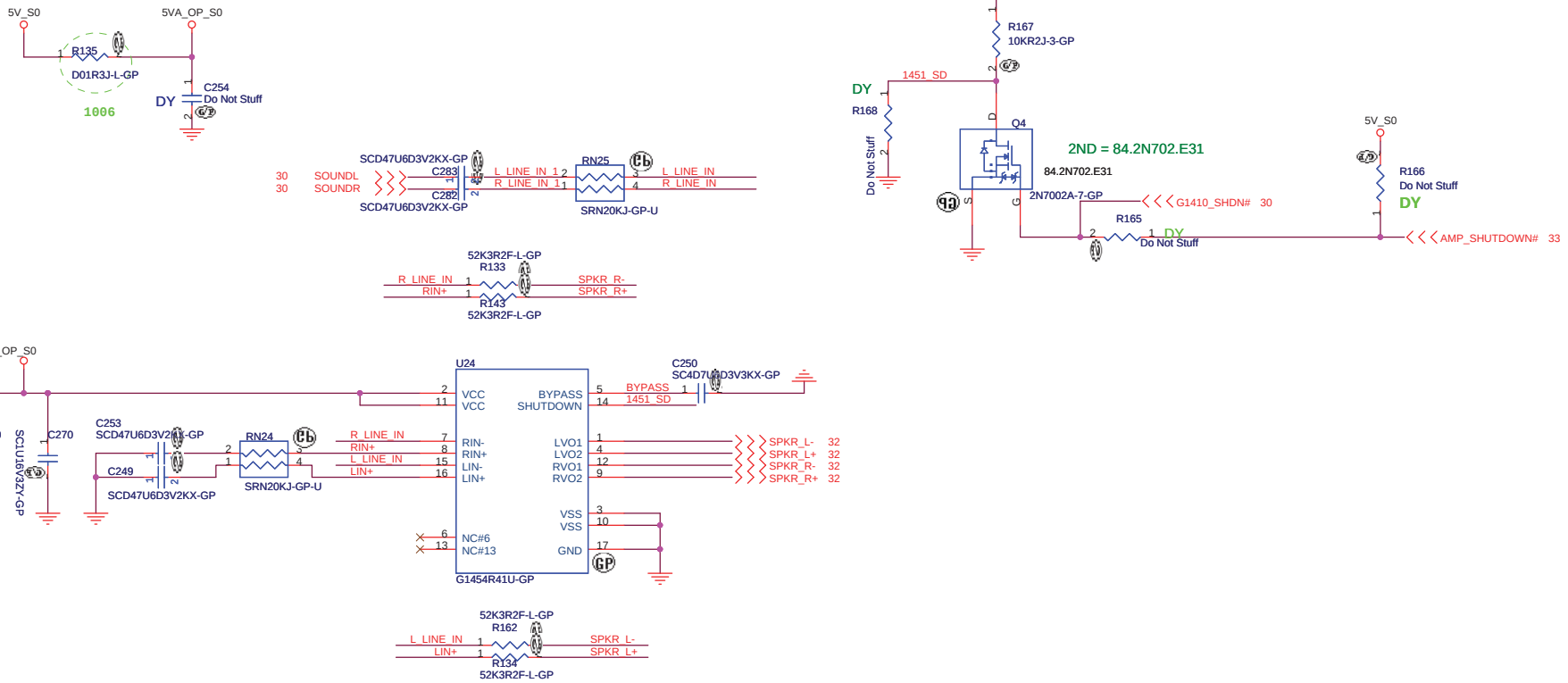
AUDIO OP AMPLIFIER



UMA 2nd

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*AUDIO AMP*	
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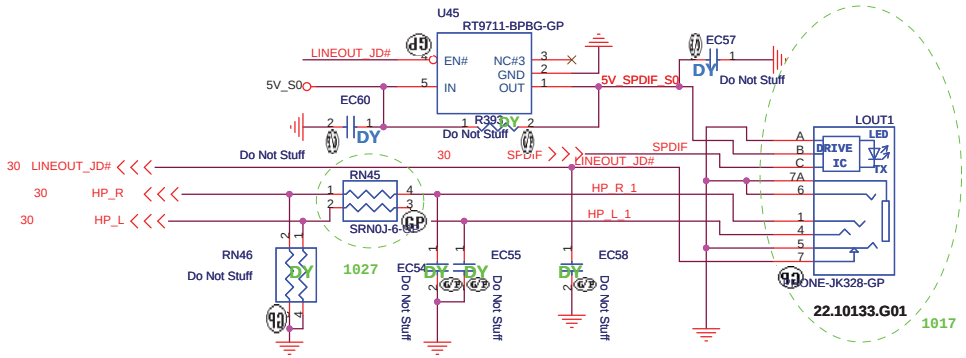
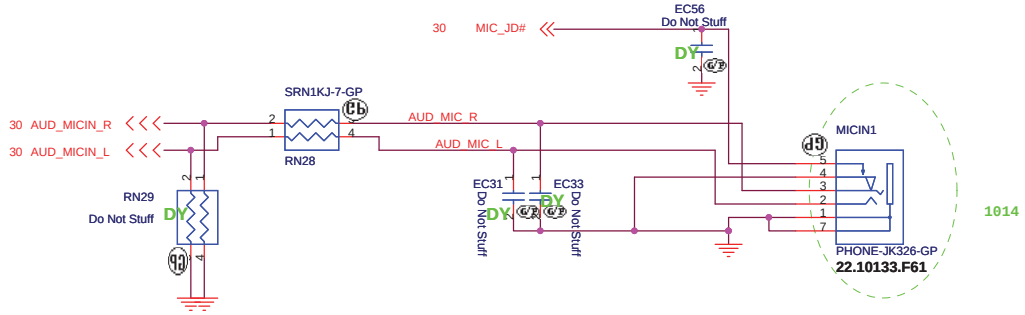
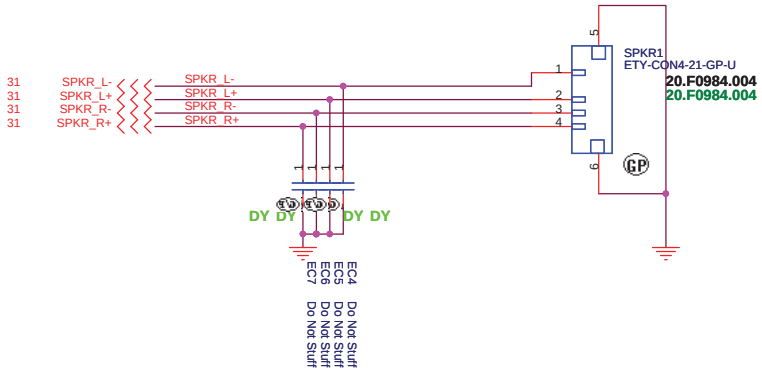
LINE OUT



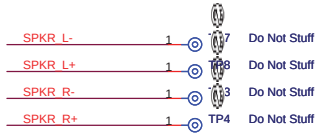
MIC IN



Internal Speaker



SPKR1 Conn. Test Point



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO JACK	
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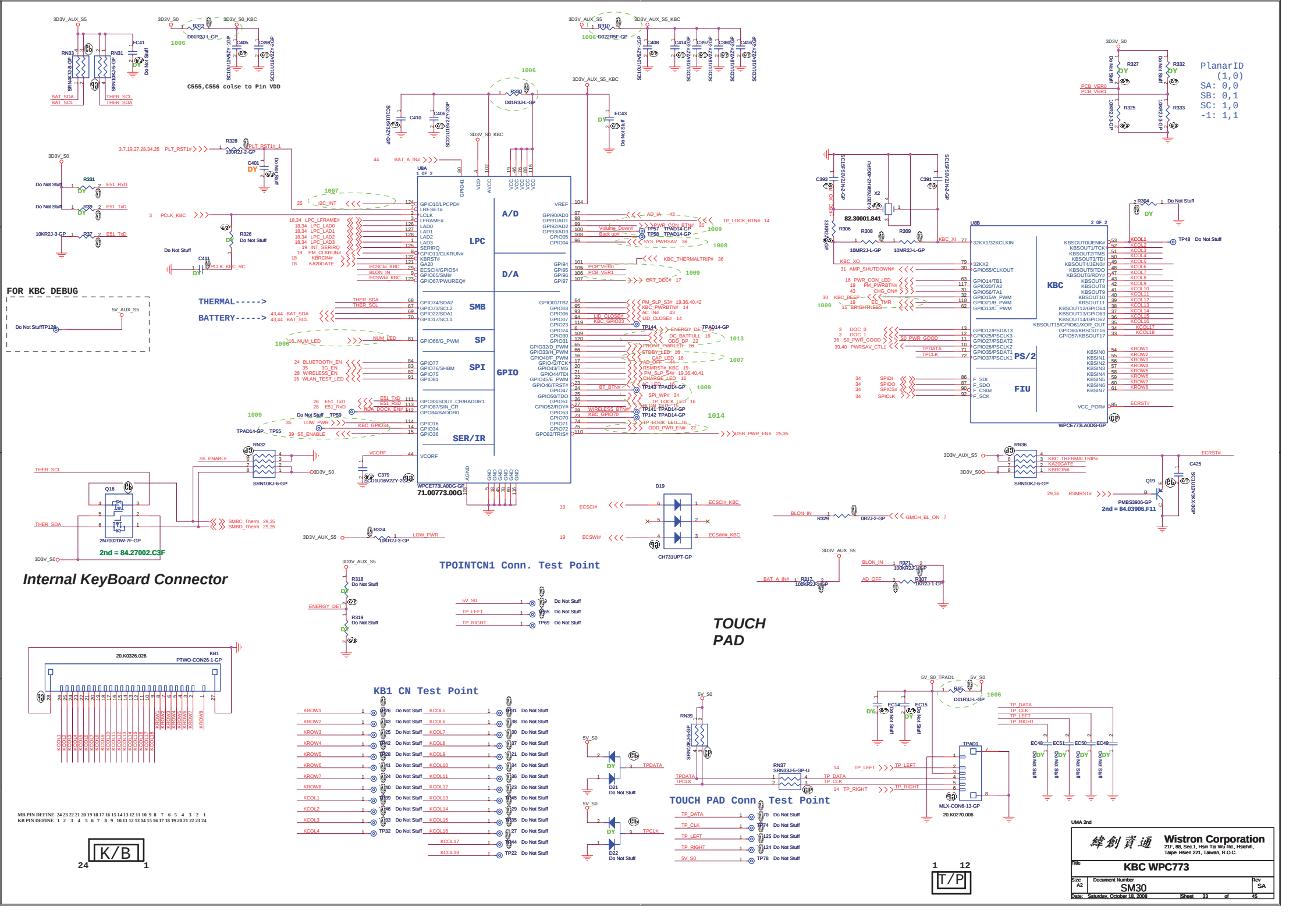
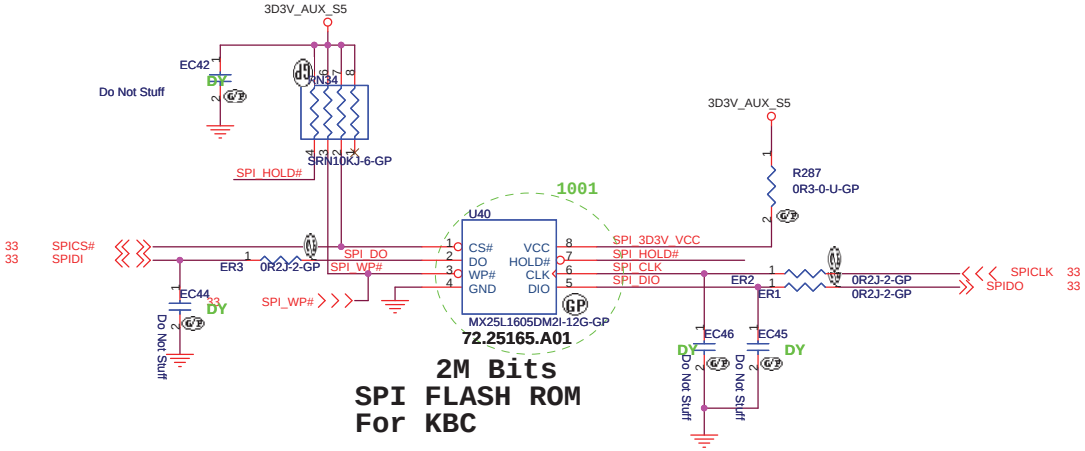
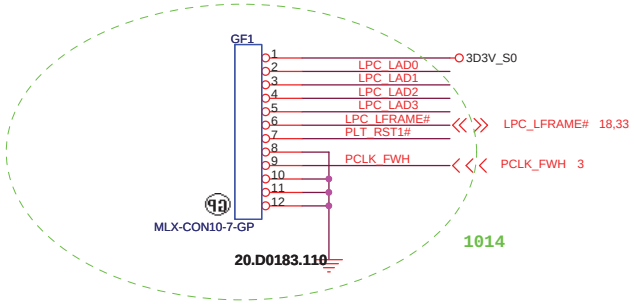

C555,C556 colse to Pin VDD
FOR KBC DEBUG
THERMAL----->
BATTERY----->
Internal KeyBoard Connector
TPOINTCN1 Conn. Test Point
TOUCH PAD
KB1 CN Test Point
TOUCH PAD Conn. Test Point
PlanarID (1,0)
SA: 0,0
SB: 0,1
SC: 1,0
-1: 1,1
U8A
U8B
WPCE773LA0DG-GP
71.00773.00G
2nd = 84.27002.C3F
2nd = 84.03906.F11
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
MB PIN DEFINE 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
K/B
T/P
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773
SM30
Saturday, October 18, 2008





GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

UMA 2nd

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BIOS & TPM***

Size | Document Number: **SM30** | Rev: SA

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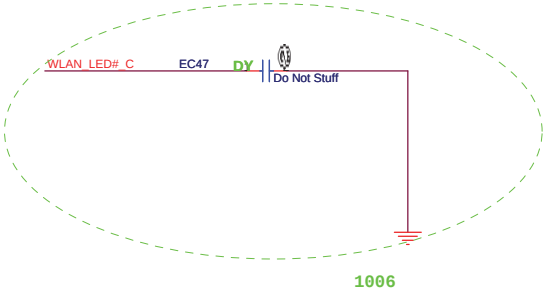
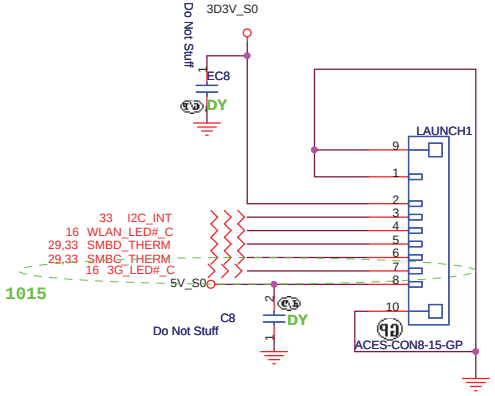
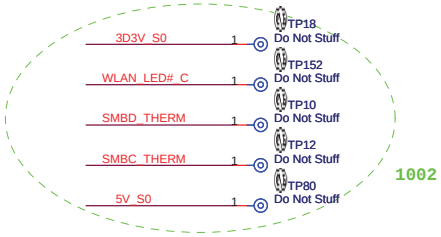
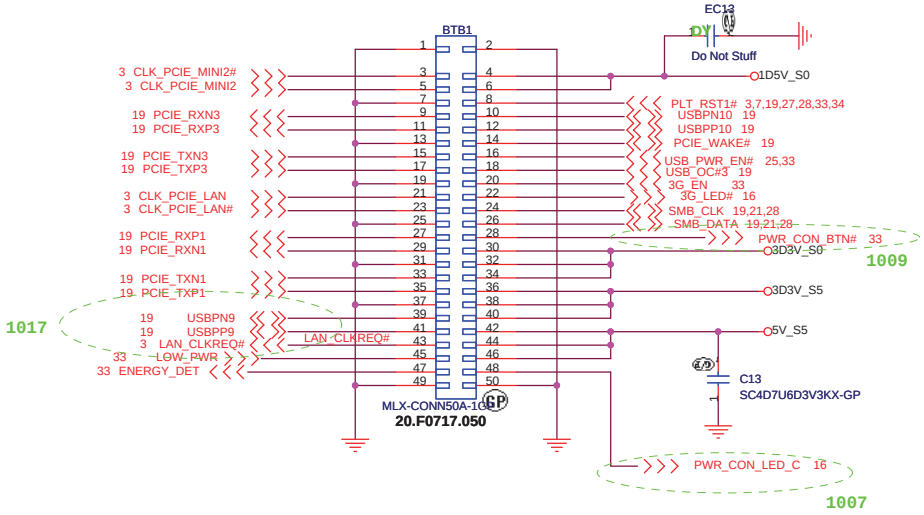
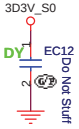


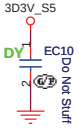


LAUNCH Test Point









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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAUNCH**

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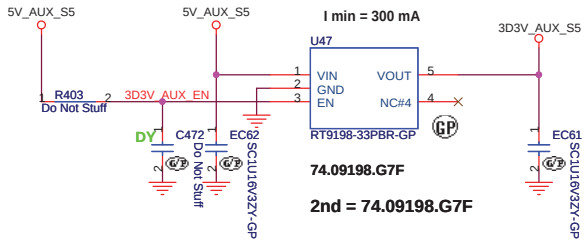
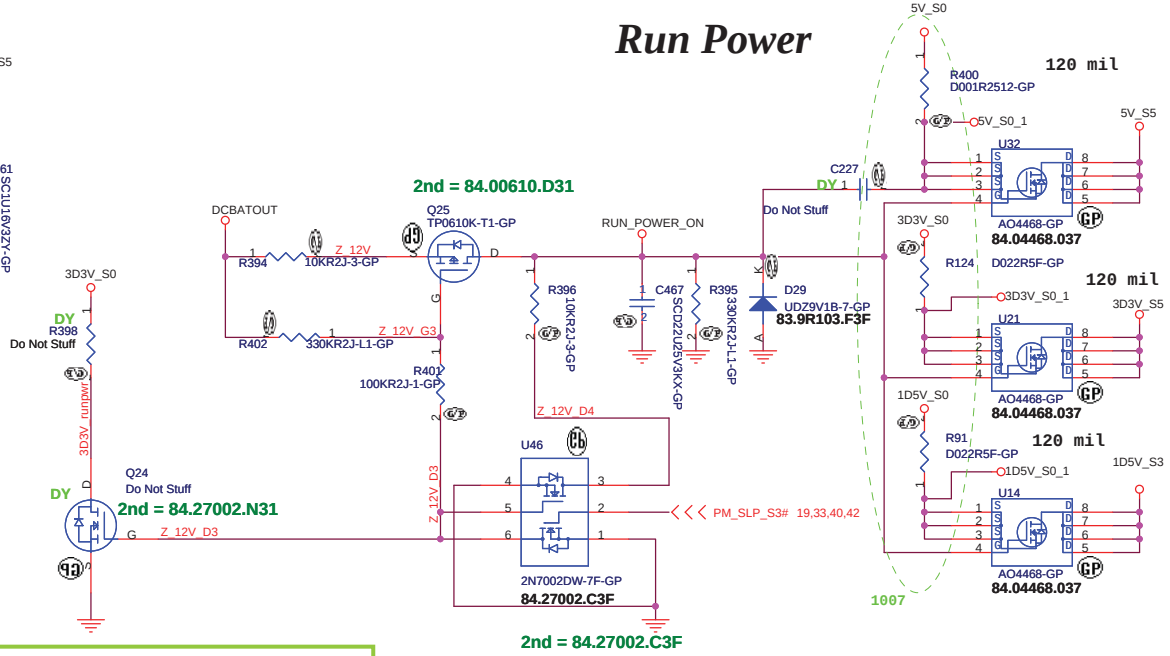
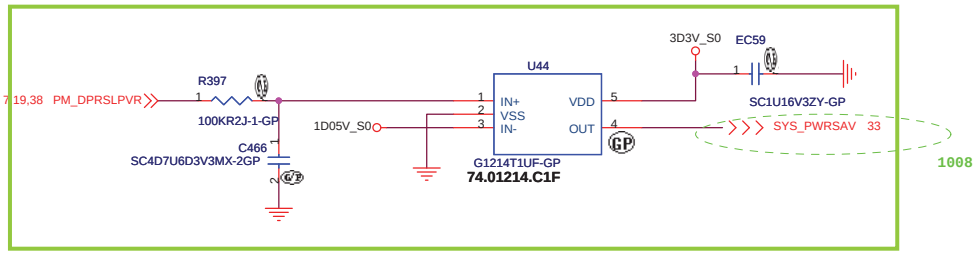
Aux Power

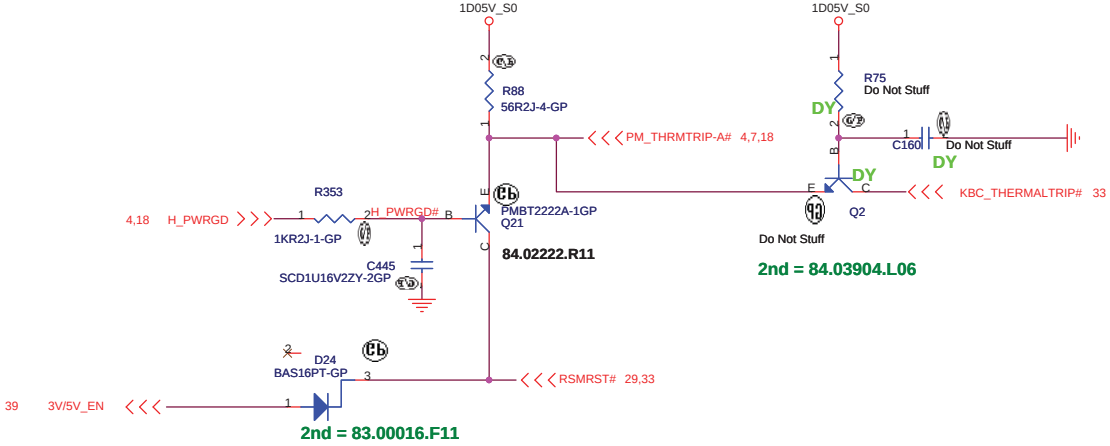
3D3V_AUX_S5

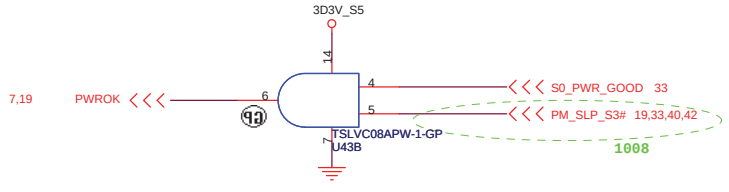


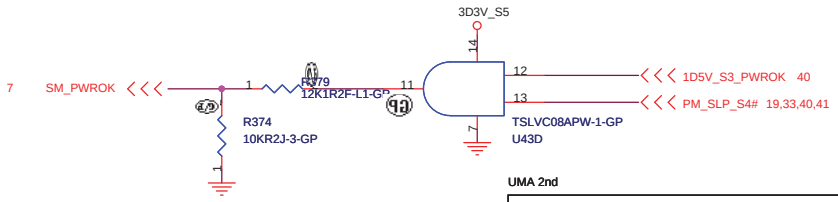
Run Power











UMA 2nd

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and 3D3V_AUX_S5**

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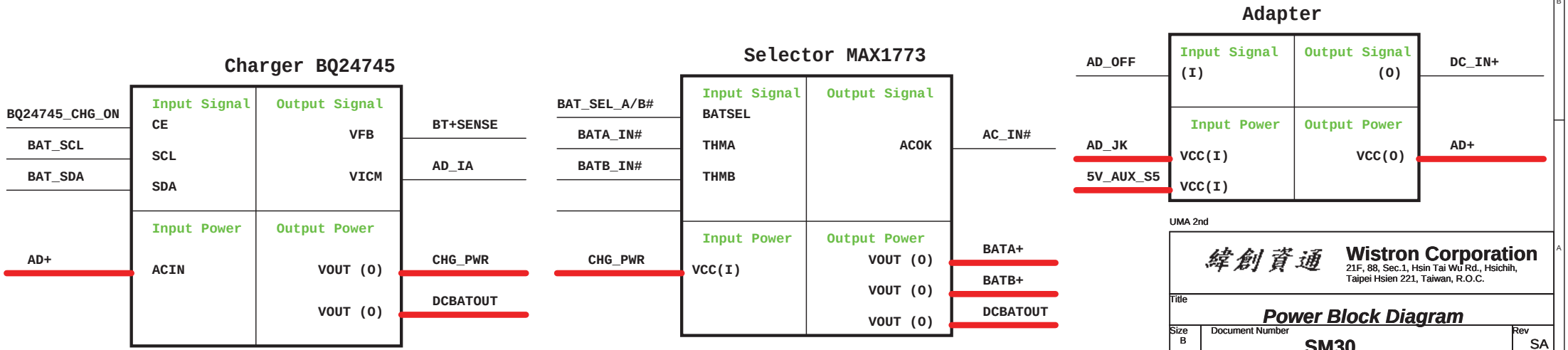

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

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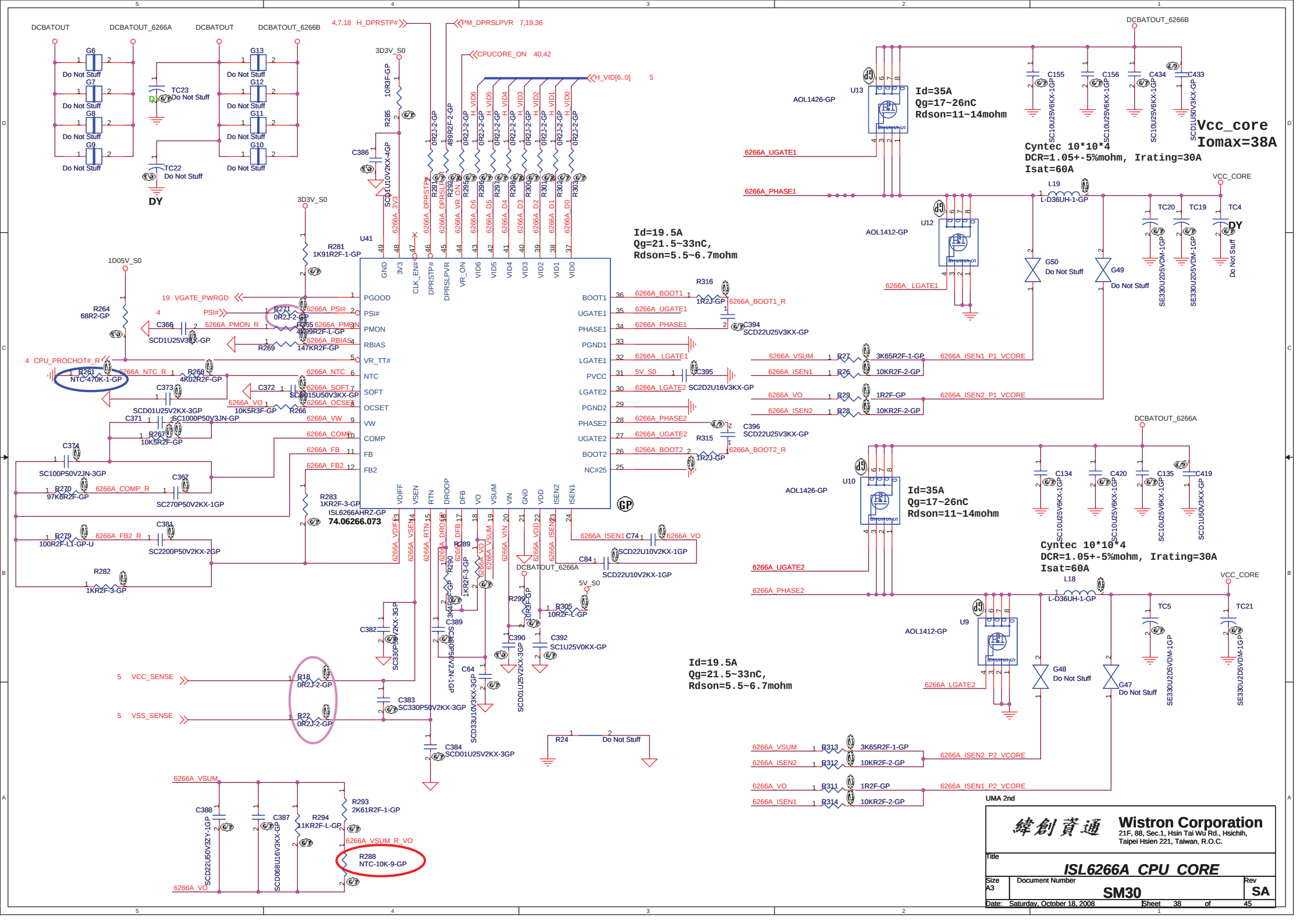
DCBATOUT
DCBATOUT_6266A
DCBATOUT
DCBATOUT_6266B
4,7,18 H_DPRSTP#
PM_DPRSLPVR 7,19,36
CPUCORE_ON 40,42
H_VID[6..0] 5
3D3V_S0
1D05V_S0
5V_S0
U41
ISL6266AHRZ-GP
74.06266.073
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Id=35A
Qg=17~26nC
Rdson=11~14mohm
AOL1426-GP
AOL1412-GP
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
VCC_CORE
DY
Do Not Stuff
UMA 2nd
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A CPU CORE
SM30
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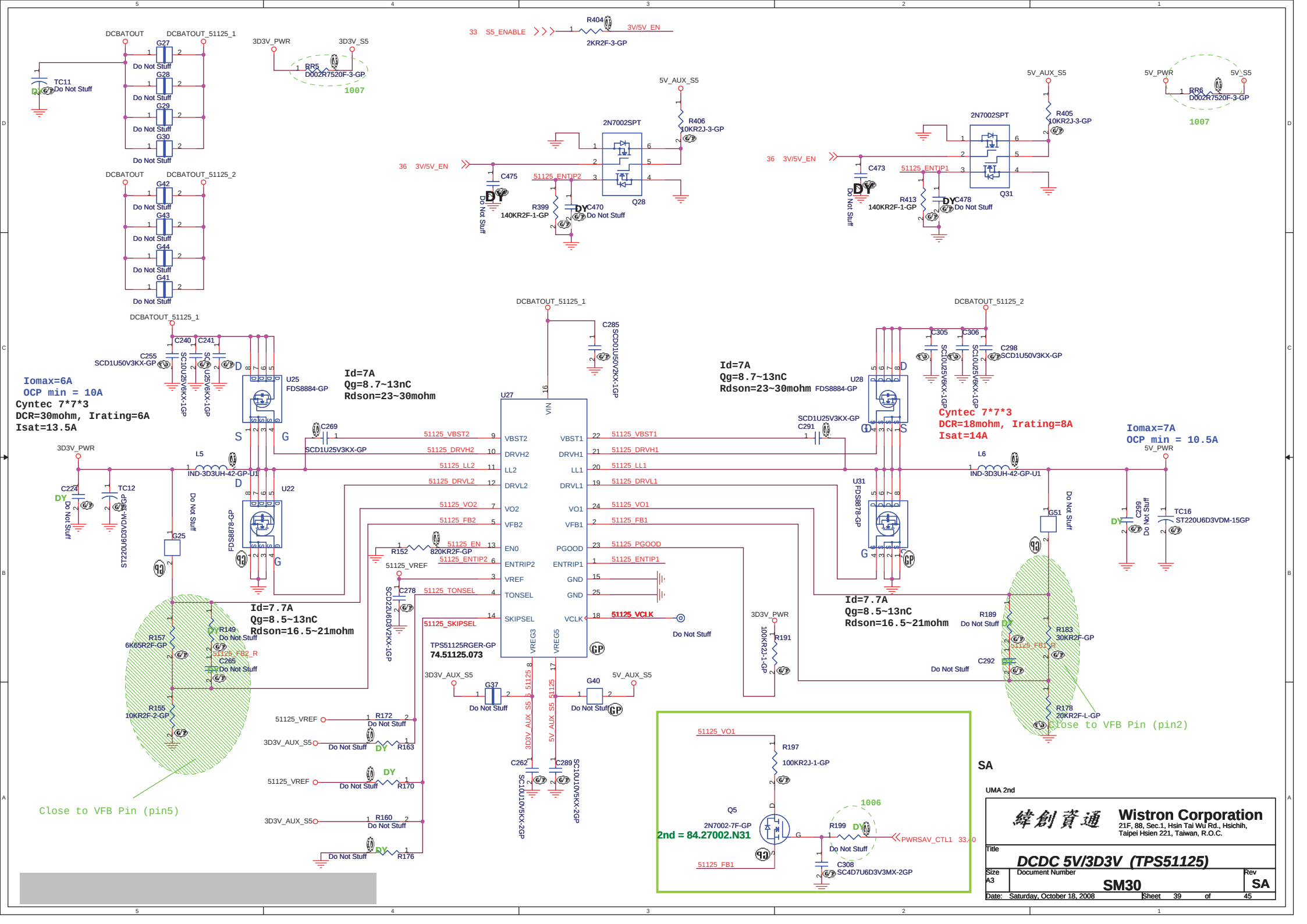
DCBATOUT
DCBATOUT_51125_1
DCBATOUT_51125_2
3D3V_PWR
3D3V_S5
5V_AUX_S5
5V_PWR
5V_S5
33 S5_ENABLE
36 3V/5V_EN
3V/5V_EN
R404
2KR2F-3-GP
RR5
RR6
D002R7520F-3-GP
1007
2N7002SPT
R406
10KR2J-3-GP
R405
C475
51125_ENTIP2
R399
140KR2F-1-GP
C470
Q28
C473
51125_ENTIP1
R413
C478
Q31
Do Not Stuff
DY
TC11
G27
G28
G29
G30
G42
G43
G44
G41
G25
G37
G40
G51
C240
C241
C255
SCD1U50V3KX-GP
SC1U25V6KX-1GP
U25
FDS8884-GP
C269
SCD1U25V3KX-GP
L5
IND-3D3UH-42-GP-U1
C224
TC12
ST220U6D3VDM-15GP
U22
FDS8878-GP
R152
820KR2F-GP
C278
SCD220U6D3V2KX-1GP
R157
6K65R2F-GP
R149
C265
R155
10KR2F-2-GP
R172
R163
R170
R160
R176
C262
C289
SC1U10V5KX-2GP
U27
TPS51125RGER-GP
74.51125.073
C285
SCD01U50V2KX-1GP
R191
100KR2J-1-GP
C291
U28
C305
C306
C298
SC1U25V6KX-1GP
Cyntec 7*7*3
DCR=18mohm, Irating=8A
Isat=14A
U31
L6
C299
TC16
ST220U6D3VDM-15GP
R189
R183
30KR2F-GP
C292
R178
20KR2F-L-GP
Close to VFB Pin (pin2)
Close to VFB Pin (pin5)
Iomax=6A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Iomax=7A
OCP min = 10.5A
Q5
2N7002-7F-GP
2nd = 84.27002.N31
R197
100KR2J-1-GP
R199
PWRSAV_CTL1
C308
SC4D7U6D3V3MX-2GP
1006
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
ENTRIP2
VREF
TONSEL
SKIPSEL
VIN
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
GND
PGOOD
ENTRIP1
VCLK
VREG3
VREG5
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_VREF
51125_ENTIP2
51125_TONSEL
51125_SKIPSEL
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_PGOOD
51125_ENTIP1
51125_VCLK
51125_FB1_R
3D3V_AUX_S5
5V_AUX_S5
SA
UMA 2nd
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Size A3
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SM30
Rev SA
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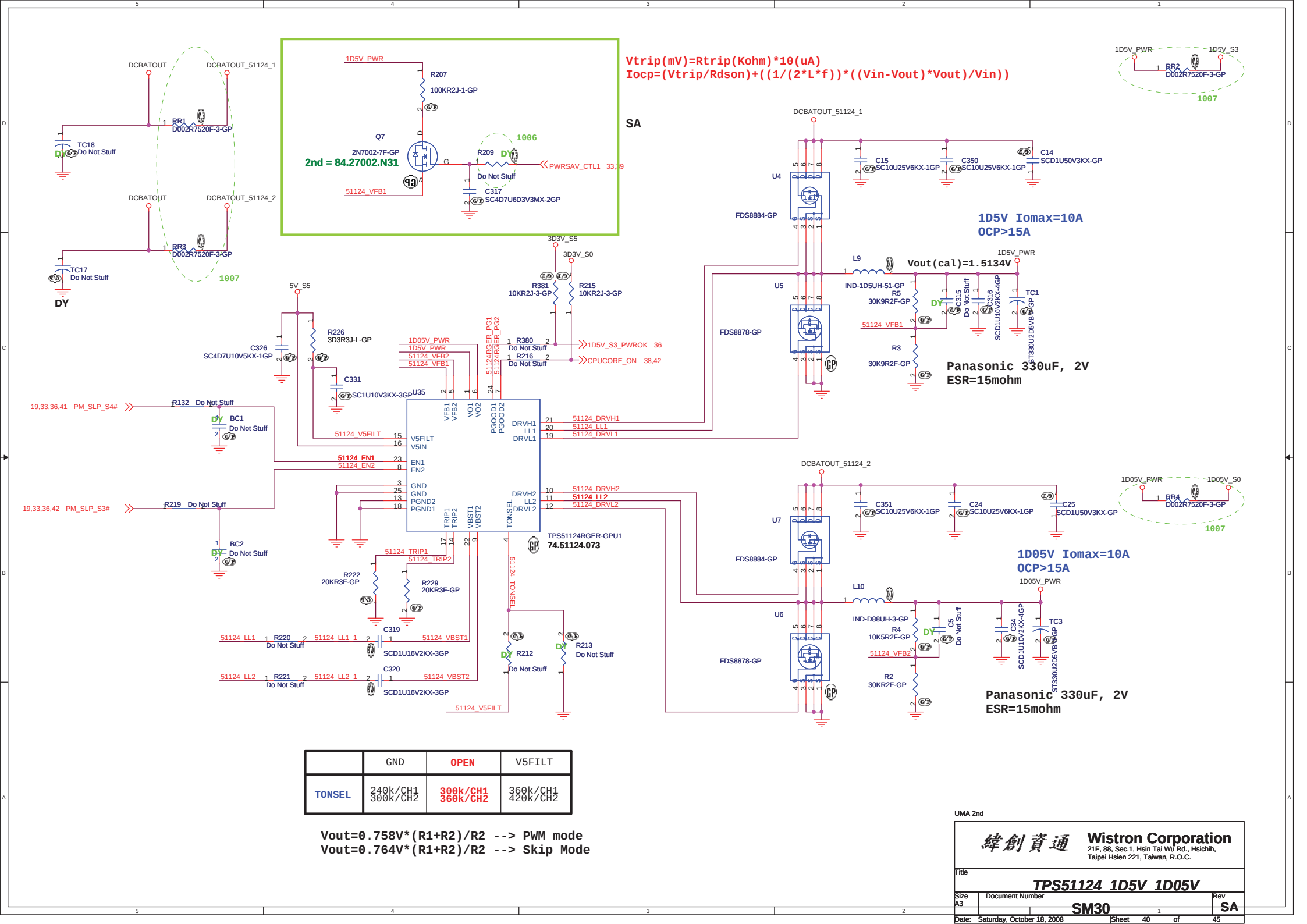
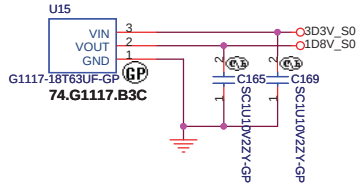
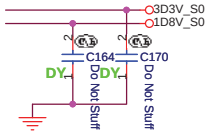
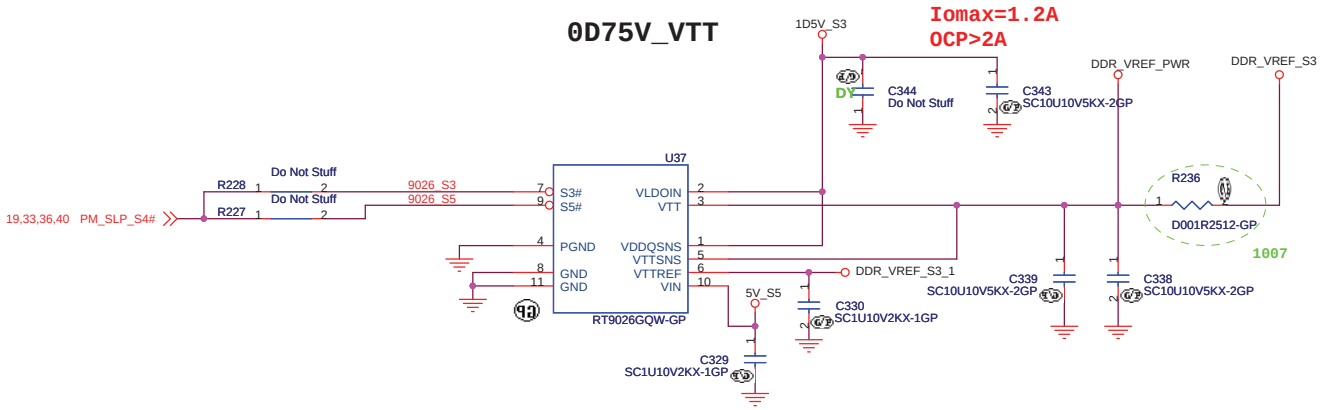


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2







UMA 2nd

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***0D75V & 1D8V***	
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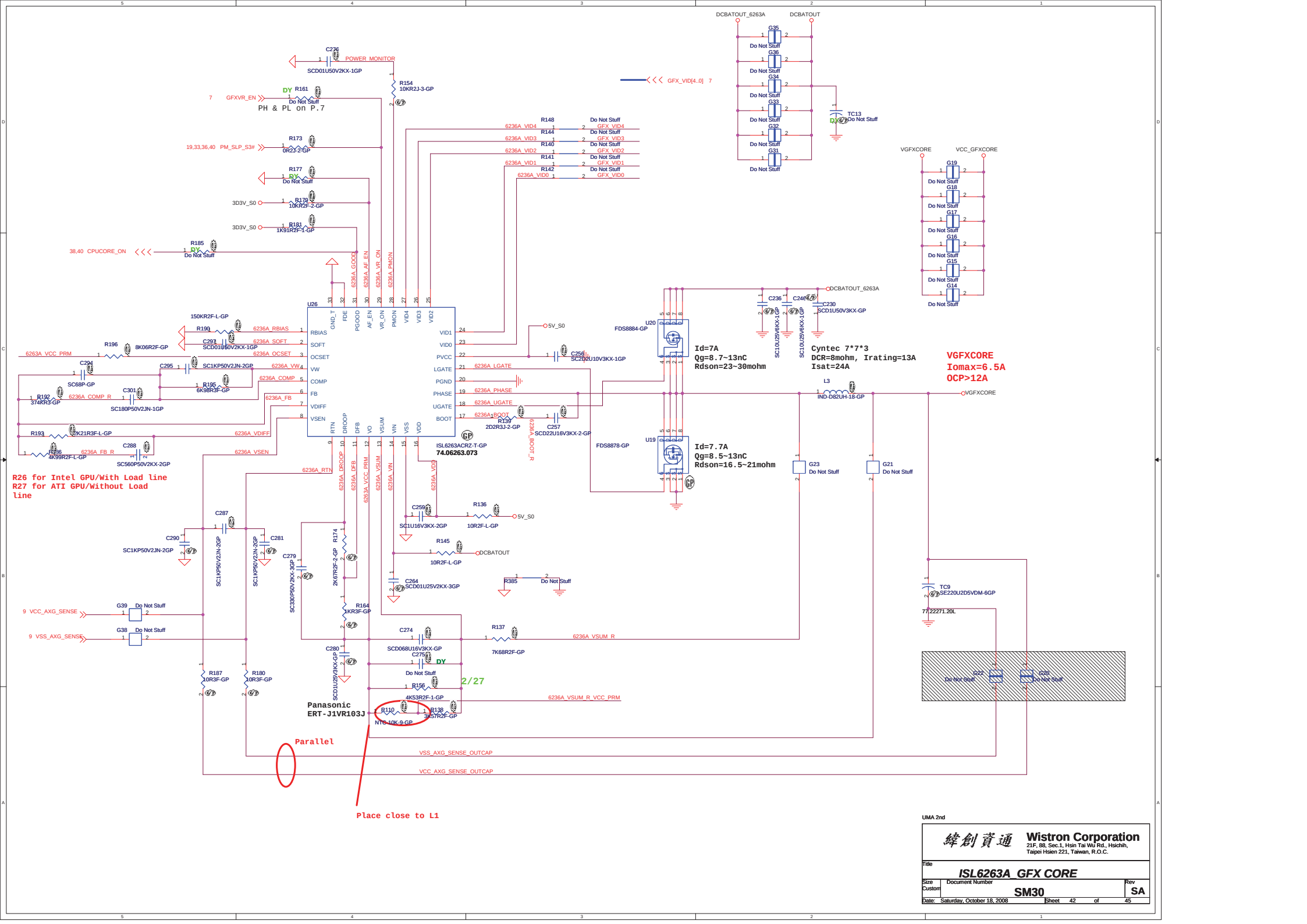
U26
ISL6263ACRZ-T-GP
74.06263.073
U20
FDS8884-GP
U19
FDS8878-GP
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Cyntec 7*7*3
DCR=8mohm, Irating=13A
Isat=24A
VGFXCORE
Iomax=6.5A
OCP>12A
R26 for Intel GPU/With Load line
R27 for ATI GPU/Without Load line
Panasonic
ERT-J1VR103J
Parallel
Place close to L1
2/27
DCBATOUT_6263A
DCBATOUT
VGFXCORE
VCC_GFXCORE
POWER_MONITOR
GFX_VID[4..0]
PH & PL on P.7
Do Not Stuff
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
UMA 2nd
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6263A_GFX CORE
SM30
SA
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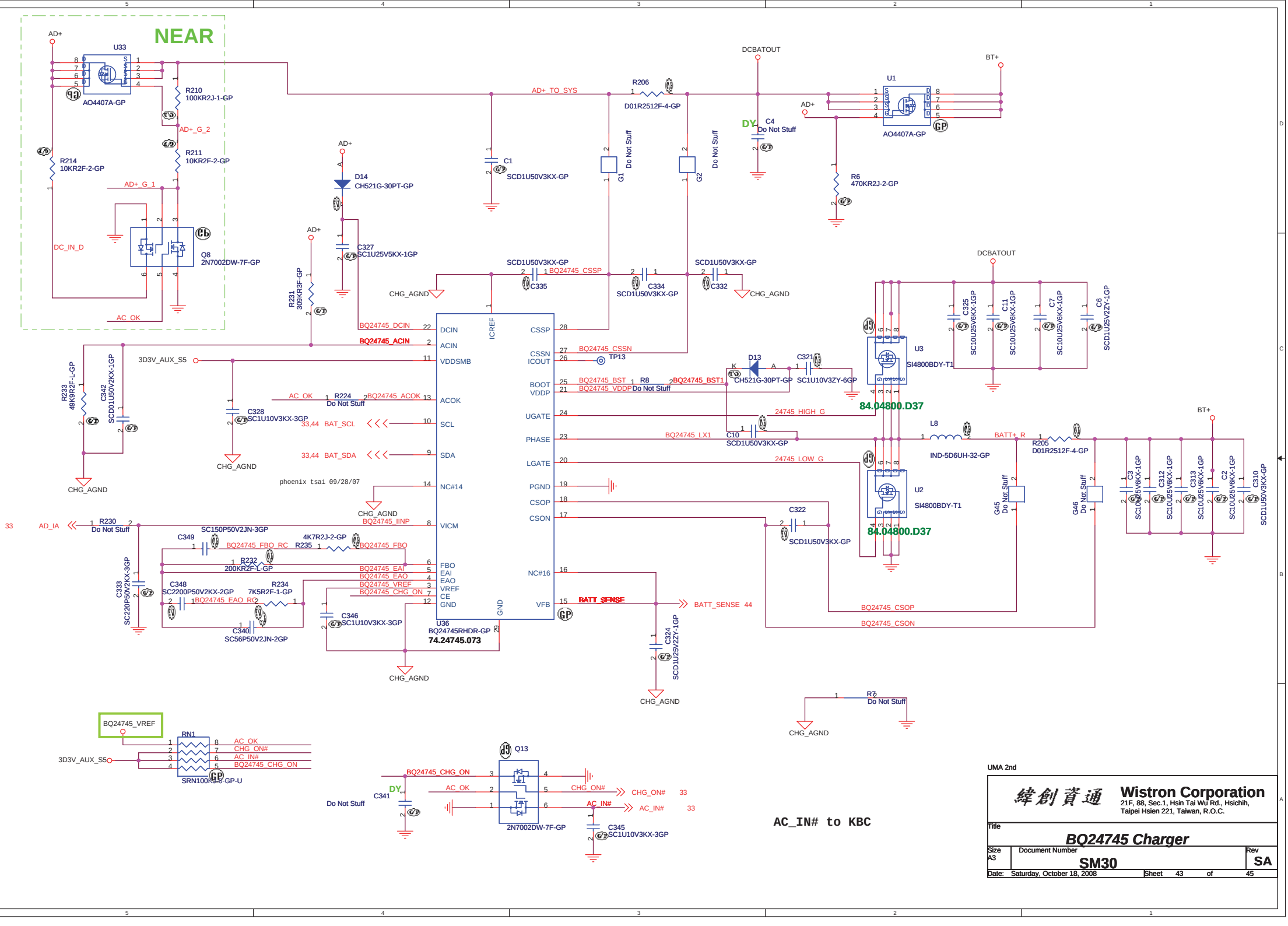
NEAR
U33
AO4407A-GP
R210
100KR2J-1-GP
R211
10KR2F-2-GP
R214
10KR2F-2-GP
AD+_G_2
AD+_G_1
DC_IN_D
Q8
2N7002DW-7F-GP
AC_OK
AD+
AD+_TO_SYS
R206
D01R2512F-4-GP
DCBATOUT
BT+
U1
AO4407A-GP
DY
C4
Do Not Stuff
R6
470KR2J-2-GP
D14
CH521G-30PT-GP
C327
SC1U25V5KX-1GP
R231
309KR3F-GP
C1
SCD1U50V3KX-GP
G1
G2
Do Not Stuff
SCD1U50V3KX-GP
C335
BQ24745_CSSP
C334
SCD1U50V3KX-GP
C332
CHG_AGND
BQ24745_DCIN
BQ24745_ACIN
3D3V_AUX_S5
R233
49K9R2F-L-GP
C342
SCD01U50V2KX-1GP
C328
SC1U10V3KX-3GP
AC_OK
R224
Do Not Stuff
BQ24745_ACOK
33,44 BAT_SCL
33,44 BAT_SDA
phoenix tsai 09/28/07
BQ24745_IINP
33
AD_IA
R230
Do Not Stuff
SC150P50V2JN-3GP
C349
BQ24745_FBO_RC
R235
4K7R2J-2-GP
BQ24745_FBO
R232
200KR2F-L-GP
C333
SC220P50V2KX-3GP
C348
SC2200P50V2KX-2GP
BQ24745_EAO_RC
R234
7K5R2F-1-GP
C340
SC56P50V2JN-2GP
C346
SC1U10V3KX-3GP
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
U36
BQ24745RHDR-GP
74.24745.073
ICREF
GND
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
BQ24745_CSSN
TP13
BQ24745_BST
BQ24745_VDDP
R8
Do Not Stuff
BQ24745_BST1
D13
CH521G-30PT-GP
C321
SC1U10V3ZY-6GP
24745_HIGH_G
BQ24745_LX1
C10
SCD1U50V3KX-GP
24745_LOW_G
C322
SCD1U50V3KX-GP
BATT_SENSE
BATT_SENSE 44
C324
SCD1U25V2ZY-1GP
U3
SI4800BDY-T1
84.04800.D37
U2
SI4800BDY-T1
84.04800.D37
L8
IND-5D6UH-32-GP
BATT+_R
R205
D01R2512F-4-GP
G45
Do Not Stuff
G46
Do Not Stuff
C325
SC10U25V6KX-1GP
C11
SC10U25V6KX-1GP
C7
SC10U25V6KX-1GP
C6
SCD1U25V2ZY-1GP
C3
SC10U25V6KX-1GP
C312
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C313
SC10U25V6KX-1GP
C2
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C310
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R7
Do Not Stuff
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AC_IN#
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Q13
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C341
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C345
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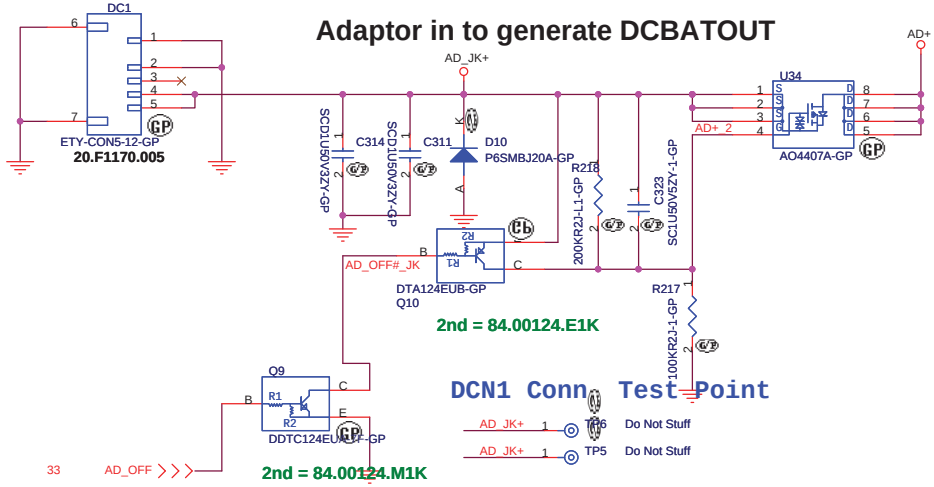
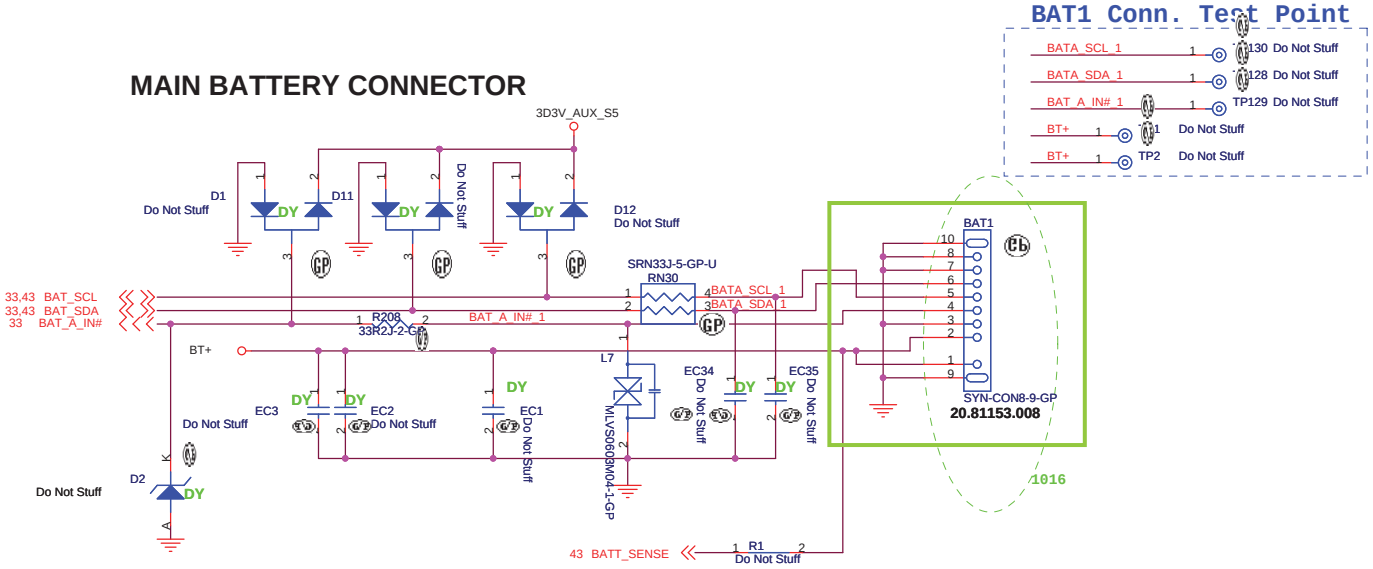
CHG_ON#
AC_IN#
AC_IN# to KBC
UMA 2nd
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size
A3
Document Number
SM30
Rev
SA
Date: Saturday, October 18, 2008
Sheet 43 of 45





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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AD&BTY CONNECTER & BTY SWITCH***

Size	Document Number	Rev
	SM30	SA

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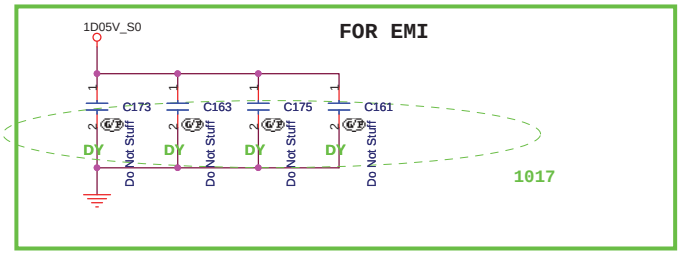
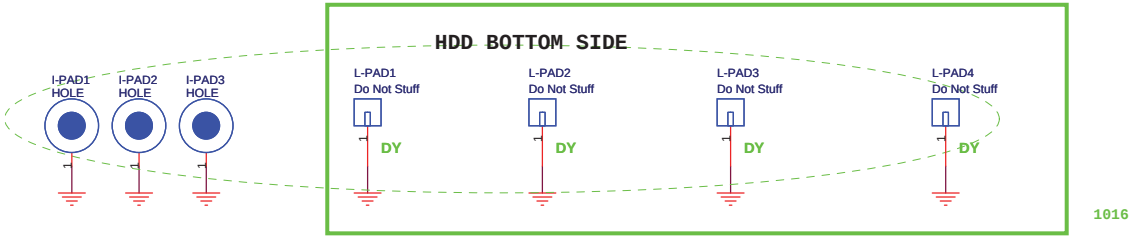
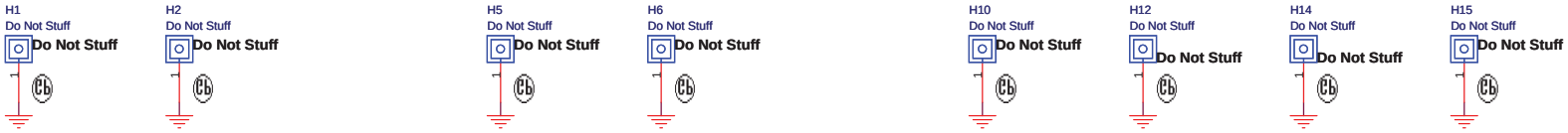
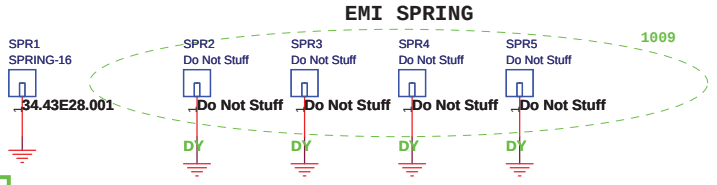
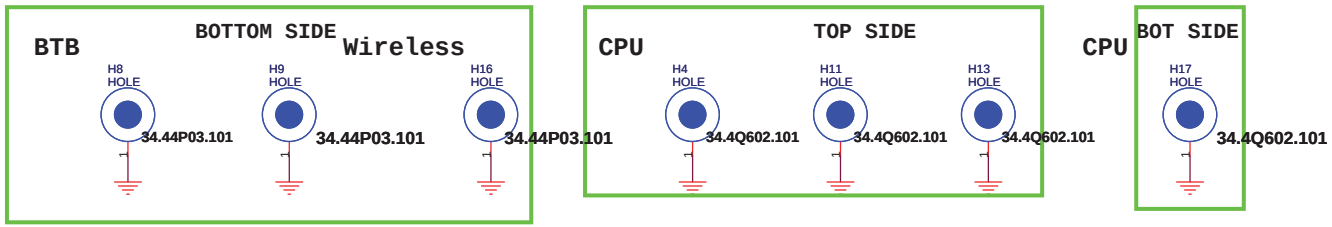








Stand off Location



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***EMI/Spring/Boss***

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	SM30	SA

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