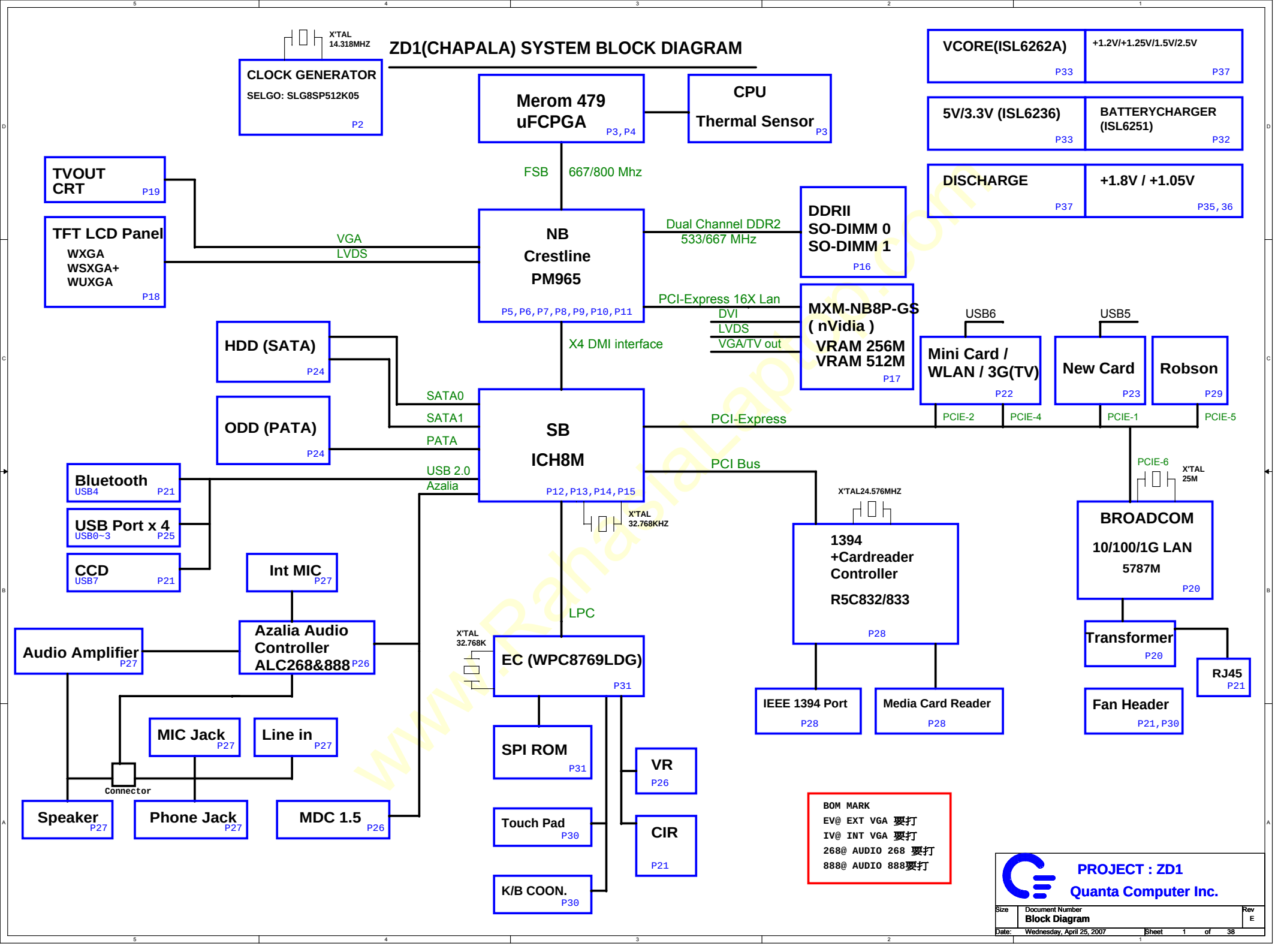
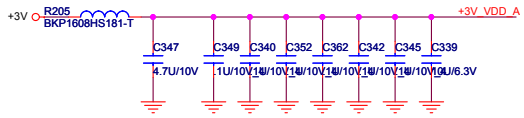
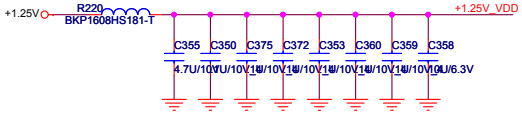
ZD1(CHAPALA) SYSTEM BLOCK DIAGRAM

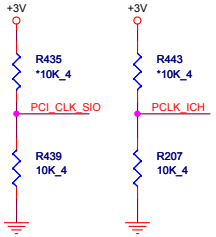


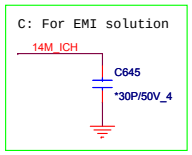
Clock Generator

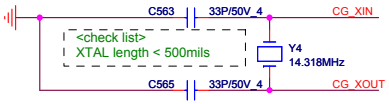
Change list:
B-test
1.Change U31 P/N to ALPRS365K13 (ICS)







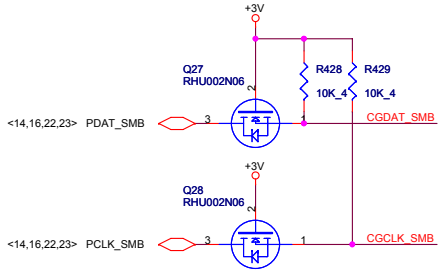




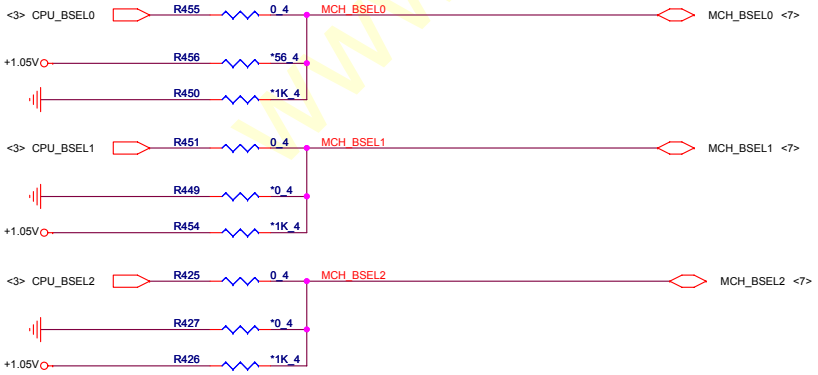
ICS9LPRS365BGLFT

Main: ICS9LPRS365BGLFT:ALPRS365K13
SLG8SP512T: AL8SP512K05

Clock Gen I2C



CPU Clock select



BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR CK505 W/REGULATOR	E
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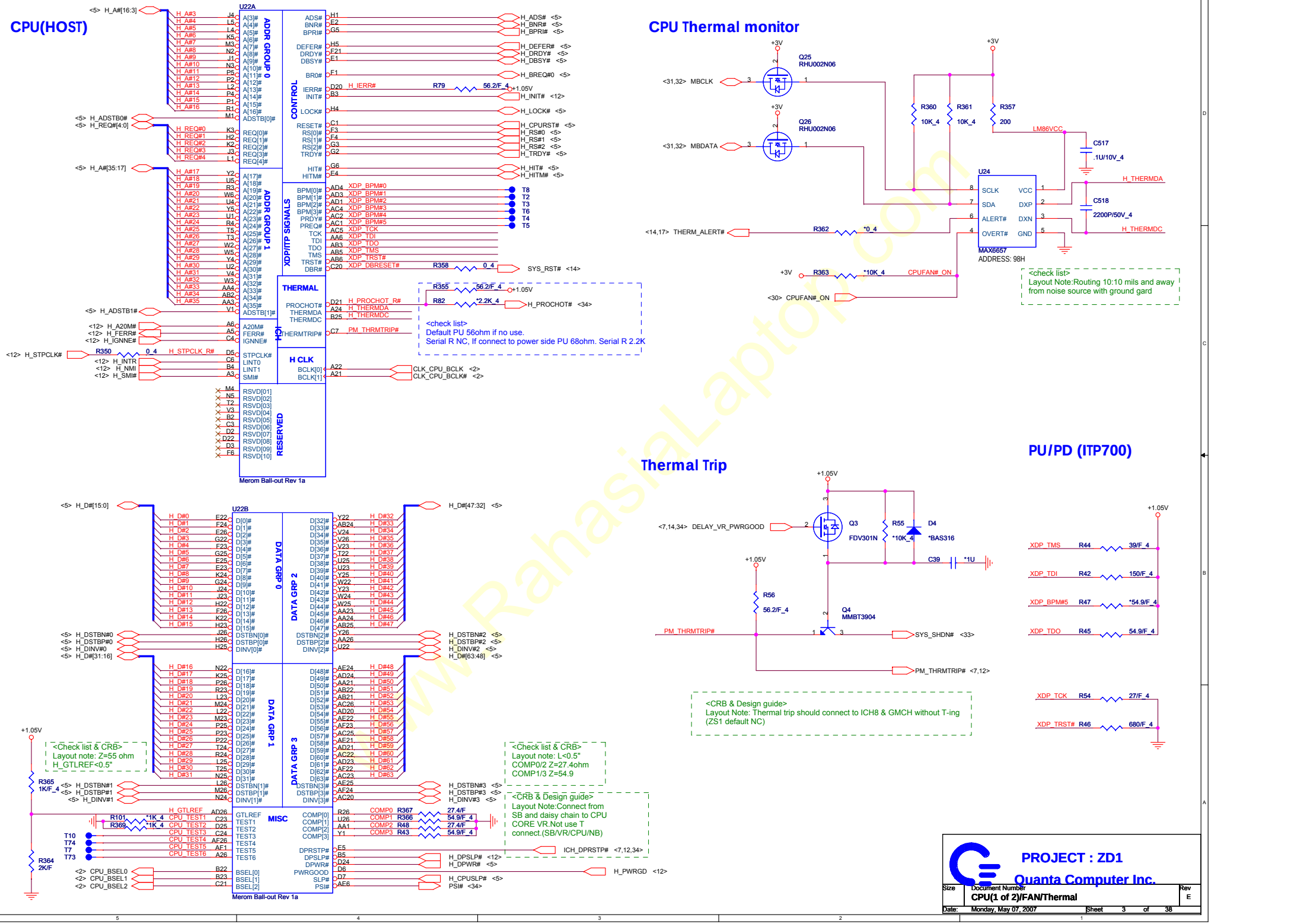
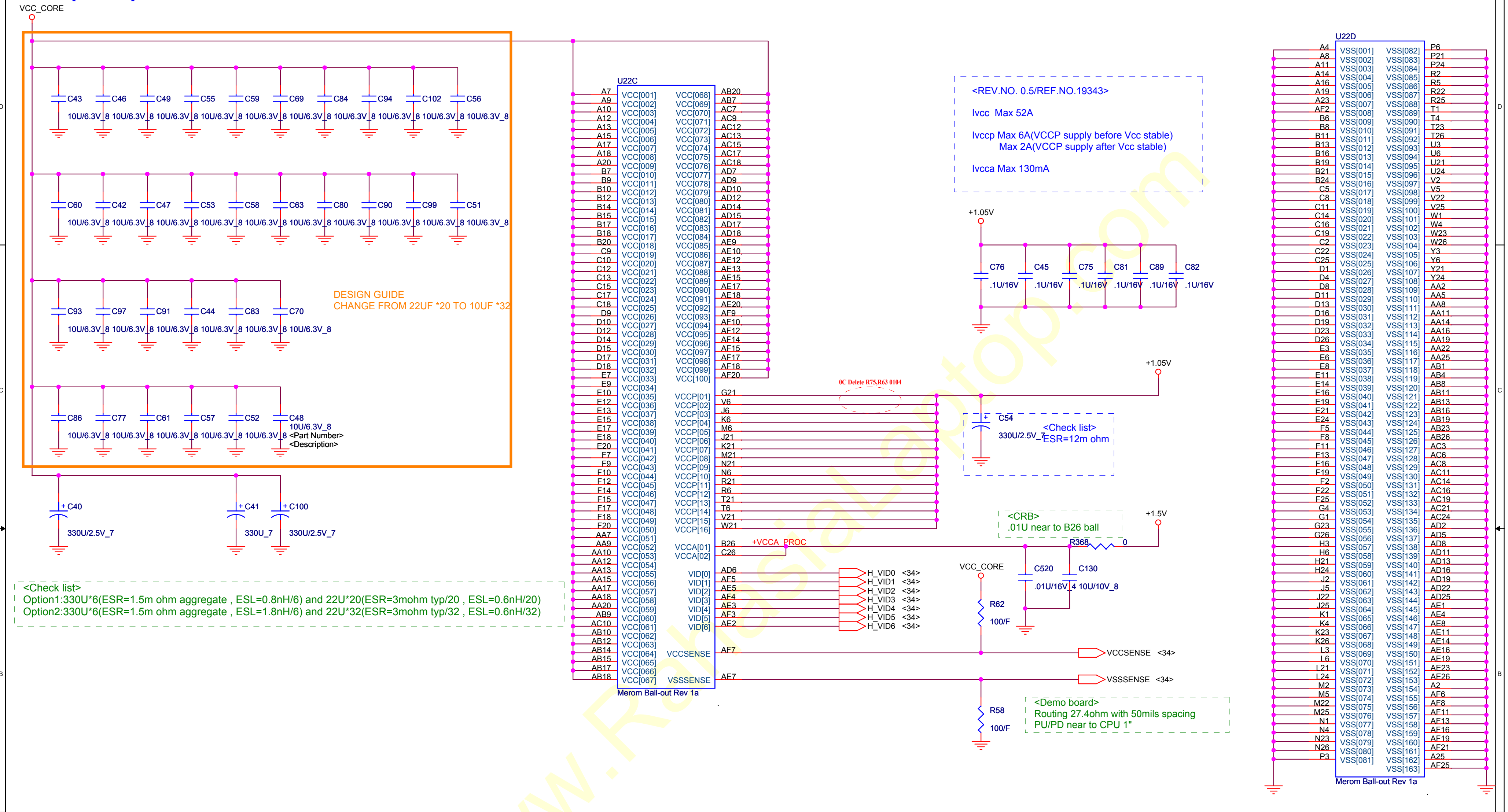


PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	CPU(1 of 2)/FAN/Thermal	E
Date: Monday, May 07, 2007	Sheet 3 of 38	

CPU(Power)



PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	CPU(2 of 2)	E

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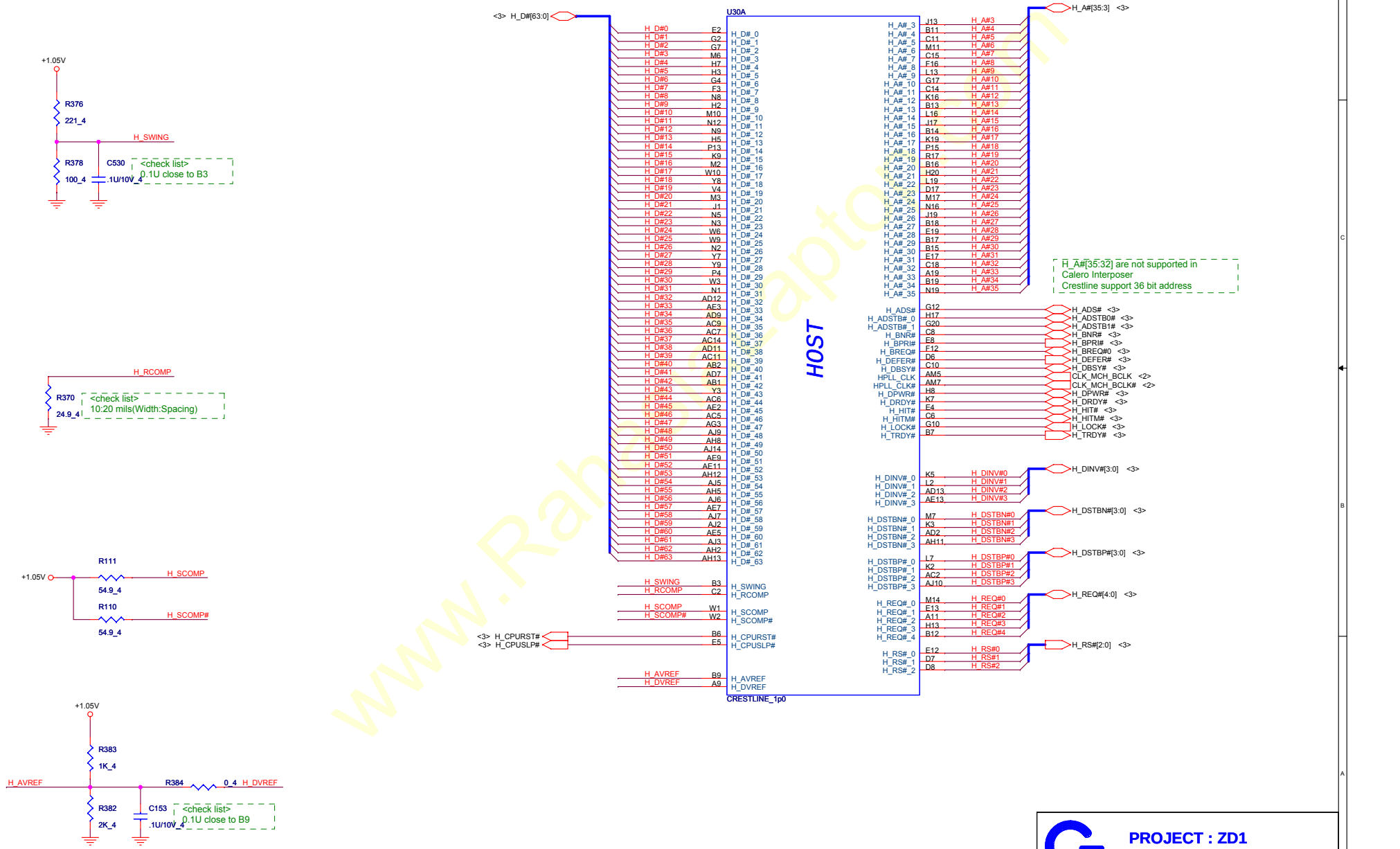
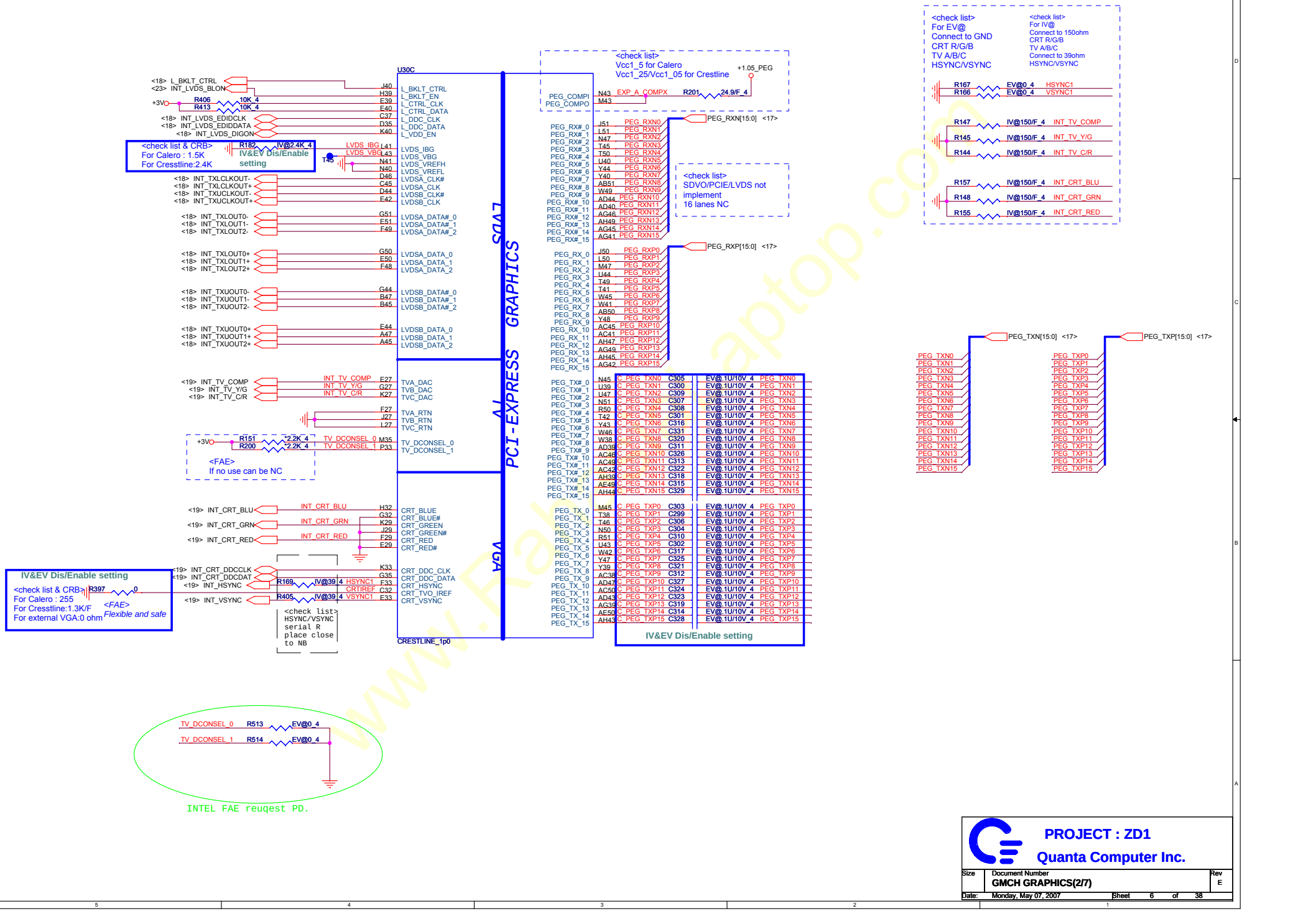
NB(HOST)



PROJECT : ZD1		
Quanta Computer Inc.		
Size	Document Number: GMCH HOST(1/7)	Rev: E
Date: Monday, May 07, 2007	Sheet 5 of 38	



PROJECT : ZD1			
Quanta Computer Inc.			
Size	Document Number		Rev
	GMCH GRAPHICS(2/7)		E
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Strapping table

All strap are sampled with respect to the leading edge of the GMCH power ok signal
CFG[17:3] have internal pull-up
CFG[18:19] have internal pull-down
Any CFG signal strapping option not list below should be left NC pin

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
CFG8	Low Power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reserved Lanes 1 = Normal operation (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ ALLZ/ Clock Un gating	00 = Clock gating disable 01 = ALL-Z Mode Enable 10 = XOR Mode Enable 11 = Normal Cperation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation 1 = Reverse Lanes (Default)
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation (Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card Present

INTEL CRB
CRESSTLINE SHOULD USE 20OHM

<check list & CRB>
R Value select
For Calero : 80.6ohm
For Cresstline:20ohm
But check list use 80.6ohm

M_RCOMP# — R387 20/F_4 — <FAE> 80.6ohm — R388 20/F_4 — +1.8VSUS
M_RCOMP

INTEL CRB
ADD 0.1UF
C165 .1U/10V_4

U30B

RSVD
P36 RSVD1
P37 RSVD2
R35 RSVD3
N35 RSVD4
AR12 RSVD5
AR13 RSVD6
AM12 RSVD7
AN13 RSVD8
J12 RSVD9
AR37 RSVD10
AM36 RSVD11
AL36 RSVD12
AM37 RSVD13
D20 RSVD14

H10 RSVD20
B51 RSVD21
BJ20 RSVD22
BK22 RSVD23
BF19 RSVD24
BH20 RSVD25
BK18 RSVD26
BJ18 RSVD27
BF23 RSVD28
BG23 RSVD29
BC23 RSVD30
BD24 RSVD31

BH39 RSVD32
AW20 RSVD33
BK20 RSVD34
C48 RSVD35
D47 RSVD36
B44 RSVD37
C44 RSVD38
A35 RSVD39
B37 RSVD40
B36 RSVD41
B34 RSVD42
C34 RSVD43

DDR MUXING
SM_CK_0 AV29 M_CLK0 <16>
SM_CK_1 BB23 M_CLK1 <16>
SM_CK_3 BA25 M_CLK2 <16>
SM_CK_4 AV23 M_CLK3 <16>
SM_CK#_0 AW30 M_CLK#0 <16>
SM_CK#_1 BA23 M_CLK#1 <16>
SM_CK#_3 AW25 M_CLK#2 <16>
SM_CK#_4 AW23 M_CLK#3 <16>
SM_CKE_0 BE29 M_CKE0 <16>
SM_CKE_1 AY32 M_CKE1 <16>
SM_CKE_3 BD39 M_CKE2 <16>
SM_CKE_4 BG37 M_CKE3 <16>
SM_CS#_0 BG20 M_CS#0 <16>
SM_CS#_1 BK16 M_CS#1 <16>
SM_CS#_2 BG16 M_CS#2 <16>
SM_CS#_3 BE13 M_CS#3 <16>
SM_ODT_0 BH18 M_ODT0 <16>
SM_ODT_1 BJ15 M_ODT1 <16>
SM_ODT_2 BJ14 M_ODT2 <16>
SM_ODT_3 BE16 M_ODT3 <16>
SM_RCOMP BL15 M_RCOMP
SM_RCOMP# BK14 M_RCOMP#
SM_RCOMP_VOH BK31 SM_RCOMP_VOH
SM_RCOMP_VOL BL31 SM_RCOMP_VOL
SM_VREF_0 AR49 +SM_VREF_MCH
SM_VREF_1 AW4

CLK
DPLL_REF_CLK B42 CLK_DREFCLK CLK_DREFCLK <2>
DPLL_REF_CLK# C42 CLK_DREFCLK# CLK_DREFCLK# <2>
DPLL_REF_SSCLK H48 CLK_DREFSSCLK CLK_DREFSSCLK <2>
DPLL_REF_SSCLK# H47 CLK_DREFSSCLK# CLK_DREFSSCLK# <2>
PEG_CLK K44 CLK_PCIE_3GPLL CLK_PCIE_3GPLL <2>
PEG_CLK# K45 CLK_PCIE_3GPLL# CLK_PCIE_3GPLL# <2>

DMI
DMI_RXN_0 AN47 DMI_TXN0
DMI_RXN_1 AJ38 DMI_TXN1
DMI_RXN_2 AN42 DMI_TXN2
DMI_RXN_3 AN46 DMI_TXN3
DMI_TXN[3:0] <13>
DMI_RXP_0 AM47 DMI_TXP0
DMI_RXP_1 AJ39 DMI_TXP1
DMI_RXP_2 AN41 DMI_TXP2
DMI_RXP_3 AN45 DMI_TXP3
DMI_TXP[3:0] <13>
DMI_TXN_0 AJ46 DMI_RXN0
DMI_TXN_1 AJ41 DMI_RXN1
DMI_TXN_2 AM40 DMI_RXN2
DMI_TXN_3 AM44 DMI_RXN3
DMI_RXN[3:0] <13>
DMI_TXP_0 AJ47 DMI_RXP0
DMI_TXP_1 AJ42 DMI_RXP1
DMI_TXP_2 AM39 DMI_RXP2
DMI_TXP_3 AM43 DMI_RXP3
DMI_RXP[3:0] <13>

CFG
<2> MCH_BSEL0 P27 CFG_0
<2> MCH_BSEL1 N27 CFG_1
<2> MCH_BSEL2 N24 CFG_2
CFG_3
T30 MCH_CFG_3 C21
T75 MCH_CFG_4 C23
MCH_CFG_5 F23 CFG_4
CFG_5
T34 MCH_CFG_6 N23 CFG_6
T24 MCH_CFG_7 G23 CFG_7
T29 MCH_CFG_8 J20 CFG_8
MCH_CFG_9 C20 CFG_9
T37 MCH_CFG_10 R24 CFG_10
T28 MCH_CFG_11 L23 CFG_11
MCH_CFG_12 J23 CFG_12
MCH_CFG_13 E23 CFG_13
MCH_CFG_14 E20 CFG_14
T25 MCH_CFG_15 K23 CFG_15
T27 MCH_CFG_16 M20 CFG_16
MCH_CFG_17 M24 CFG_17
T32 MCH_CFG_18 L32 CFG_18
T40 MCH_CFG_19 N33 CFG_19
MCH_CFG_20 L35 CFG_20

PM
<14> PM_BMBUSY# R184 0_4 PM_BMBUSY#_R G41 PM_BM_BUSY#
<3,12,34> ICH_DPRSTP# R177 0_4 ICH_DPRSTP#_R L39 PM_DPRSTP#
<16> PM_EXTTS#0 R401 0_4 PM_EXTTS#0_R L36 PM_EXT_TS#_0
<16> PM_EXTTS#1 R150 0_4 PM_EXTTS#1_R J36 PM_EXT_TS#_1
<3,14,34> DELAY_VR_PWRGOOD AW49 PWROK
<13> PLTRST#_NB R140 100_4 RST_IN#_MCH AV20 RSTIN#
<3,12> PM_THRMTRIP# R130 *0_4 PM_THRMTRIP#_GMCH N20 THERMTRIP#
<14,34> PM_DPRSLPVR R407 0_4 PM_DPRSLPVR_GMCH G36 DPRSLPVR

GRAPHICS VID
GFX_VID_0 E35 MCH_GFX_VID_0 T41
GFX_VID_1 A39 MCH_GFX_VID_1 T42
GFX_VID_2 C38 MCH_GFX_VID_2 T43
GFX_VID_3 B39 MCH_GFX_VID_3 T44
GFX_VR_EN E36 R183 *0_4 SUSB# <14,31>

ME
CL_CLK AM49 CL_CLK0 <14>
CL_DATA AK50 CL_DATA0 <14>
CL_PWROK AT43 MPWROK <14,31>
CL_RST# AN49 CL_RST#0 <14>
CL_VREF AM50 +1.25V_CL_VREF

MISC
SDVO_CTRL_CLK H35
SDVO_CTRL_DATA K36
CLK_REQ# G39 CLK_MCH_OE#
ICH_SYNC# G40 MCH_ICH_SYNC# <14>
TEST_1 A37 GMCH_TEST1 R178 0_4
TEST_2 R32 GMCH_TEST2 R168 20K_4

NC
BJ51 NC_1
BK51 NC_2
BK50 NC_3
BL50 NC_4
BL49 NC_5
BL3 NC_6
BL2 NC_7
BK1 NC_8
BJ1 NC_9
E1 NC_10
A5 NC_11
C51 NC_12
B50 NC_13
A50 NC_14
A49 NC_15
BK2 NC_16

CRESTLINE_1p0

+3V
R170 10K_4 CLK_MCH_OE#
R395 10K_4 PM_EXTTS#0
R149 10K_4 PM_EXTTS#1

MCH_CFG_5 R138 *4.02K/F_4
MCH_CFG_9 R127 *4.02K/F_4
MCH_CFG_12 R139 *4.02K/F_4
MCH_CFG_13 R137 *4.02K/F_4
MCH_CFG_16 R129 *4.02K/F_4

+3V
MCH_CFG_19 R171 *4.02K/F_4
MCH_CFG_20 R174 *4.02K/F_4

+1.25V
R422 1K/F_4
C559 .1U/10V_4
R420 392/F

+SMDDR_VREF
+1.8VSUS
R416 *1K/F_4
R417 BK1608LL121
+SM_VREF_MCH
R418 *1K/F_4
C295 .1U/10V_4
C143 1U/10V_4

+1.8VSUS R154 1K/F_4 SM_RCOMP_VOH
R165 3.01K/F_4 C241 .01U/16V_4 C232 2.2U/6.3V
SM_RCOMP_VOL
R163 1K/F_4 C250 .01U/16V_4 C233 2.2U/6.3V

+1.25V
CLK_DREFCLK R409 *4.7K_4
CLK_DREFCLK# R529 EV@0_4
R531 EV@0_4
CLK_DREFSSCLK R411 *4.7K_4
CLK_DREFSSCLK# R532 EV@0_4
R533 EV@0_4
DC Delete R410 and R408 0110

INTEL FAE suggest PD for external graphics

PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH (STRAPPING/OTHER 3/7)	E
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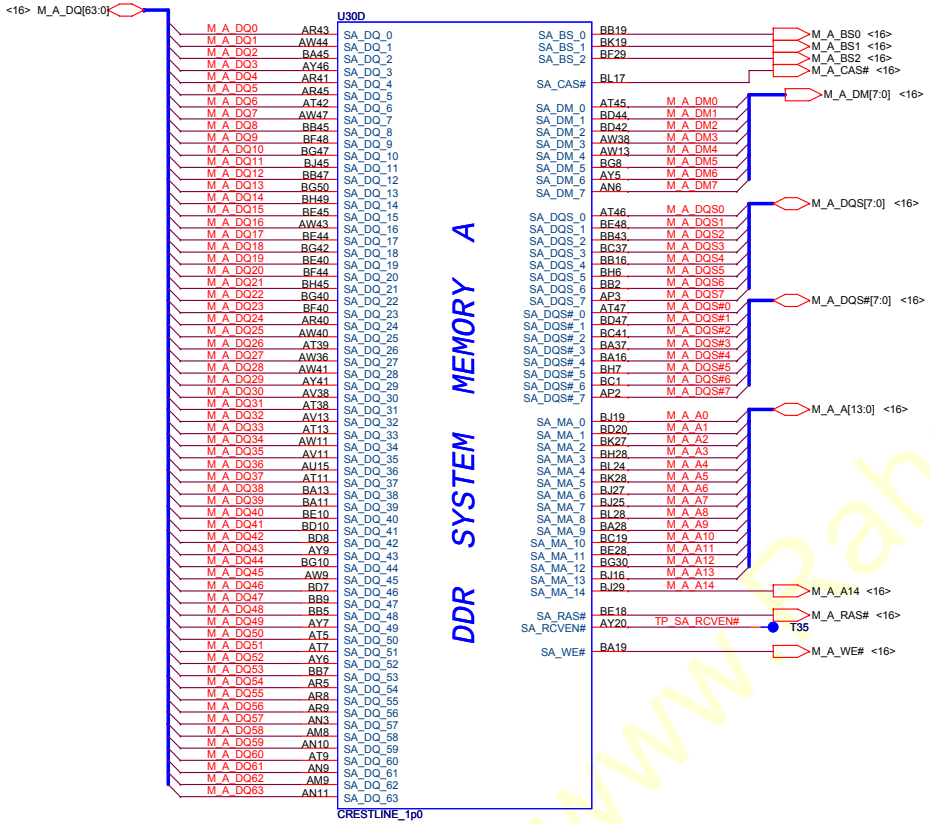
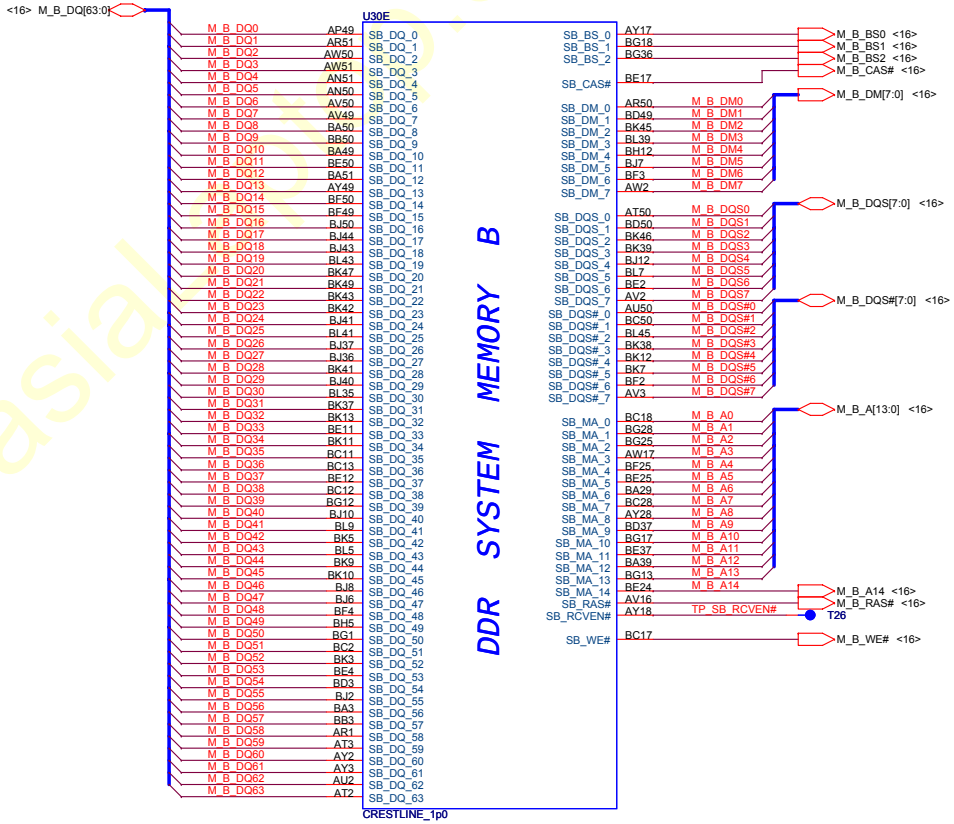
NB(Memory controller)





PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DDR(4/7)	E

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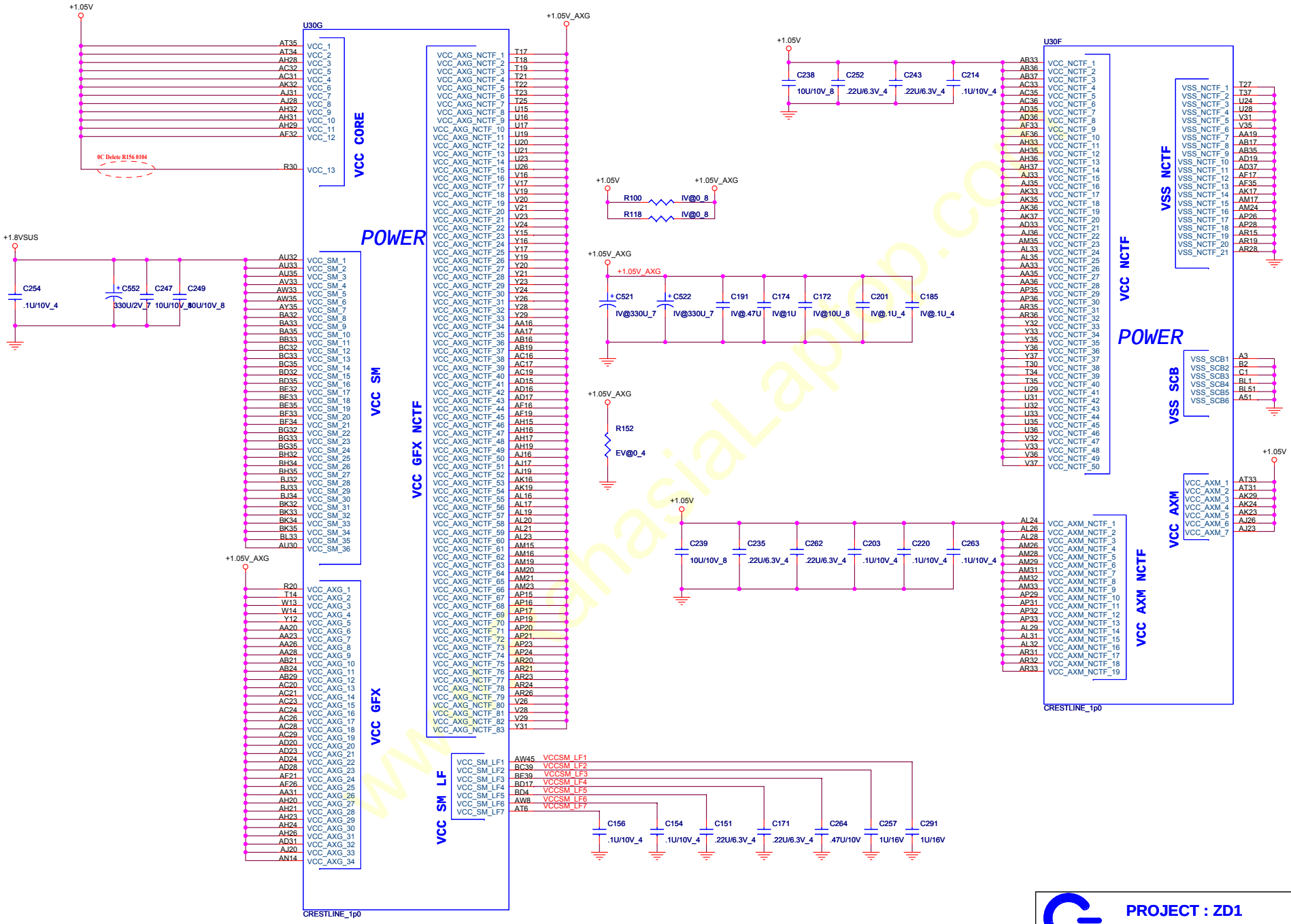
NB(Power-1)



PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Power-1(5/7)	E
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NB(Power-2)

CRT/TV Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V

EXTERNAL / INTERNAL

<FAE>
INT VGA disable
VCCSYNC connect to GND

IV&EV Dis/Enable setting

CRB RECOMMEND
180OHM@100MHz
Rdc= 0.09OHM (max)

IV&EV Dis/Enable setting

<FAE>
INT VGA disable
VCCD_TVDAC still +1.5V

Change to
100 ohm Resistor

Use site for filter cap with Gfx enabled CS

IV&EV Dis/Enable setting

<FAE>
VCC_RXR_DMI and VCC_PEG connect to+1.05V

<CRB>
+1.25V AND +1.25M shall be
+1.5V for Calero Interposer

CRESTLINE_1p0

PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Power-2(6/7)	E

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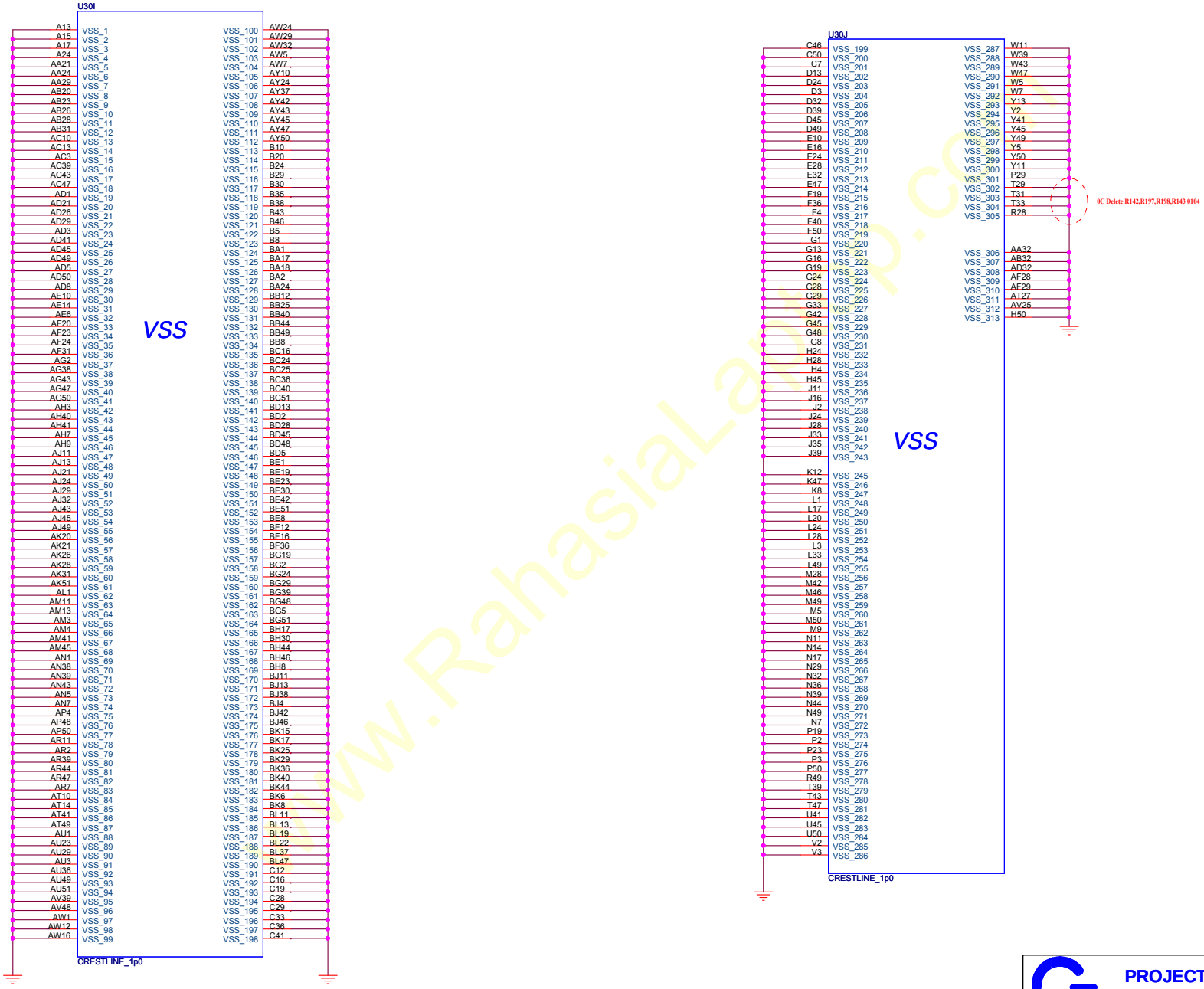
NB(Power-3)



PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Power-3(7/7)	E
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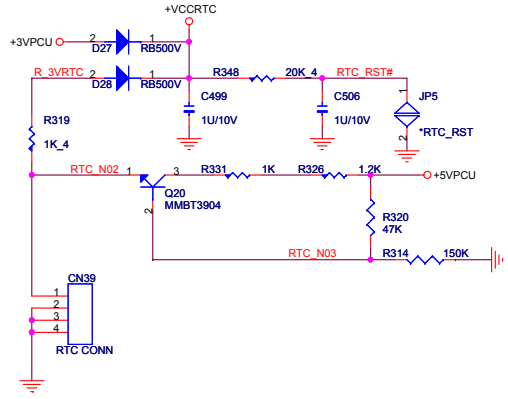
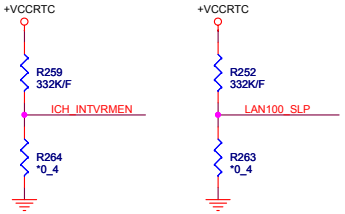
RTC



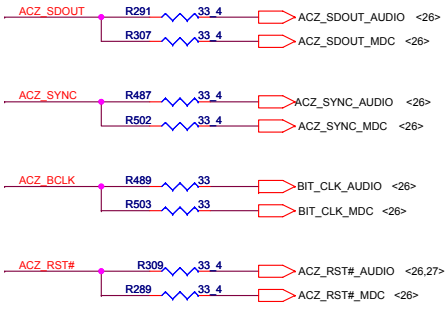
SB Strap

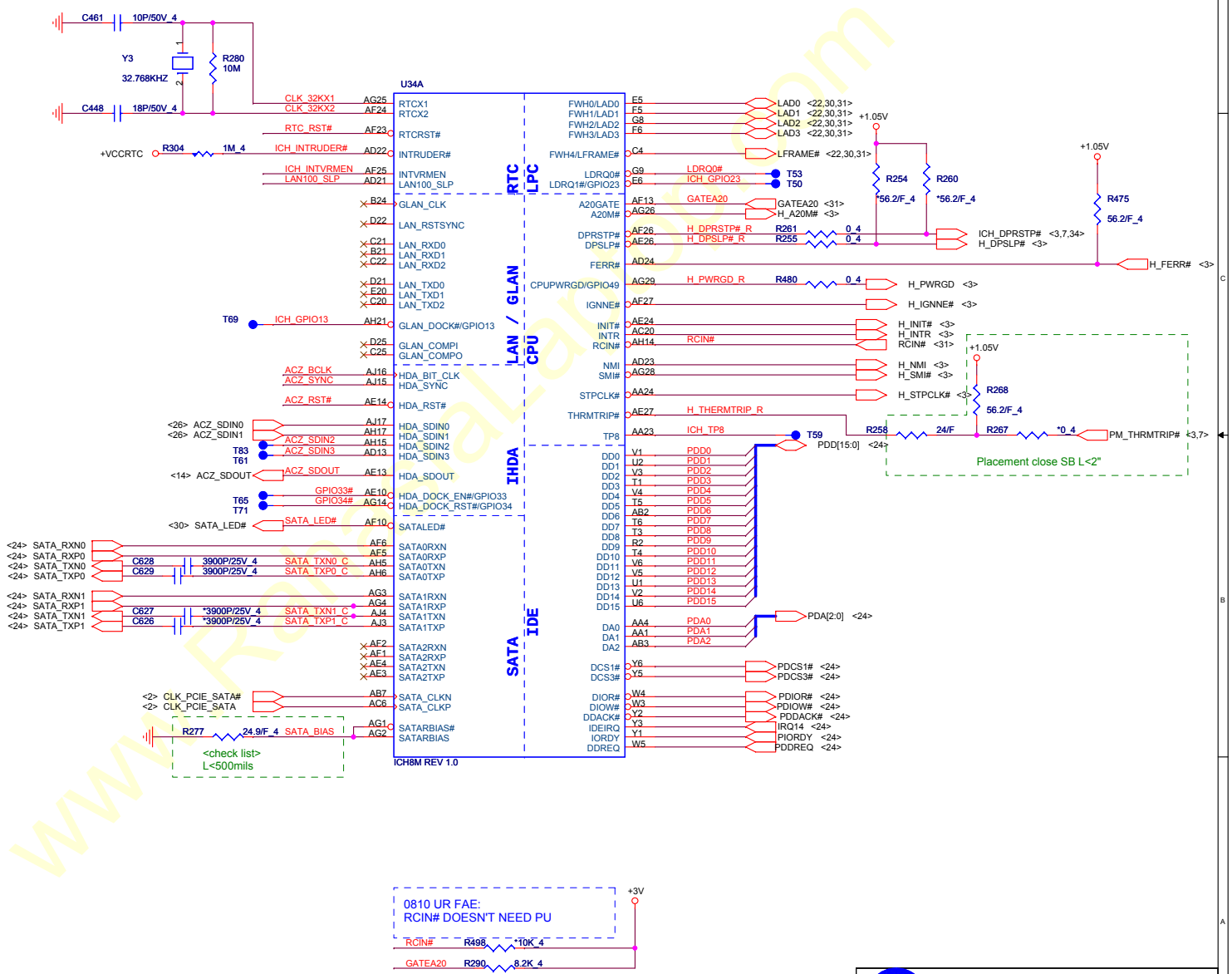
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)



HDA





PROJECT : ZD1		
Quanta Computer Inc.		
Size	Document Number: ICH8M HOST(1/4)	Rev: E
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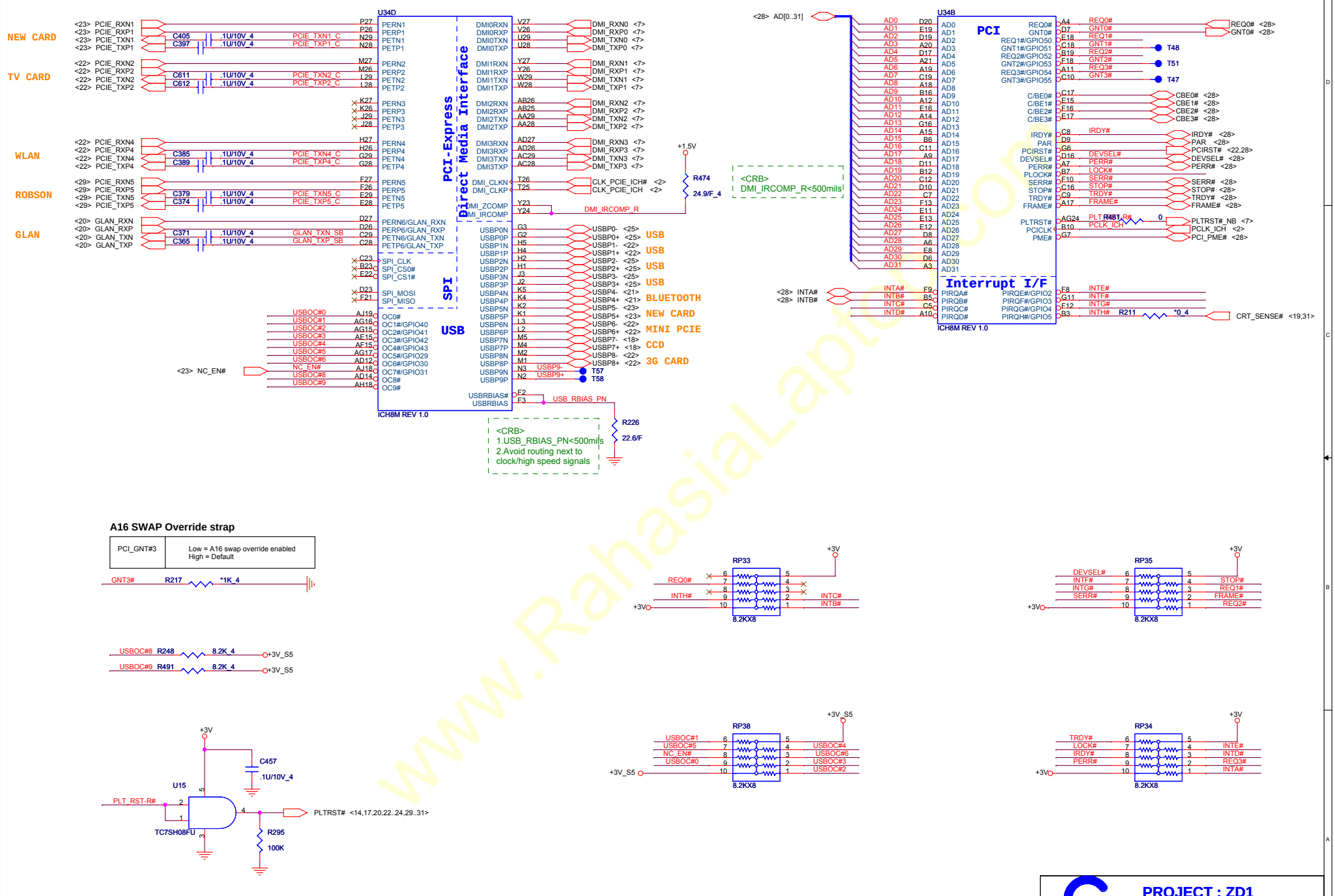
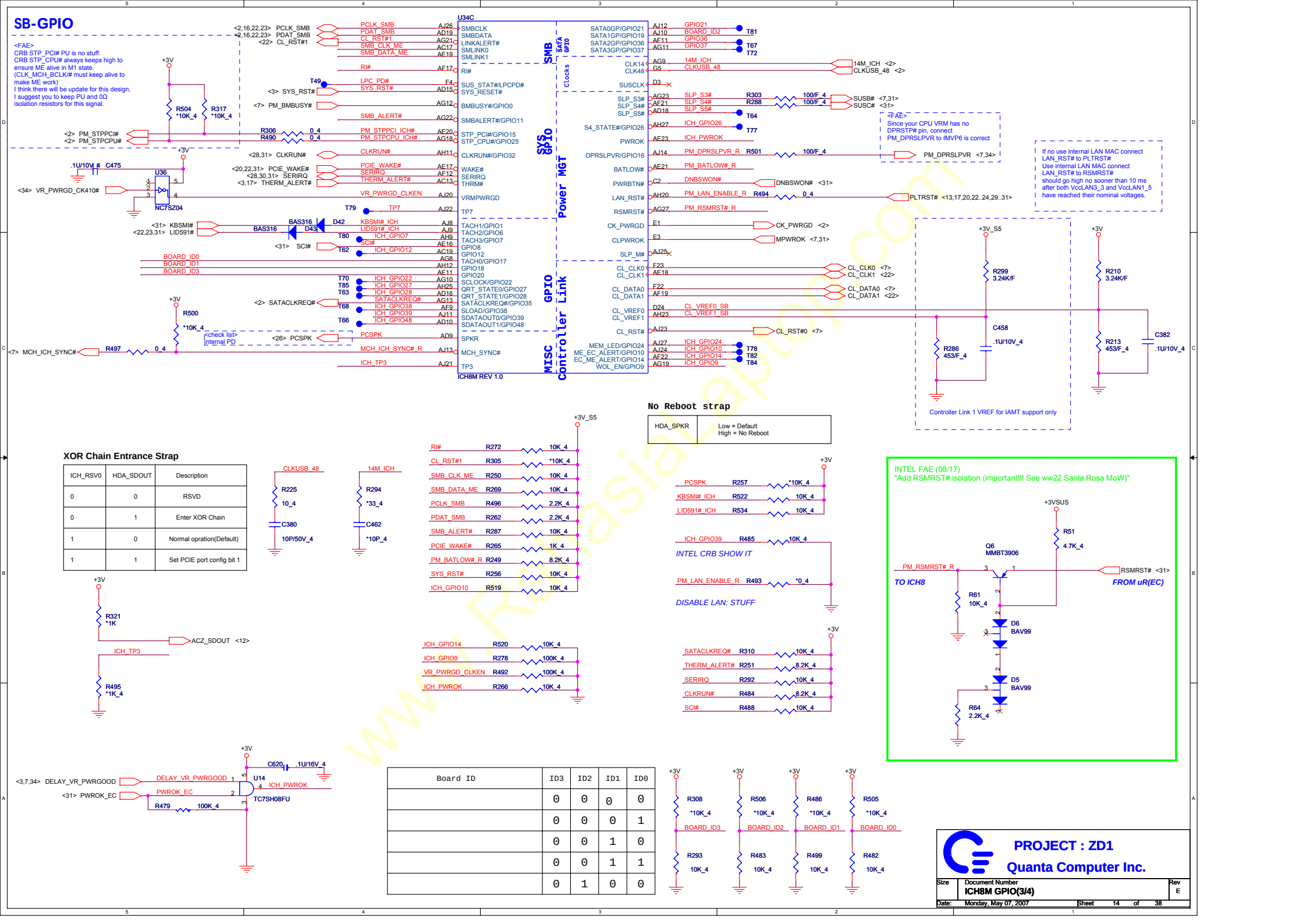


SB-GPIO



<FAE>
CRB STP_PCI# PU is no stuff.
CRB STP_CPU# always keeps high to ensure ME alive in M1 state.
(CLK_MCH_BCLK/# must keep alive to make ME work)
I think there will be update for this design, I suggest you to keep PU and 0Ω isolation resistors for this signal.

<FAE>
Since your CPU VRM has no DPRSTP# pin, connect PM_DPRSLPVR to IMVP6 is correct

If no use internal LAN MAC connect LAN_RST# to PLTRST#
Use internal LAN MAC connect LAN_RST# to RSMRST#
should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.

Controller Link 1 VREF for IAMT support only

No Reboot strap

HDA_SPKR	Low = Default High = No Reboot

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"

Board ID	ID3	ID2	ID1	ID0
	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M GPIO(3/4)	E
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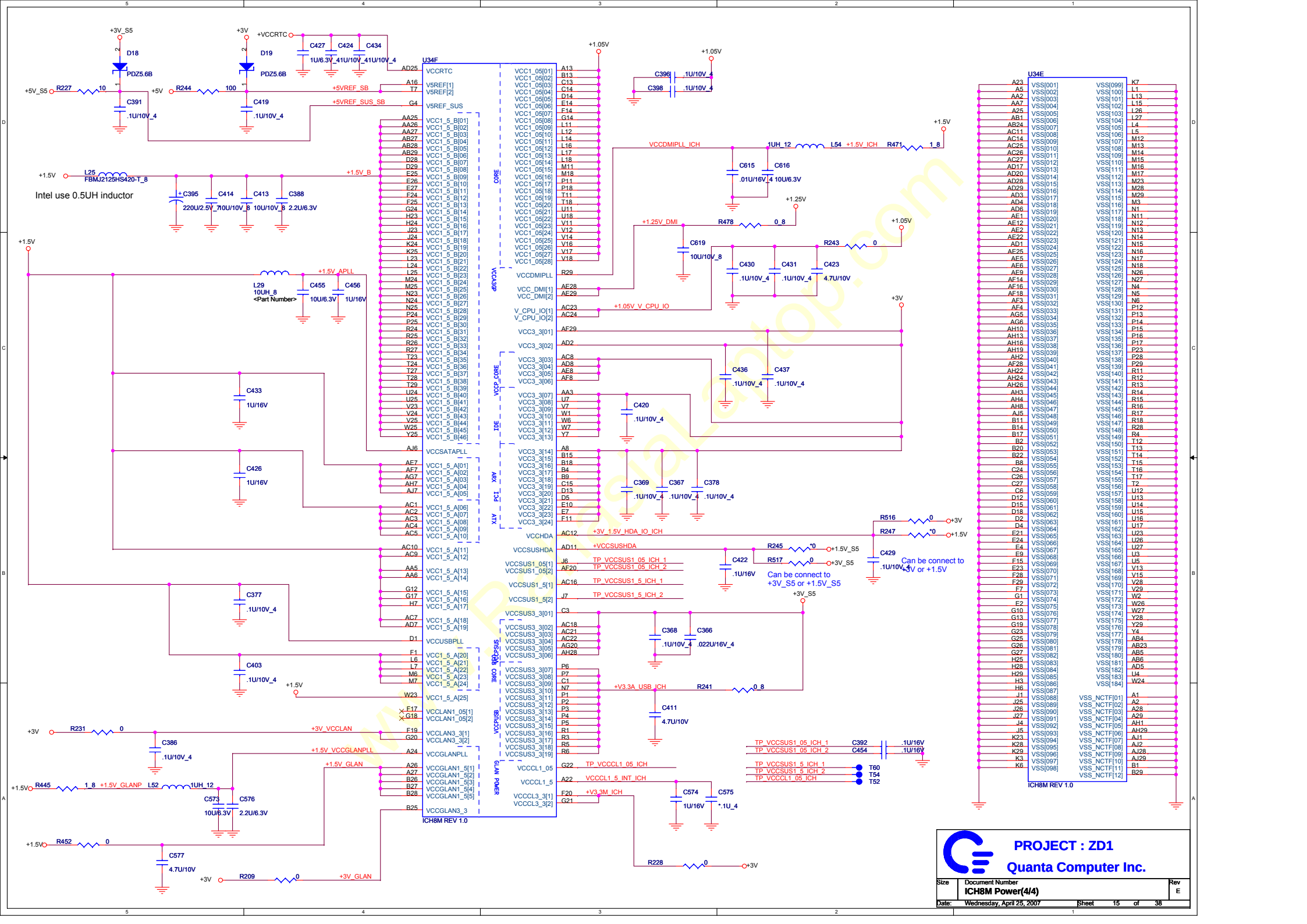
U34F
ICH8M REV 1.0
U34E
ICH8M REV 1.0
Intel use 0.5UH inductor
PROJECT : ZD1
Quanta Computer Inc.
Size
Document Number
ICH8M Power(4/4)
Rev
E
Date: Wednesday, April 25, 2007
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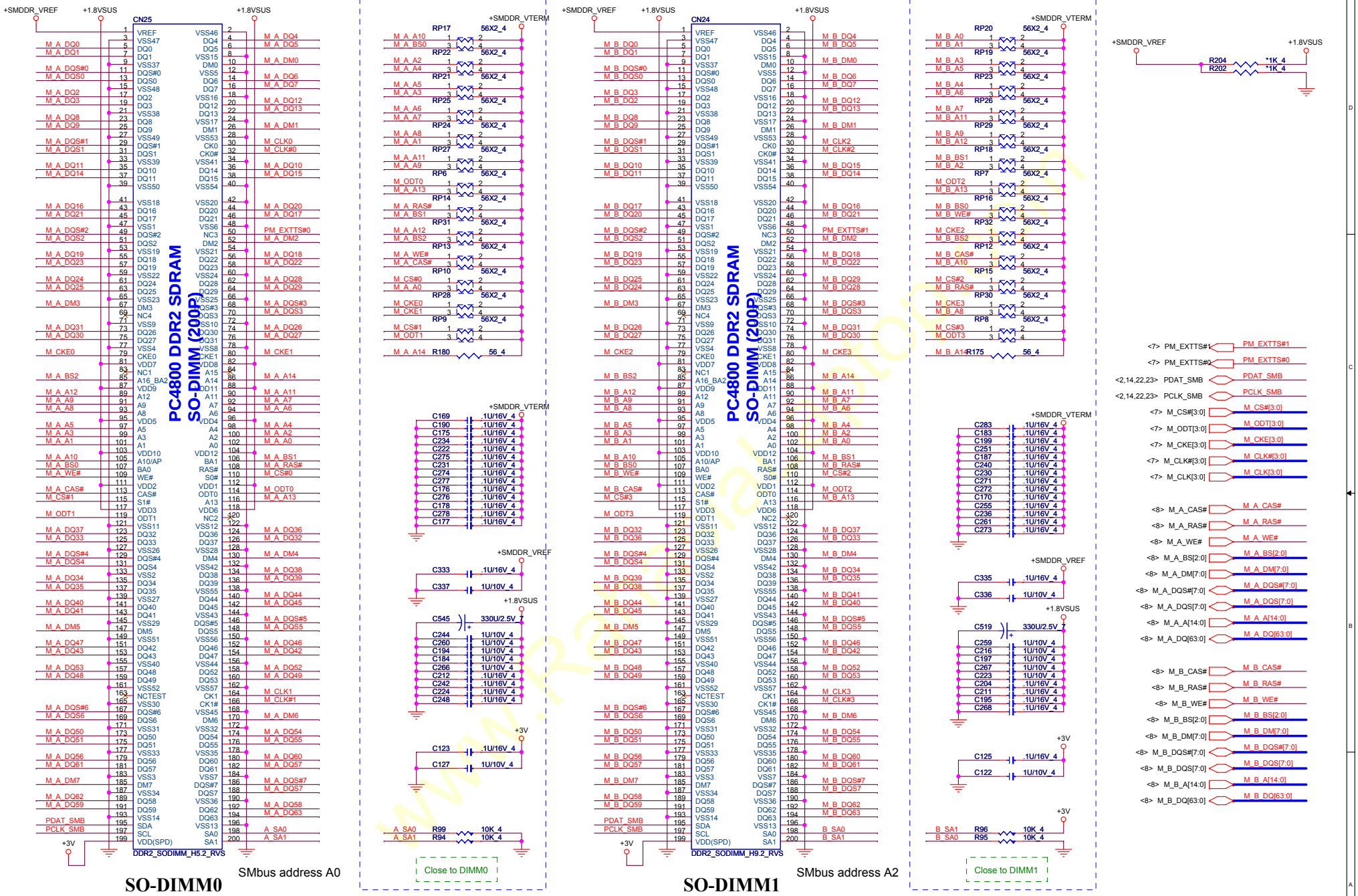
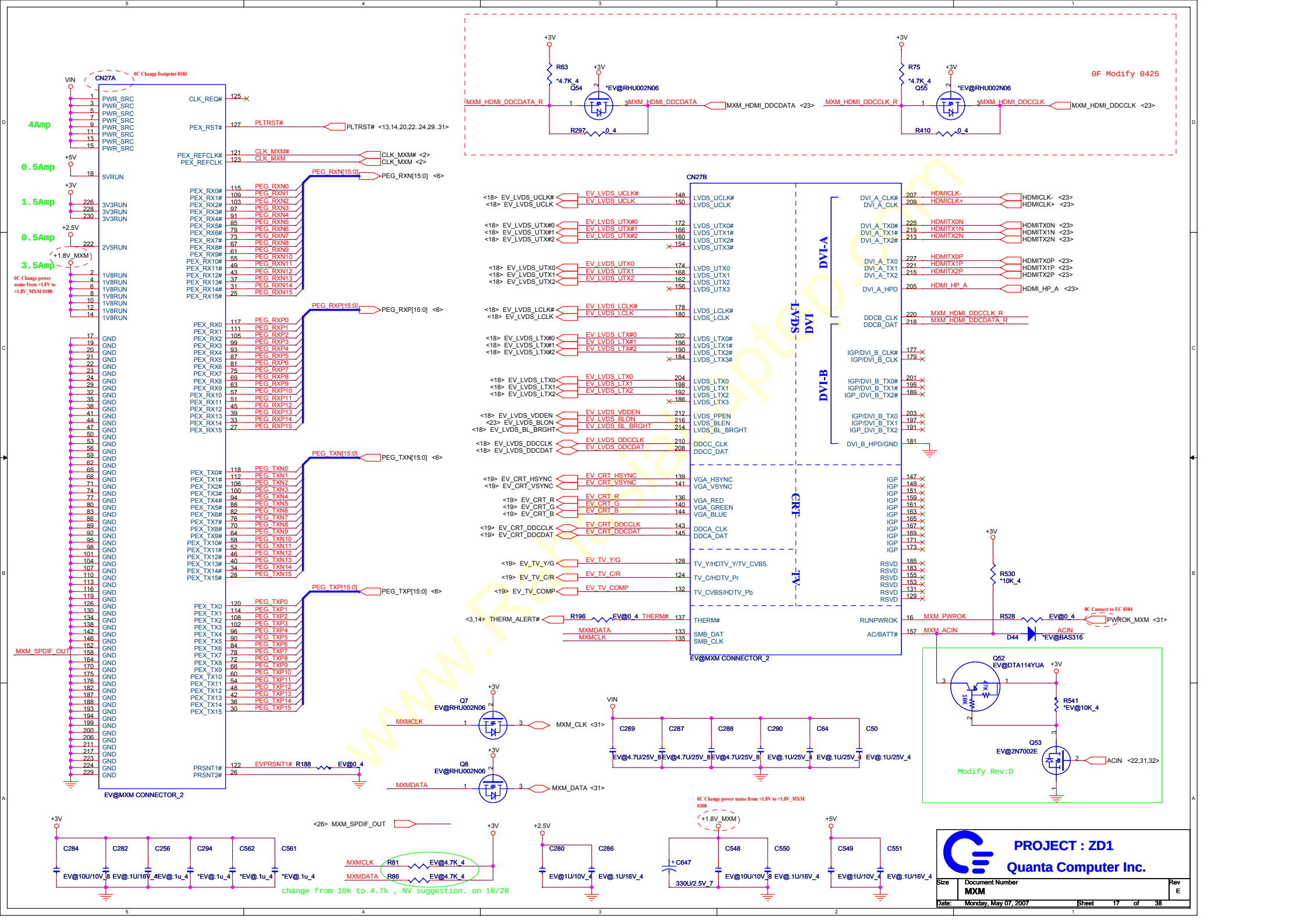

CN25
PC4800 DDR2 SDRAM
SO-DIMM (200P)
DDR2_SODIMM_H5.2_RVS
+SMDDR_VREF
+1.8VSUS
+SMDDR_VTERM
+3V
SO-DIMM0
SMbus address A0
Close to DIMM0
CN24
PC4800 DDR2 SDRAM
SO-DIMM (200P)
DDR2_SODIMM_H9.2_RVS
SO-DIMM1
SMbus address A2
Close to DIMM1
PROJECT : ZD1
Quanta Computer Inc.
DDRII SO-DIMM
Monday, May 07, 2007


CN27A
0C Change footprint 0103
EV@MXM CONNECTOR_2
CN27B
EV@MXM CONNECTOR_2
0F Modify 0425
0C Change power name from +1.8V to +1.8V_MXM 0108
change from 10k to 4.7k , NV suggestion. on 10/20
Modify Rev:D
PROJECT : ZD1
Quanta Computer Inc.
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MXM
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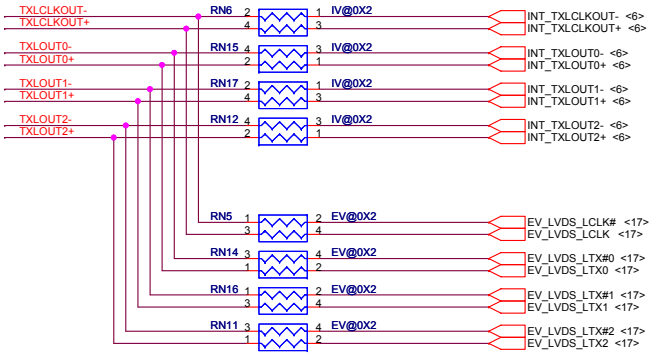
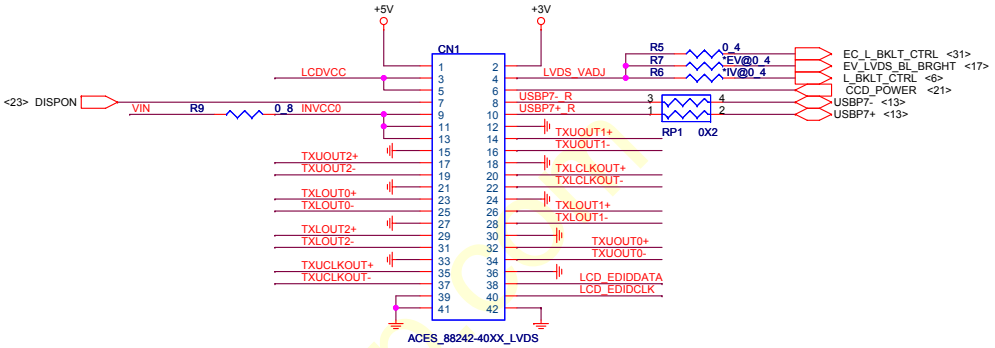
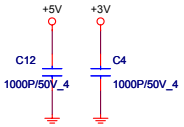
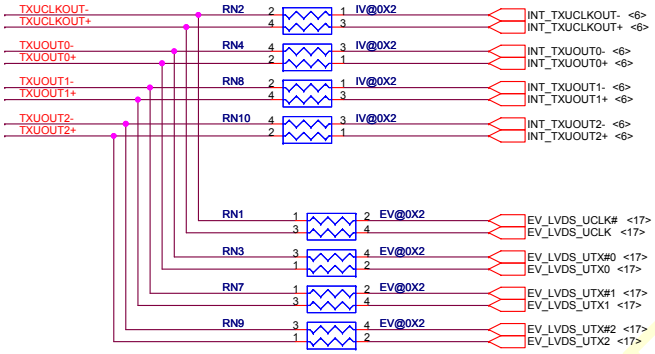
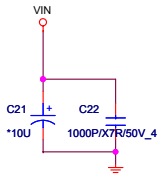
LVDS

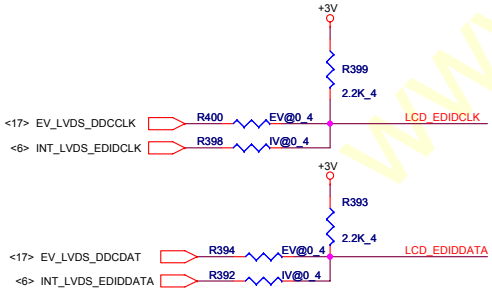


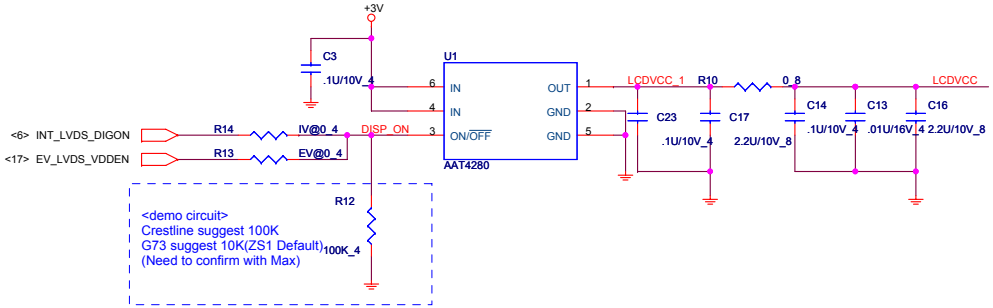












PROJECT : ZD1

Quanta Computer Inc.

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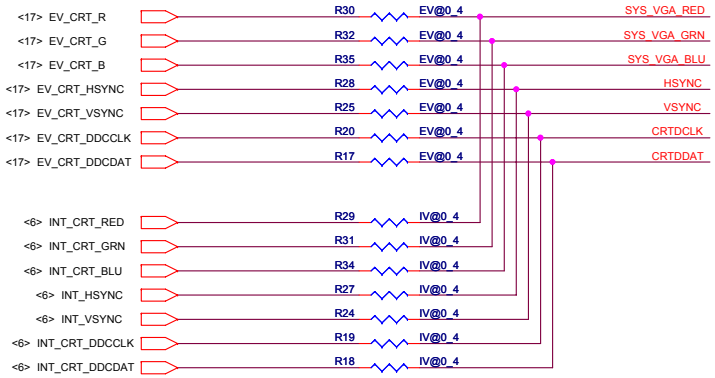
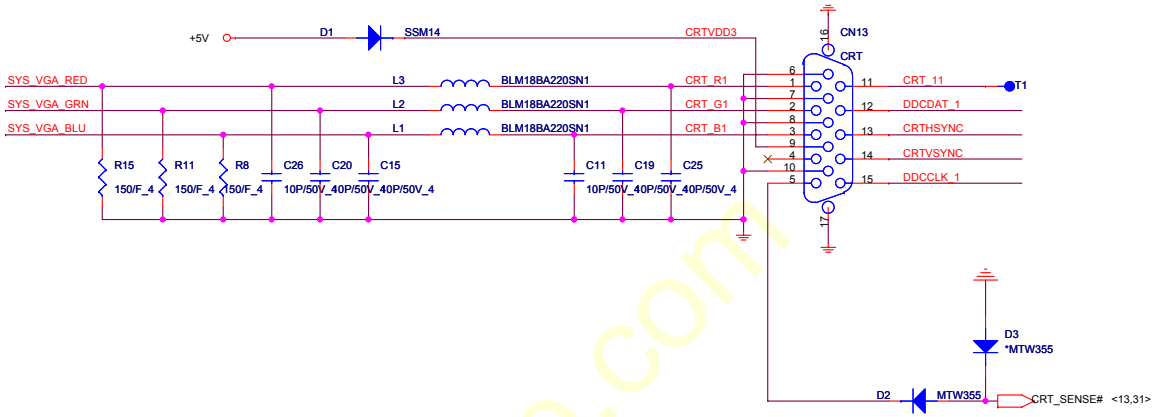
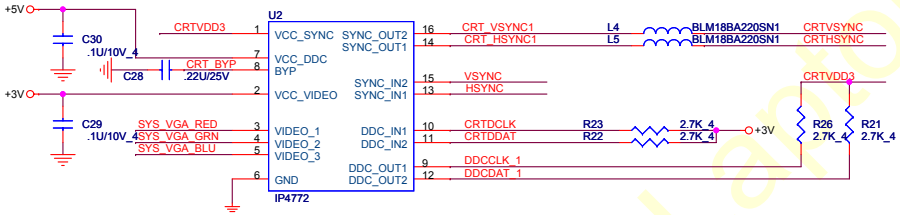
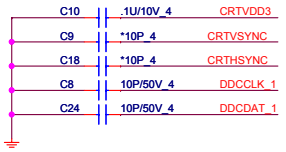
CRT Select



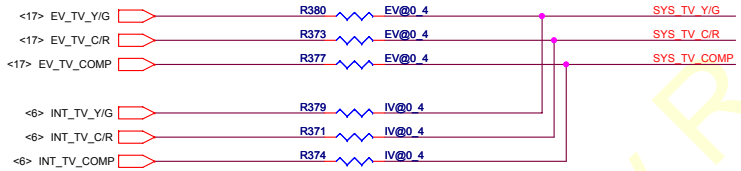
CRT CONNECTOR AND ESD

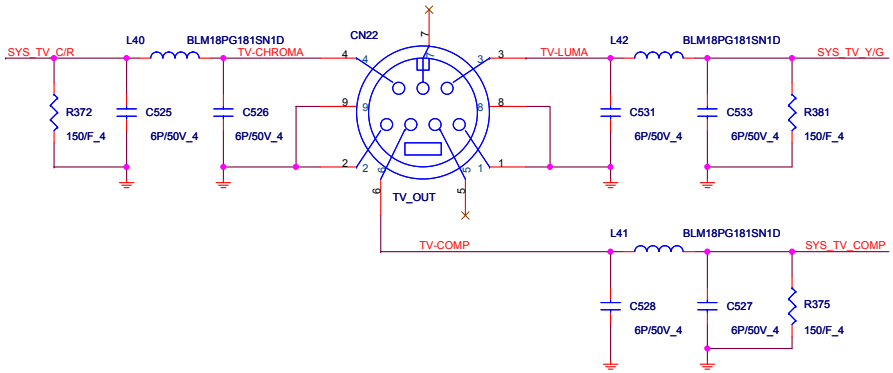


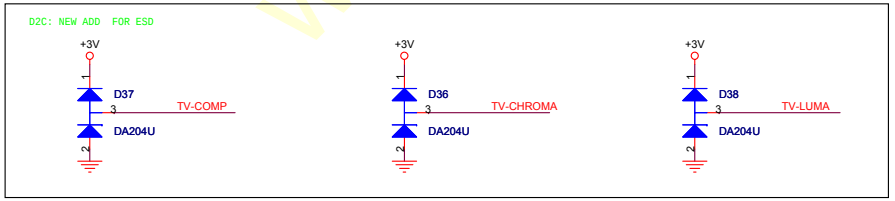




TV Out (SVHS) MiniDIN 7-pin







PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	CRT/TVOUT	E
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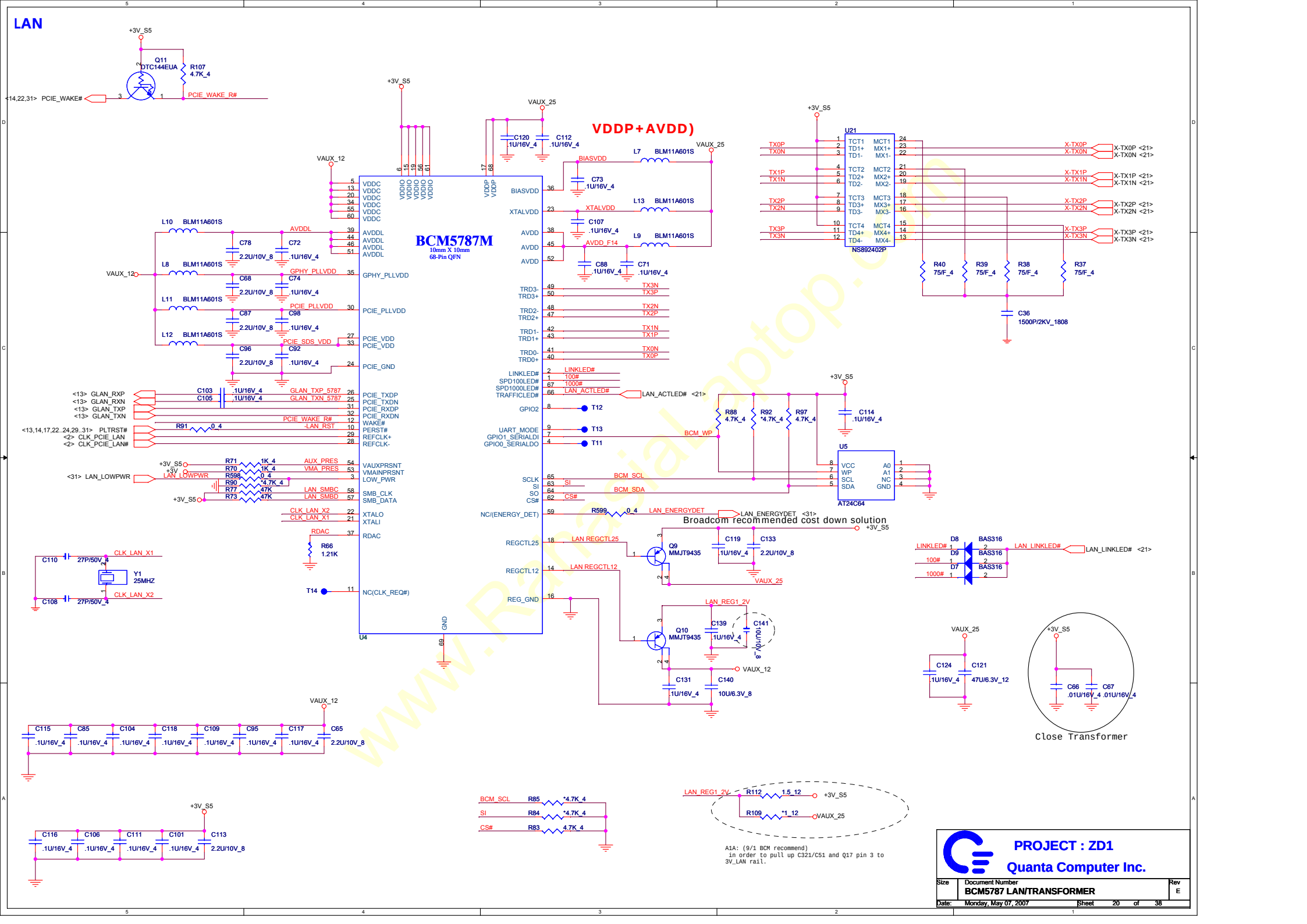
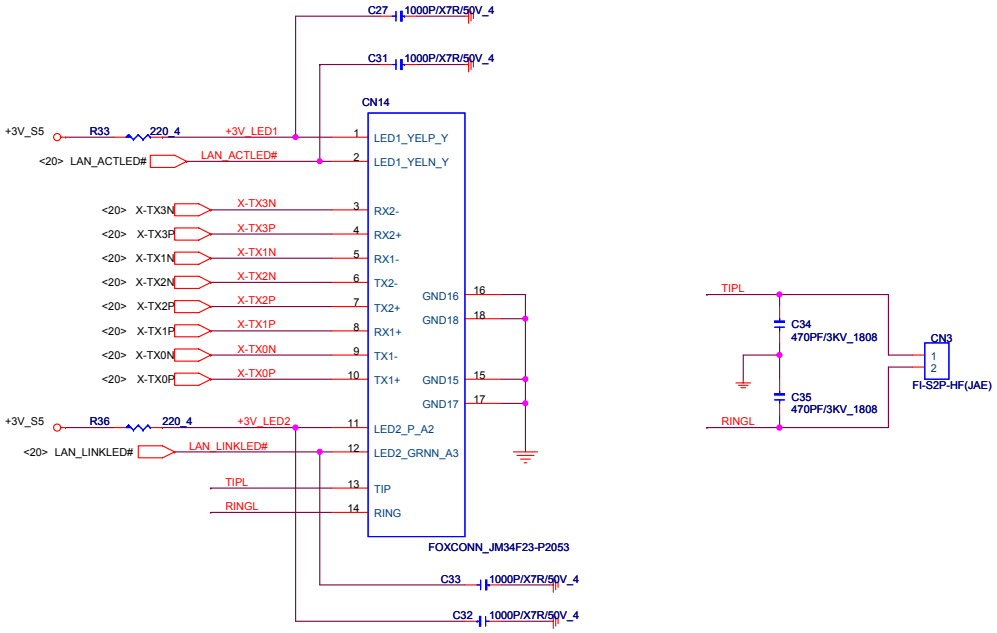
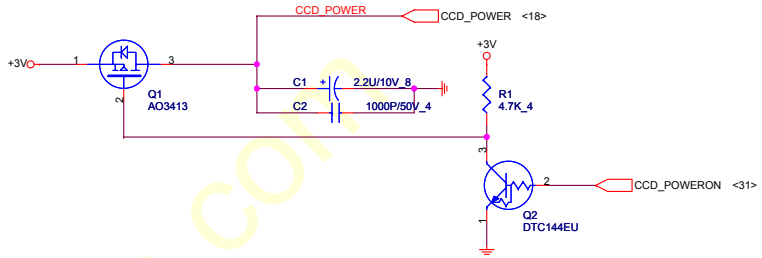
LAN



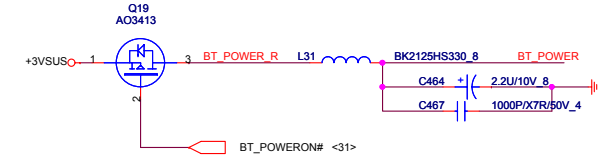
RJ45-11

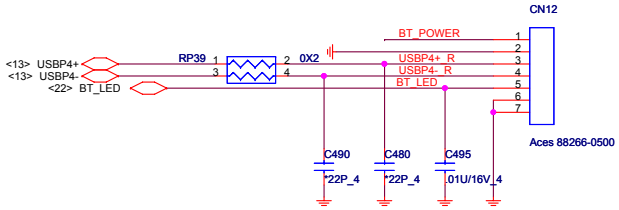


CAMERA MODULE CONNECTOR

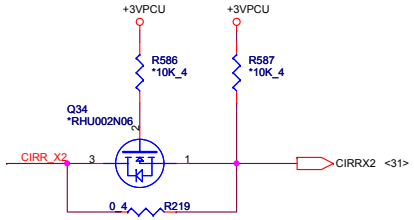


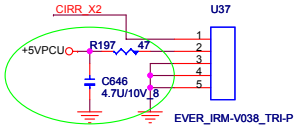
BLUETOOTH MODULE CONNECTOR





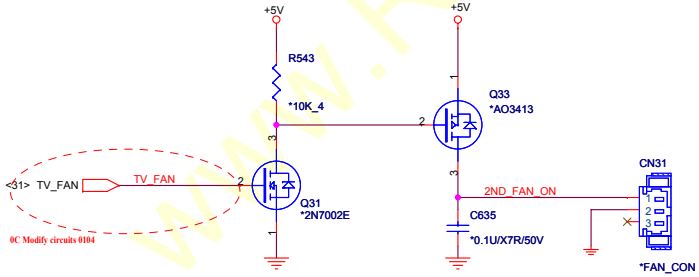
CIR





Modify Rev:D

2nd FAN



PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	BT/CCD/RJ45-11/CIR/2nd FAN	E
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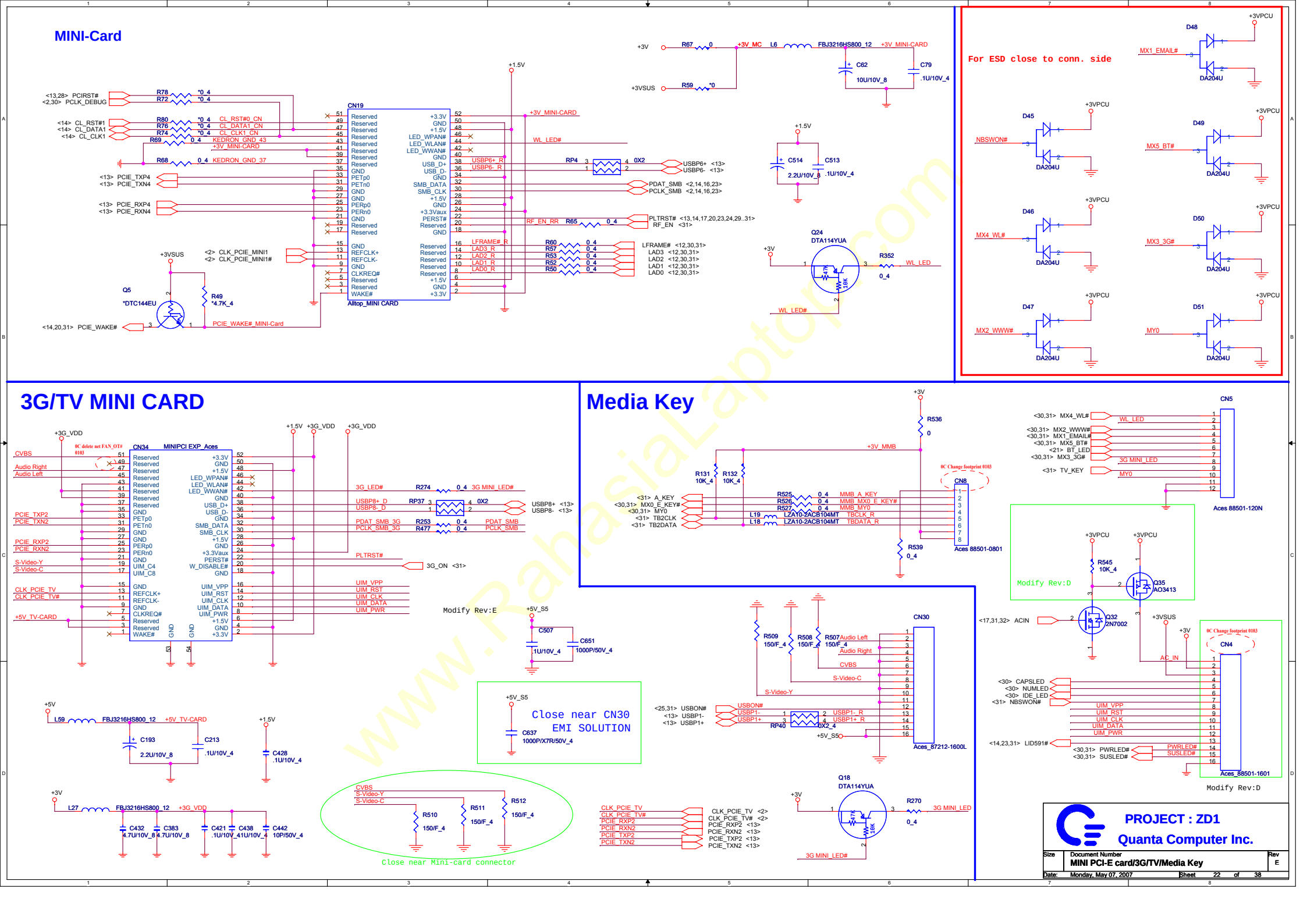
MINI-Card
CN19
Alltop_MINI CARD
Q5
*DTC144EU
R49
*4.7K_4
PCIE_WAKE#_MINI-Card
Q24
DTA114YUA
R352
WL_LED
WL_LED#
For ESD close to conn. side
D48
MX1_EMAIL#
D45
NBSWON#
D49
MX5_BT#
D46
MX4_WL#
D50
MX3_3G#
D47
MX2_WWW#
D51
MY0
DA204U
3G/TV MINI CARD
CN34
MINIPCI EXP_Aces
Modify Rev:E
Close near CN30
EMI SOLUTION
Close near Mini-card connector
Media Key
CN8
Aces 88501-0801
CN5
Aces 88501-120N
CN30
Aces_87212-1600L
CN4
Aces_88501-1601
Modify Rev:D
Q35
AO3413
Q32
2N7002
Q18
DTA114YUA
www.RahasiaLaptop.com
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Quanta Computer Inc.
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MINI PCI-E card/3G/TV/Media Key
Rev
E
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New card

CN9

<13> PCIE_TXP1
<13> PCIE_TXN1
<13> PCIE_RXP1
<13> PCIE_RXN1
<2> CLK_PCIE_NEW_C
<2> CLK_PCIE_NEW_C#
<13> NC_EN#
C381
C376
PERP3
PERN3
+NEW_3V
PERST#
+NEW_3VAUX
+NEW_1.5V
NEW_SMDATA
NEW_SMCLK
<13> USBP5+
<13> USBP5-
R441 0_4 USBP5+_R
R442 0_4 USBP5-_R

GND5 GND1 PETp0 PETn0 GND2 PERp0 PERn0 GND3 REFCLK+ REFCLK- CPPE# CLKREQ# +3.3V1 +3.3V2 PERST# +3.3VAUX WAKE# +1.5V1 +1.5V2 SMB_DATA SMB_CLK RESERVED1 RESERVED2 CPUSB# USB_D+ USB_D- GND4 GND6 GND27 GND28

*Aces_NEW CARD

CN44

PCIE_TXP1
PCIE_TXN1
PERP3
PERN3
CLK_PCIE_NEW_C
CLK_PCIE_NEW_C#
NC_EN#
+NEW_3V
PERST#
+NEW_3VAUX
+NEW_1.5V
NEW_SMDATA
NEW_SMCLK
USBP5+_R
USBP5-_R

GND1 PETp0 PETn0 GND2 PERp0 PERn0 GND3 REFCLK+ REFCLK- CPPE# CLKREQ# +3.3V1 +3.3V2 PERST# +3.3VAUX WAKE# +1.5V1 +1.5V2 SMB_DATA SMB_CLK RESERVED1 RESERVED2 CPUSB# USB_D+ USB_D- GND4 GND29 GND30 GND27 GND28

*Taitwun_NEW CARD

CN43

PCIE_TXP1
PCIE_TXN1
PERP3
PERN3
CLK_PCIE_NEW_C
CLK_PCIE_NEW_C#
NC_EN#
+NEW_3V
PERST#
+NEW_3VAUX
+NEW_1.5V
NEW_SMDATA
NEW_SMCLK
USBP5+_R
USBP5-_R

GND1 PETp0 PETn0 GND2 PERp0 PERn0 GND3 REFCLK+ REFCLK- CPPE# CLKREQ# +3.3V1 +3.3V2 PERST# +3.3VAUX WAKE# +1.5V1 +1.5V2 SMB_DATA SMB_CLK RESERVED1 RESERVED2 CPUSB# USB_D+ USB_D- GND4 GND29 GND30 GND27 GND28

FOX_EXPCARD

NEW CARD'S POWER SWITCH

U33
QFN-TPS2231RGP

+3V
+3V_S5
+1.5V
PLTRST#_NEW
*RCLKEN
NC
GND
GNDPAD
3.3VIN 3.3VOUT
AUXIN AUXOUT
1.5VIN 1.5VOUT
*SYSRST# *SHDN#
*STBY# *CPPE# *CPUSB#
PERST# OC#

+NEW_3V 1.3A
+NEW_3VAUX 275mA
+NEW_1.5V 650mA
NC_EN#
0C Connect to NC_EN# 0103
PERST#

REV:B MODIFY

TI : AL002231001
RICOH : AL005538001
GMT : AL000577008

<13,14,17,20,22,24,29..31> PLTRST#
Q37 2N7002
PLTRST#_NEW

REV:B MODIFY

+3V_S5 C599 .1U/10V_4
+3V C581 .1U/10V_4 C582 .1U/10V_4
+1.5V C598 .1U/10V_4 C597 .1U/10V_4
+NEW_3VAUX C351 .1U/10V_4
+NEW_3V C579 2.2U/10V_8 C354 .1U/10V_4 C357 .1U/10V_4
+NEW_1.5V C348 2.2U/10V_8 C344 .1U/10V_4

+NEW_3V
Q30 2N7002E
RP41 10KX2_4
<2,14,16,22> PDAT_SMB
NEW_SMDATA

+NEW_3V
Q29 2N7002E
<2,14,16,22> PCLK_SMB
NEW_SMCLK

LID SWITCH

+3V
R194 100K_4
<18> DISPON
DISPON D11 BAS316
LID591# <14,22,31>
D10 BAS316
R190 IV@0_4
R189 EV@0_4
INT_LVDS_BLON <6>
EV_LVDS_BLON <17>
R192 *1K_4
R191 100K_4
<demo circuit>
Crestline suggest 100K
G73 suggest 10K(ZS1 Default)
(Need confirm with Max)
Q12 DTC144EU
EC_FPBACK# <31>

HDMI

+5V
D35 BAS316 D34 BAS316
NV suggestion near HDMI connector
R354 2K_4 R353 2K_4
<17> MXM_HDMI_DDCCLK
L39 220R_100MHZ
HDMI_DDCCLK
C515 *.1U_4
<17> MXM_HDMI_DDCDATA
L38 220R_100MHZ
HDMI_DDCDATA
C516 *.1U_4

+5V
CN21
0C Change footprint 0103

<17> HDMITX2P HDMITX2P
<17> HDMITX2N HDMITX2N
<17> HDMITX1P HDMITX1P
<17> HDMITX1N HDMITX1N
<17> HDMITX0P HDMITX0P
<17> HDMITX0N HDMITX0N
<17> HDMICLK+ HDMICLK+
<17> HDMICLK- HDMICLK-
HDMI_DDCCLK
HDMI_DDCDATA
<17> HDMI_HP_A
R359 EV@10K_4 R602 1K_4 HP_DET
R356 EV@10K_4

D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET SHELL1 SHELL2 GND GND

HDMI CON

HDMI monitor default have PU to 5V.So ZY3 PD for level change.And serial R for current limited

+5V
C632 .1U/16V_4 C631 .1U/16V_4 C633 .1U/16V_4

U26 *RClamp0514M_AG
HDMITX0P HDMITX0N HDMI_HP_A

U27 *RClamp0514M_AG
HDMITX2P HDMITX2N HDMITX1P HDMITX1N

U25 *RClamp0514M_AG
HDMICLK+ HDMICLK- HDMI_DDCCLK HDMI_DDCDATA

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Quanta Computer Inc.

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	NEW CARD/HDMI/LID	E
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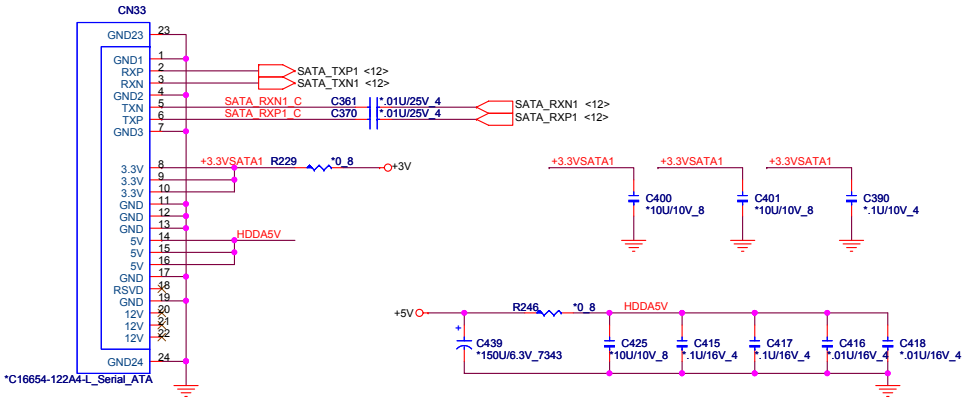
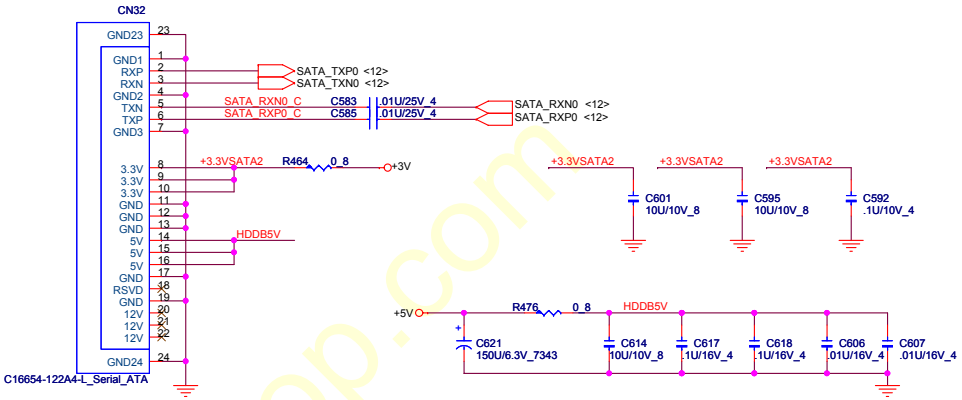
SATA HDD1

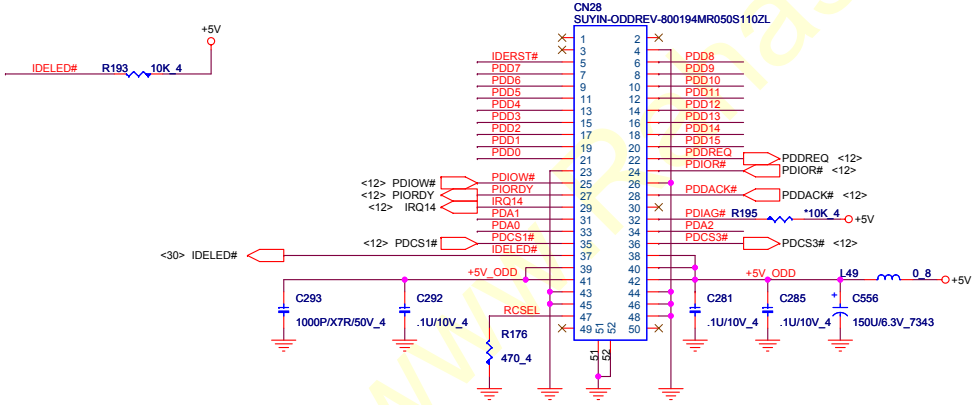


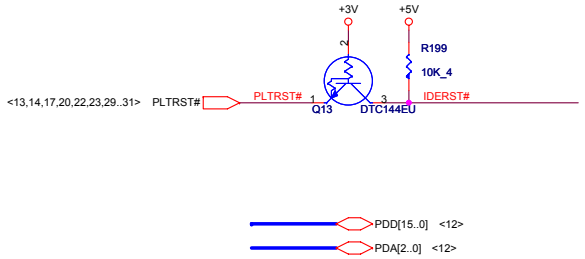
SATA HDD2

Main



ODD (PATA)





PROJECT : ZD1

Quanta Computer Inc.

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	SATA-HDD & PATA-ODD	E
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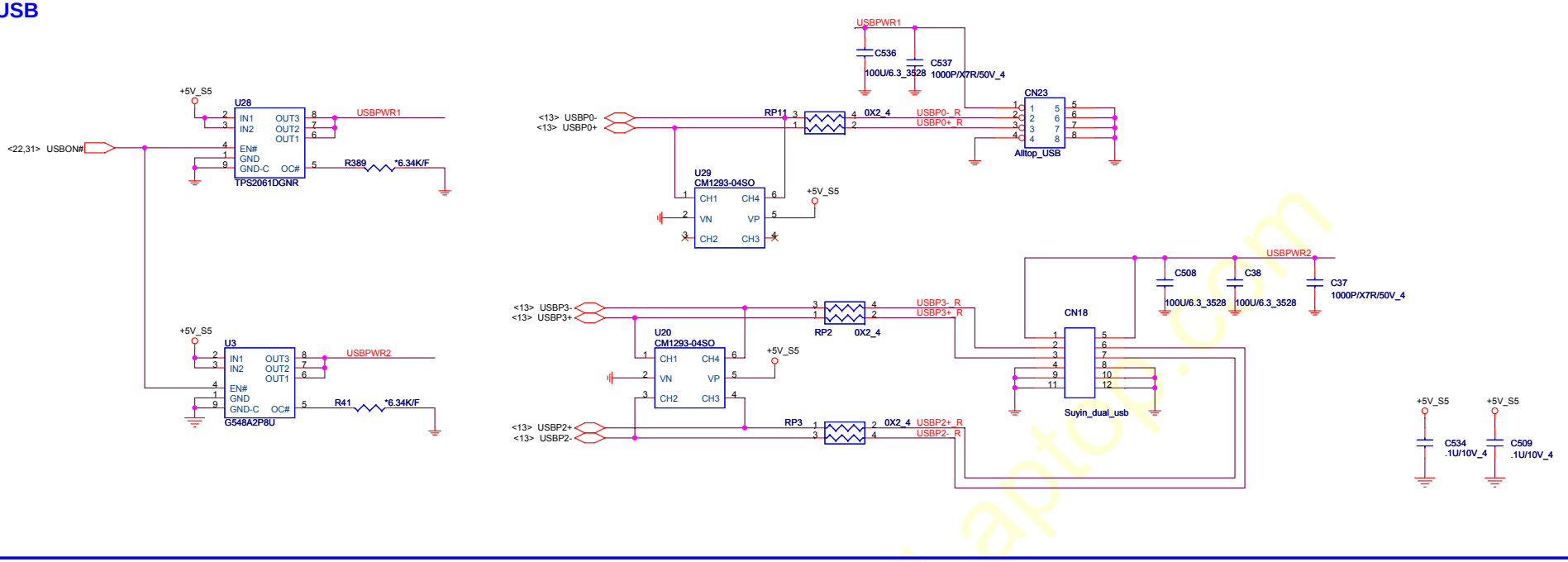
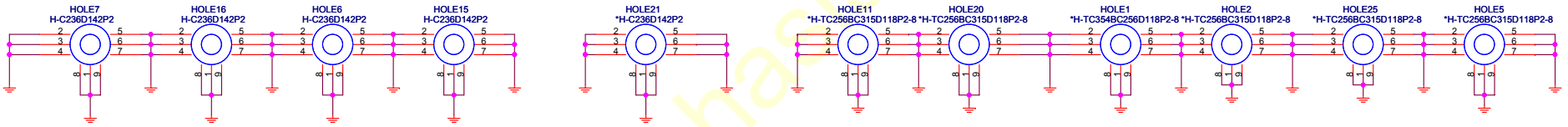
USB

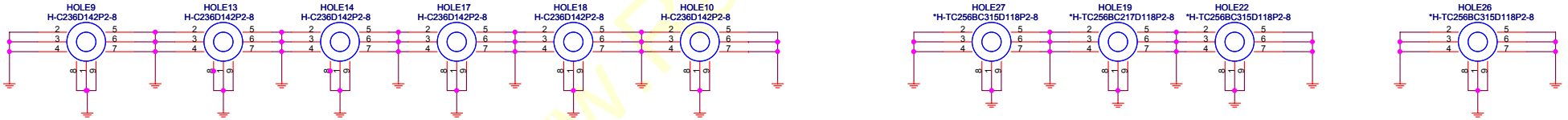


HOLES

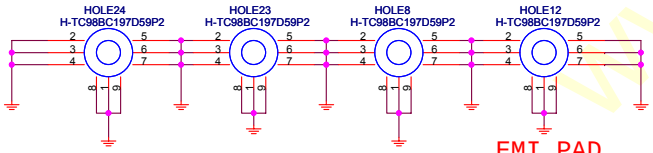
CPU NUT



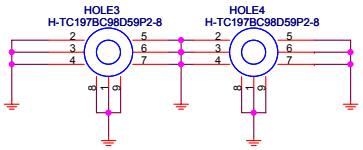
MXM NUT



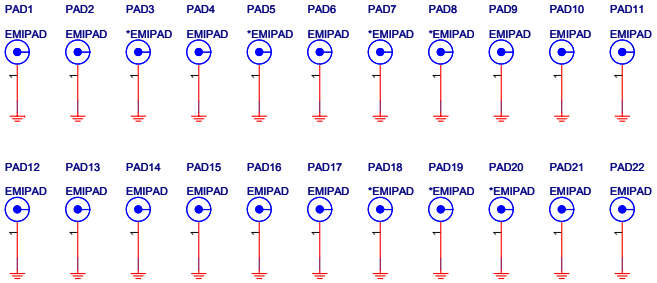
MINI CARD NUT



MDC NUT

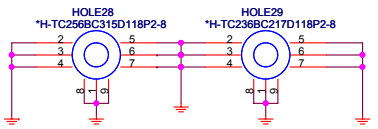


EMI PAD



Footprint error: PAD15 , PAD4 ,PAD16:
emipad97x87

Modify Rev:E



PROJECT : ZD1

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	USB/HOLE	E
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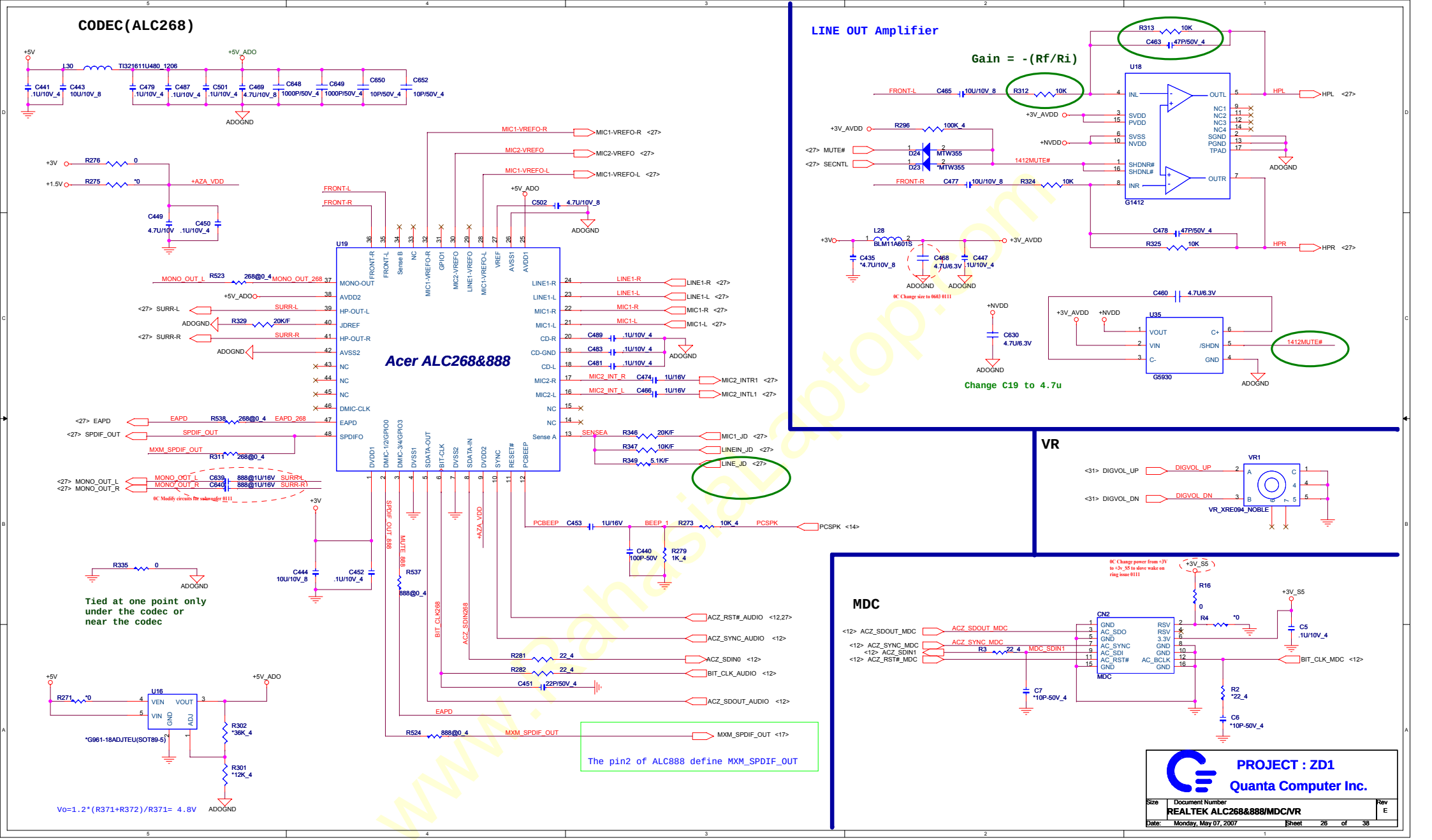
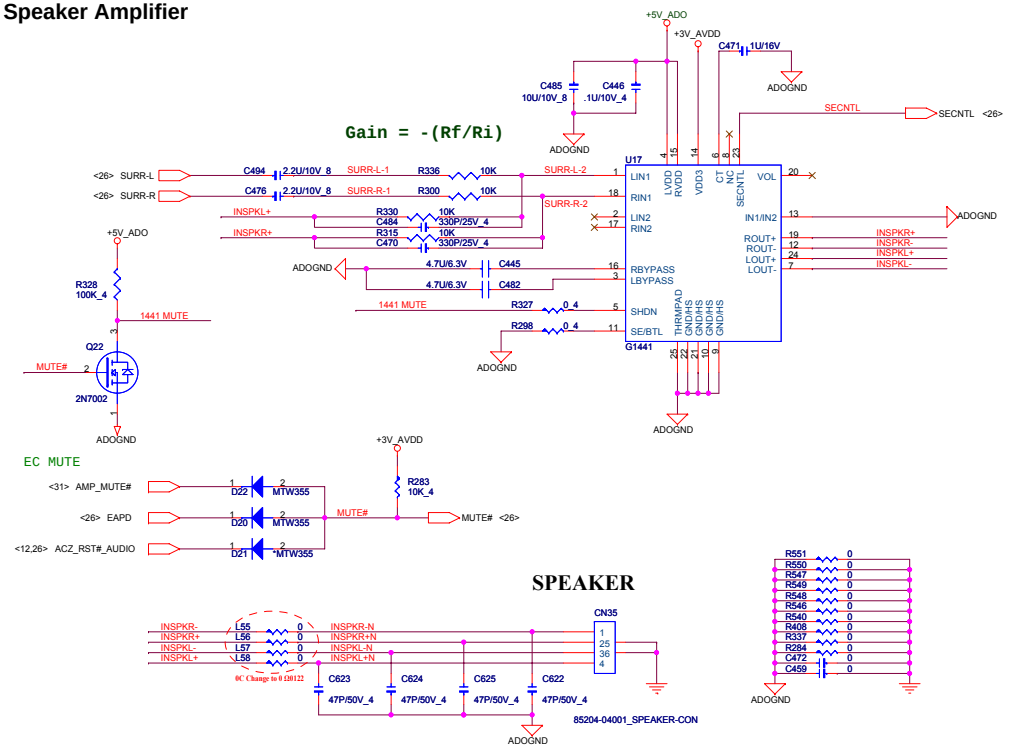
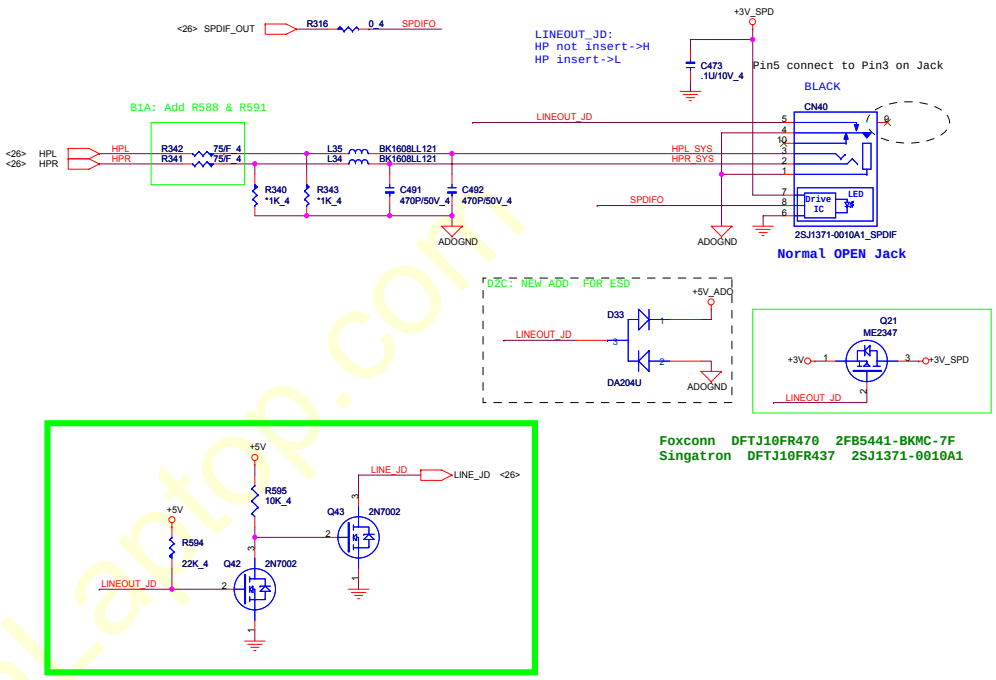


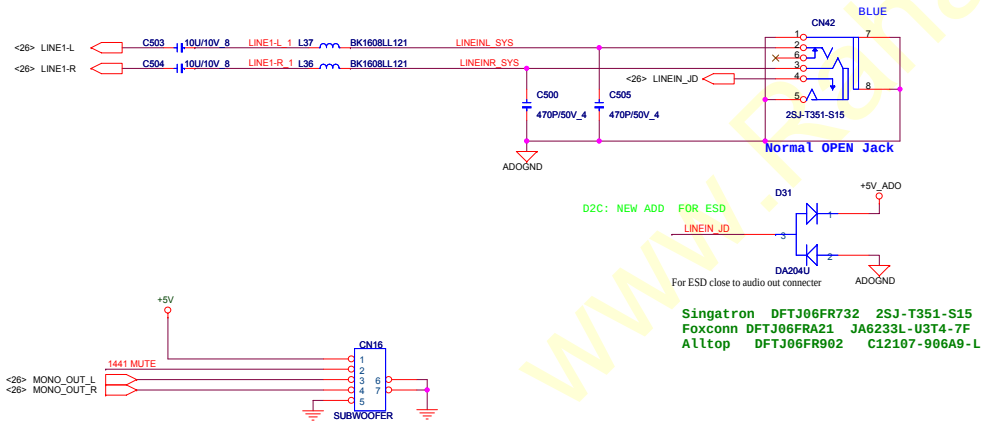
Speaker Amplifier



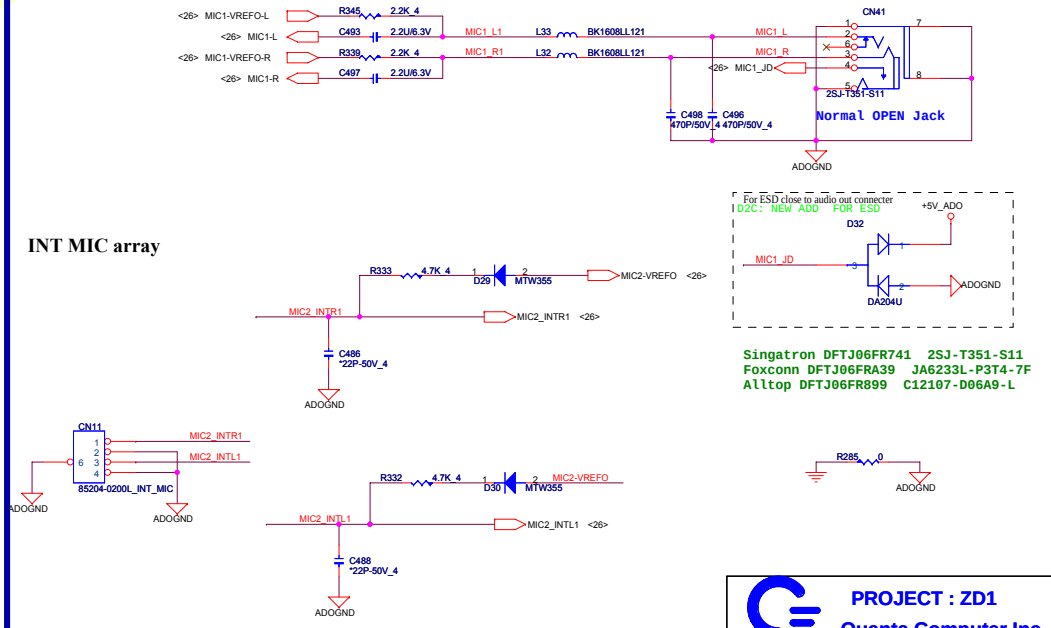
SYSTEM LINE OUT/SPDIF



SYSTEM LINE IN/SUBWOOFER



MIC



PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	E
Date: Monday, May 07, 2007	Sheet 27 of 38	

R5C832 : AJ5C8320H26
R5C833 : AJ5C8330H05

1394

AS CLOSE AS POSSIBLE TO R5C833

COMMON MODE CHOKE NEAR CONN.

38M030006-00
IEEE 1394 CONN 6POLE R/A 787956-1 DIP AMP
<MOUNTED>

5 IN 1 CARD READER

Memory Card Power Supply

*CARD_READER_PLASTREN-CM47-X-38P-L

*PROCONN-MXP038-A0-4010

CARD_READER_TTN_R013-B10-XX-C

PowerOnReset for VccCore

When GRESET# is controlled by system, the pull-up resistor(R762) and capacitor(C492) do not need to apply.

When HWSPND# is controlled by system, the pull-up resistor(R755) dose not need to apply.

* NOT Use EEPROM : PU
* Use EEPROM : PD

Ground guard

GUARD GND

* NOT Use EEPROM : R759 : installed R760,U43,C505 : NOT installed
* Use EEPROM : R760,U43,C505 : installed R759 : NOT installed

> 1 ms >60 ns

> 100 ns

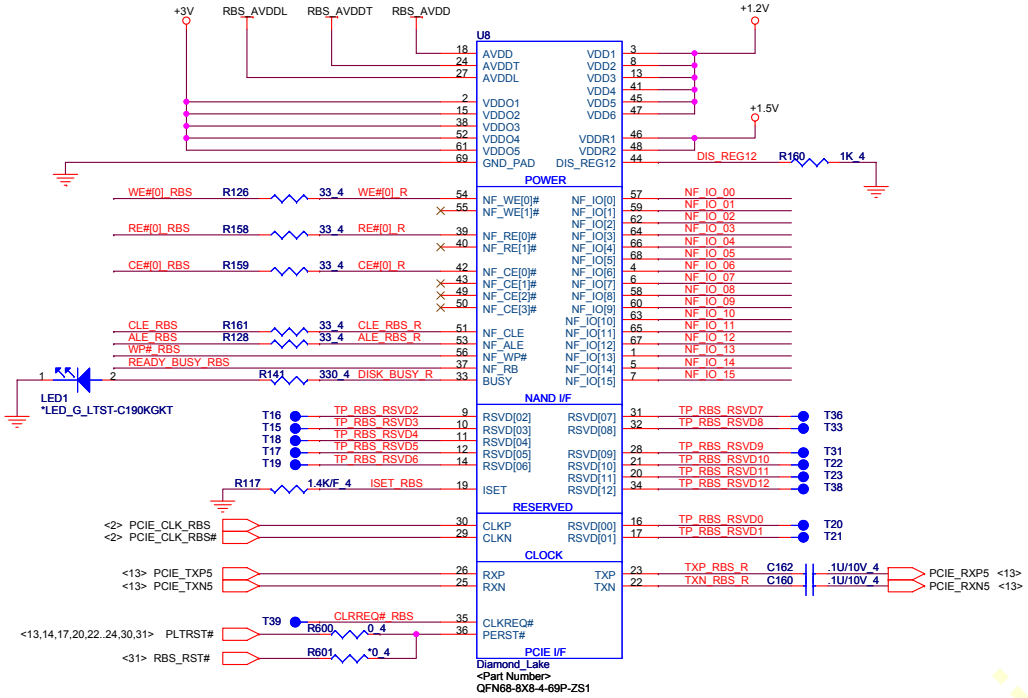
VCC
GRST#
PRST#
HWSPND#
PCLK(33MHz)

PROJECT : ZD1
Quanta Computer Inc.

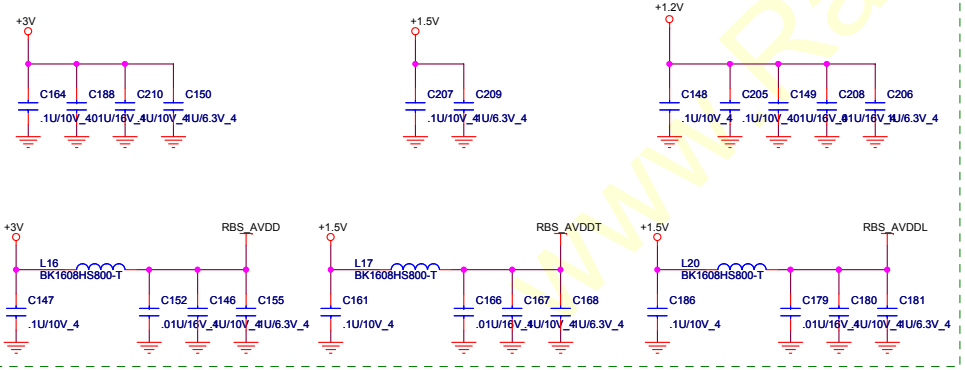
Size	Document Number	Rev
	R5C832/833(5IN1/1394)	E
Date: Monday, May 07, 2007	Sheet 28 of 38	

ROBSON

DIAMOND-LAKE ASIC



PLACE AS CLOSE AS POSSIBLE TO DIAMOND-LAKE ASIC.

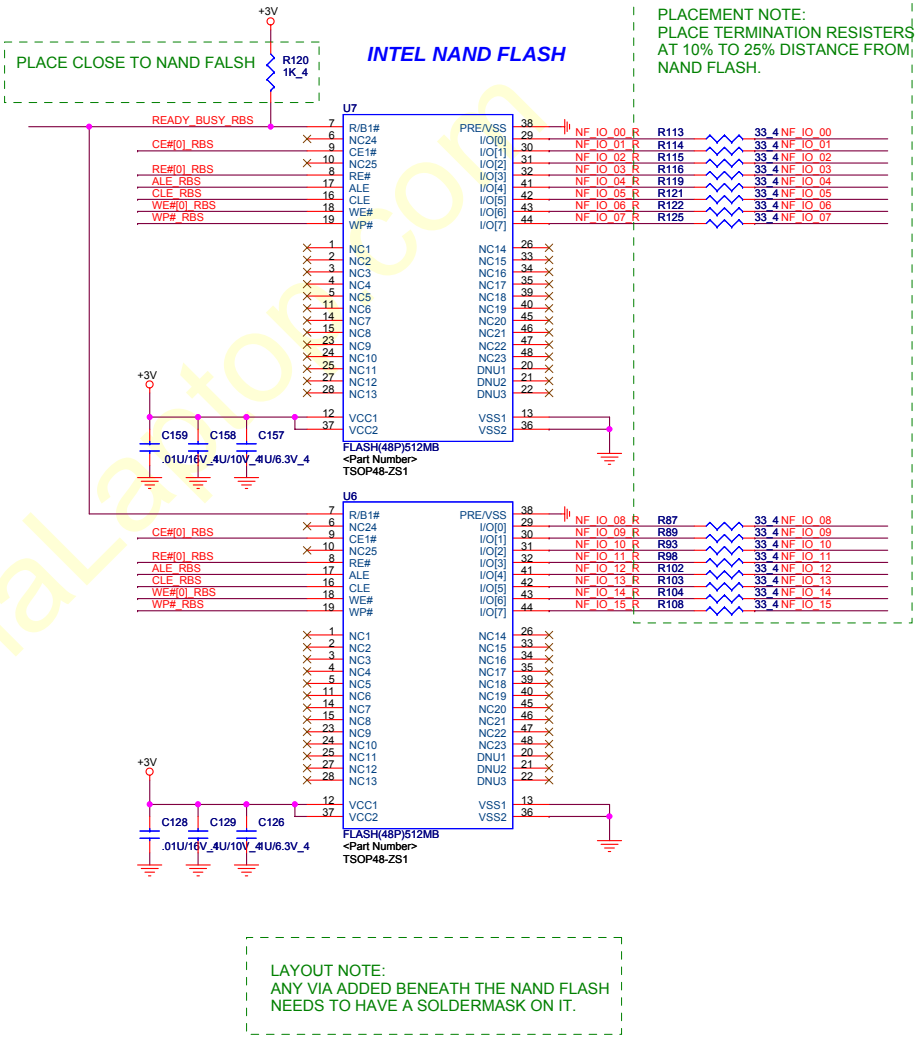


NF_IO_00 — R123 *10K_4

STUFF: INDICATES A 2KB VIRTUAL PAGE. => 256MB
DESTUFF: INDIACTESS A 4KB VIRTUAL PAGE => 512MB & 1024MB

INTEL NAND FLASH

PLACE CLOSE TO NAND FALSH



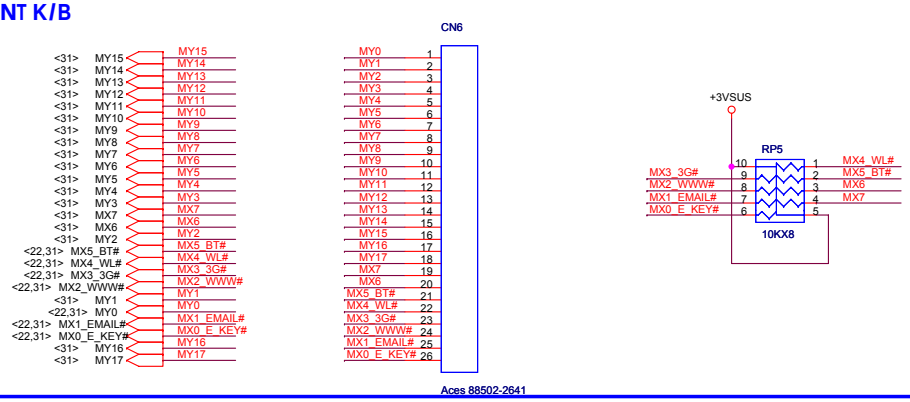
PLACEMENT NOTE:
PLACE TERMINATION RESISTERS AT 10% TO 25% DISTANCE FROM NAND FLASH.

LAYOUT NOTE:
ANY VIA ADDED BENEATH THE NAND FLASH NEEDS TO HAVE A SOLDERMASK ON IT.

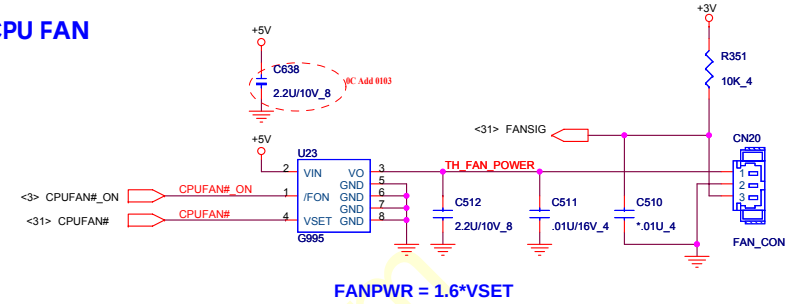
PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	ROBSON	E
Date: Monday, May 07, 2007	Sheet 29 of 38	

INT K/B

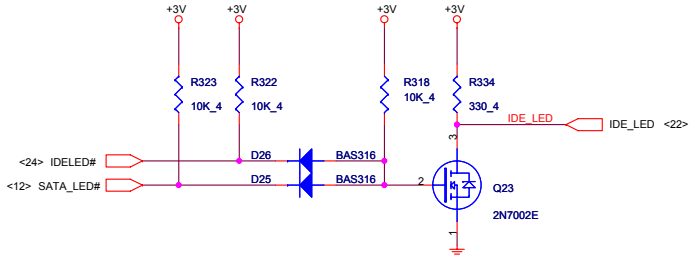


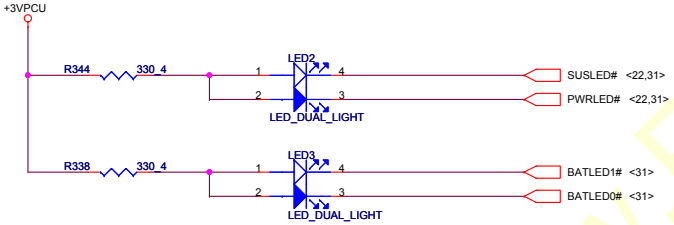
CPU FAN

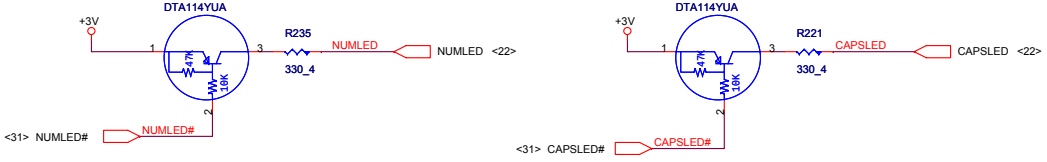


FANPWR = 1.6*VSET

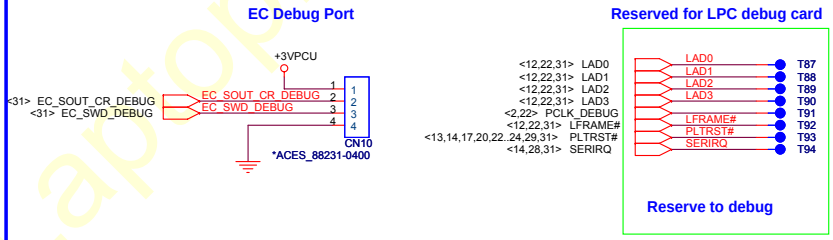
LED



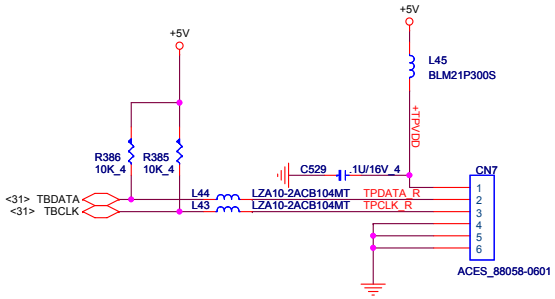




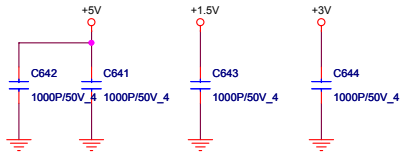
DEBUG PORT



T/P



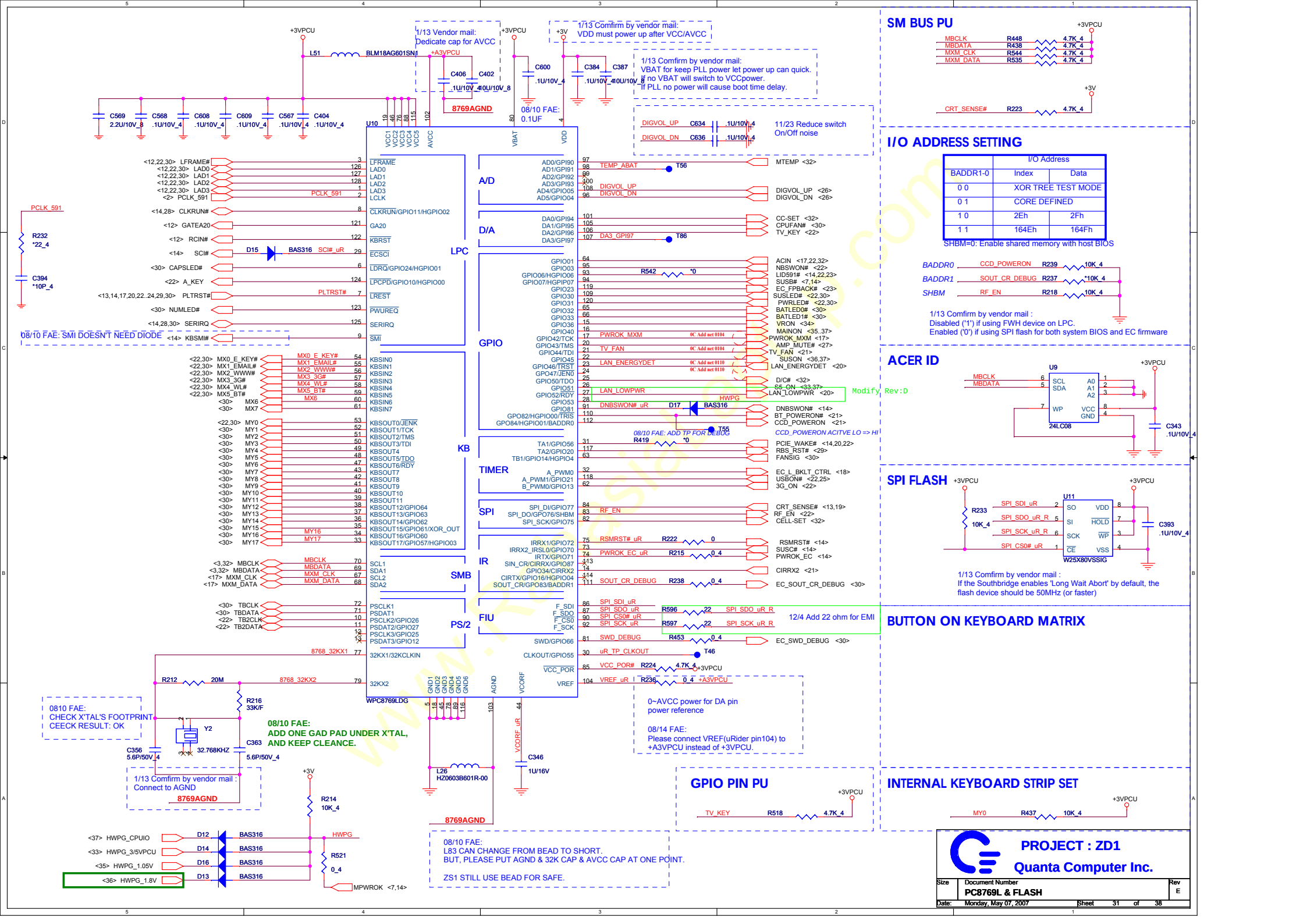
EMI solution

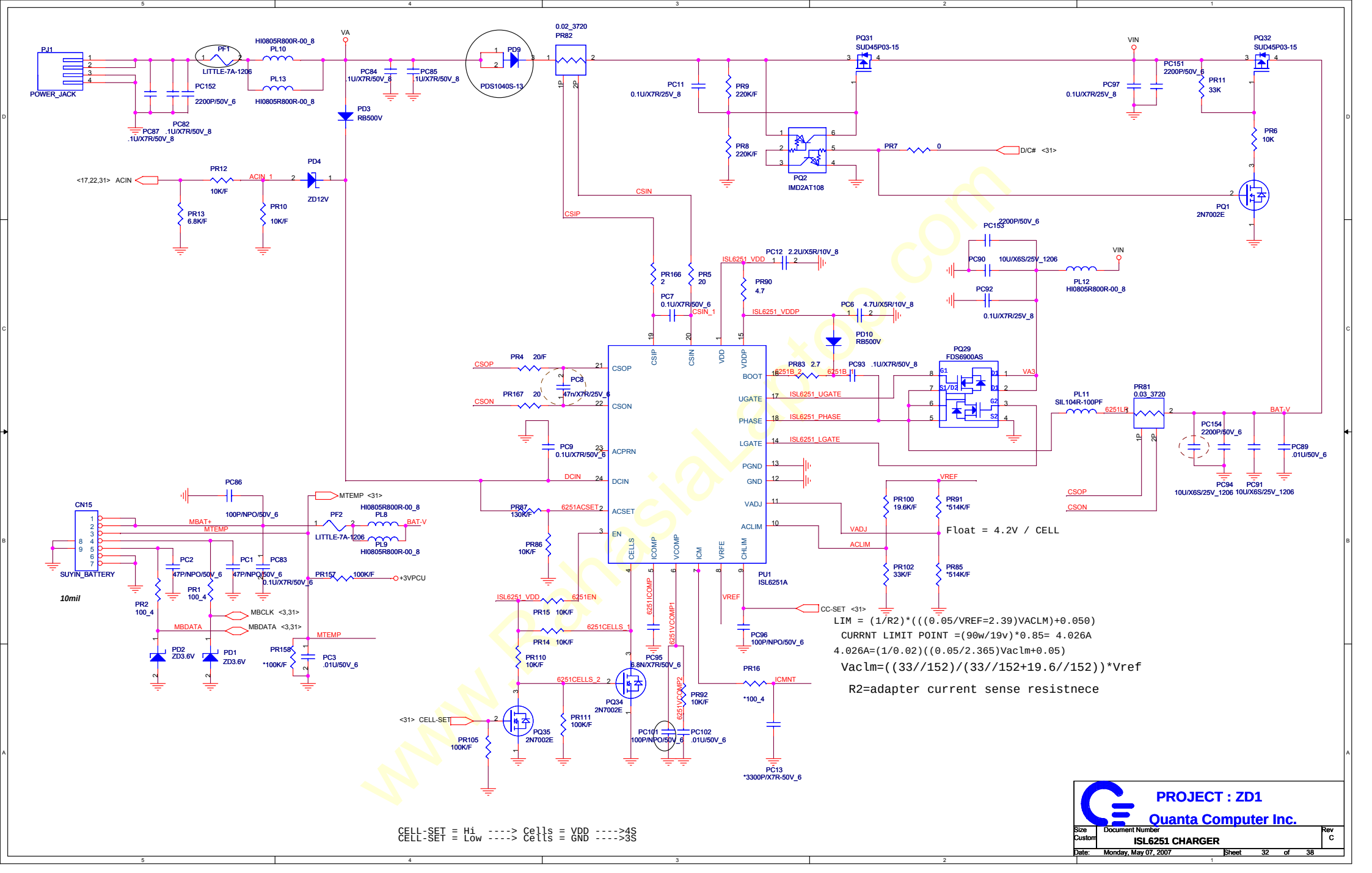


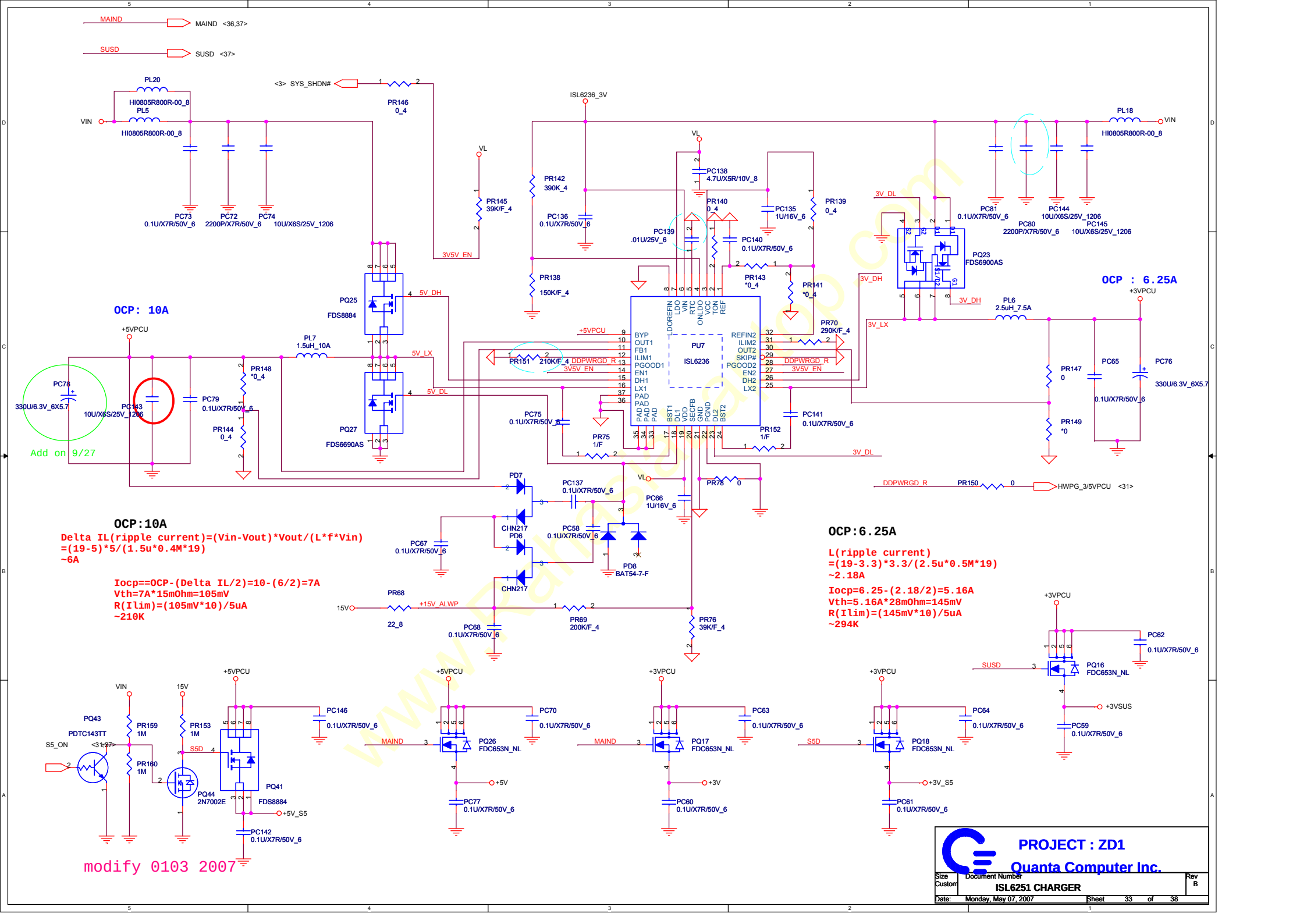
PROJECT : ZD1

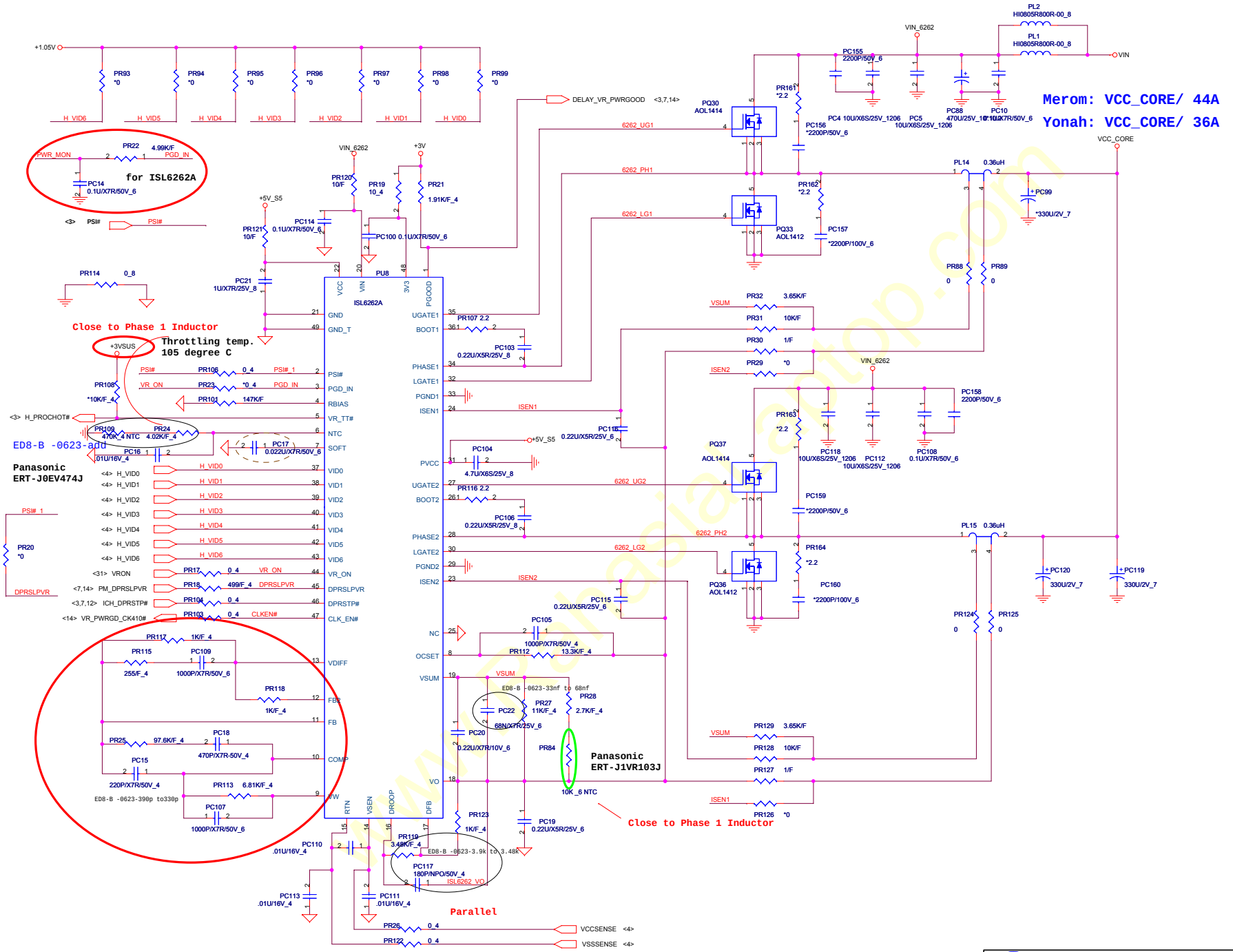
Quanta Computer Inc.

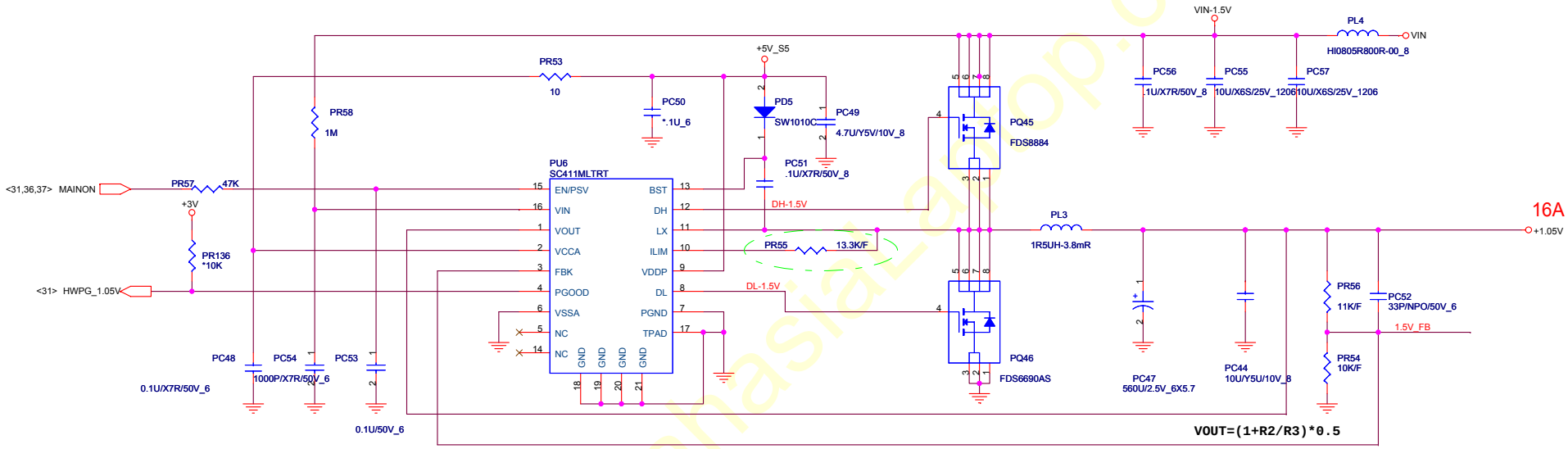
Size	Document Number	Rev
	FAN,LED,KB,DEBUG PORT,TP	E
Date: Monday, May 07, 2007	Sheet 30 of 38	


U10
WPC8769LDG
LPC
A/D
D/A
GPIO
KB
TIMER
SPI
IR
SMB
PS/2
FIU
LFRAME
LAD0
LAD1
LAD2
LAD3
LCLK
CLKRUN/GPIO11/HGPIO02
GA20
KBRST
ECSCI
LDRQ/GPIO24/HGPIO01
LPCPD/GPIO10/HGPIO00
LRESET
PWUREQ
SERIRQ
SMI
KBSIN0
KBSIN1
KBSIN2
KBSIN3
KBSIN4
KBSIN5
KBSIN6
KBSIN7
KBSOUT0/JENK
KBSOUT1/TCK
KBSOUT2/TMS
KBSOUT3/TDI
KBSOUT4
KBSOUT5/TDO
KBSOUT6/RDY
KBSOUT7
KBSOUT8
KBSOUT9
KBSOUT10
KBSOUT11
KBSOUT12/GPIO64
KBSOUT13/GPIO63
KBSOUT14/GPIO62
KBSOUT15/GPIO61/XOR_OUT
KBSOUT16/GPIO60
KBSOUT17/GPIO57/HGPIO03
SCL1
SDA1
SCL2
SDA2
PSCLK1
PSDAT1
PSCLK2/GPIO26
PSDAT2/GPIO27
PSCLK3/GPIO25
PSDAT3/GPIO12
32KX1/32KCLKIN
32KX2
AD0/GPI90
AD1/GPI91
AD2/GPI92
AD3/GPI93
AD4/GPIO05
AD5/GPIO04
DA0/GPI94
DA1/GPI95
DA2/GPI96
DA3/GPI97
GPIO01
GPIO03
GPIO06/HGPIO06
GPIO07/HGPIP07
GPIO23
GPIO30
GPIO31
GPIO32
GPIO33
GPIO36
GPIO40
GPIO42/TCK
GPIO43/TMS
GPIO44/TDI
GPIO45
GPIO46/TRST
GPIO47/JENO
GPIO50/TDO
GPIO51
GPIO52/RDY
GPIO53
GPIO81
GPO82/HGPIO00/TRIS
GPO84/HGPIO01/BADDR0
TA1/GPIO56
TA2/GPIO20
TB1/GPIO14/HGPIO4
A_PWM0
A_PWM1/GPIO21
B_PWM0/GPIO13
SPI_DI/GPIO77
SPI_DO/GPO76/SHBM
SPI_SCK/GPIO75
IRRX1/GPIO72
IRRX2_IRSL0/GPIO70
IRTX/GPIO71
SIN_CR/CIRRX/GPIO87
GPIO34/CIRRX2
CIRTX/GPIO16/HGPIO04
SOUT_CR/GPO83/BADDR1
F_SDI
F_SDO
F_CS0
F_SCK
SWD/GPIO66
CLKOUT/GPIO55
VCC_POR
VREF
+3VPCU
+A3VPCU
+3V
8769AGND
L51 BLM18AG601SN1
C406 C402 .1U/10V_4 10U/10V_8
C600 .1U/10V_4
C384 C387 .1U/10V_4 10U/10V_8
C569 2.2U/10V_8
C568 .1U/10V_4
C608 .1U/10V_4
C609 .1U/10V_4
C567 .1U/10V_4
C404 .1U/10V_4
1/13 Vendor mail:
Dedicate cap for AVCC
1/13 Comfirm by vendor mail:
VDD must power up after VCC/AVCC
1/13 Comfirm by vendor mail:
VBAT for keep PLL power let power up can quick.
If no VBAT will switch to VCCpower.
If PLL no power will cause boot time delay.
08/10 FAE:
0.1UF
DIGVOL_UP C634 .1U/10V_4
DIGVOL_DN C636 .1U/10V_4
11/23 Reduce switch
On/Off noise
R232 *22_4
C394 *10P_4
PCLK_591
D15 BAS316 SCI#_uR
PLTRST#
08/10 FAE: SMI DOESN'T NEED DIODE
R542 *0
R419 *0
HWPG
D17 BAS316
T55
08/10 FAE: ADD TP FOR DEBUG
Modify Rev:D
CCD_POWERON ACITVE LO => HI
R222 0
R215 0_4
R238 0_4
R596 22
R597 22
SPI_SDO_uR_R
SPI_SCK_uR_R
12/4 Add 22 ohm for EMI
R453 0_4
R224 4.7K_4
R236 0_4
T46
0~AVCC power for DA pin
power reference
08/14 FAE:
Please connect VREF(uRider pin104) to
+A3VPCU instead of +3VPCU.
R212 20M
R216 33K/F
Y2 32.768KHZ
C356 5.6P/50V_4
C363 5.6P/50V_4
0810 FAE:
CHECK X'TAL'S FOOTPRINT
CEECK RESULT: OK
08/10 FAE:
ADD ONE GAD PAD UNDER X'TAL,
AND KEEP CLEANCE.
1/13 Comfirm by vendor mail :
Connect to AGND
L26 HZ0603B601R-00
C346 1U/16V
VCORF_uR
R214 10K_4
D12 BAS316
D14 BAS316
D16 BAS316
D13 BAS316
HWPG
R521 0_4
MPWROK <7,14>
<37> HWPG_CPUIO
<33> HWPG_3/5VPCU
<35> HWPG_1.05V
<36> HWPG_1.8V
08/10 FAE:
L83 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.
SM BUS PU
MBCLK R448 4.7K_4
MBDATA R438 4.7K_4
MXM_CLK R544 4.7K_4
MXM_DATA R535 4.7K_4
CRT_SENSE# R223 4.7K_4
I/O ADDRESS SETTING
I/O Address
BADDR1-0 | Index | Data
0 0 XOR TREE TEST MODE
0 1 CORE DEFINED
1 0 2Eh 2Fh
1 1 164Eh 164Fh
SHBM=0: Enable shared memory with host BIOS
BADDR0 CCD_POWERON R239 10K_4
BADDR1 SOUT_CR_DEBUG R237 *10K_4
SHBM RF_EN R218 10K_4
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
ACER ID
U9
24LC08
C343 .1U/10V_4
SPI FLASH
U11
W25X80VSSIG
R233 10K_4
C393 .1U/10V_4
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the
flash device should be 50MHz (or faster)
BUTTON ON KEYBOARD MATRIX
GPIO PIN PU
TV_KEY R518 4.7K_4
INTERNAL KEYBOARD STRIP SET
MY0 R437 10K_4
PROJECT : ZD1
Quanta Computer Inc.
PC8769L & FLASH
Rev E
Monday, May 07, 2007
Sheet 31 of 38




MAIND
MAIND <36,37>
SUSD
SUSD <37>
<3> SYS_SHDN#
VIN
PL20
HI0805R800R-00_8
PL5
HI0805R800R-00_8
PC73 0.1U/X7R/50V_6
PC72 2200P/X7R/50V_6
PC74 10U/X6S/25V_1206
PR146 0_4
3V5V_EN
VL
PR145 39K/F_4
ISL6236_3V
PR142 390K_4
PC136 0.1U/X7R/50V_6
PR138 150K/F_4
PC139 .01U/25V_6
PC138 4.7U/X5R/10V_8
PR140 0_4
PC135 1U/16V_6
PC140 0.1U/X7R/50V_6
PR139 0_4
PR143 *0_4
PR141 *0_4
PL18
HI0805R800R-00_8
PC81 0.1U/X7R/50V_6
PC80 2200P/X7R/50V_6
PC144 10U/X6S/25V_1206
PC145 10U/X6S/25V_1206
PQ23 FDS6900AS
3V_DH
3V_LX
3V_DL
OCP : 6.25A
+3VPCU
PL6 2.5uH_7.5A
PR70 290K/F_4
PR147 0
PR149 *0
PC65 0.1U/X7R/50V_6
PC76 330U/6.3V_6X5.7
OCP: 10A
+5VPCU
PL7 1.5uH_10A
PQ25 FDS8884
5V_DH
5V_LX
5V_DL
PQ27 FDS6690AS
PR148 *0_4
PR144 0_4
PC78 330U/6.3V_6X5.7
PC143 10U/X6S/25V_1206
PC79 0.1U/X7R/50V_6
Add on 9/27
PU7 ISL6236
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD PAD
DDREFIN LDO VIN RTO ONLDO VCC TON REF
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DLI VDD SRFB SRGD PGND DL2 BST2
PR151 210K/F_4
DDPWRGD_R
PR150 0
HWPG_3/5VPCU <31>
PC75 0.1U/X7R/50V_6
PR75 1/F
PR152 1/F
PC141 0.1U/X7R/50V_6
PD7
CHN217
PD6
CHN217
PC137 0.1U/X7R/50V_6
PC66 1U/16V_6
PC67 0.1U/X7R/50V_6
PC58 0.1U/X7R/50V_6
PD8 BAT54-7-F
PR78 0
OCP:10A
Delta IL(ripple current)=(Vin-Vout)*Vout/(L*f*Vin)
=(19-5)*5/(1.5u*0.4M*19)
~6A
Iocp==OCP-(Delta IL/2)=10-(6/2)=7A
Vth=7A*15mOhm=105mV
R(Ilim)=(105mV*10)/5uA
~210K
OCP:6.25A
L(ripple current)
=(19-3.3)*3.3/(2.5u*0.5M*19)
~2.18A
Iocp=6.25-(2.18/2)=5.16A
Vth=5.16A*28mOhm=145mV
R(Ilim)=(145mV*10)/5uA
~294K
15V
PR68 22_8
+15V_ALWP
PC68 0.1U/X7R/50V_6
PR69 200K/F_4
PR76 39K/F_4
PQ43 PDTC143TT
S5_ON
PR159 1M
PR160 1M
PR153 1M
S5D
PQ44 2N7002E
PQ41 FDS8884
+5V_S5
PC146 0.1U/X7R/50V_6
PC142 0.1U/X7R/50V_6
PQ26 FDC653N_NL
PC70 0.1U/X7R/50V_6
+5V
PC77 0.1U/X7R/50V_6
PQ17 FDC653N_NL
PC63 0.1U/X7R/50V_6
+3V
PC60 0.1U/X7R/50V_6
PQ18 FDC653N_NL
PC64 0.1U/X7R/50V_6
+3V_S5
PC61 0.1U/X7R/50V_6
PQ16 FDC653N_NL
PC62 0.1U/X7R/50V_6
+3VSUS
PC59 0.1U/X7R/50V_6
modify 0103 2007
PROJECT : ZD1
Quanta Computer Inc.
Size Custom
Document Number ISL6251 CHARGER
Rev B
Date: Monday, May 07, 2007
Sheet 33 of 38

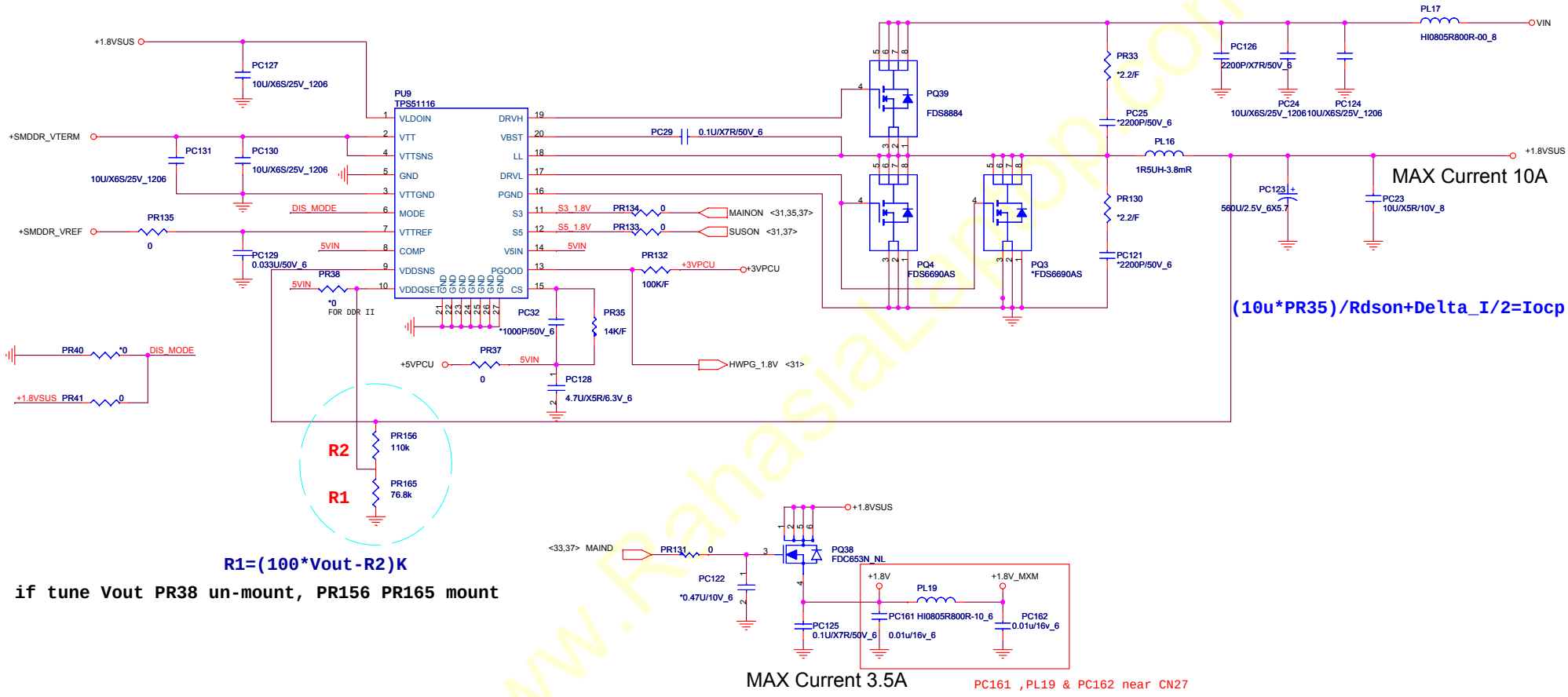

Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A
for ISL6262A
Close to Phase 1 Inductor
Throttling temp.
105 degree C
ED8-B -0623-add
Panasonic
ERT-J0EV474J
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Parallel
ISL6262A
VCC_CORE
PROJECT : ZD1
Quanta Computer Inc.
CPU CORE(ISL6262)
Monday, May 07, 2007



Rdson*Iocp=PR55*10u **Rdson=15m ohm**

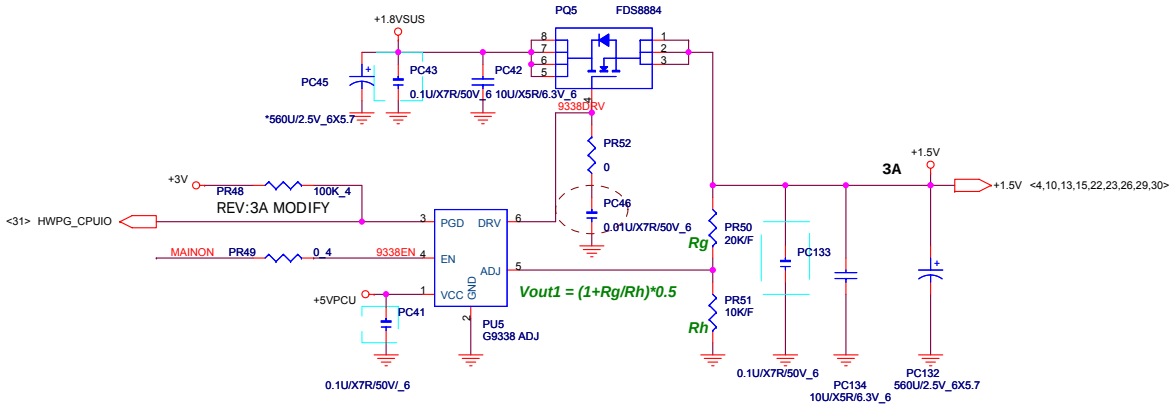
PROJECT : ZD1
Quanta Computer Inc.

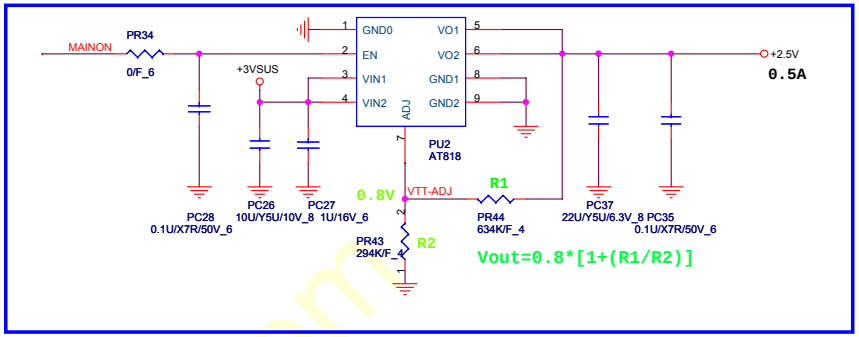
Size	Document Number	Rev
	VTT +1.05V	C
Date: Monday, May 07, 2007	Sheet 35 of 38	

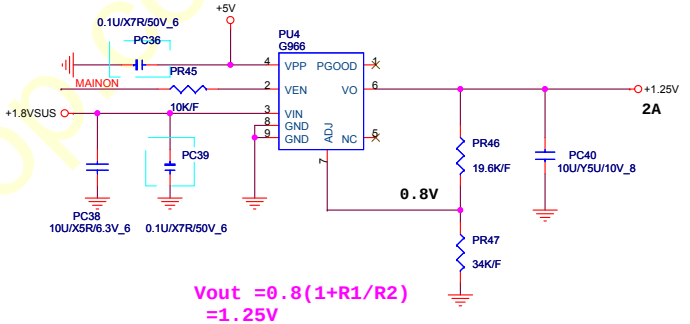


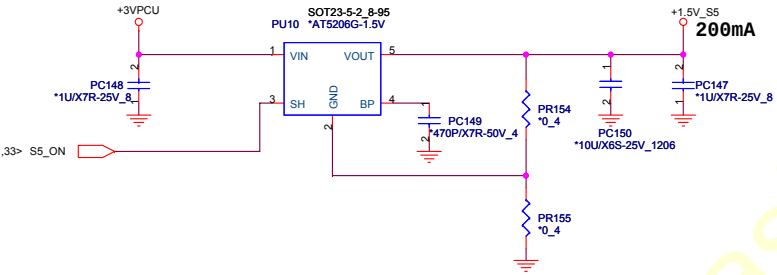
PROJECT : ZD1
Quanta Computer Inc.

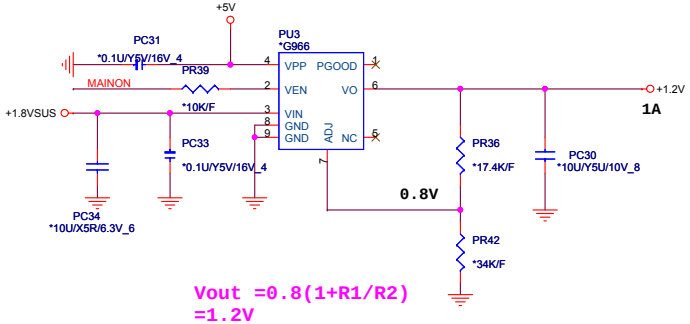
Size	Document Number	Rev
	DDR 1.8V(TPS51116)	B
Date: Monday, May 07, 2007	Sheet 36 of 38	

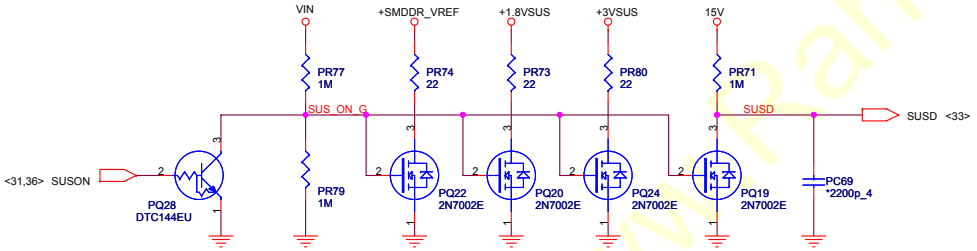




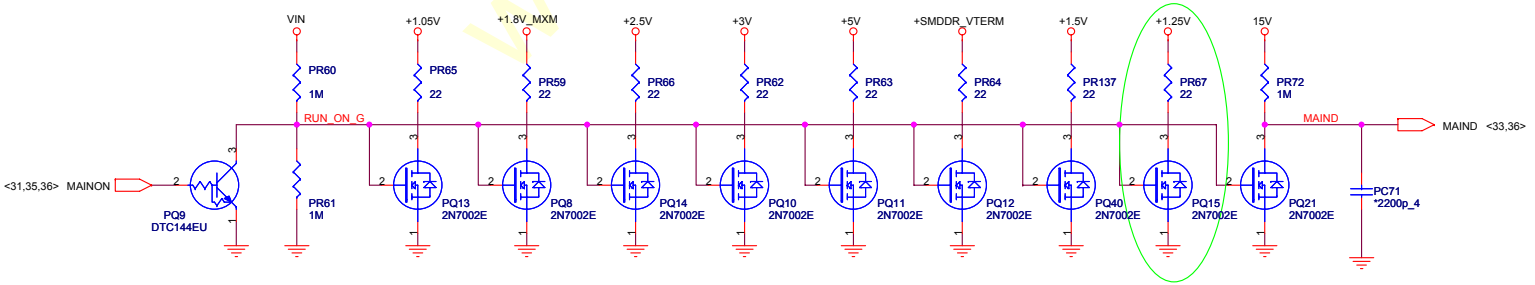








Add by power on 10/19



PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (1.5V/2.5V)	C
Date: Monday, May 07, 2007	Sheet 37 of 38	

CHANGE LIST

Model: ZD1 MB

REV	
1A	FIRST RELEASED: E200610-3793 (PCB: DA0ZD1MB6A0)
2A	Page10 : Depop R153 & pop L23 for system can not boot Page14 : U36 package didn't math footprint, change P/N. Page26 : Remove R275, install R276; remove R4, install R16; Change R245, R247 power source from +1.5V_S5/+1.5V to +3V_S5/+3V , Follow customer request modem change support to +3VSUS. Page22 : MMB(CN8) PIN define error. Page22 : TV card change support to +1.5V. Page18 : Install R5, depop R7,: Follow customer request use EC to control backlight ON/OFF function. Page14 : GPIO10: Reserve PU, 10K +> It is GPO and OD; GPIO14: Reserve PD, 10K => It is GPI as AC present and active high; Page6 : TV_DCONSEL[0:1], UMA =>NC, External VGA tie to GND. Page31 : 2nd FAN change design Page23 : New card power SW (location: U33) change same as ZO1 Page31 : add 2 capacity 0.1uF(C634,C636) in DIGVOL_UP / DIGVOL_DN pins Page26 : Co-layout ALC268 and 888S Page28 : SD card can not be detected , U32(ES2) sample will fix this issue. Page28 : MMC card can not be detected , U32(ES2) sample will fix this issue. Page14 : The CLPWROK pin of ICH8 connect with HWPG signal Page22 : change CN7 pin definition for T/P no function. Page24 : change CN8 pin definition MMB no function. Page14 : The signal of KBSMI#_ICH add diode , and it PU to +3V_S5 The signal of LID591#_ICH add diode , and it PU to +3V_S5 for ICH8 electric leakage issue. Page26 : Change subwoofer from 4pin to 5pin connector.
2B	Page 2 : Add C645 for EMI solution Page31 : Follow customer request 2nd FAN is controlled by EC Page19 : Floating CN13.16 & CN13.17 ,CN14.15 & CN14.16 for ESD test Page07 : DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK and DPLL_REF_SSCLK#. To GND Page36 : Add PI filter to reduce the power ripple of +1.8V. Page16 : Modify SMbus address A2 , The signal of B_SA1 need to PU and B_SA0 need to PD Page26 : add 2 capacity 1uF(C639,C640) for subwoofer Page30 : add capacity 2.2uF(C638)
2C	Page17 : Adding (Q52 & R541 & Q53) extra circuitry to prevent power leakage from system into MXM Page21 : Change power of CIR from +3VPCU and +5VPCU. Page31 : AEC pin24 is multi function pin, when EC power up, pin17 will change to JTAG/TCK function not GPIO. So,need to change from pin24 (GPIO47) to pin27 (GPIO52). Page22: Power/B connector add two LED control signal and change to 16 pin from 14-pin for meet ACER LED spec . Page22: Q35 change to AO3413 form DTA114 for increase LED driving power. Page23: BL_ON pull up resistor from 10kohm to 100Khom(R194).+3V pull up will cause power on leakage on BL_ON signal due to our VGA have 10kohm pull low.
2D	Page19 : Connect CRT of CN13.16 & 17 to GND for ESD Page17 : Add capacity 330uF(C647) & Remove R541 Page22 & 25: Combine USB/B (CN17) and TV/B(CN30) connector, Connector change to 16 pin. and +5_S5 from 1pin to 2pin. Page25 : Connect HOLE 28 & 29 to GND for ESD Page32~37 : Update power circuit Page37 : Remove 1.2V circuit Page26 : Add 1000pF and 10pF total 4 PCS Location: C648 , C649, C650, C652 (between +5V_ADOand AGND). Page22 : CN8.8 remove +5V & R540 & connect to +3V (K) Page27 : Modify and ADD. AGND bridge (R337,R284,C459 and C472 = 0 Ohm). Page34 : Remove PR161, PR163, PC156, PC159 Page22 : Add D45~D51 for ESD Page28 : Change CN36.37 & 38 ,CN37.37 & 38 ,CN38.42 & 43 from ADOGND and GND.
3A	Page32 : PD9 Change footprint Page25 : Add EMI Spring Page27 : Add GND & AGND bridge (R546,R540,R408) Page22 : Modify pin define (TV/B(CN30) connector)
F	Page23 & 17 : HDMI circuits modify: Add level-shifter for MXM_HDMI_DDCCLK and MXM_HDMI_DDCDATA.(Location: Q54 ,Q55 , R75, R63, R297, R410 & R602) .

MODEL	ZY3 FROM	ZY3 To
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	2B	3A

PROJECT : ZD1
Quanta Computer Inc.

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DOC NO.					
PROJECT MODEL :	ZD1	APPROVED BY:		DATE:	2007/ 2/15
PART NUMBER:		DRAWING BY:		REVISON:	3A