Discrete/UMA /Muxless Schematics Document

AMD LIANO CPU FS1

AMD GPU Manhattan(Park/Madison M2) and Vancouver(Seymour/Whistler M2)

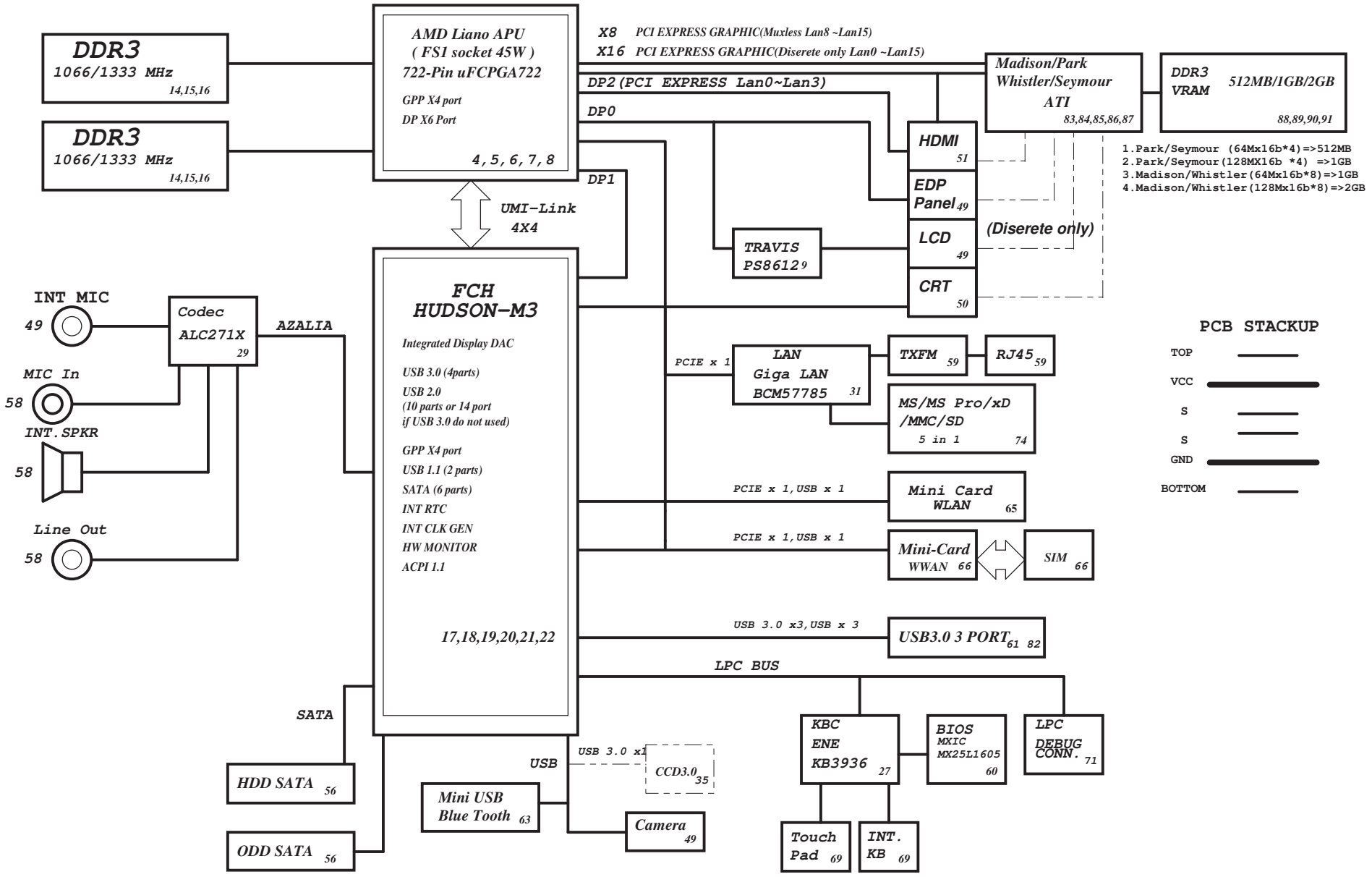
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A4	Document Number: JE50_SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 1 of 102	

JE50-SB Block Diagram

JE50-SB Project code:91.4M701.001



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC
RT8239 — 41

INPUTS	OUTPUTS
DCBATOUT	5V_S5(5.5A) 3D3V_S5(5A)

SYSTEM DC/DC
RT8207 — 44

5V_S5	1D5V_S3(15A)

RT8207 — 44

5V_S5	0D75_S0(1.2A)

SYSTEM DC/DC
RT8238 — 46

INPUTS	OUTPUTS
5V_S5	1D1V_S5(1.4A)

RT8238 — 45

5V_S5	1D2V_S0(5.2A)

RT9025 — 93

3D3V_S5	1D8V_VGA_S0
1D5V_S3	1V_VGA_S0

RT9025 — 48

3D3V_S0	2D5V_S0 (200mA)

RT8208 — 92

5V_S5	VGA_CORE

CHARGER
BQ24745 — 40

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC
ISL6267 — 42,43

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.55V 18A VDDNB 0~1.55V 4A

<Variant Name>

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Title: Block Diagram

Size	Document Number	Rev
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Strapping

REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

USB Table

USB	
Pair	Device
0	USB 2.0 EXT2(For SW Debug)
1	WLAN
2	NC
3	WWAN
4	BT
5	3G SIM Card
6	NC
7	CCD
8	NC
9	Card Reader
10	USB 3.0 port 1
11	USB 2.0 EXT2
12	USB 2.0 EXT3
13	NC

PCIE Routing

	APU
LANE0	LAN
LANE1	WWAN
LANE2	LAN
LANE3	

	FCH
LANE0	
LANE1	
LANE2	
LANE3	

<Variant Name>

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Title: Table of Content

Size: A3 | Document Number: JE50_SB | Rev: SB

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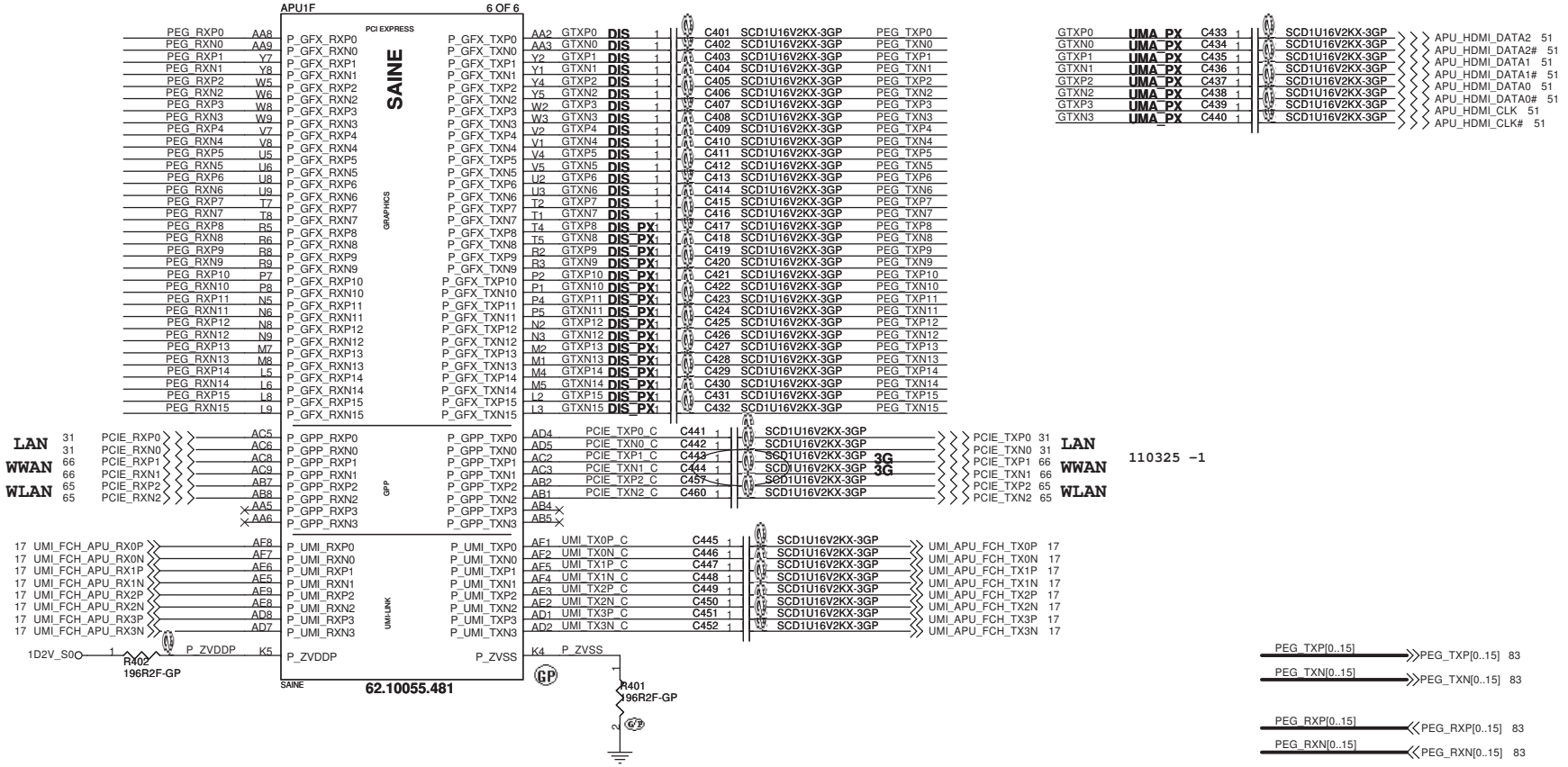

<Variant Name>

緯創資通 Wistron Corporation
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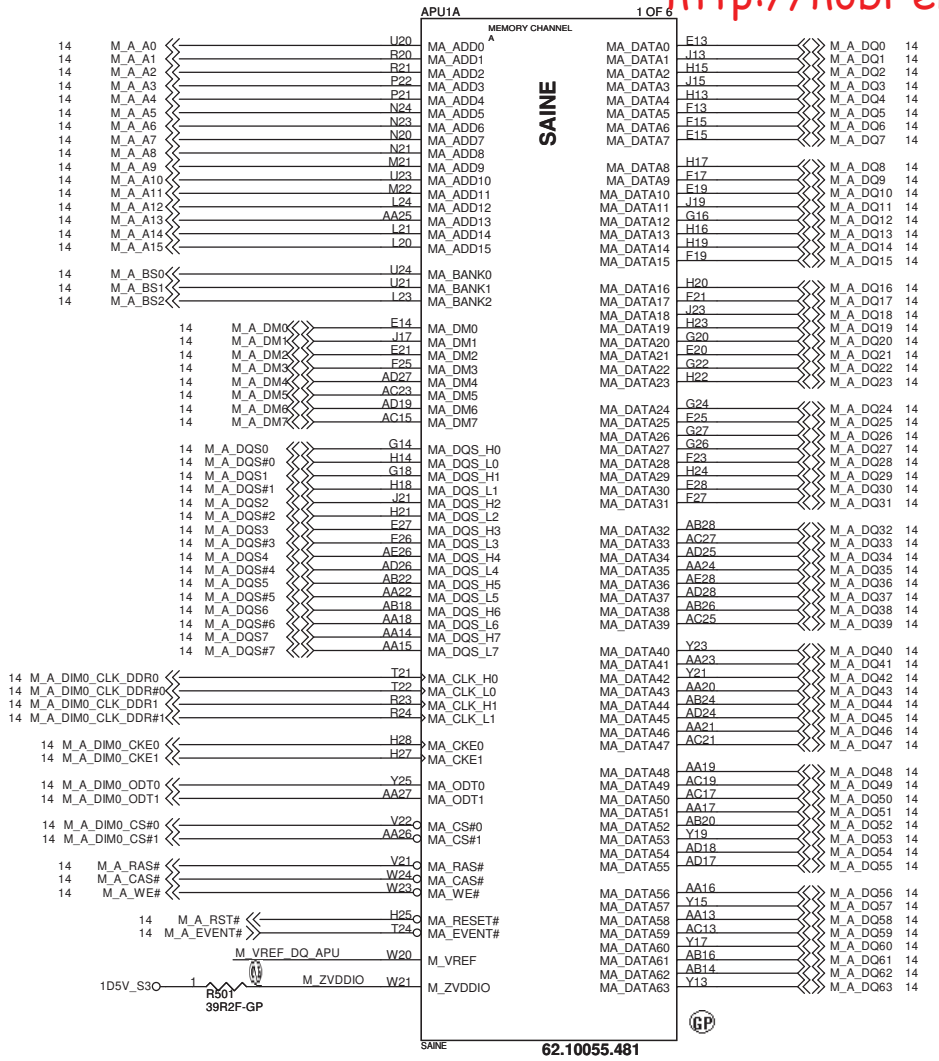
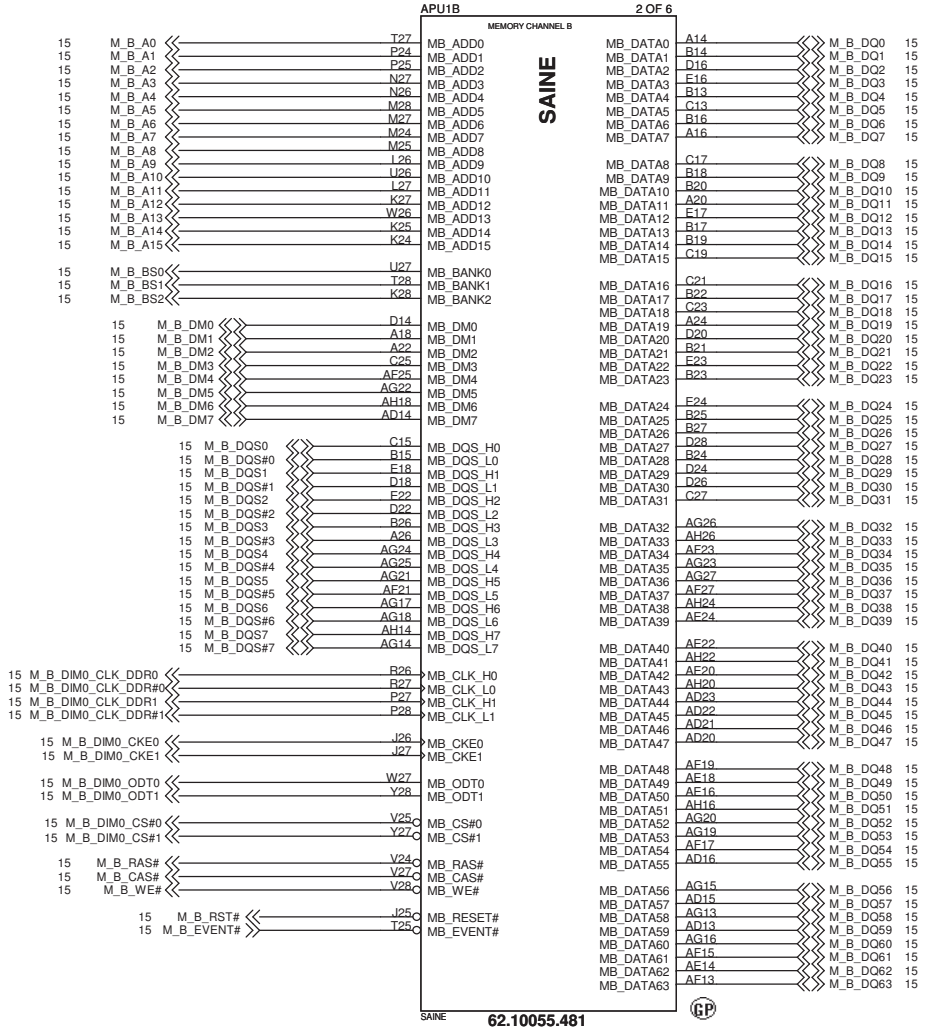
Title: APU_PCIE(1/5)

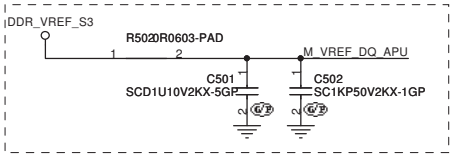
Size: A3 | Document Number: JE50_SB | Rev: SB

Date: Friday, April 01, 2011 | Sheet 4 of 102

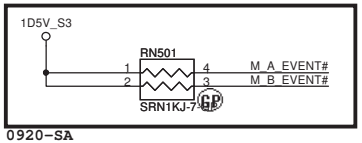




APU_VREF_DQ



LAYOUT: place them close to APU



0920-SA

<Variant Name>

緯創資通 Wistron Corporation
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Title	APU_DDR(2/5)	
Size A3	Document Number JE50_SB	Rev SB
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SVC	SVD	Boot Voltage (VCC/GND)	Boot Voltage (open)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.1
1	1	0.8	0.9

EDP

TRAVIS LVDS Panel

VGA output from FCH

100MHz

100MHz

110218 SB change to short pad

110328 -1

[AMD HDMI desing guidance]

Strap define PU :Enable HDMI
PD:Disable HDMI

[AMD FAE Frank]:
this is electrical key
do not allow power to turn on if this pin is still "L"
FS1 package is open pin
in the futur,FS1r2 will have this pin tied to VSS
if the wrong processor is plugged the socket
This is more of a problem on desktop platforms
(changing CPUs)

CPU exceeds to 125℃

S3 Power

Variant Name	
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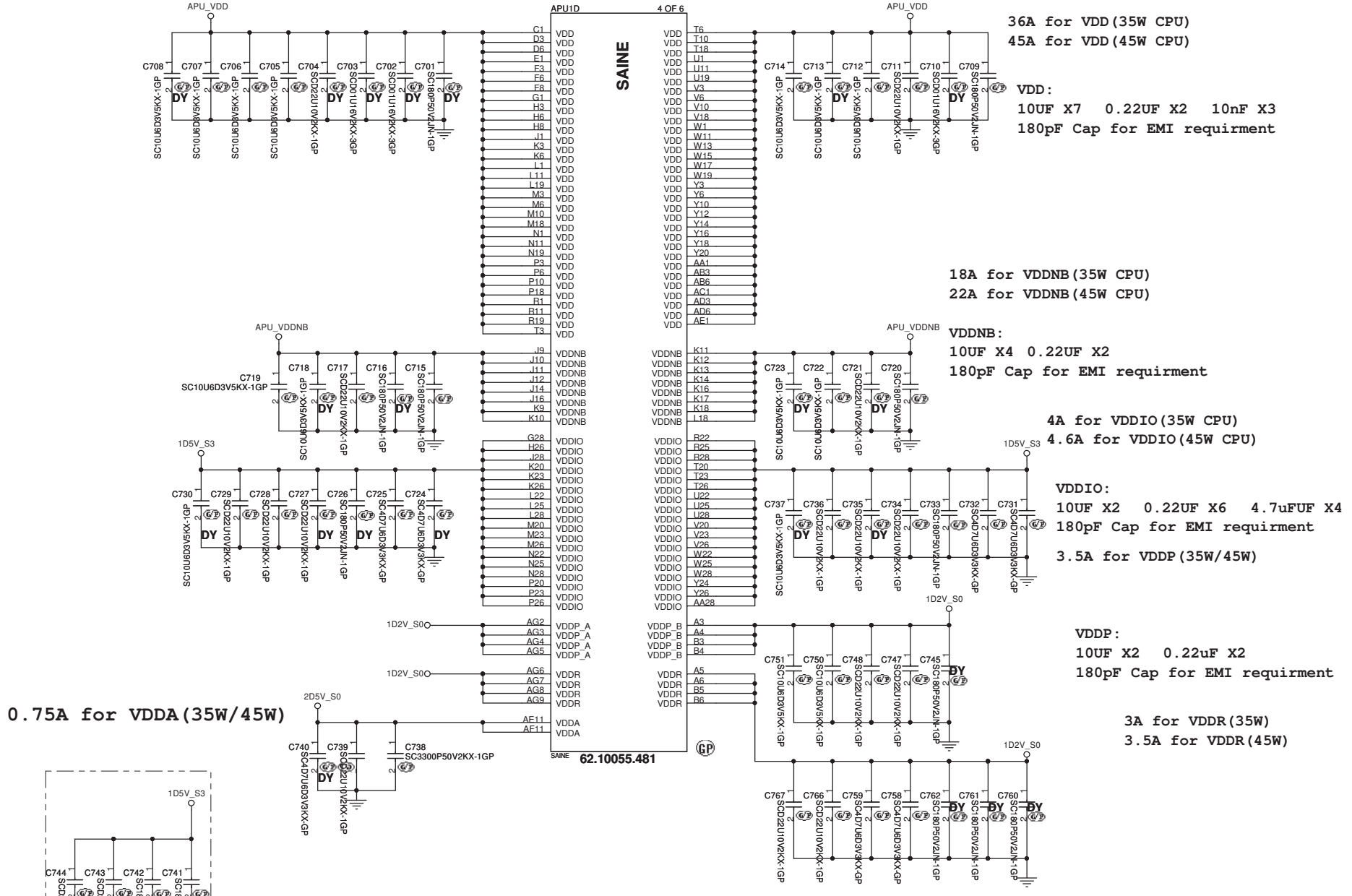
Title	APU_Control&Debug(3/5)
Size: Custom	Document Number: JE50_SB
Rev	SB
Date: Friday, April 01, 2011	Sheet 6 of 102



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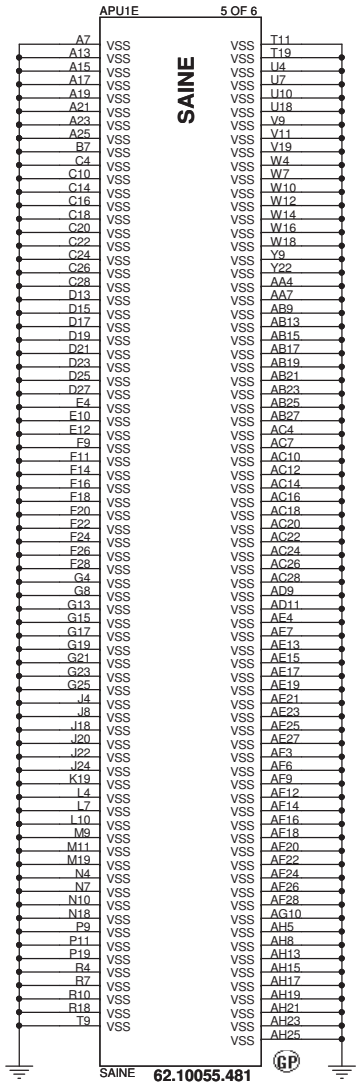
Size: A3	Document Number: JE50_SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 7 of 102	



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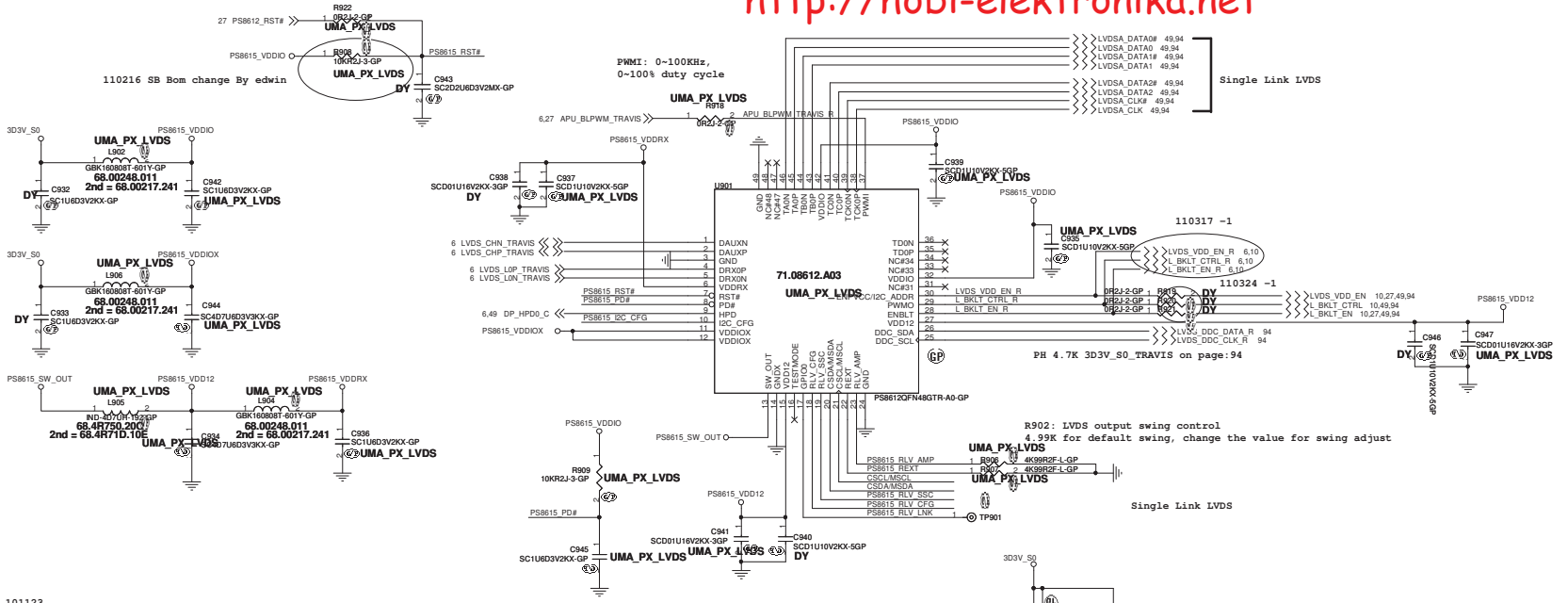
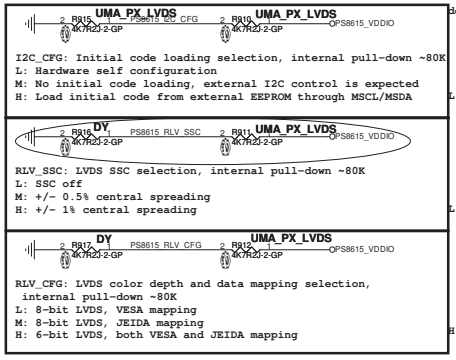
Size A3	Document Number JE50_SB
Rev	SB
Date: Friday, April 01, 2011	Sheet 8 of 102





default setting

L: Hardware self configuration

110221 SB Bom change By EMI

L: SSC off

H: 6-bit LVDS, both VESA and JEIDA mapping

<Variant Name>

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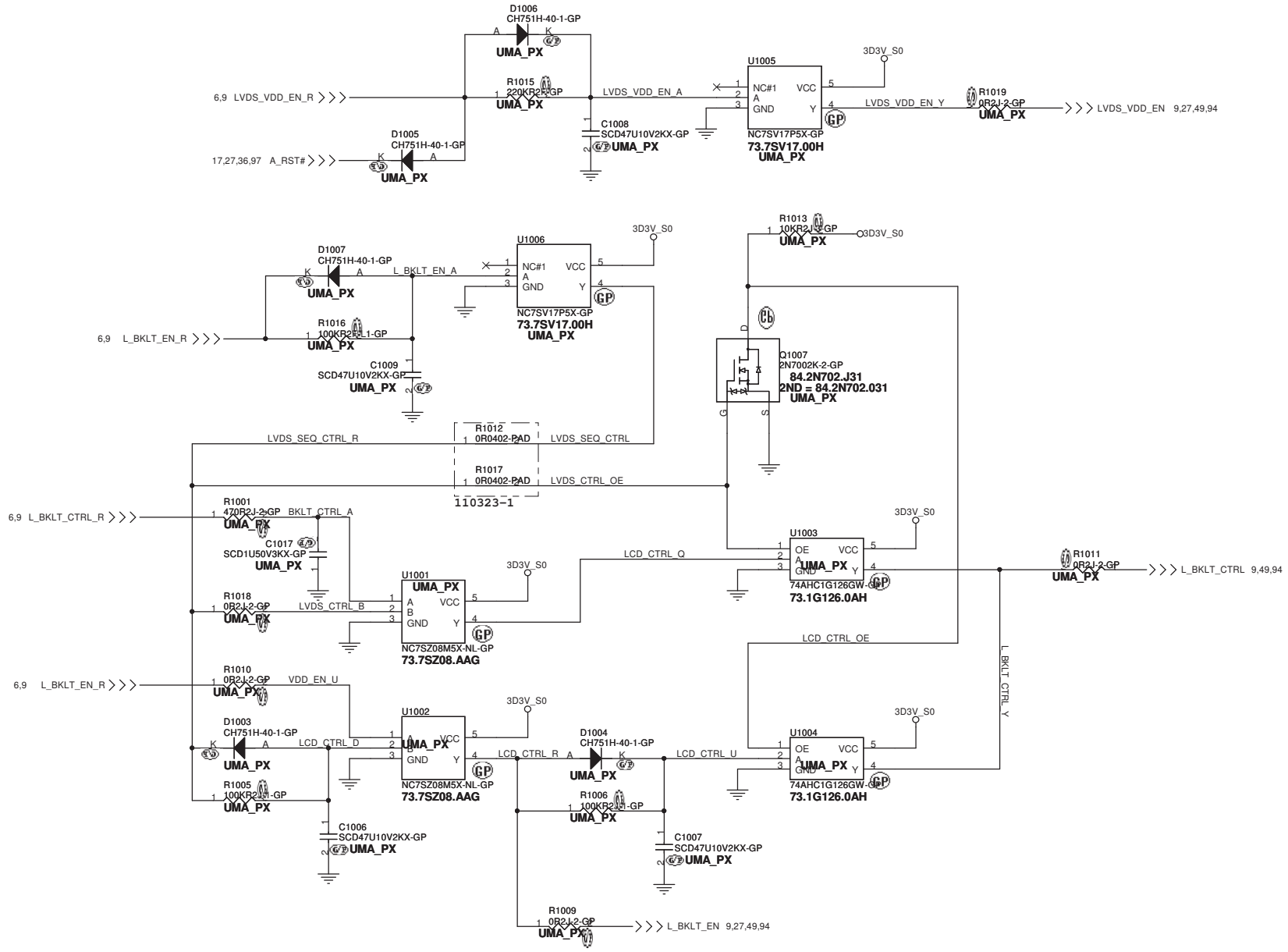
Title: TRAVIS		
Size: A2	Document Number: JE50_SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 9 of 102	



<Variant Name>

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Title: ***Reserved***

Size	Document Number	Rev
A3	JE50_SB	SB

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<Variant Name>

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Title
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Size	Document Number	Rev
A4	JE50_SB	SB

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<Variant Name>

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Size	Document Number	Rev
A4	JE50_SB	SB

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<Variant Name>

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Title

Reserved

Size	Document Number	Rev
A4	JE50_SB	SB

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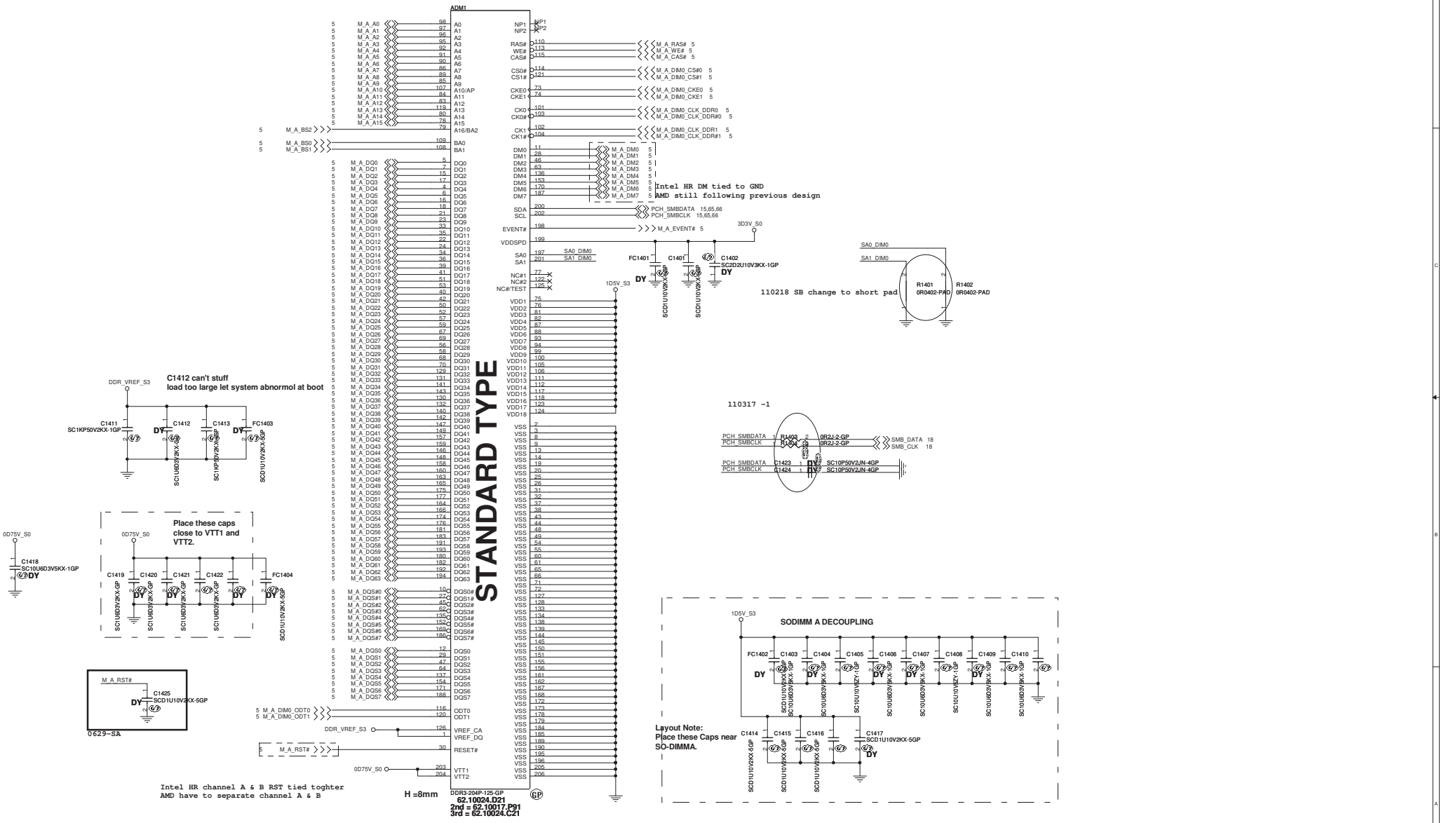

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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR3-SODIMM1		
Size: A2	Document Number: JE50_SB	Rev: SB
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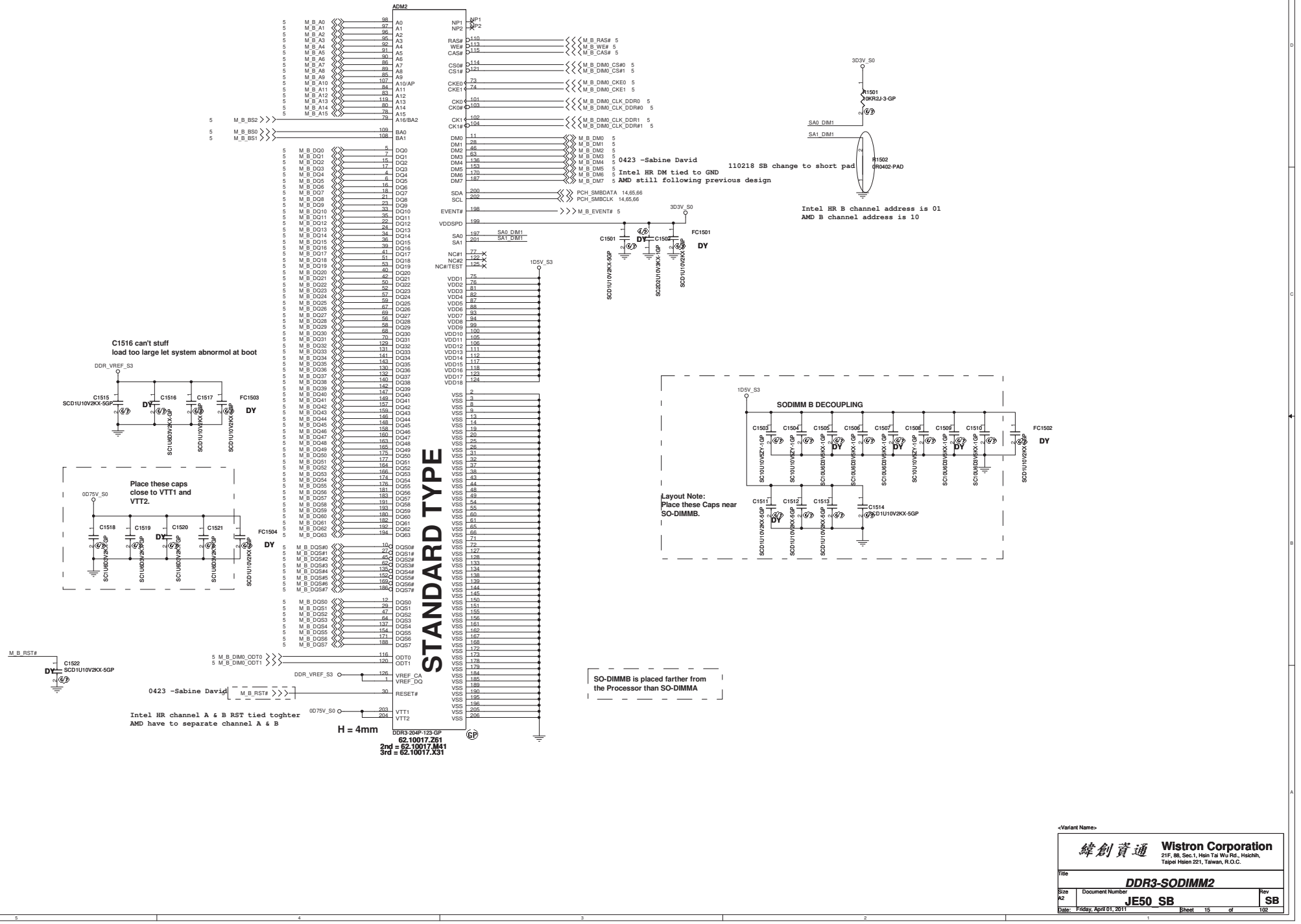

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: DDR3-SODIMM2

Size	Document Number	Rev
A2	JE50_SB	SB

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<Variant Name>

緯創資通 Wistron Corporation
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Title

Reserved

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110307 SB change bom by siv

FCH1E

Part 5 of 5

GPP CLK port	Device	CLKREQ#
0	New Card	0
1	WLAN	1
2	WWAN	2
3	LAN	3
4	X	
5	X	
6	X	
7	X	
8	X	

CL = 12pF
Freq tolertance :+/- 30ppm

110317 -1

EXT clock_Gen

For TRAVIS

1005-SA

NEW

110317 -1

Debug Strap

Muxless support
PE_GPIO0 ->VGA_RESET
PE_GPIO1 ->VGA_PowerEnable

PM_CLKRUN#

checklist:No PU Res
Integrated Resistor PU10K

110218_SB change to short pad

LDT_STP# connection is just for chipset automation purpose. It is an automatic test for AMD validation team only

folloiwng Intel HR netname

-Sabin David
for SW Jin define

110301 SB bom change

CL = 7pF
Freq tolertance :+/- 20 ppm

71.HUDM2.M03

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HUDSON-M2(1/6)

Size: Custom | Document Number: JE50_SB | Rev: SB

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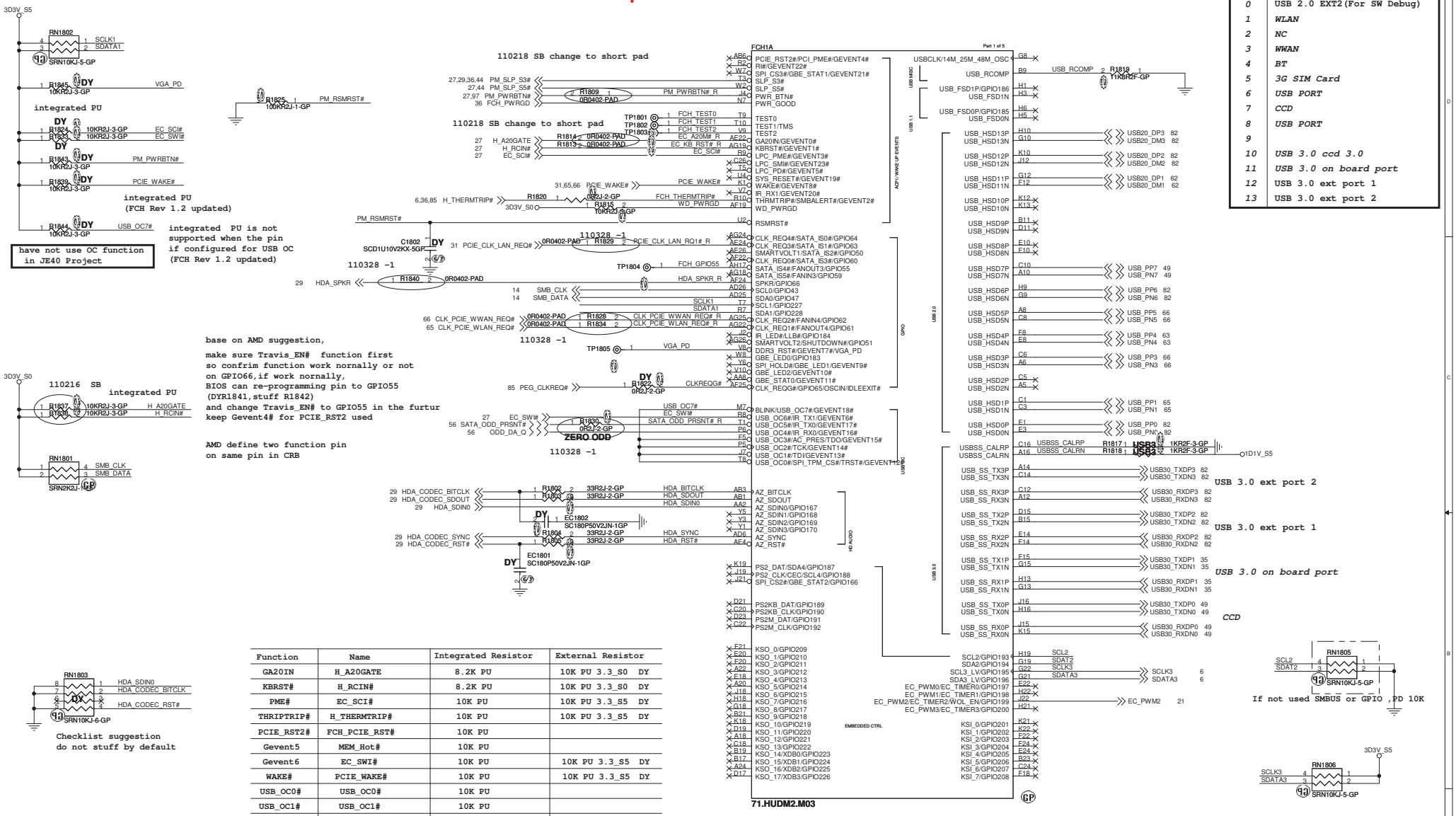

USB

Pair	Device
0	USB 2.0 EXT2(For SW Debug)
1	WLAN
2	NC
3	WWAN
4	BT
5	3G SIM Card
6	USB PORT
7	CCD
8	USB PORT
9	
10	USB 3.0 ccd 3.0
11	USB 3.0 on board port
12	USB 3.0 ext port 1
13	USB 3.0 ext port 2

Function	Name	Integrated Resistor	External Resistor
GA20IN	H_A20GATE	8.2K PU	10K PU 3.3_S0 DY
KBRST#	H_RCIN#	8.2K PU	10K PU 3.3_S0 DY
PME#	EC_SCI#	10K PU	10K PU 3.3_S5 DY
THRIPTRIP#	H_THERMTRIP#	10K PU	10K PU 3.3_S5 DY
PCIE_RST2#	FCH_PCIE_RST#	10K PU	
Gevent5	MEM_Hot#	10K PU	
Gevent6	EC_SWI#	10K PU	10K PU 3.3_S5 DY
WAKE#	PCIE_WAKE#	10K PU	10K PU 3.3_S5 DY
USB_OC0#	USB_OC0#	10K PU	
USB_OC1#	USB_OC1#	10K PU	
USB_OC2#	USB_OC2#	10K PU	
Gevent15#	SATA_ODD_PRSNT#	10K PU	
Gevent16#	ODD_DA	10K PU	
USB_OC5#	USB_OC5#	10K PU	
Gevent17#	EC_SWI#	10K PU	10K PU 3.3_S0 DY
USB_OC7#	USB_OC7#	10K PU	
LPC_SMI#	EC_SMI#	8.2K PU	10K PU 3.3_S5 DY
GPIO35	SATA_ODD_DA#	8.2K PU	
SERIRQ	INT_SERIRQ	8.2K PU	10K PU 3.3_S0 DY
CLK_REQ0	CLK_PCIE_NEW_REQ#	8.2K PU	
CLK_REQ1	CLK_PCIE_WLAN_REQ#	8.2K PU	
CLK_REQ2	CLK_PCIE_WWAN_REQ#	8.2K PU	
CLK_REQ3	PCIE_CLK_LAN_RQ1#	8.2K PU	
CLK_REQG	PEG_CLKREQ#	8.2K PU	

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<Variant Name>

Title: HUDSON-M2(2/6)

Size: Custom | Document Number: JE50 SB | Rev: SB

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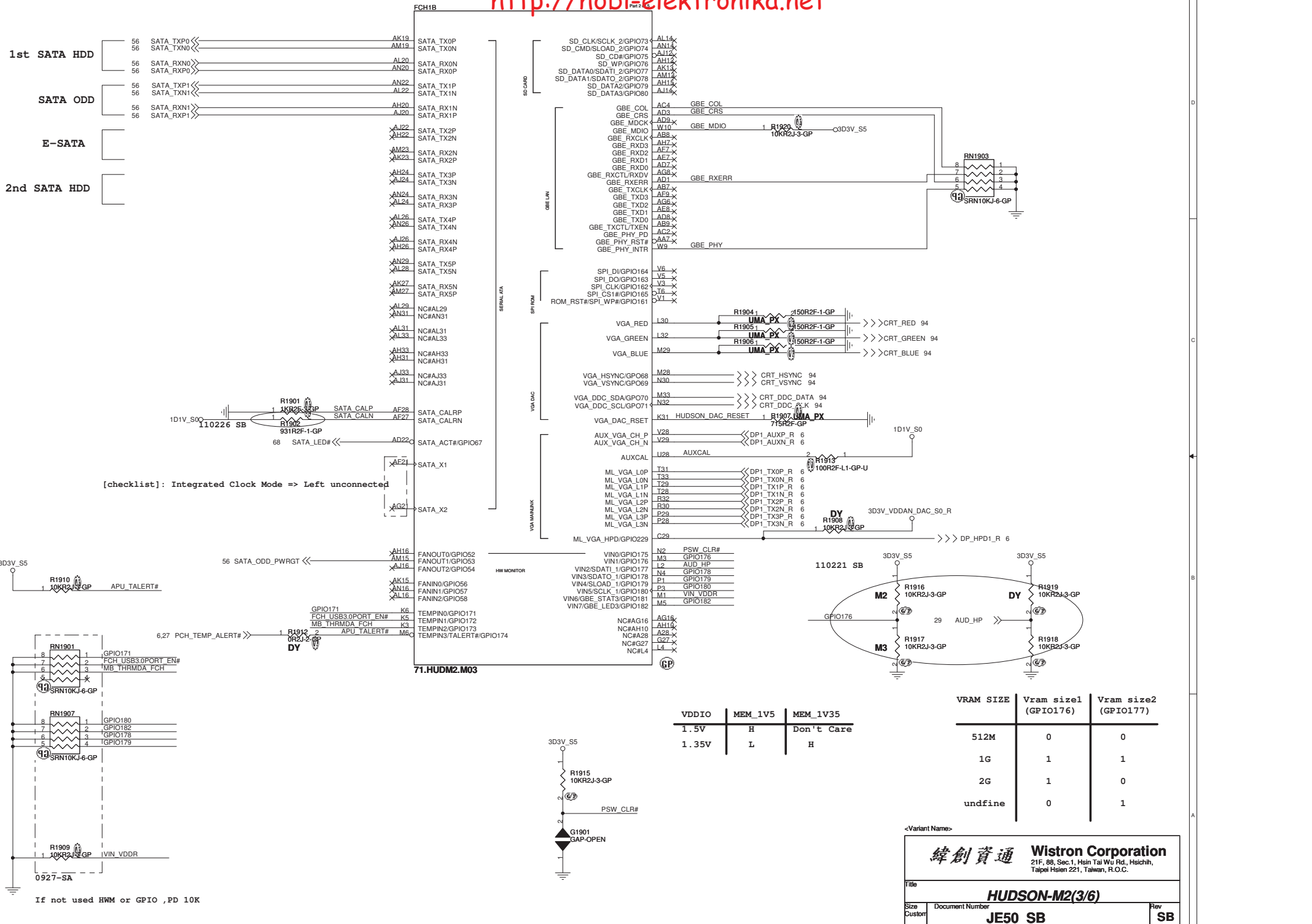

VDDIO	MEM_1V5	MEM_1V35
1.5V	H	Don't Care
1.35V	L	H

VRAM SIZE	Vram size1 (GPIO176)	Vram size2 (GPIO177)
512M	0	0
1G	1	1
2G	1	0
undfine	0	1

<Variant Name>

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Title: HUDSON-M2(3/6)

Size: Custom | Document Number: JE50_SB | Rev: SB

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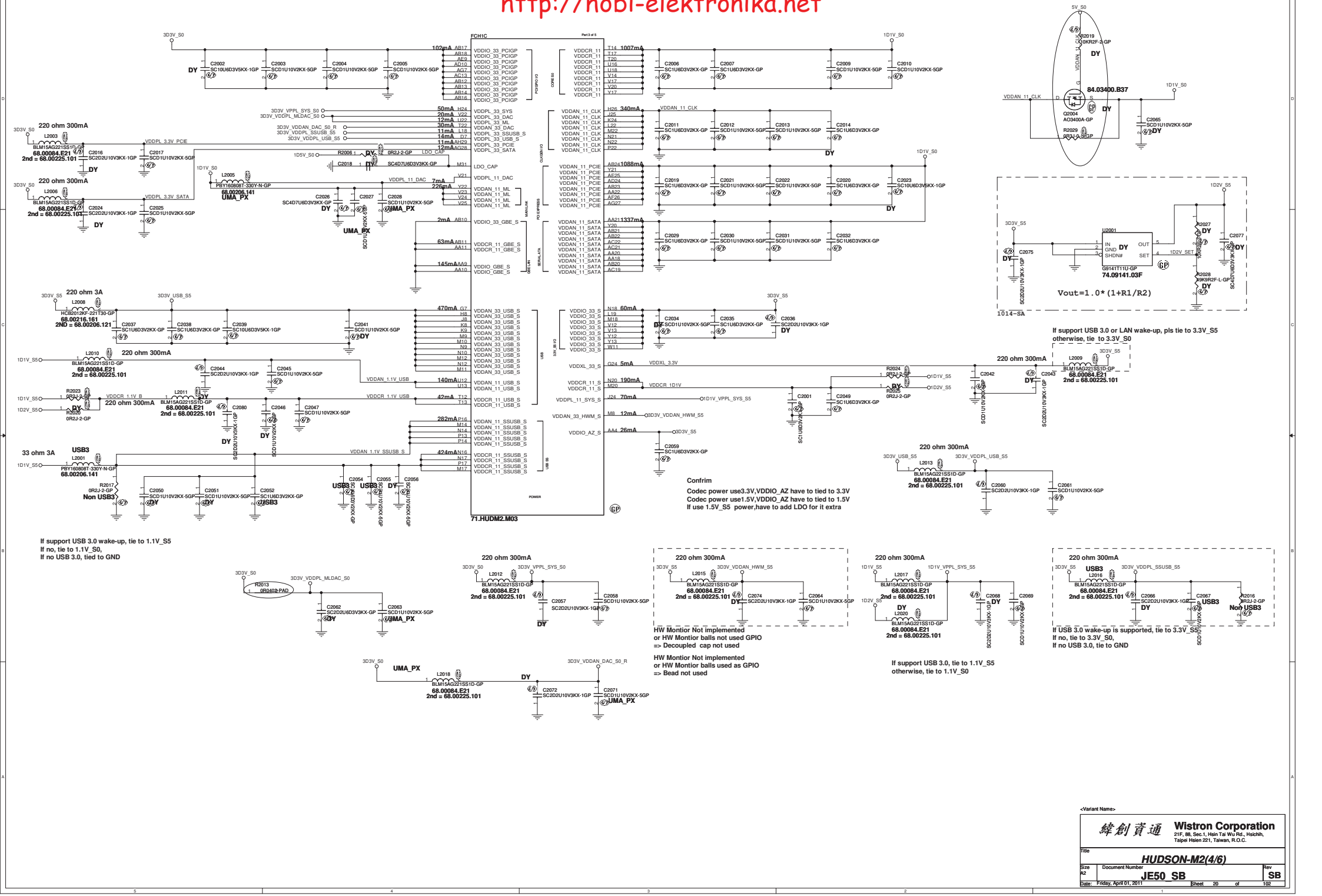

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Title: HUDSON-M2(4/6)

Size	Document Number	Rev
A2	JE50_SB	SB

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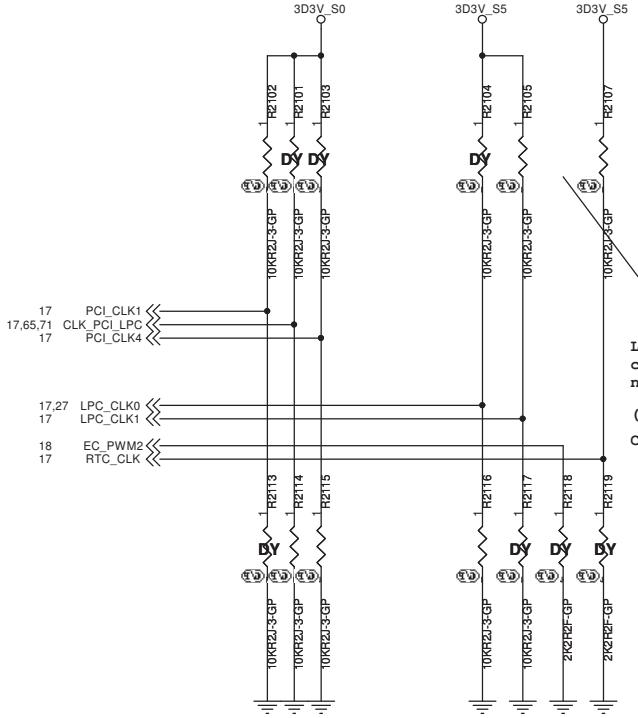
SSID = S.B

REQUIRED STRAPS

CRB:PU 3.3V_AUX_S5

checklist:PU 3.3V_S5

no support S5 PLUS funciton,PU 3.3V_S5



LPC ROM implemented
checklistsuggestion:
no PU or PD required

(integrated PU 10K)

CRB: do not stuff PU Res

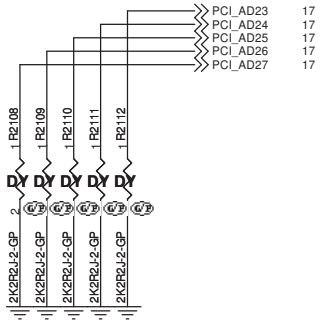
USE this pin to determine INT/EXT CLK

REQUIRED SYSTEM STRAPS

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

Ball Name	Strap Function	Description
[redacted]	ROM Type	SPI ROM: 2.2-KΩ 5% pull-down LPC ROM: Pull-up to 3.3V_S5. External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V_S5.

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI_AD[27:23]

<Variant Name>

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Title: HUDSON-M2(5/6)

Size: A3 | Document Number: JE50 SB | Rev: SB

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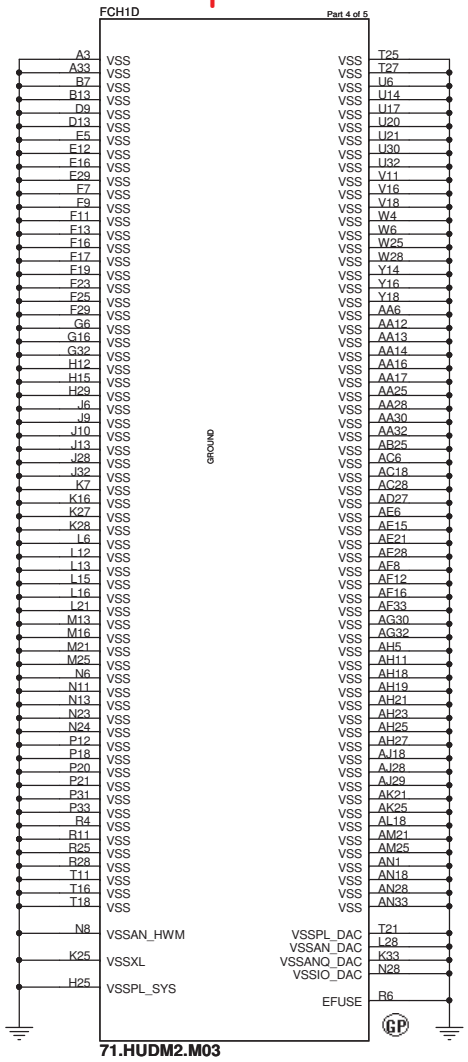

<Variant Name>

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Title: ***HUDSON-M2(6/6)***

Size	Document Number	Rev
A3	**JE50_SB**	**SB**

Date: Friday, April 01, 2011 Sheet 22 of 102

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<Variant Name>

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Title: *Reserved*

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 23 of 102

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<Variant Name>

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Title

Reserved

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 24 of 102

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **Reserved**

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 25 of 102

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<Variant Name>

緯創資通 Wistron Corporation
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Title: *Reserved*

Size	Document Number	Rev
A4	JE50_SB	SB

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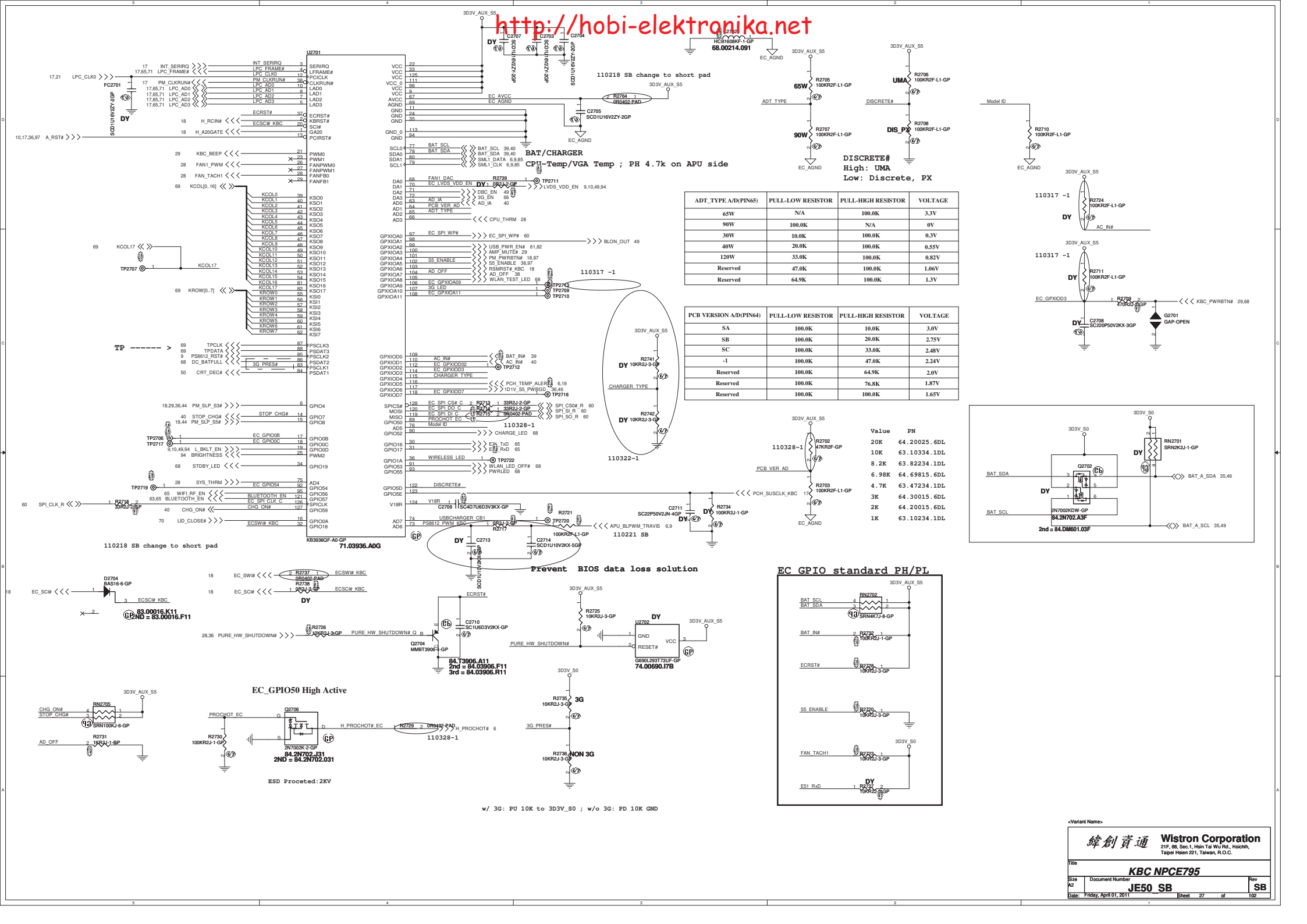


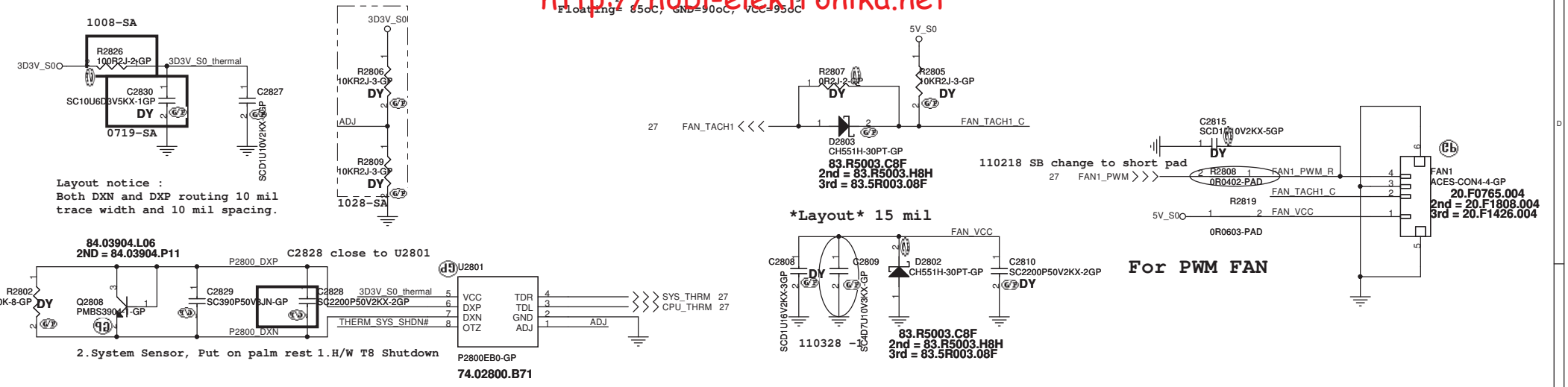
ADT_TYPE A/D(PIN65)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

PCB VERSION A/D(PIN64)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

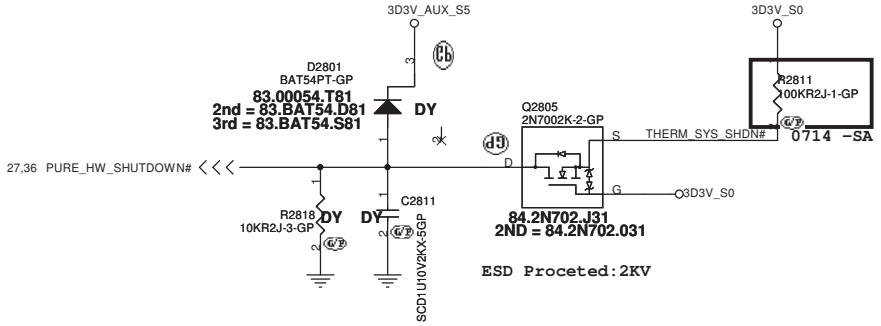
Value	PN
20K	64.20025.6DL
10K	63.10334.1DL
8.2K	63.82234.1DL
6.98K	64.69815.6DL
4.7K	63.47234.1DL
3K	64.30015.6DL
2K	64.20015.6DL
1K	63.10234.1DL

<Variant Name>

Size	Document Number	Rev
A2	JE50_SB	SB
Date: Friday, April 01, 2011	Sheet 27 of 102	



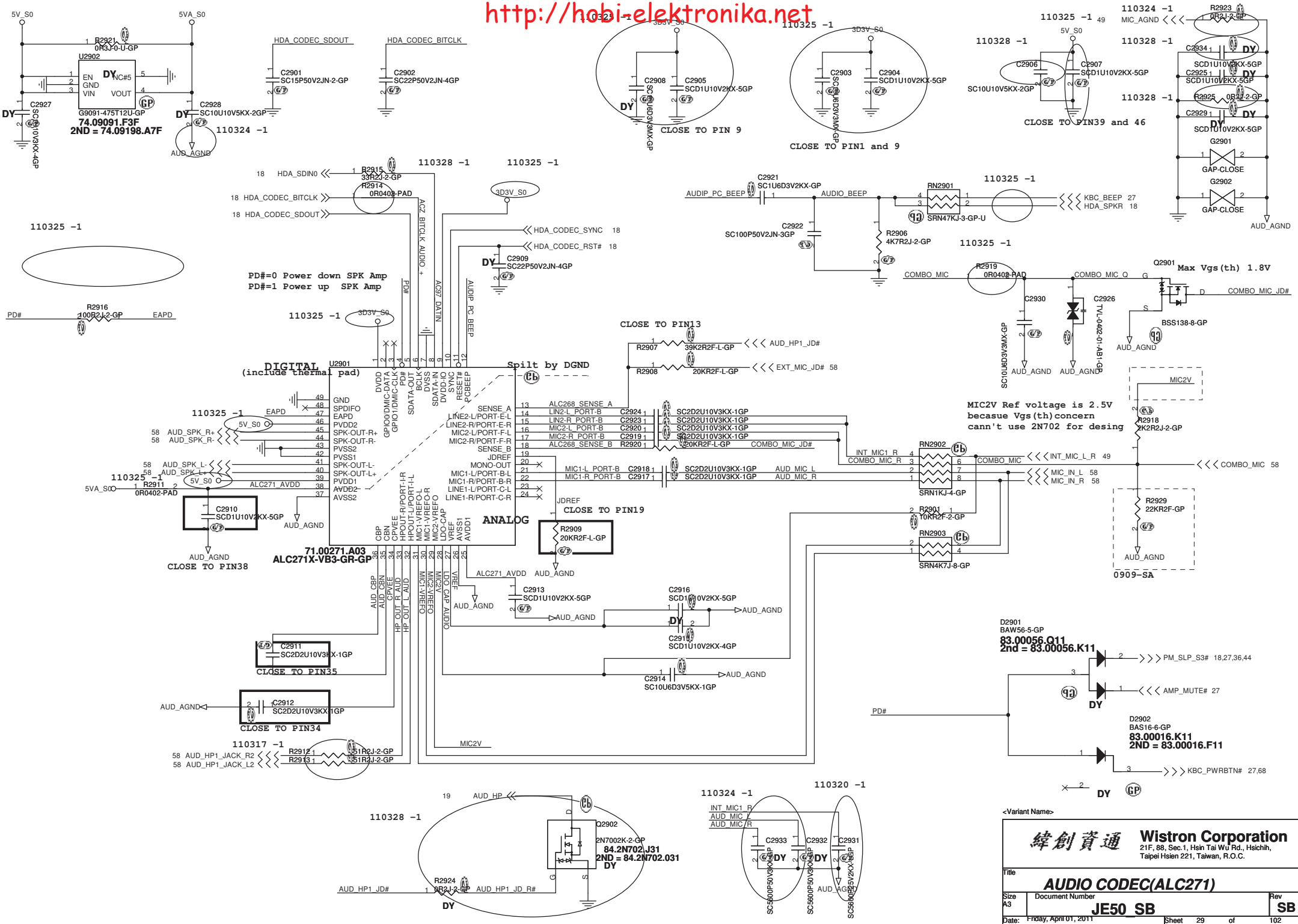
VGA Thermal sensor P2800



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Thermal P2800*	
Size A3	Document Number JE50_SB	Rev SB
Date: Friday, April 01, 2011	Sheet 28 of 102	



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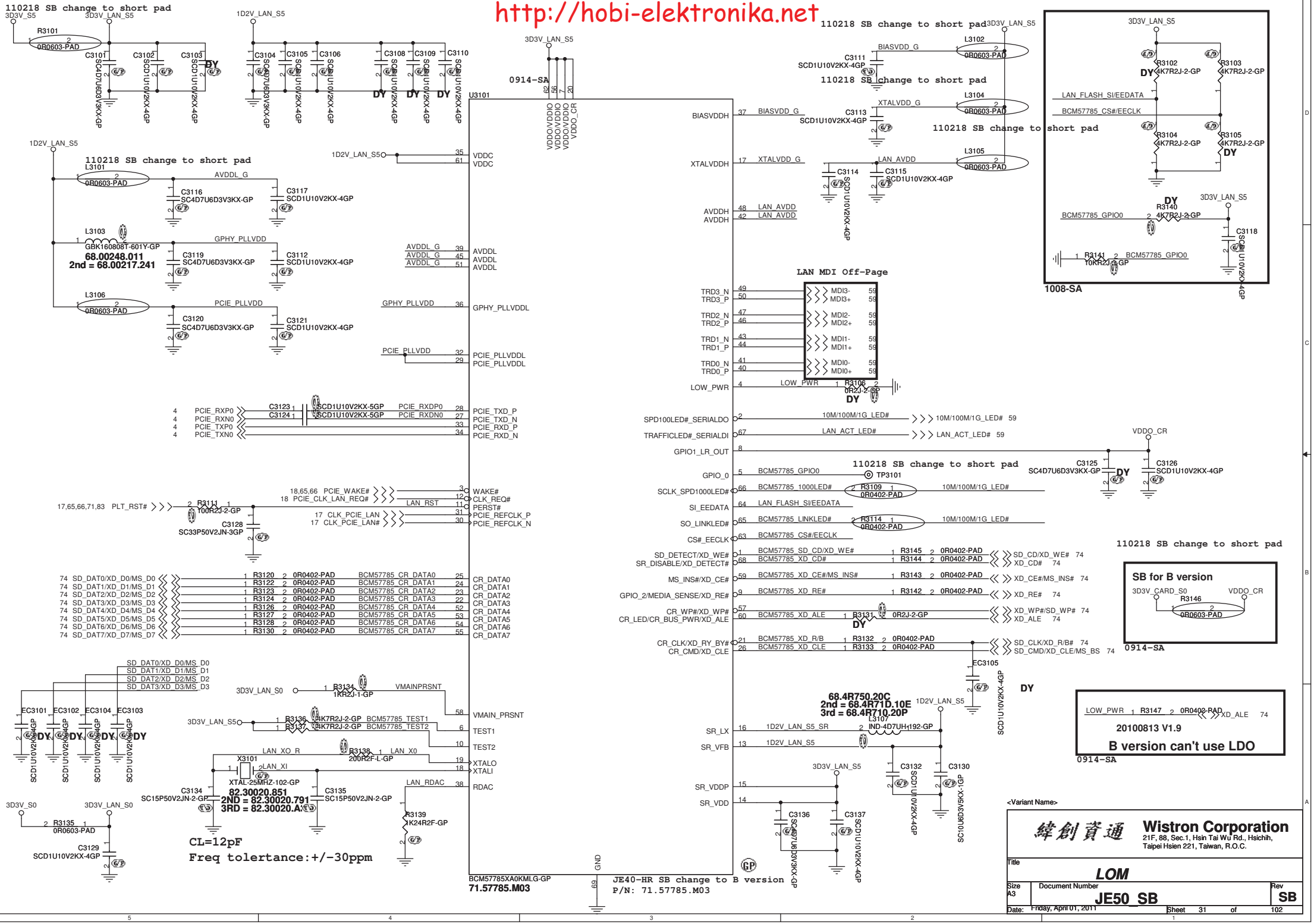
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMP

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 30 of 102



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LOM

Size: A3 | Document Number: JE50_SB | Rev: SB

Date: Friday, April 01, 2011 | Sheet 31 of 102

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RTS5138

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 32 of 102

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 33 of 102

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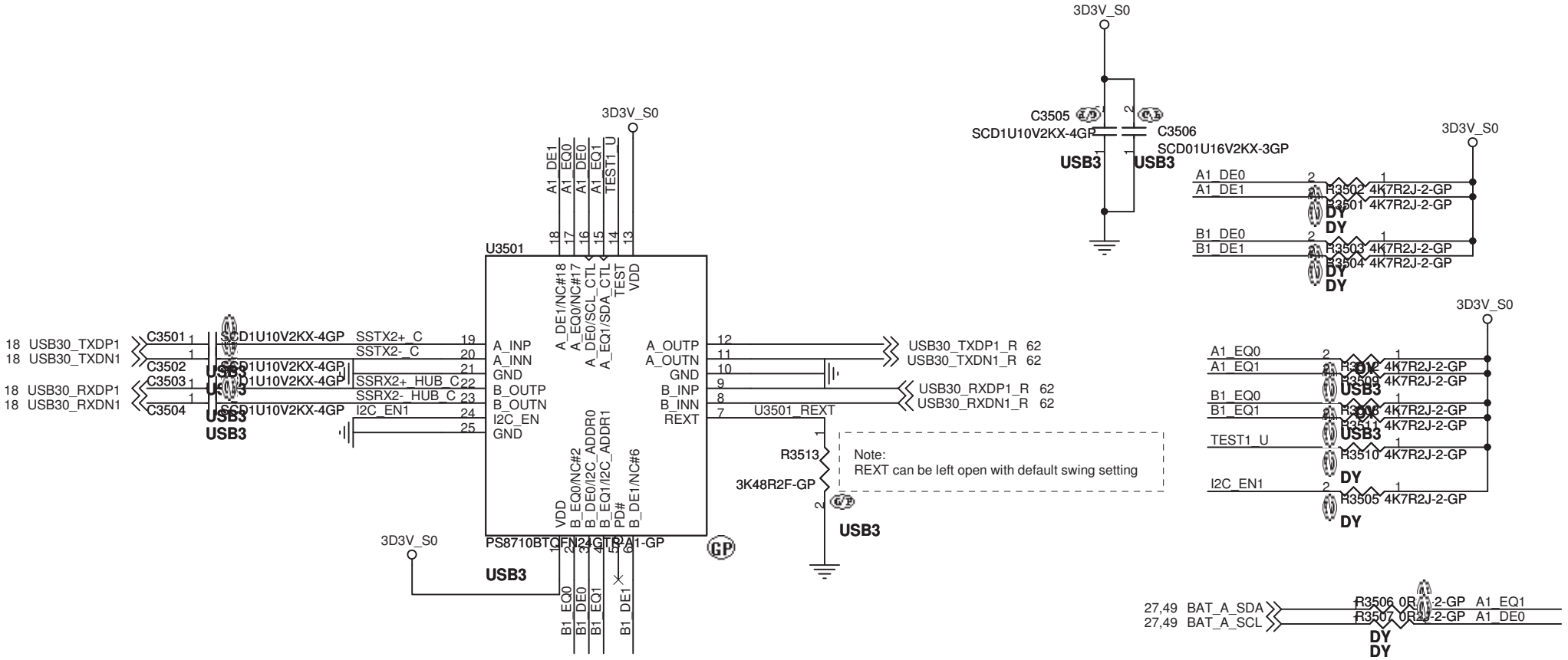
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 34 of 102



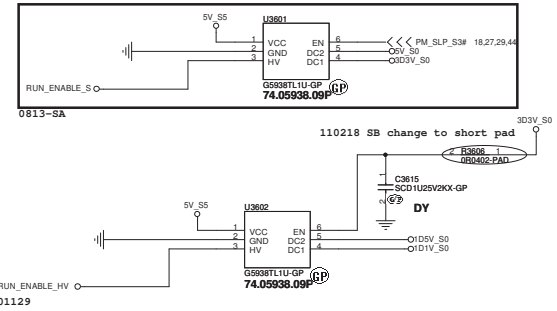
<Variant Name>

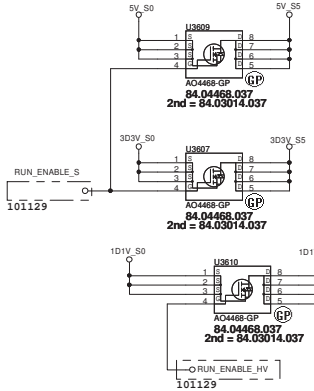
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

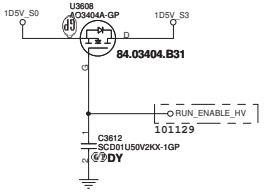
Title: ***Reserved***

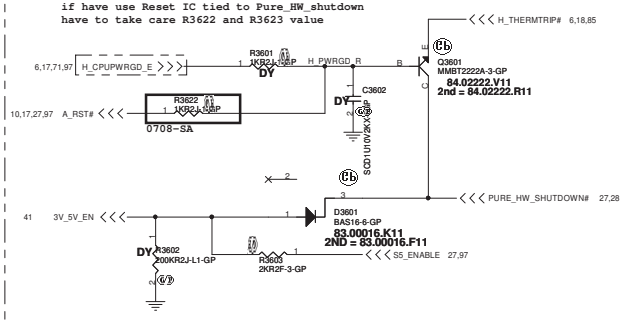
Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 35 of 102

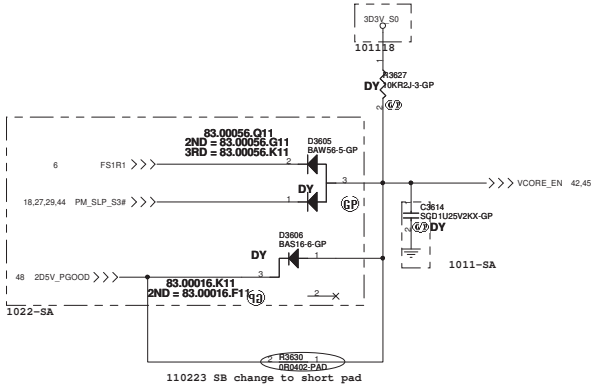


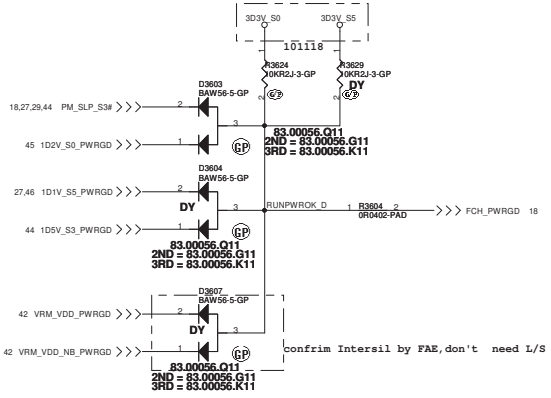






Power Sequence





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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*Power On Logic*	
Size: Custom	Document Number: JE50_SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 36 of 102	

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

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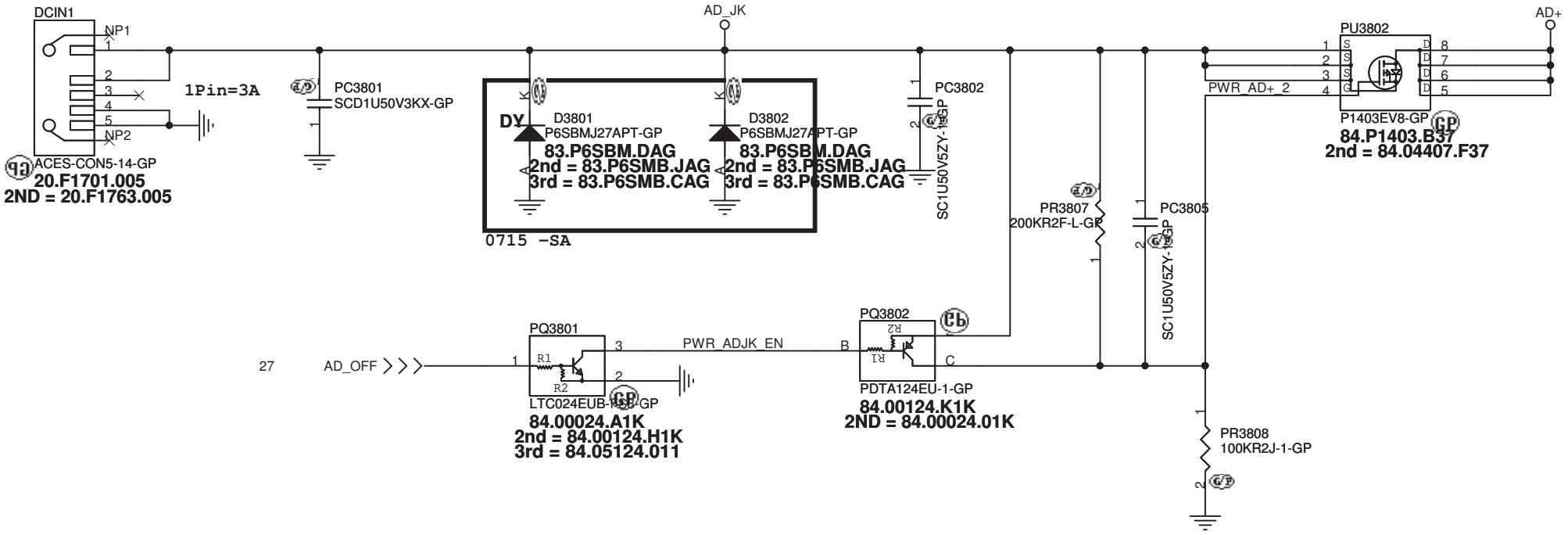
Adaptor in to generate DCBATOUT



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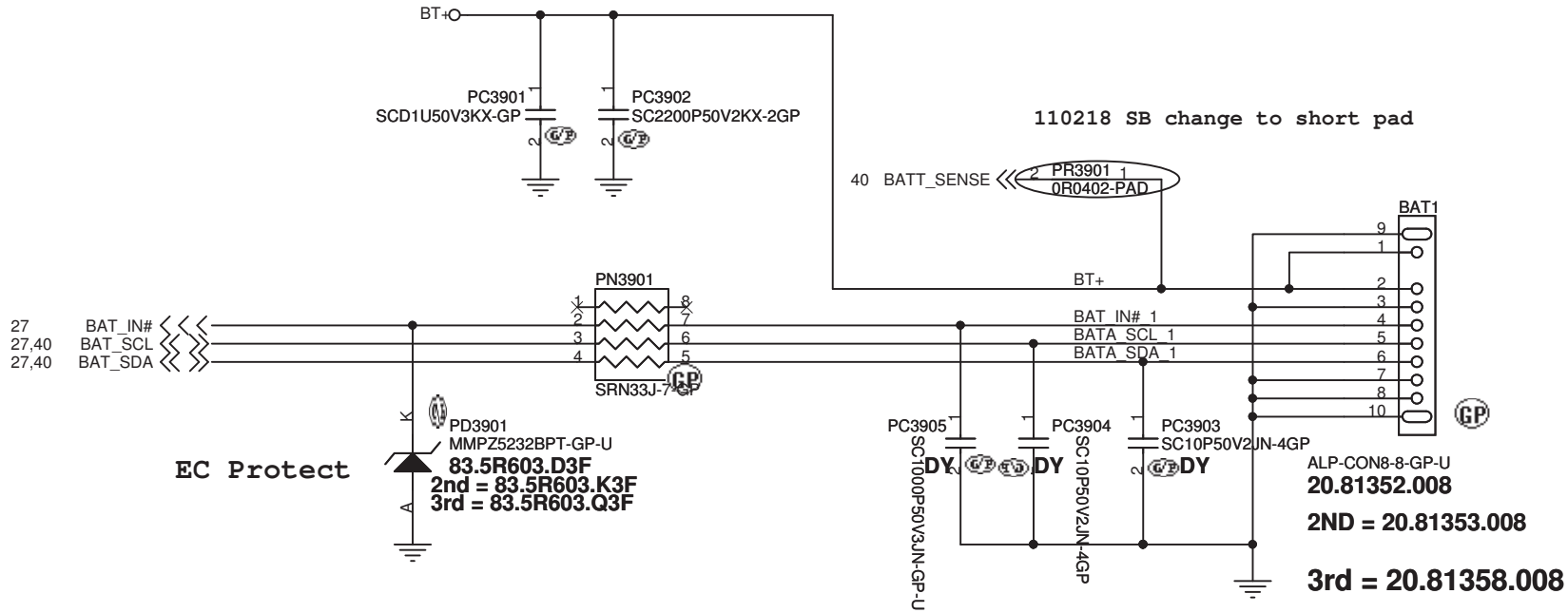
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DCIN_JACK		
Size: A4	Document Number: JE50_SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 38 of 102	

BATTERY CONNECTOR



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT_CONN	
Size A4	Document Number JE50_SB	Rev SB
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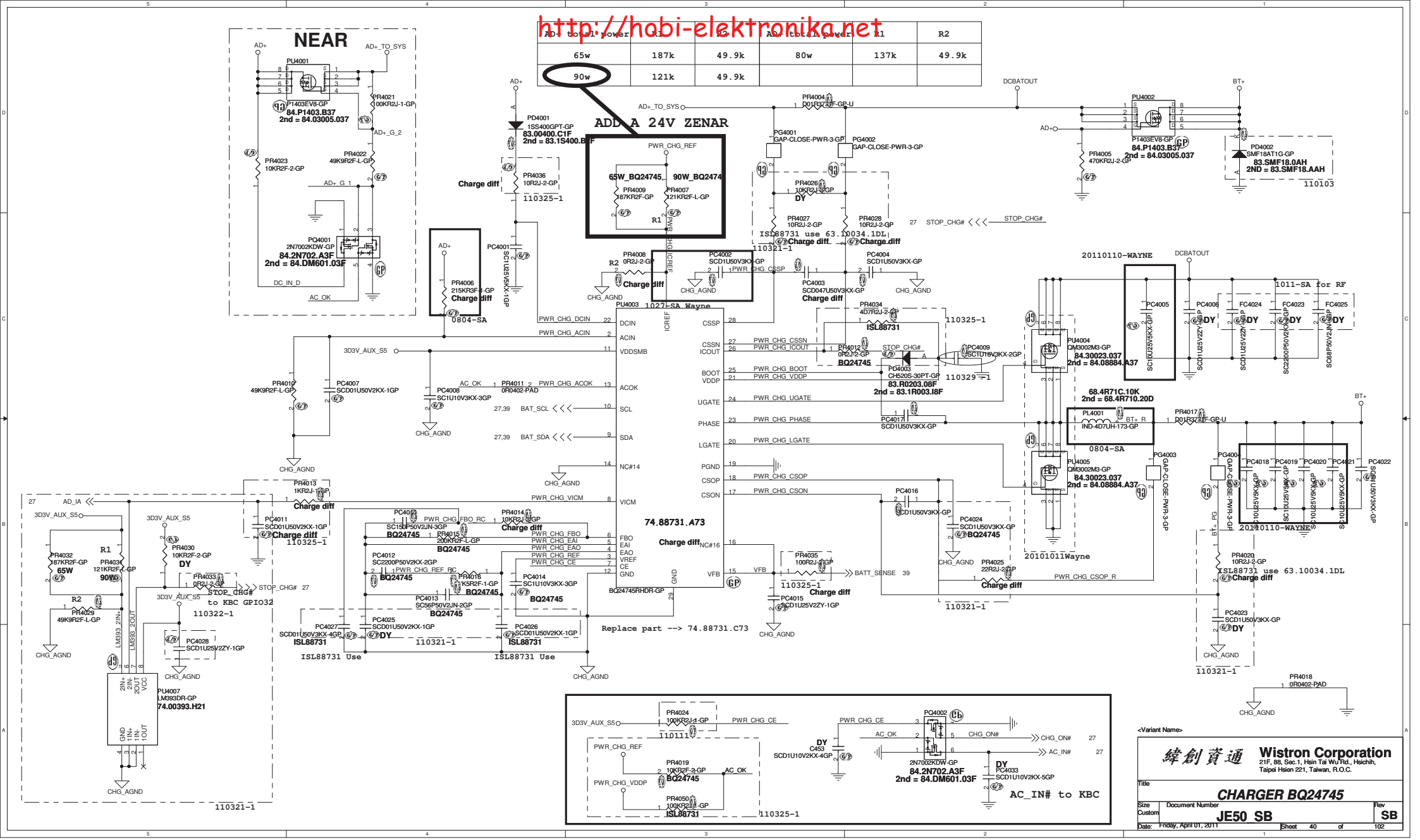
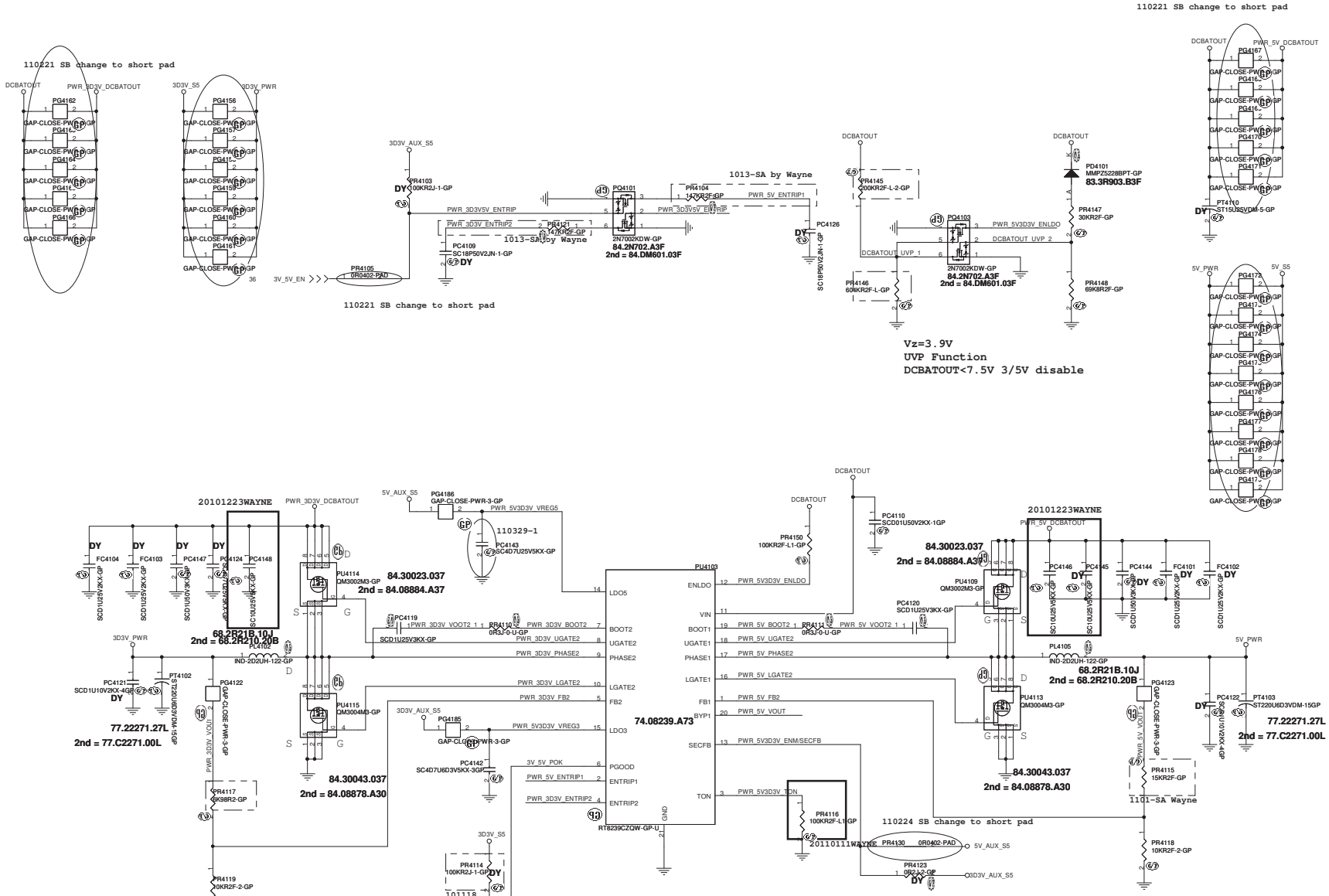
AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			





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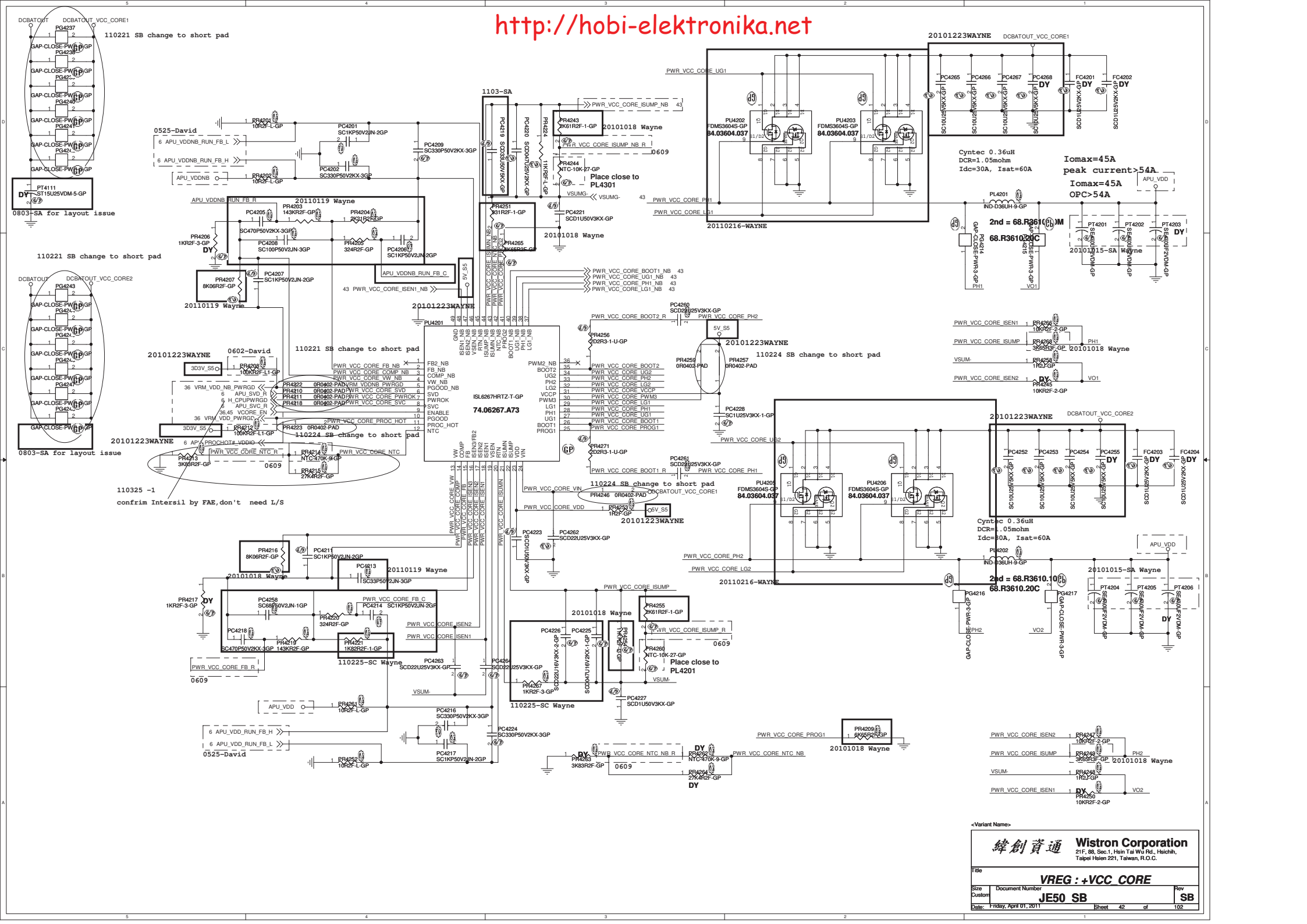
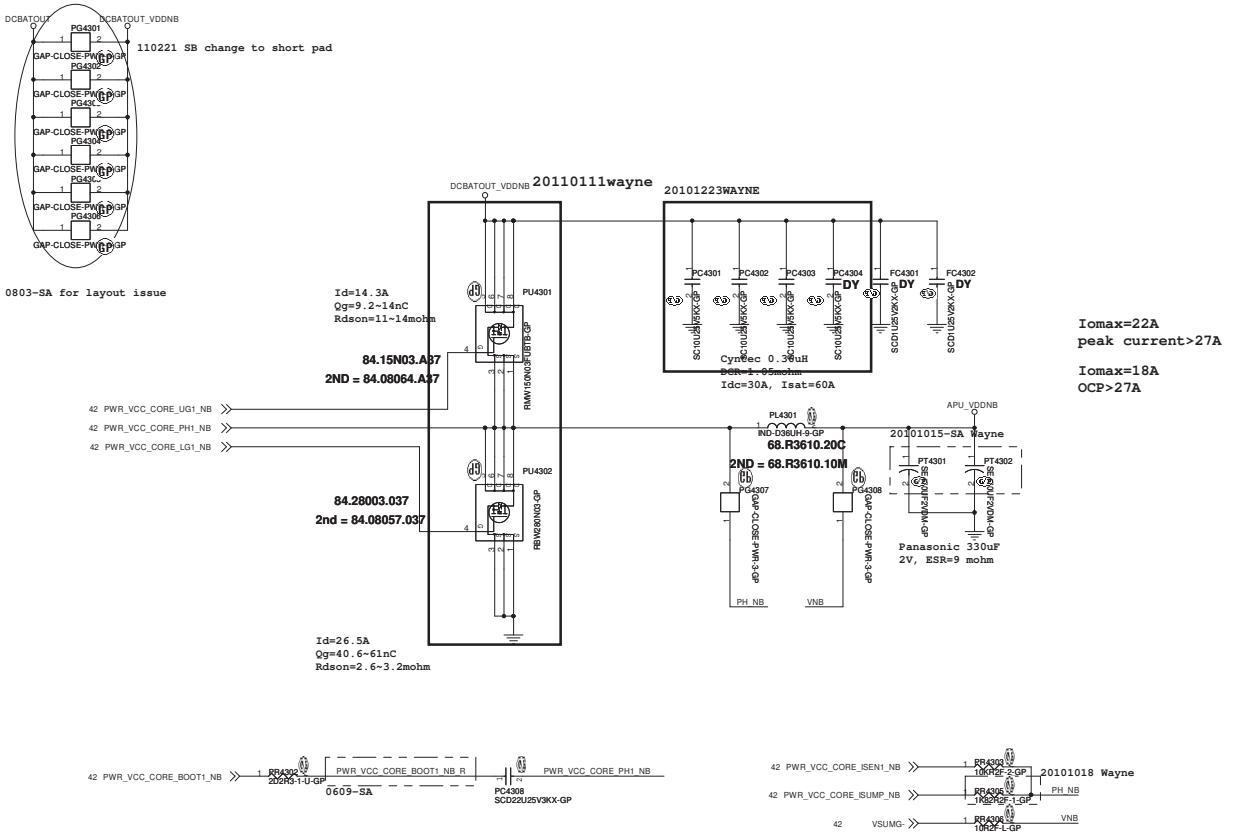
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8239		
Size: A2	Document Number: JE50_SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 41 of 102	





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG : +VCC_NB

Size: A2 | Document Number: JE50_SB | Rev: SB

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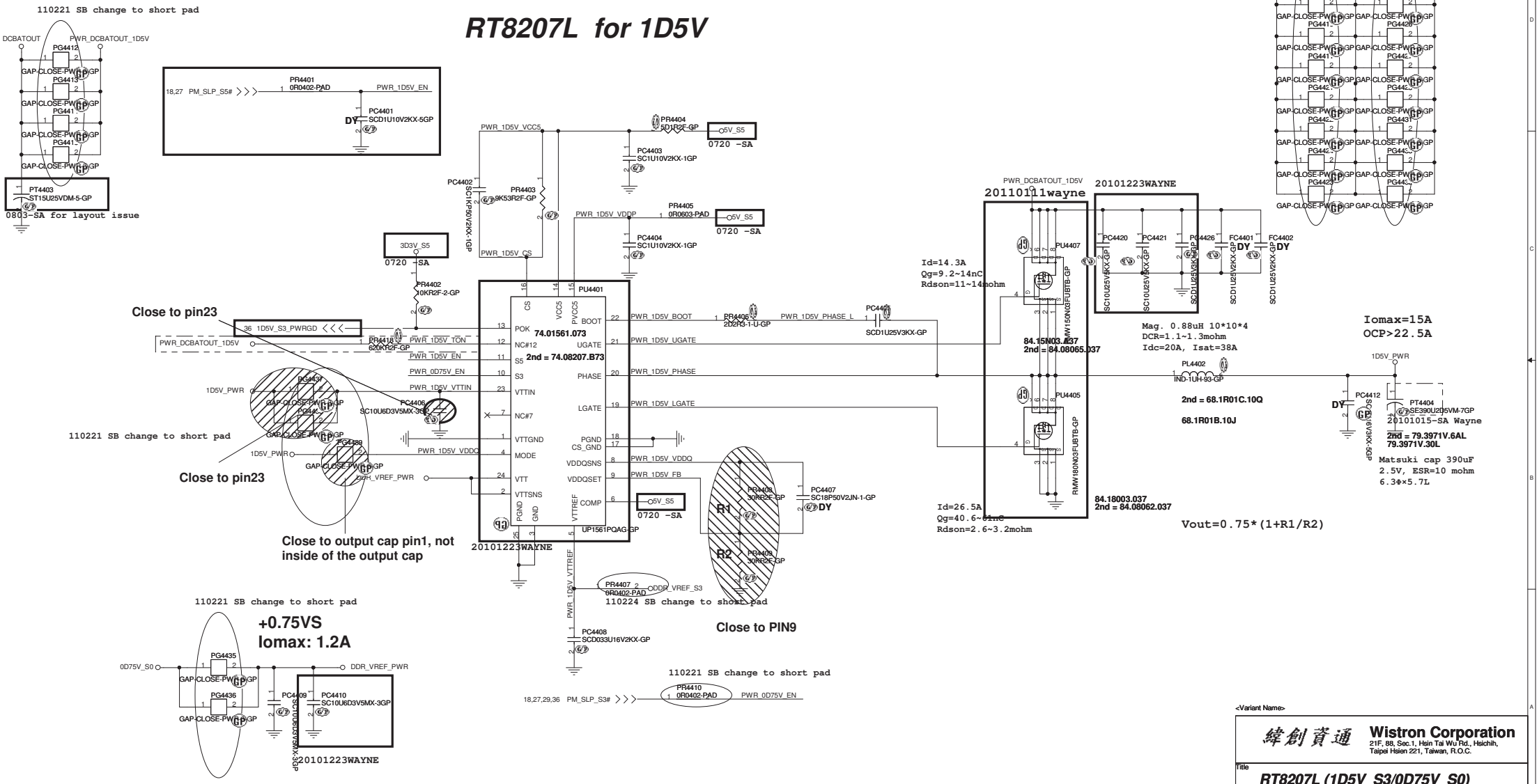
RT8207L for 1D5V



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8207L (1D5V_S3/0D75V_S0)

Size: Custom | Document Number: JE50_SB | Rev: SB

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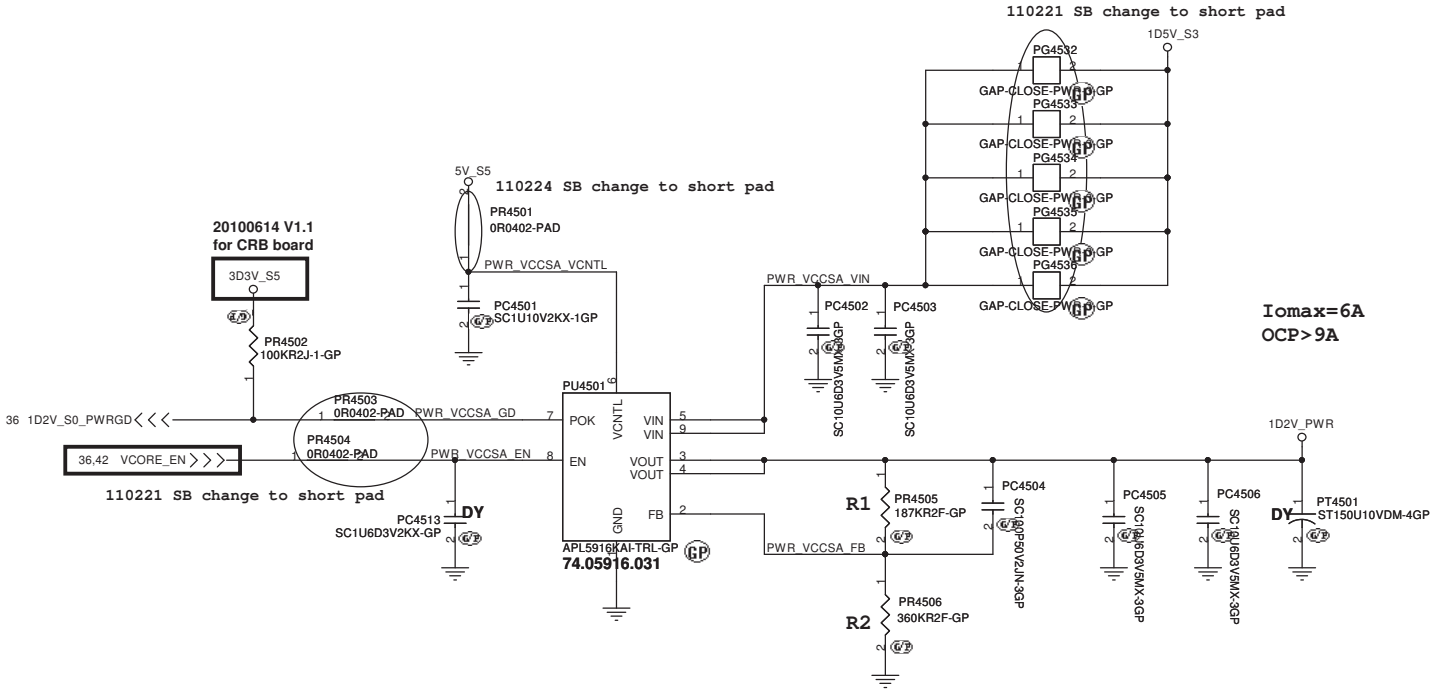
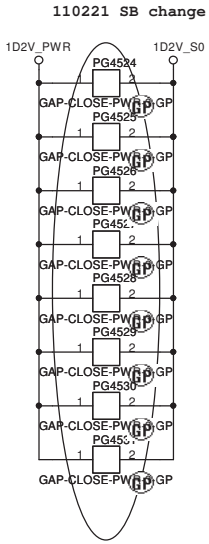
APL5916 for VDDR&VDDP(1D2V_S0)





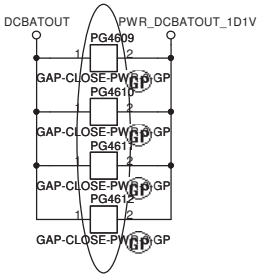
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

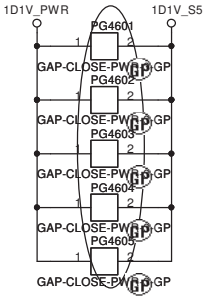
Title	APL5916(1D2V_S0)	
Size A3	Document Number JE50_SB	Rev SB
Date: Friday, April 01, 2011	Sheet 45 of 102	

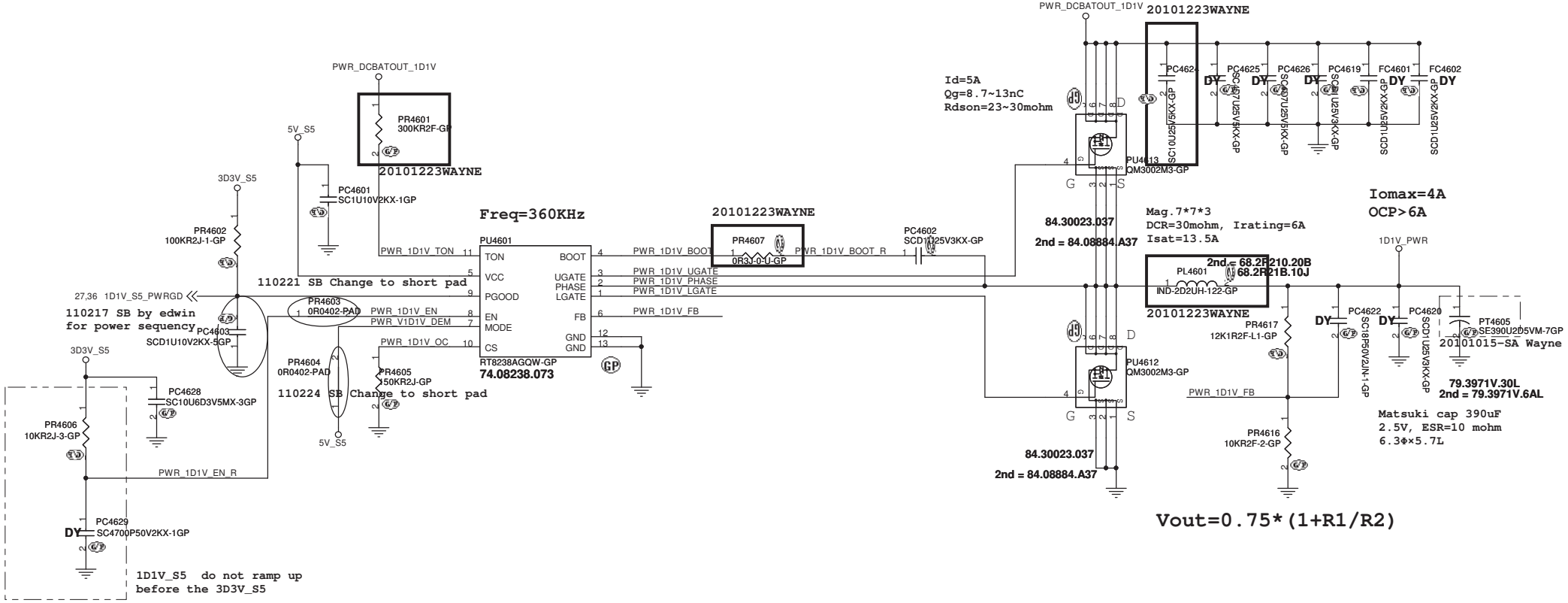
RT8238 for 1D1V_S5

110221 SB Change to short pad



110221 SB Change to short pad





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8238 (1D1V_S5)	
Size A3	Document Number JE50_SB	Rev SB
Date: Friday, April 01, 2011	Sheet 46 of 102	

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	JE50_SB	SB

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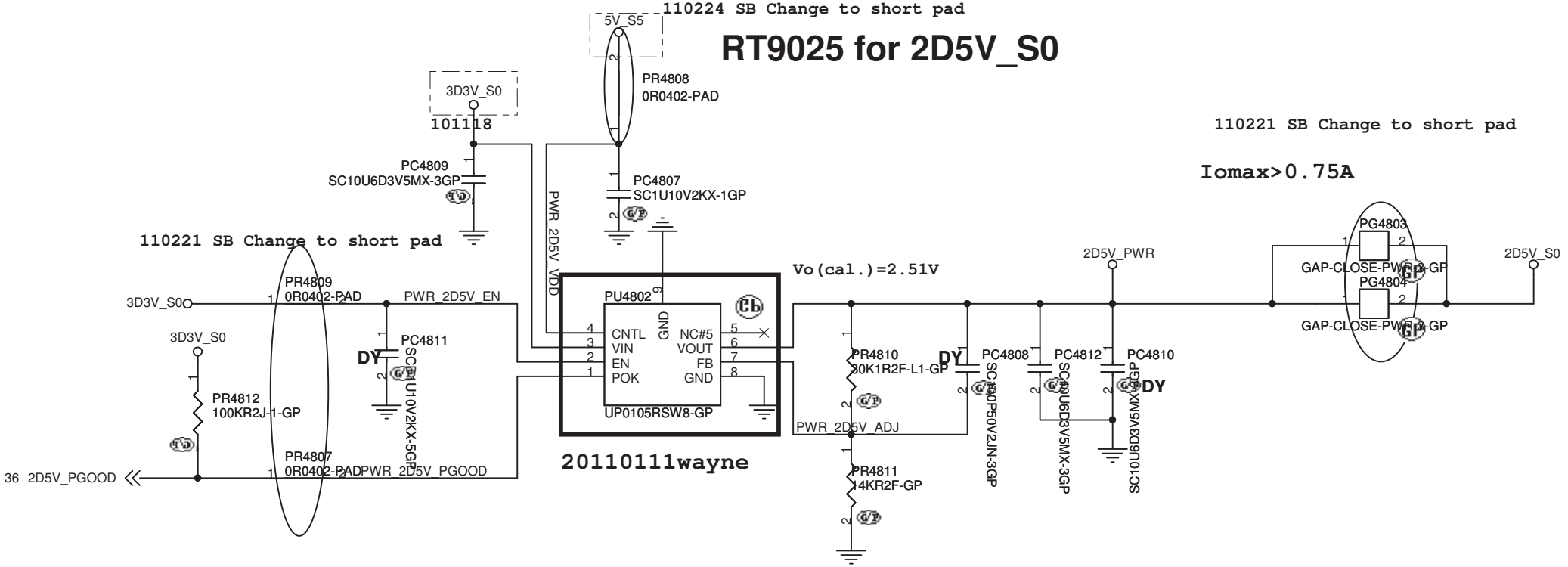
0608-SA

110224 SB Change to short pad

RT9025 for 2D5V_S0



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9025(2D5V_S0)

Size	Document Number	Rev
A4	JE50_SB	SB

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LVDS VS EDP Co-layout CONNECTOR(30 Pin)

INVERTER POWER

DCBATOUT_LCD — F4901 POLYSW-1D1A24V-GP-U — DCBATOUT

C4906 SC47U25V5KX-GP

C4904 SC1KP50V2KX-1GP

C4905 SCD1U50V3KX-GP

69.50007.A31

2nd = 69.50007.A41

Camera Power

3D3V_S0 — F4902 FUSE-1D1A6V-GP-U — 3D3V_CAMERA_S0

69.50007.691

2ND = 69.50007.771

C4903 SC10U6D3V5MX-3GP

3D3V_S0

R4919 DY 100KR2J-1-GP DP_AUXP_CPU_C

R4912 DY 100KR2J-1-GP DP_AUXN_CPU_C

110325 -1

INT_MIC_L_RR

EC4906 MLVG0402220NV05BP-GP-U

R4913 DY 100KR2J-1-GP DP_AUXP_CPU_C

R4917 DY 100KR2J-1-GP DP_AUXN_CPU_C

110221 ADD R4932

LCD1 — DCBATOUT_LCD

DBC_EN_C — R4910 EDP 0R2J-2-GP — INT_MIC_L_RR — R4932 0R2J-2-GP — INT_MIC_L_R 29

BLON_OUT_C

LCD_BRIGHTNESS — R4902 33R2J-2-GP — L_BKLT_CTRL 9,10,94

3D3V_CAMERA_S0

DP_HPD0_C 6,9

For Camera GND

MIC_GND — DY R4933 0R2J-2-GP — 110324-1 — R4934 0R2J-2-GP — MIC_AGND 29

L4901 FILTER-137-GP DY

USB_PN7 18

USB_PP7 18

LVDSA_CLK 9,94

LVDSA_CLK# 9,94

DP_AUXP_CPU_C — R4904 LVDS 0R2J-2-GP — LVDSA_DATA2 9,94 / LVDSA_DATA2# 9,94

DP_AUXN_CPU_C — R4905 LVDS 0R2J-2-GP

DP_TXP0_CPU_C — R4906 LVDS 0R2J-2-GP — LVDSA_DATA1 9,94 / LVDSA_DATA1# 9,94

DP_TXN0_CPU_C — R4907 LVDS 0R2J-2-GP

LVDSA_DATA0 9,94

LVDSA_DATA0# 9,94

0719 -SA

LVDS_DDC_DATA 94

LVDS_DDC_CLK 94

3D3V_S0

LCDVDD

C4901 SCD1U10V2KX-5GP

C4902 SC1U6D3V2KX-GP

PS-CON30-GP

20.F1816.030

2ND = 20.F1860.030

C4911 SCD1U16V2KX-3GP — DP_AUXN_CPU_C EDP — DP_AUXN_CPU 94

C4912 SCD1U16V2KX-3GP — DP_AUXP_CPU_C EDP — DP_AUXP_CPU 94

C4913 SCD1U16V2KX-3GP — DP_TXN0_CPU_C EDP — DP_TXN0_CPU 94

C4914 SCD1U16V2KX-3GP — DP_TXP0_CPU_C EDP — DP_TXP0_CPU 94

110221 SB Change from port3 to port0

C4960 DY SCD1U10V2KX-4GP — USB30_TXDP0 — USB30_TXDP0_R

C4957 DY SCD1U10V2KX-4GP — USB30_TXDN0 — USB30_TXDN0_R

RN4902 CRN0J-6-GP — USB30_RXDP0 — USB30_RXDP0_R — USB30_RXDN0 — USB30_RXDN0_R

110217 SB Remove USB3.0 CCD

110221 SB Change from port3 to port0

*For PS8710B: VDD = 3.3V

Pin Control Mode

C4962 SCD1U10V2KX-4GP — C4963 SCD01U16V2KX-3GP

A_DE0 — R4909 4K7R2J-2-GP

A_DE1 — R4908 4K7R2J-2-GP DY

B_DE0 — R4920 4K7R2J-2-GP DY

B_DE1 — R4921 4K7R2J-2-GP DY

110217 SB Remove USB3.0 CCD

CCD1 — IPEX-CON10-GP DY

USB30_TXDP0_R

USB30_TXDN0_R

USB30_RXDP0_R

USB30_RXDN0_R

3D3V_CAMERA_S0

110221 SB Change from port3 to port0

L4902 FILTER-137-GP DY

L4903 FILTER-137-GP DY

U4903 PS8710BTQFN24GTR-A1-GP

18 USB30_TXDP0 — C4959 DY SCD1U10V2KX-4GP — SSTX1+_C

18 USB30_TXDN0 — C4961 DY SCD1U10V2KX-4GP — SSTX1-_C

18 USB30_RXDP0 — C4954 DY SCD1U10V2KX-4GP — SSRX1+_HUB_C

18 USB30_RXDN0 — C4955 DY SCD1U10V2KX-4GP — SSRX1-_HUB_C

I2C_EN

A_DE1/NC#18 A_EQ0/NC#17 A_DE0/SCL_CTL A_EQ1/SDA_CTL TEST VDD

A_INP A_INN GND B_OUTP B_OUTN I2C_EN GND

A_OUTP A_OUTN GND B_INP B_INN REXT

VDD B_EQ0/NC#2 B_DE0/I2C_ADDR0 B_EQ1/I2C_ADDR1 PD# B_DE1/NC#6

C4958 DY SCD1U10V2KX-4GP — SSTX+_R — USB30_TXDN0_R

C4956 DY SCD1U10V2KX-4GP — SSTX-_R — USB30_RXDN0_R

U401_REXT

R4930 4K99R2F-L-GP

Note: REXT can be left open with default swing setting

3D3V_S0

A_EQ0 — R4925 4K7R2J-2-GP DY

A_EQ1 — R4926 4K7R2J-2-GP DY

B_EQ0 — R4928 4K7R2J-2-GP DY

B_EQ1 — R4927 4K7R2J-2-GP DY

TEST_U — R4922 4K7R2J-2-GP DY

I2C_EN

110217 SB Remove USB3.0 CCD

27,35 BAT_A_SDA — R4924 0R2J-2-GP A_EQ1 DY

27,35 BAT_A_SCL — R4923 0R2J-2-GP A_DE0 DY

reserve for I2C mode

9,10,27,94 LVDS_VDD_EN

LCDVDD — R4914 100KR2J-1-GP DY — C4909 SC10U16V2ZY-2GP

Layout 40 mil

U4901 G5285T11U-GP — EN GND OUT IN#5 IN#4

C4908 SC4D7U6D3V3KX-GP

74.05285.07F

2ND = 74.09724.09F

3D3V_S0 — C4907 SC4D7U6D3V3KX-GP

9,10,27,94 L_BKLT_EN — R4931 DY 1KR2J-1-GP

27 BLON_OUT — R4903 1KR2J-1-GP — BLON_OUT_C — R4911 100KR2J-1-GP — C4910 SC1KP50V2JN-3GP

DBC_EN_C — R4916 DY 10KR2J-3-GP — 3D3V_S0

R4918 33R2J-2-GP DY — DBC_EN 27

R4915 DY 10KR2J-3-GP

<Variant Name>

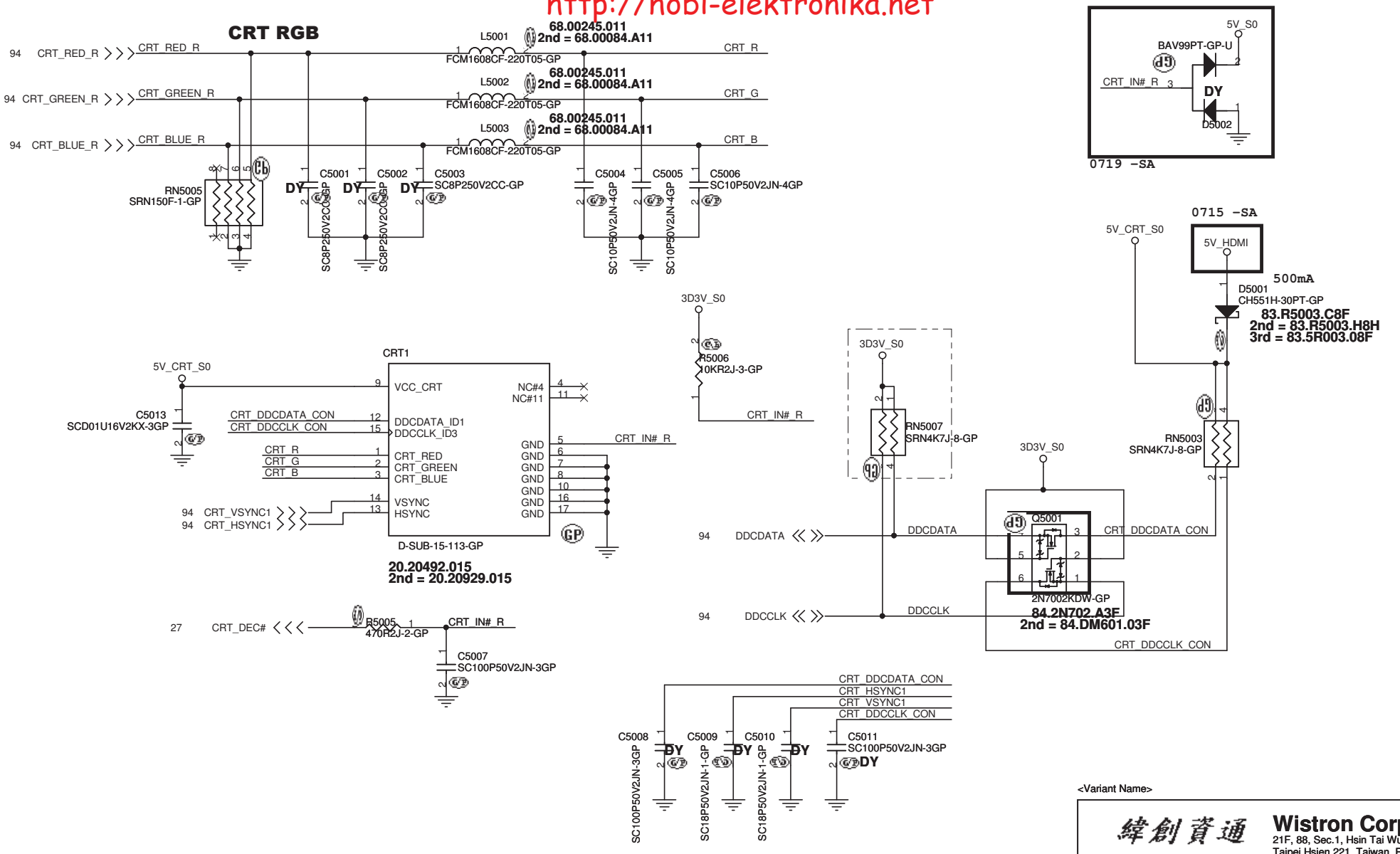
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size: A3 | Document Number: JE50_SB | Rev: SB

Date: Friday, April 01, 2011 | Sheet 49 of 102



<Variant Name>

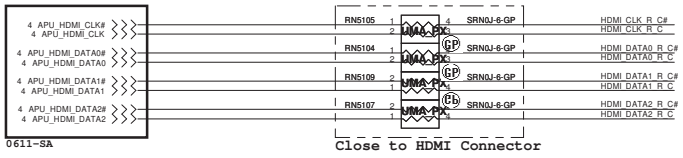
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

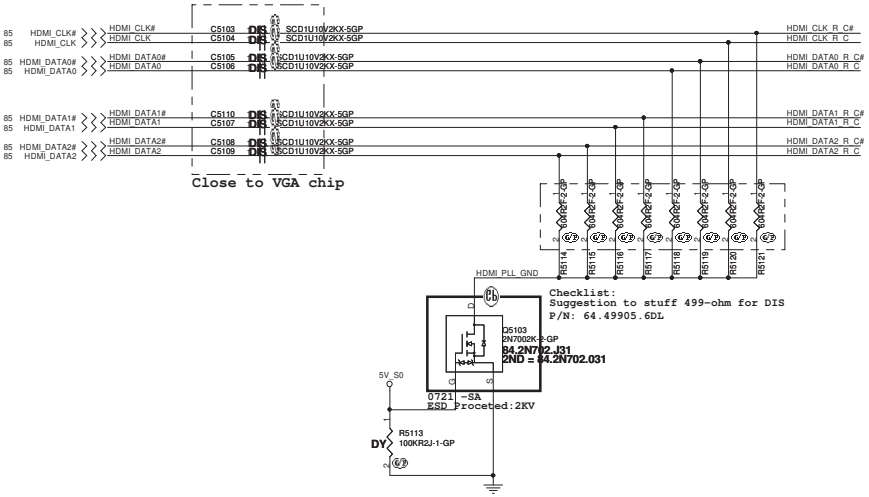
Size	Document Number	Rev
Custom	JE50 SB	SB

Date: Friday, April 01, 2011 Sheet 50 of 102

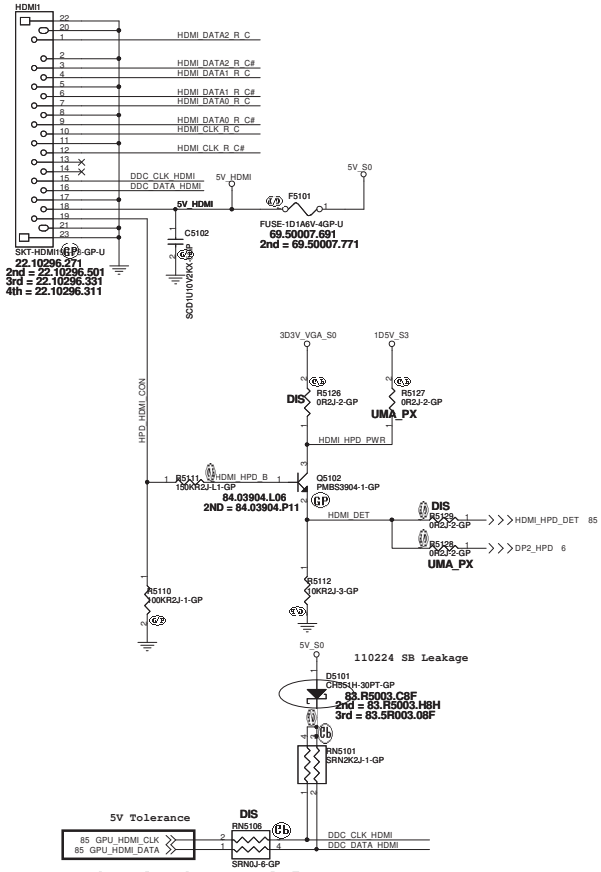
HDMI Level Shifter & CONNECTOR

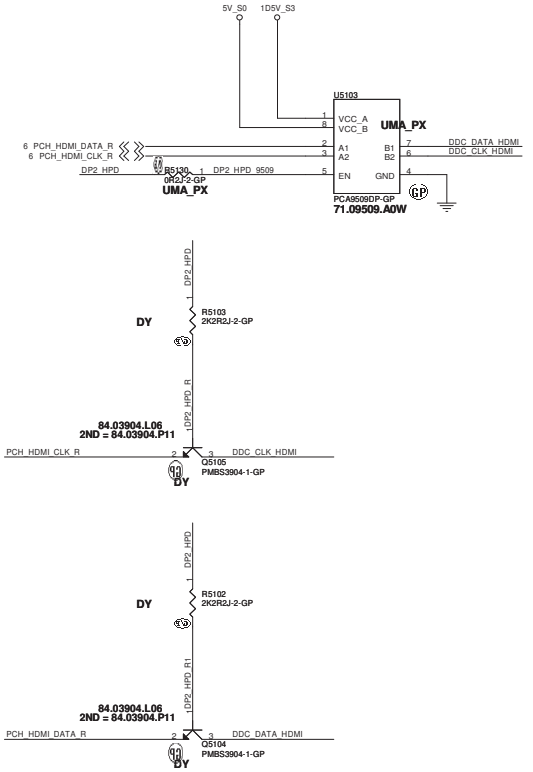


HDMI DISCRETE/ UMA Co-lay



HDMI CONN





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector
Size: A2 | Document Number: JE50_SB | Rev: SB
Date: Friday, April 01, 2011 | Sheet 51 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 52 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 53 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

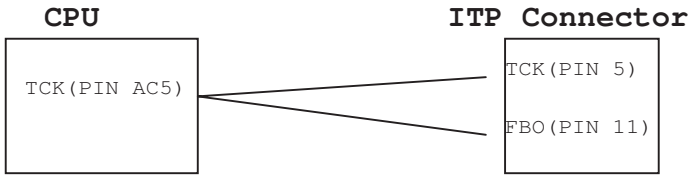
Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP		
Size: A4	Document Number: JE50_SB	Rev: SB
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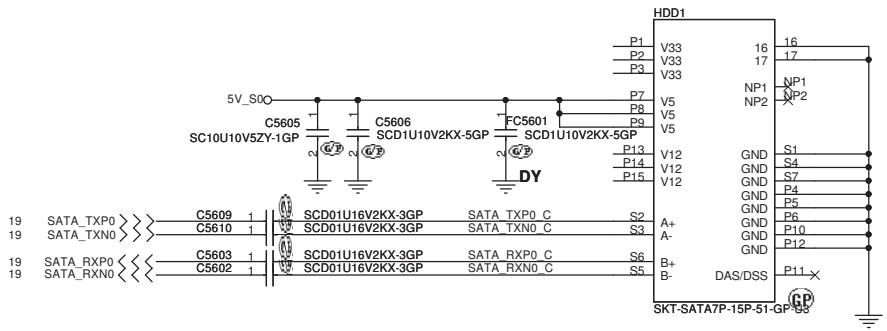
SSID = SATA

SATA HDD Connector

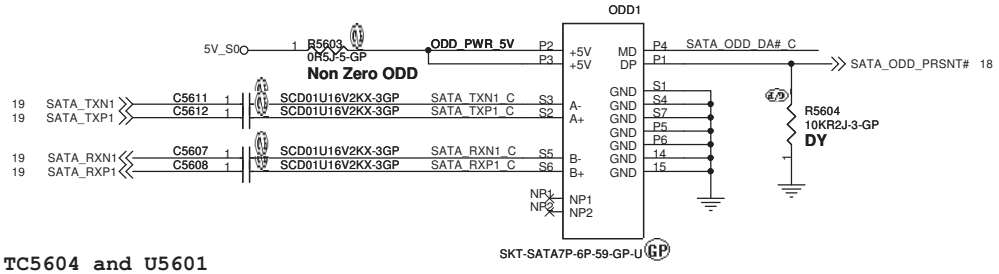


62.10065.701
2nd = 62.10065.711
3RD = 62.10065.H11

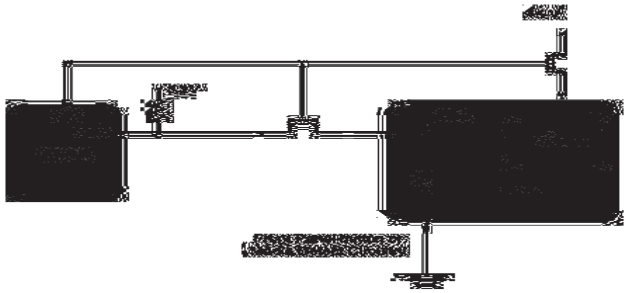
ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 10 mil

Following AMD routing table

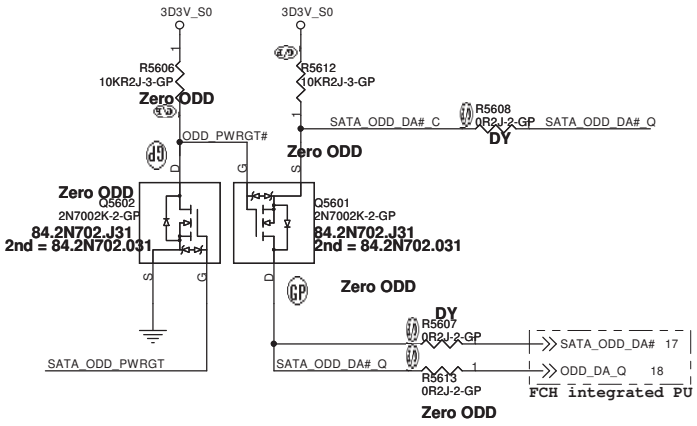


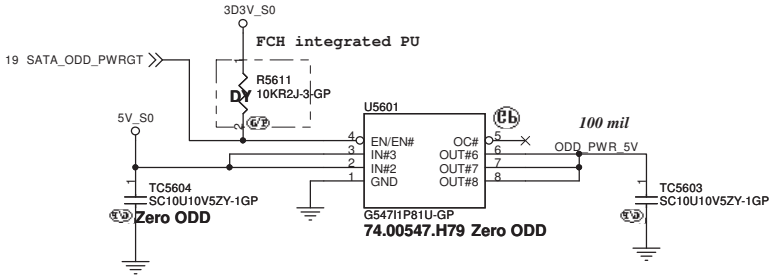
22.10300.B91
2nd = 22.10300.C21



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

If support Zero Power ODD
Stuff R5604,R5612,Q5601 and R5613 TC5604 and U5601
DY R5603





Current limit
Active High
typ =>2.5A

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD/ODD**

Size	Document Number	Rev
A3	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 56 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ESATA/USB Charger

Size	Document Number	Rev
A4	JE50_SB	SB

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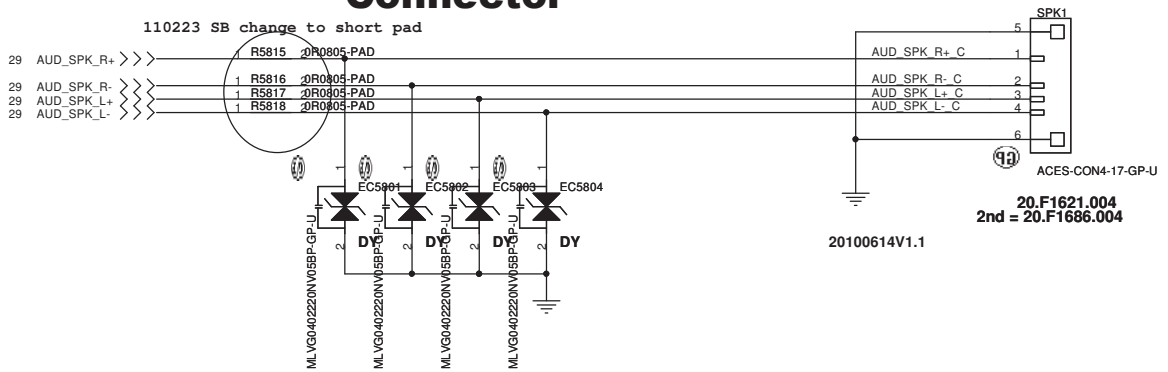
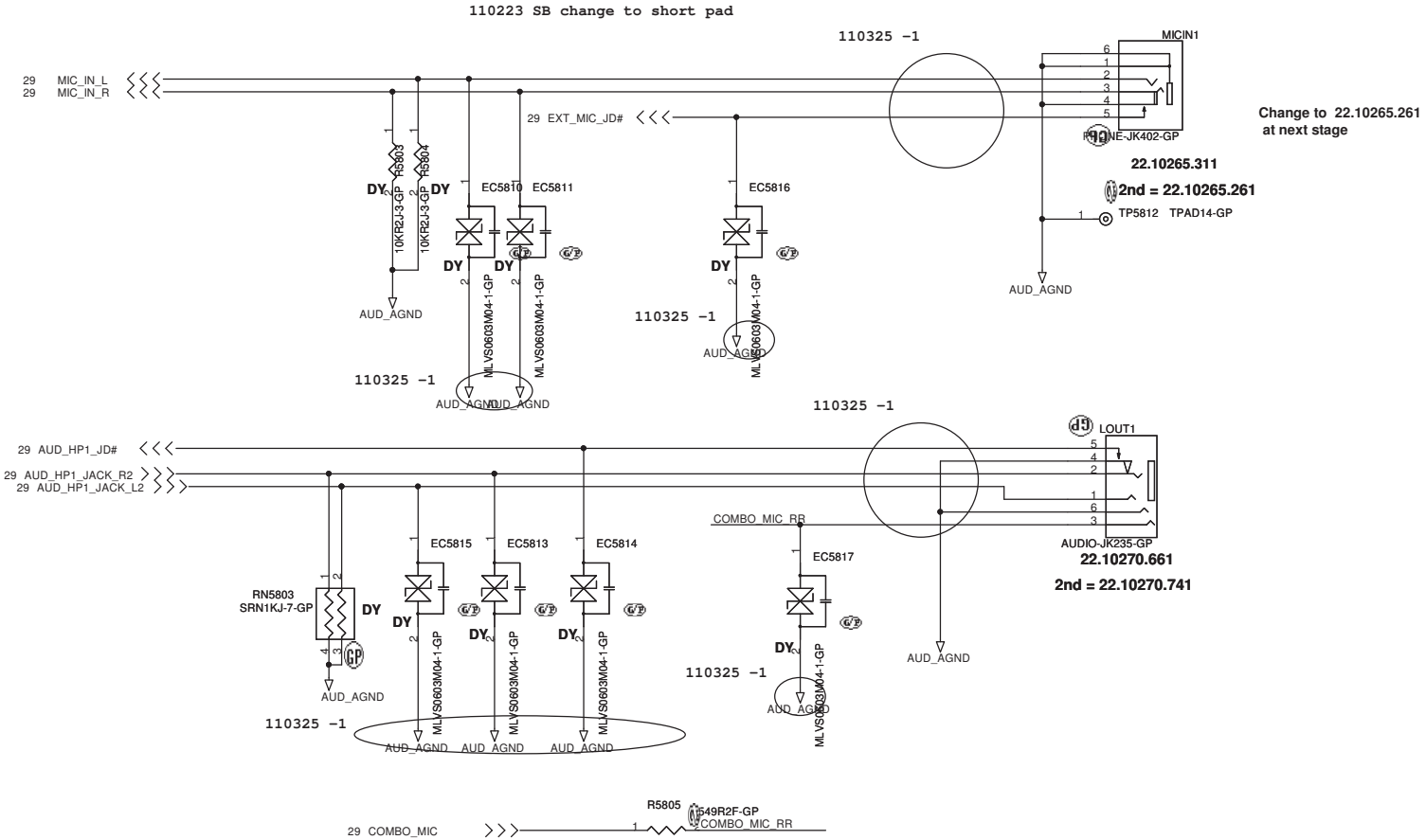
SSID = AUDIO

Speaker Connector



MIC IN



<Variant Name>

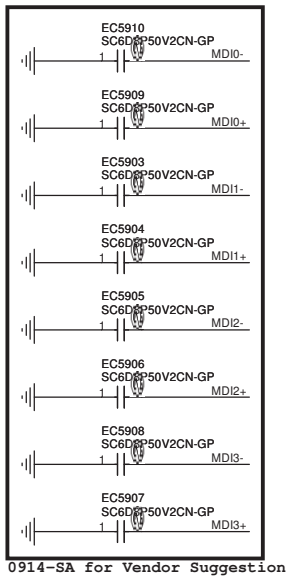
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

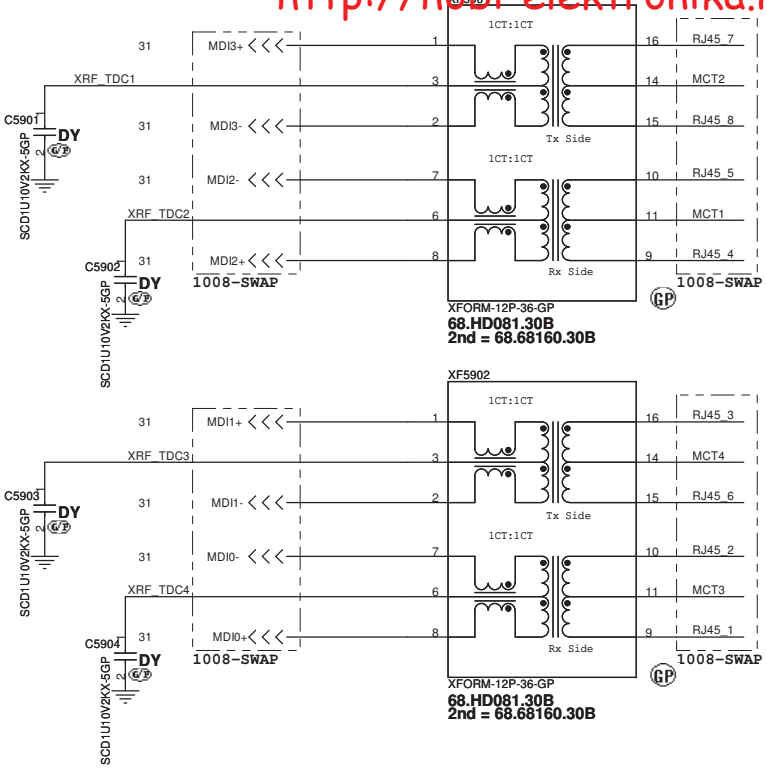
Size	Document Number	Rev
A3	JE50_SB	SB

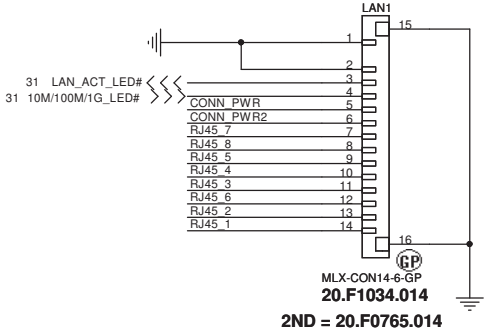
Date: Friday, April 01, 2011 Sheet 58 of 102

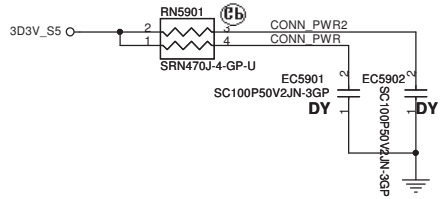
GIGA Lan Transformer

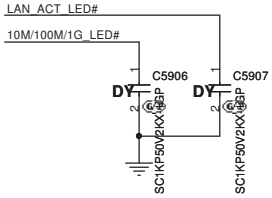


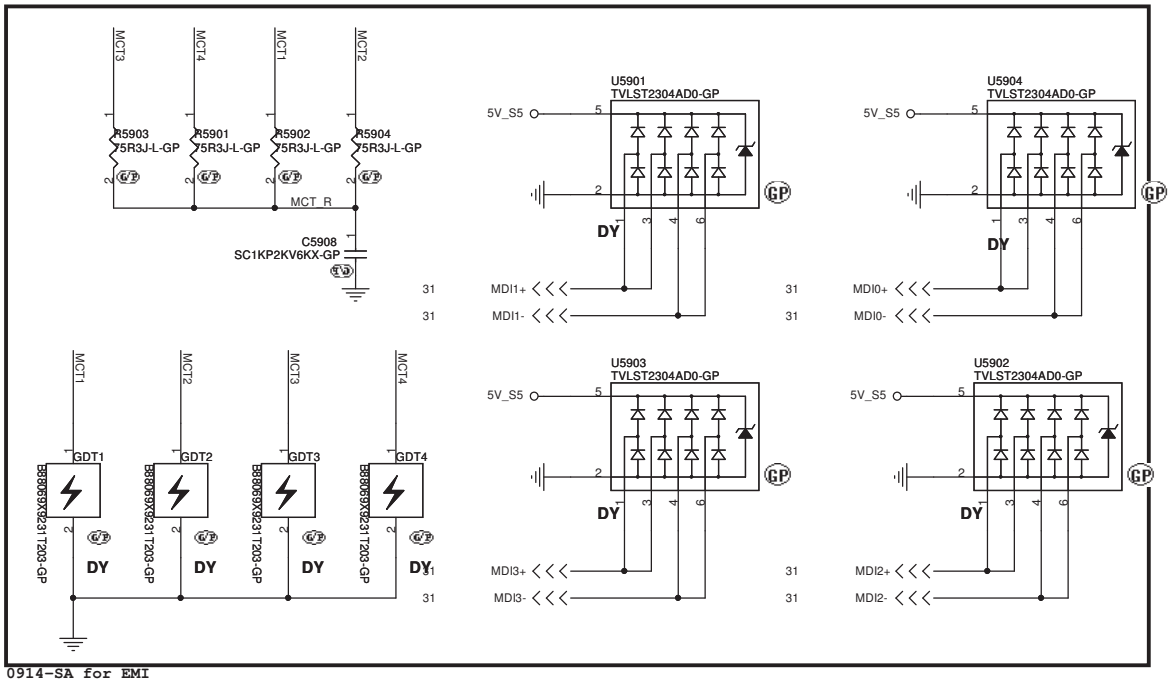
0914-SA for Vendor Suggestion











0914-SA for EMI

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN_CONN**

Size	Document Number	Rev
A3	JE50 SB	SB

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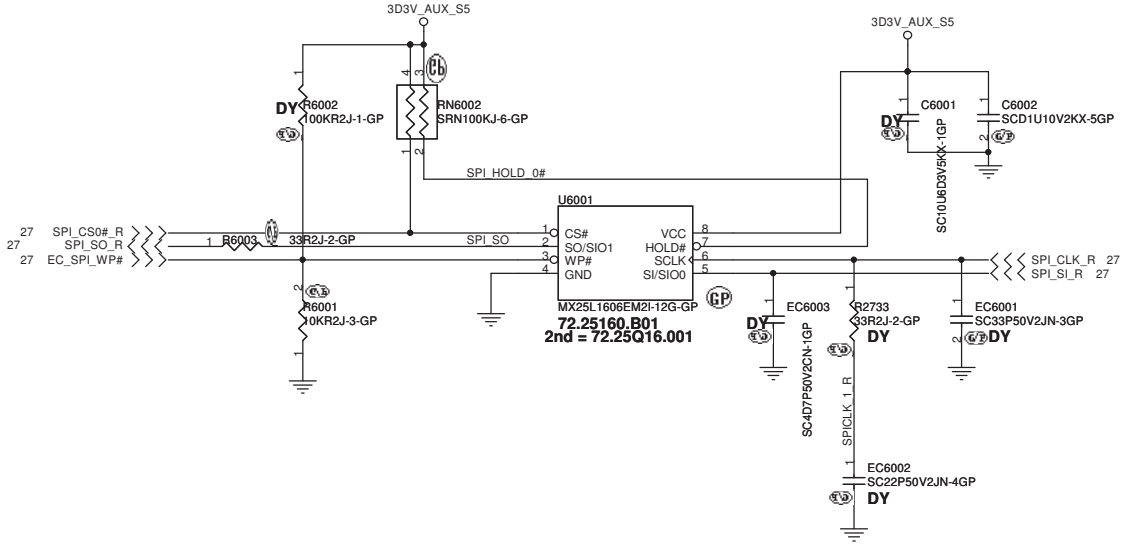
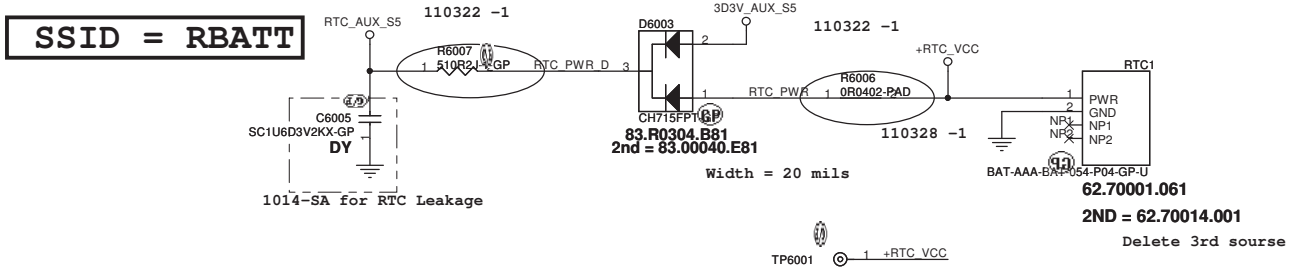
SPI FLASH ROM (2M byte) for KBC



SSID = RBATT



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Flash/RTC		
Size A3	Document Number JE50_SB	Rev SB
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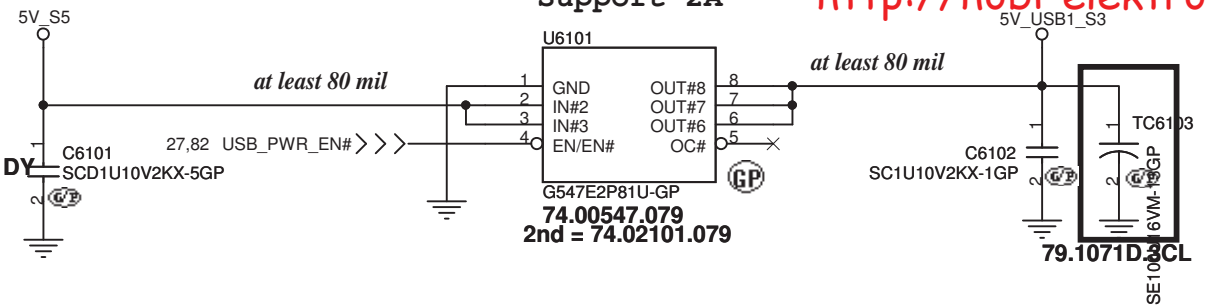

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Power SW**

Size	Document Number	Rev
A4	JE50_SB	SB

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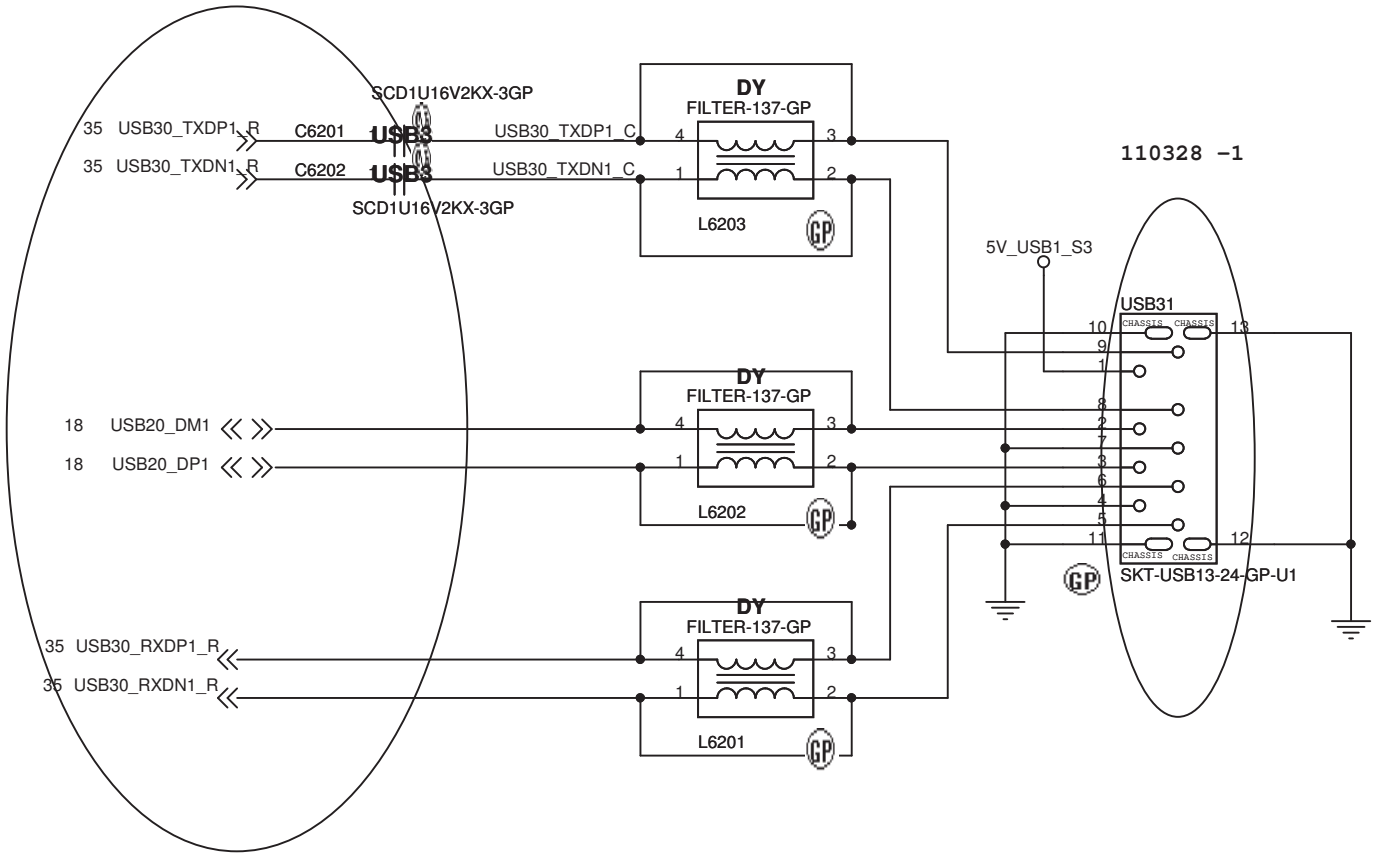
110221 SB Change from port2 to port1



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0

Size: A4 | Document Number: JE50_SB | Rev: SB

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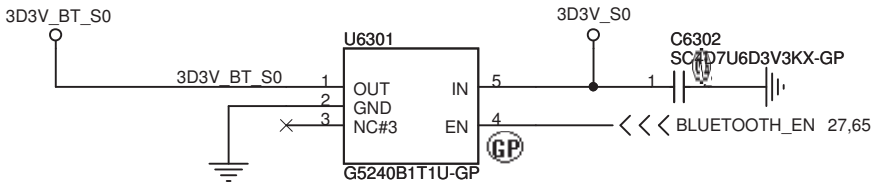
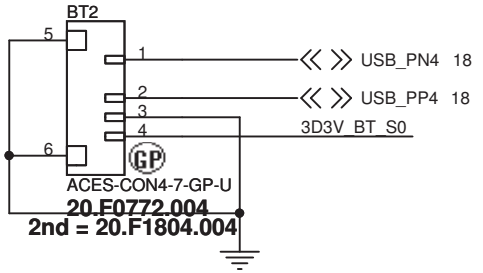
ANNIE Bluetooth Module

1.5A / High Active Voltage 2V





<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **BLUE TOOTH**		
Size: A4	Document Number: **JE50_SB**	Rev: **SB**
Date: Friday, April 01, 2011	Sheet 63 of 102	

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
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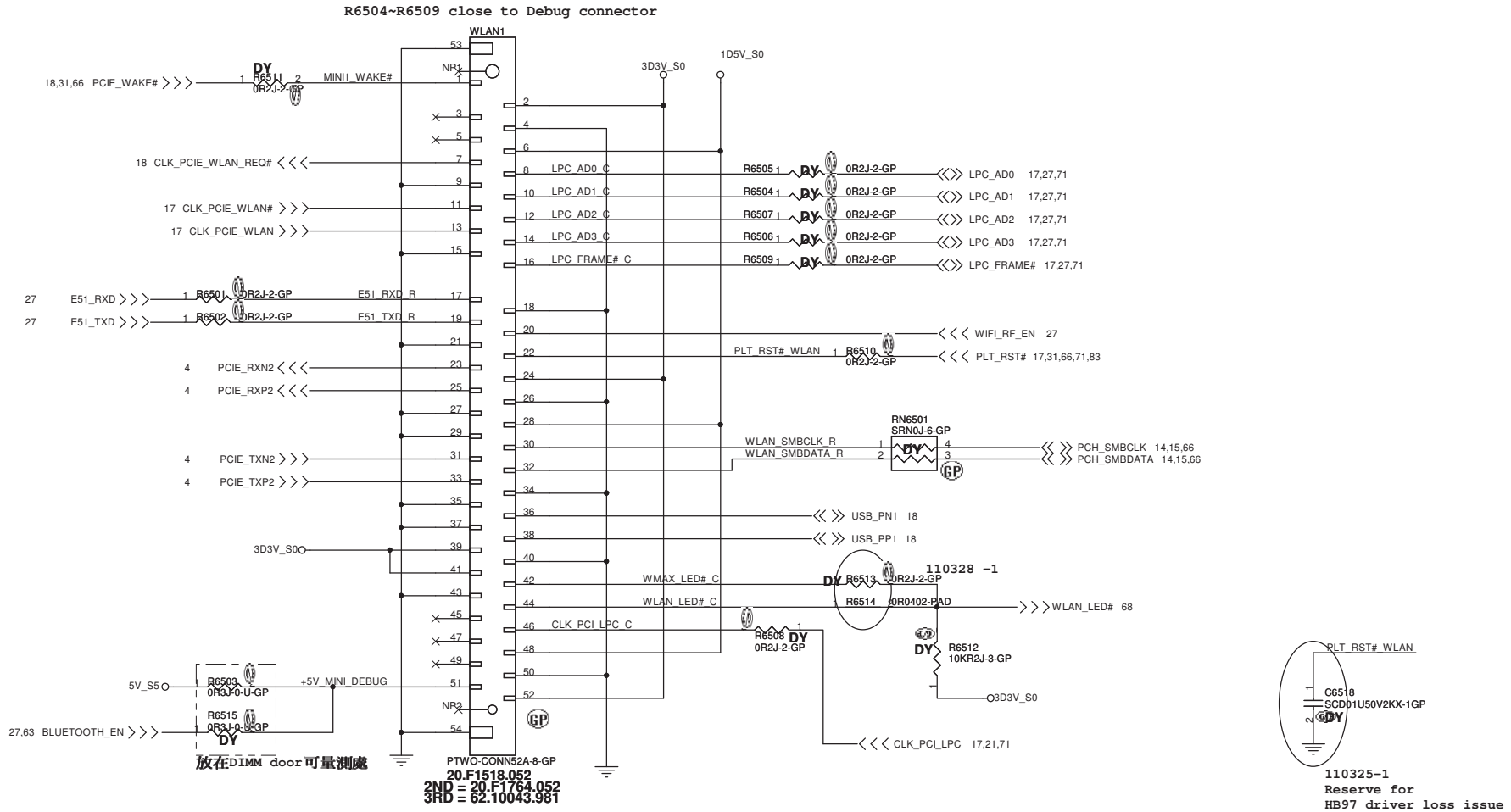
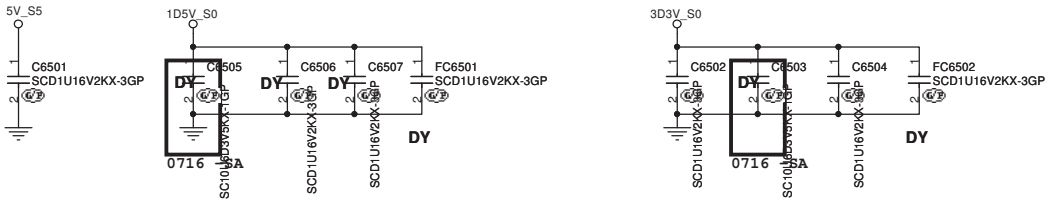
Mini Card Connector(802.11a/b/g/n)





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN
Size: A3
Document Number: JE50 SB
Rev: SB
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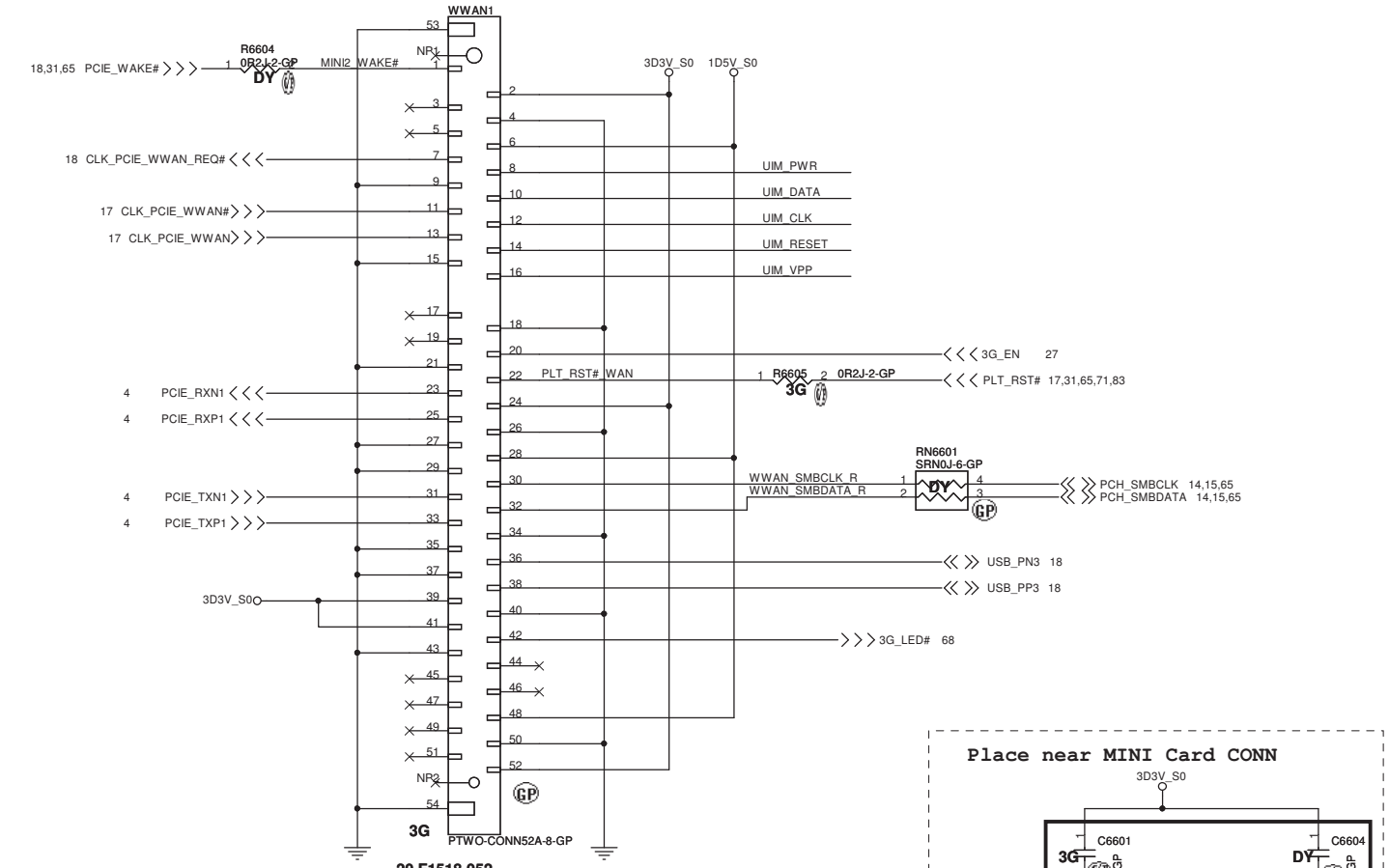
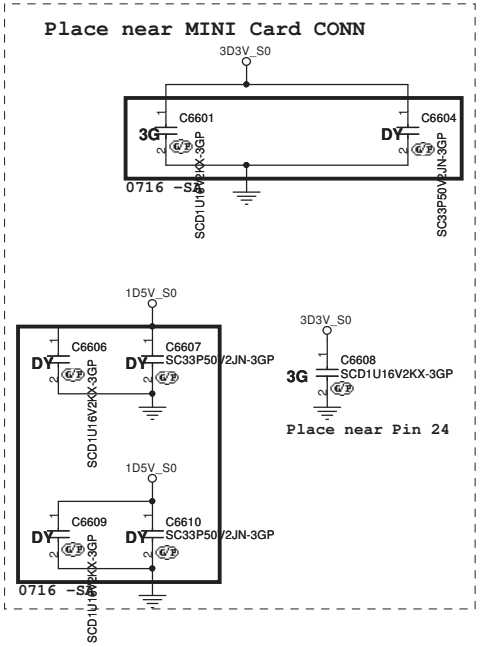
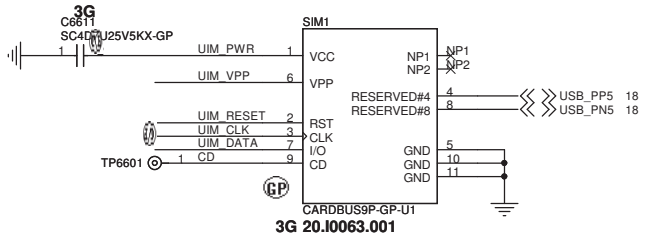
Mini Card Connector(WWAN)



20.F1518.052
2ND = 20.F1764.052
3RD = 62.10043.981





3G 20.I0063.001

ADD avl in sb stage

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **WWAN**		
Size: A3	Document Number: **JE50_SB**	Rev: **SB**
Date: Friday, April 01, 2011	Sheet 66 of 102	

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	JE50_SB	SB

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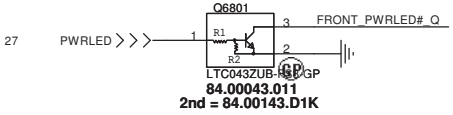
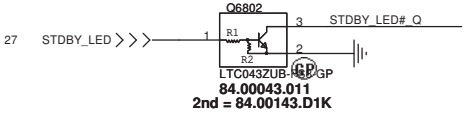
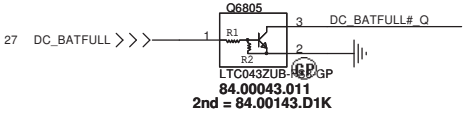
Power button LED



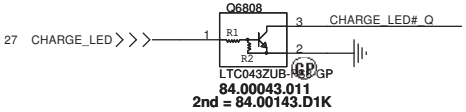
Power STDBY_LED

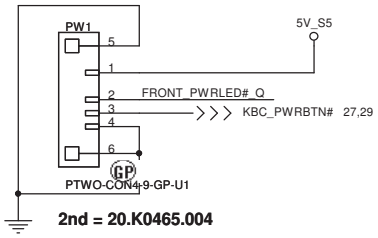


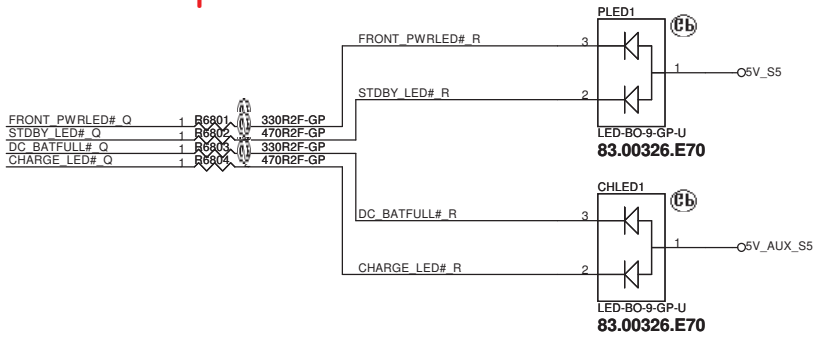
Battery LED2 (DC_BATFULL)

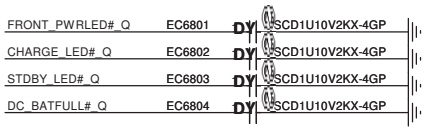


Battery LED1 (CHARGE)

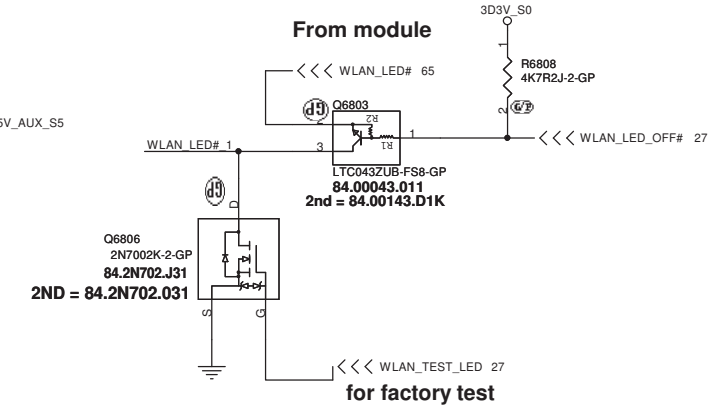




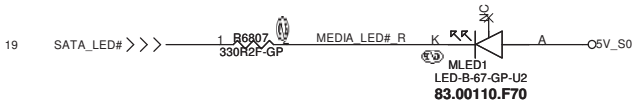




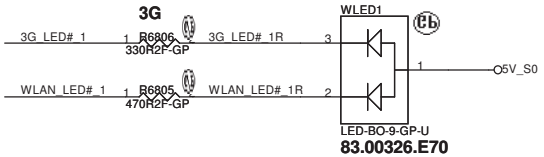
WLAN_LED

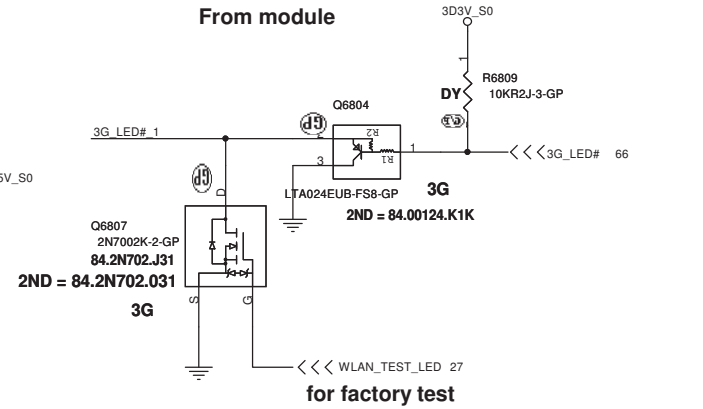


SATA HDD LED



3G LED





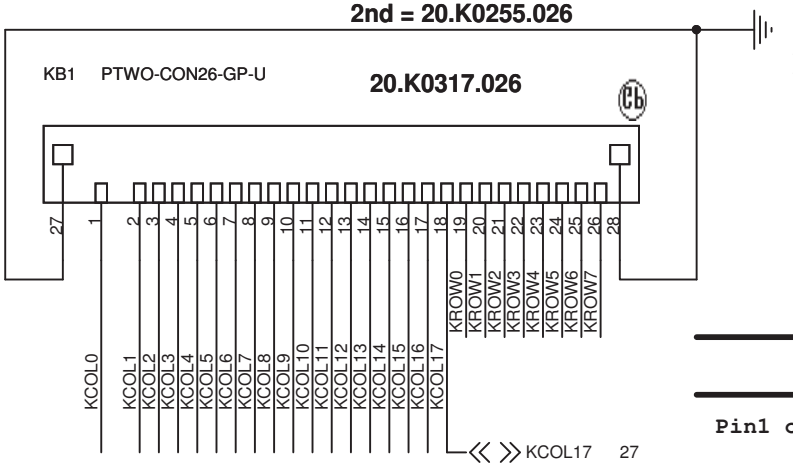
<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LED Bard/Power Button		
Size: A3	Document Number: JE50_SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 68 of 102	

Internal KeyBoard Connector

2nd = 20.K0255.026

KB1 PTWO-CON26-GP-U 20.K0317.026



27
27

KROW[0..7] 27

KCOL[0..16] 27

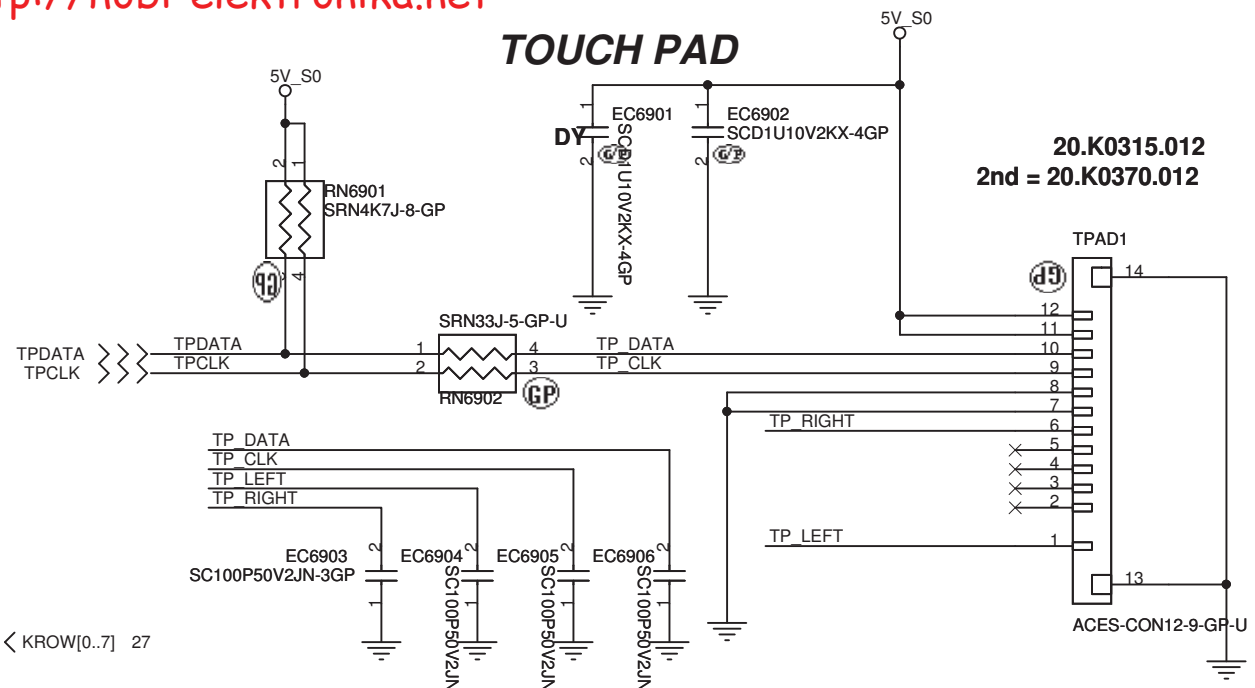
KCOL17 27

Pin1 on right side

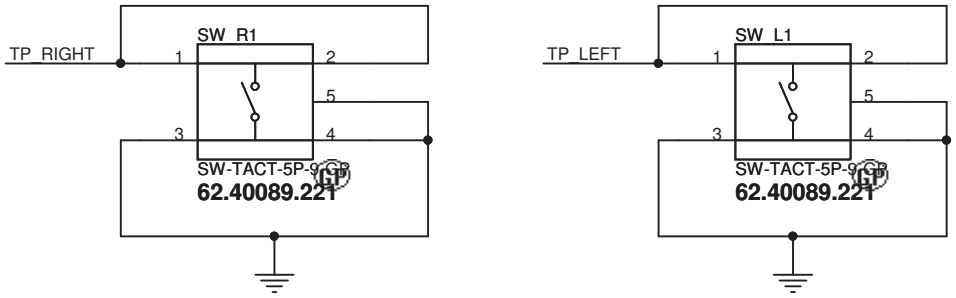
MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

1 K/B 26

TOUCH PAD

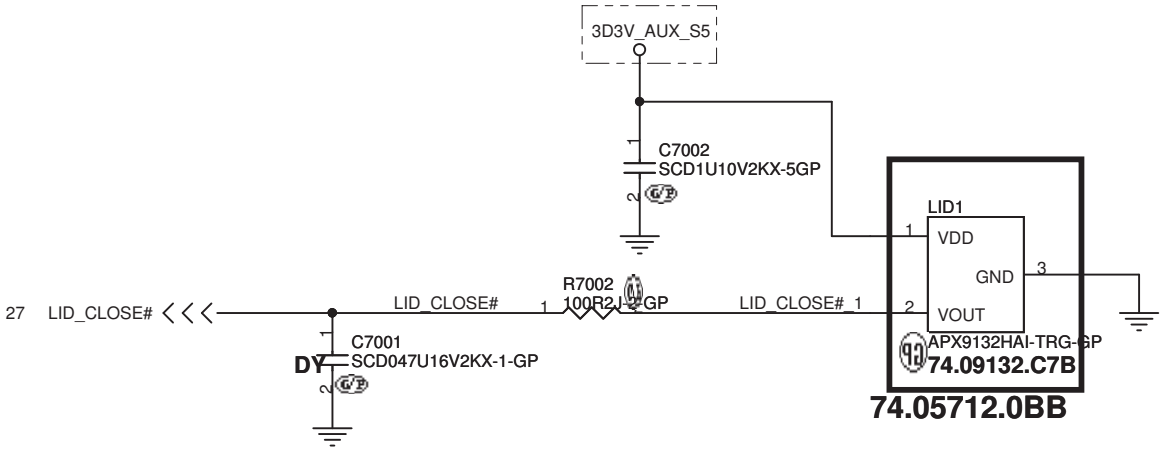


1 T/P 12



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Key Board/Touch Pad		
Size: A4	Document Number: JE50_SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 69 of 102	



<Variant Name>

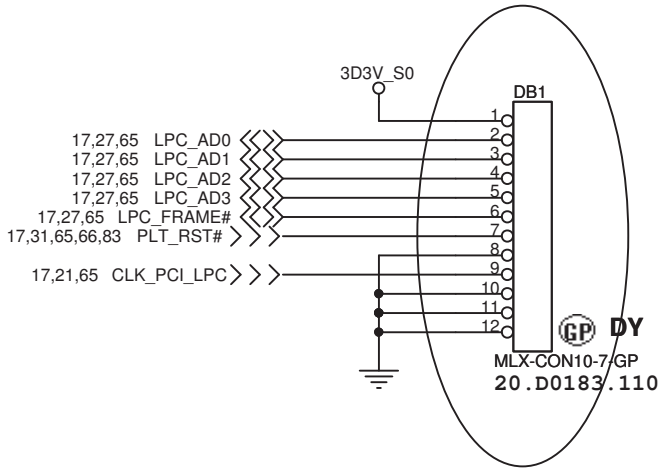
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

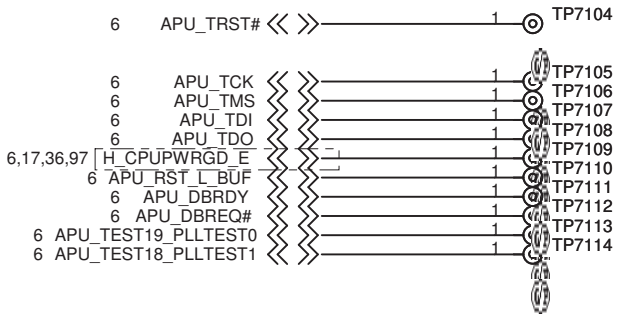
Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 70 of 102

110218 SB BOM Change



HDT+ Connectors



CRB:placed 0-ohm
Checklist: If both SCAN and HDT+ header are implement
placed 15-ohm

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 71 of 102

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 72 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

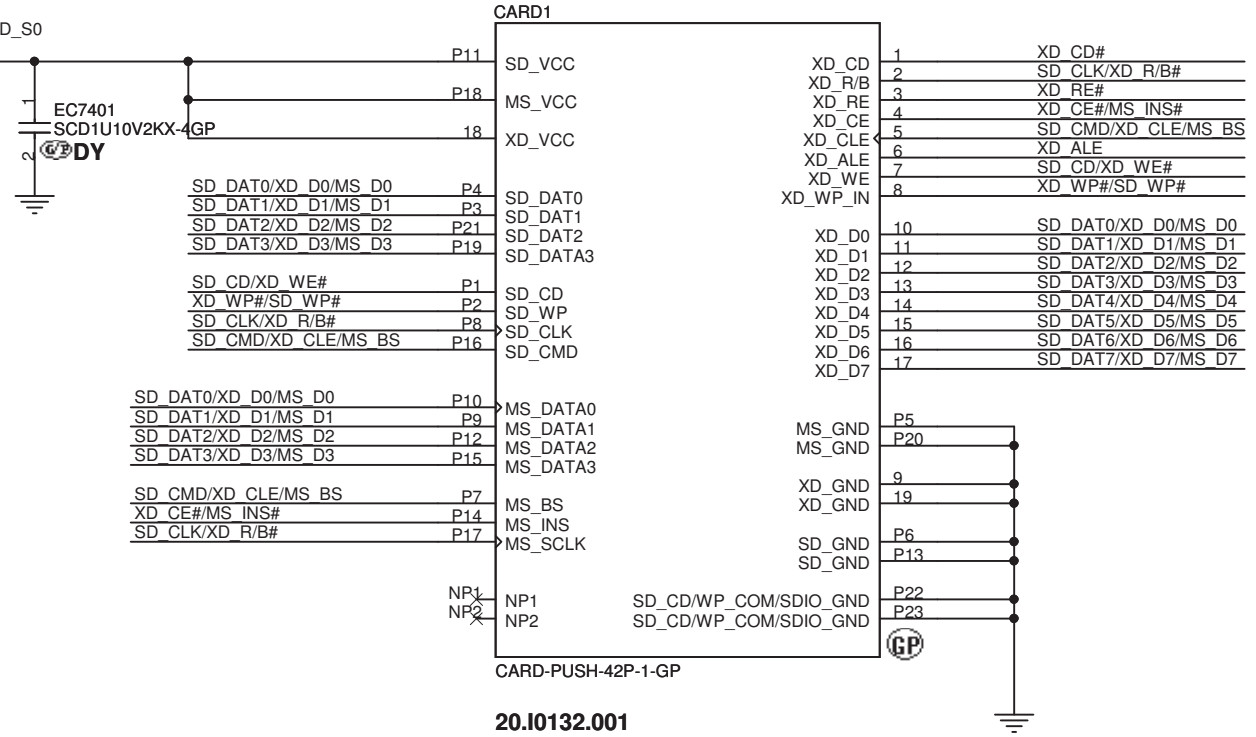
Date: Friday, April 01, 2011 Sheet 73 of 102

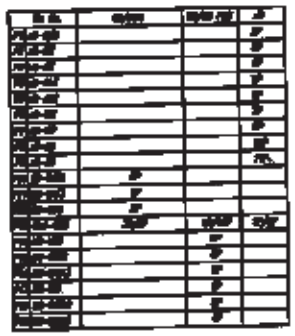
SD/XD/MS Card Reader

SSID = SDIO

31 SD_DAT0/XD_D0/MS_D0
31 SD_DAT1/XD_D1/MS_D1
31 SD_DAT2/XD_D2/MS_D2
31 SD_DAT3/XD_D3/MS_D3
31 SD_DAT4/XD_D4/MS_D4
31 SD_DAT5/XD_D5/MS_D5
31 SD_DAT6/XD_D6/MS_D6
31 SD_DAT7/XD_D7/MS_D7

31 SD_CD/XD_WE#
31 XD_CD#
31 XD_CE#/MS_INS#
31 XD_RE#
31 XD_WP#/SD_WP#
31 XD_ALE
31 SD_CLK/XD_R/B#
31 SD_CMD/XD_CLE/MS_BS





<Variant Name>

Card-reader Off-Page

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 74 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 75 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 76 of 102

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 77 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 78 of 102

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 79 of 102

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 80 of 102

(Blanking)

<Variant Name>

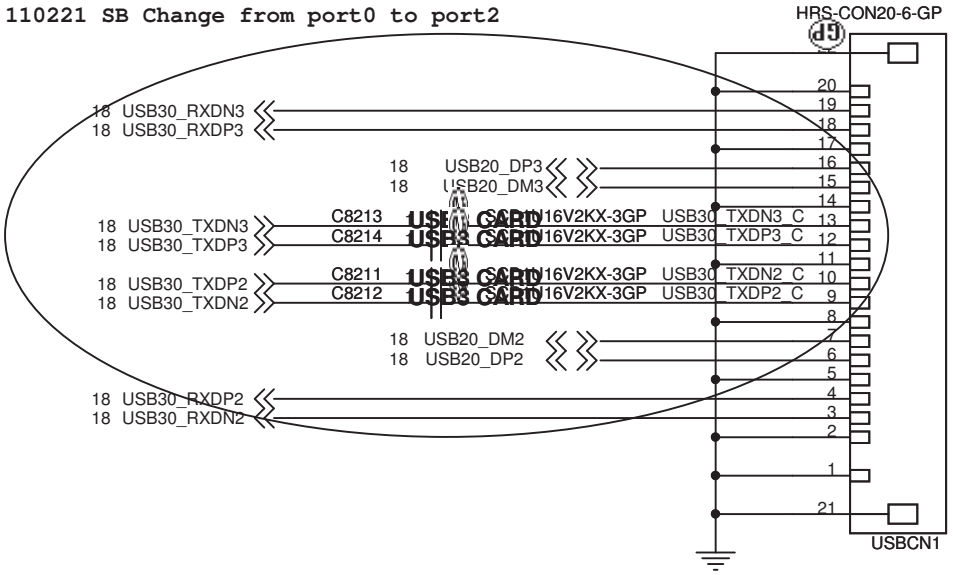
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

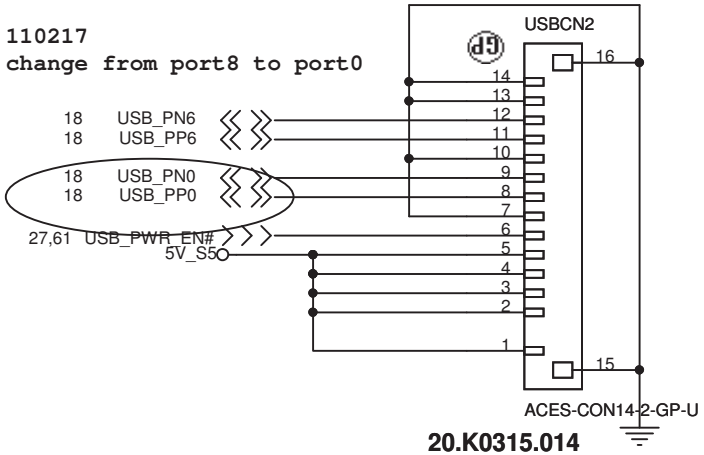
Date: Friday, April 01, 2011 Sheet 81 of 102

110221 SB Change from port1 to port3
110221 SB Change from port0 to port2



USB3 CARD

110217
change from port8 to port0



20.K0315.014
2nd = 20.K0370.014

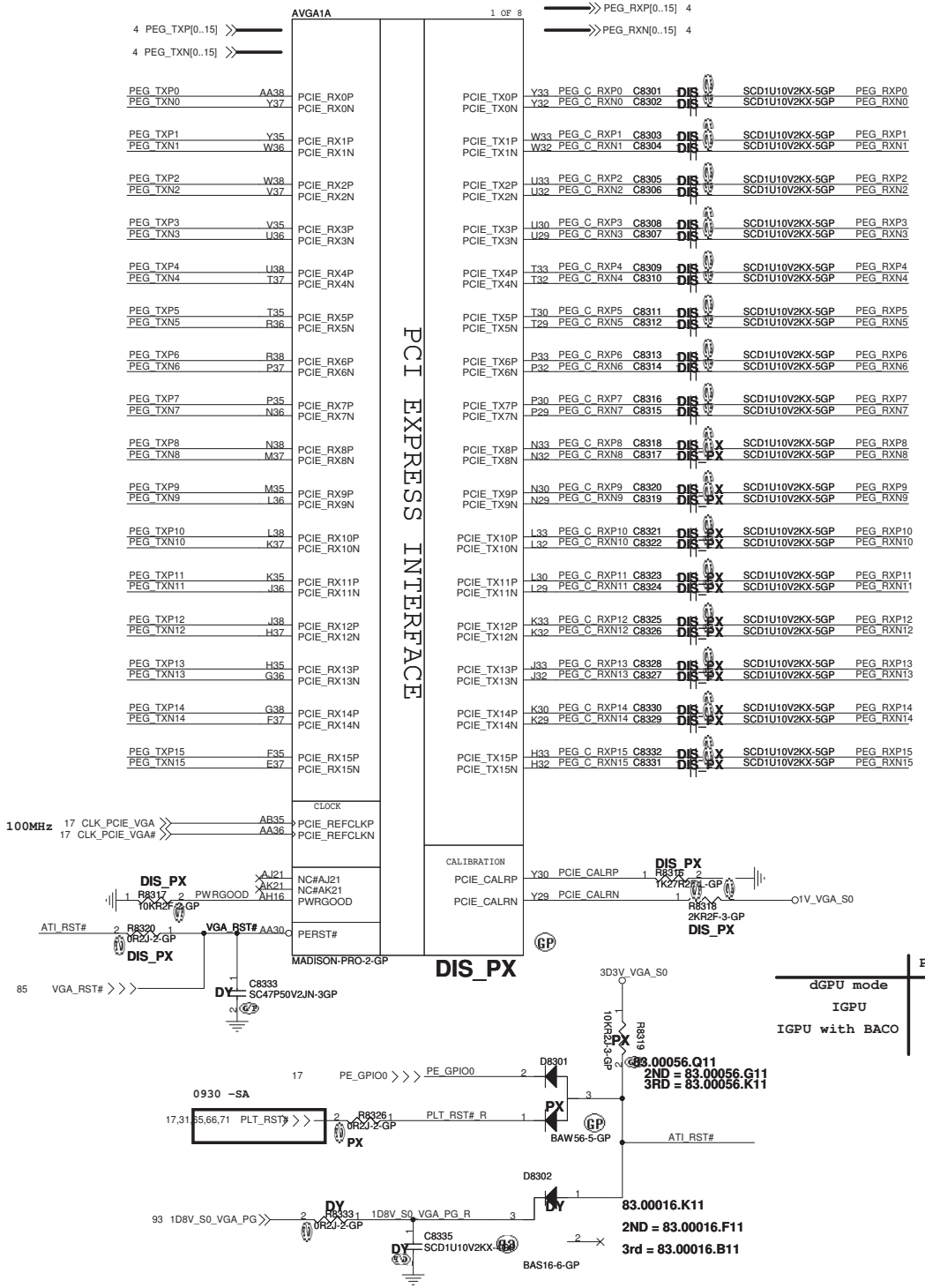
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 82 of 102



PE_GPIO0	
dGPU mode	H
IGPU	L
IGPU with BACO	H

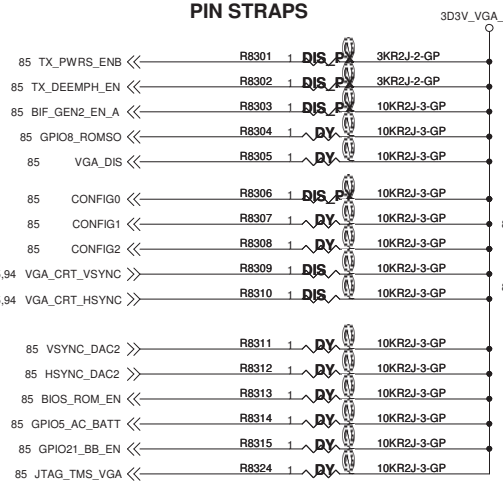
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

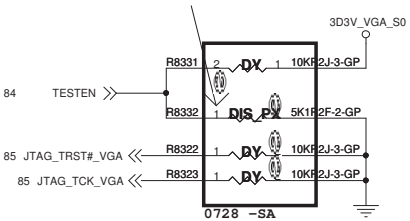
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PIN STRAPS



R8332 stuff 1K for Mannhatton VGA
stuff 5.1K for Vancouver VGA



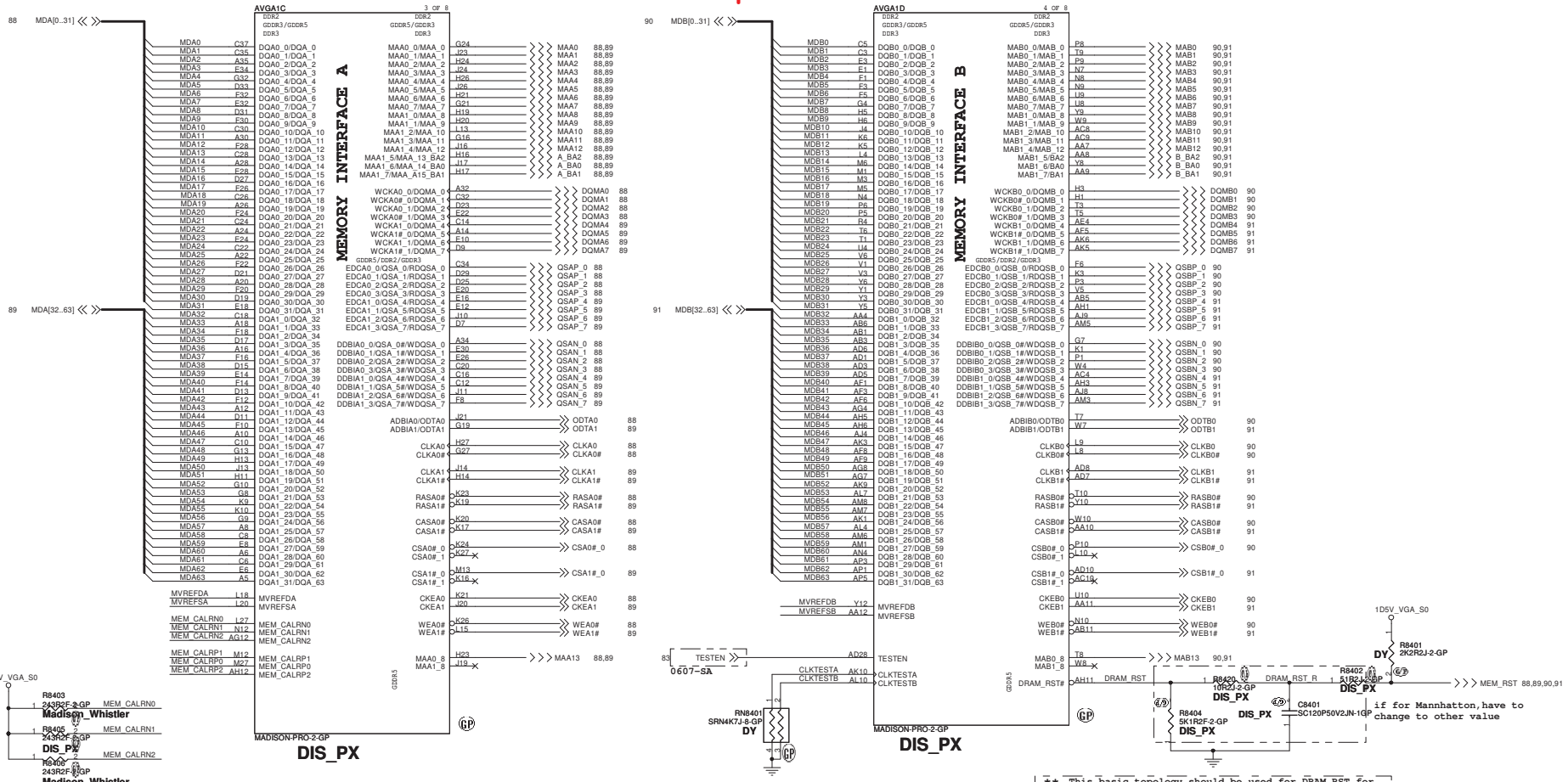
JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

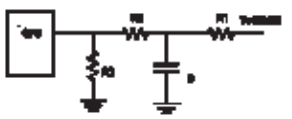
Title: GPU_PCIE/STRAPPING(1/5)
Size: Custom | Document Number: JE50_SB | Rev: SB
Date: Friday, April 01, 2011 | Sheet 83 of 102



PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Vancouver



C	R1	R2	R3
120 pF	51 Ω	10 Ω	5 kΩ

Mannhatton

C	R1	R2	R3	R4
68 pF	51 Ω	10 kΩ	0 Ω	DNI

DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_Memory(2/5)

Size: Custom | Document Number: JE50_SB | Rev: SB

Date: Friday, April 01, 2011 | Sheet 84 of 102

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request

Address	DVPDATA[3:0]	Vender	PN	Speed	
0	0 0 0 0	Hynix	H5TQ1G63DFR-11C	1Gb(64Mx16)	900Mhz	Rev D Die NEW
1	0 0 0 1	Hynix	H5TQ2G63BFR-11C	2Gb(128Mx16)	900Mhz	Rev B Die
2	0 0 1 0	Reserve			
3	0 0 1 1	Hynix	H5TQ1G63DFR-12C	1Gb(64Mx16)	800Mhz	Rev D Die NEW
4	0 1 0 0	Hynix	H5TQ1G63BFR-12C	1Gb(64Mx16)	800Mhz	Rev B Die
5	0 1 0 1	Reserve			
6	0 1 1 0	Reserve			
7	0 1 1 1	Hynix	H5TQ2G63BFR-11C	2Gb(128Mx16)	800Mhz	Rev B Die
8	1 0 0 0	Samsung	K4W1G1646E-HC12	1Gb(64Mx16)	800Mhz	Rev E Die
9	1 0 0 1	Samsung	K4W2G1646C-HC11	2Gb(128Mx16)	900Mhz	Rev C Die NEW
10	1 0 1 0	Reserve			
11	1 0 1 1	Samsung	K4W2G1646B-HC12	2Gb(128Mx16)	800Mhz	Rev B Die
12	1 1 0 0	Samsung	K4W1G1646G-BC11	1Gb(64Mx16)	900Mhz	Rev G Die NEW
13	1 1 0 1	Reserve			
14	1 1 1 0	ATI	23EY4187MA11	2GB(128M*16)	900Mhz	NEW
15	1 1 1 1	Samsung	K4W1G1646G-BC12	1Gb(64Mx16)	800Mhz	Rev G Die NEW

Apollo use Hynix D die 1GB 900MHz

LVDS Interface

I2C Bus for LVDS

Straps

For new version no 27M

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

DDC1/DDC2/DDC6 have 5V-tolerant

DDC1 channel for CRT

DDC2 channel for HDMI

AUXP PD 100K
AUXN PU 100K
Draw on EDP circuit page

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

0719 -SA
1022-SA
Use same parts for VGA DPPower
1022-SA
TM Derek Hsieh suggestion

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: JE50_SB | Rev: SB

Date: Friday, April 01, 2011 | Sheet 85 of 102

For DDR3/GDDR5, MVDDQ = 1.5V

(1.8V@504mA PCIE_VDDR)

(1.0V@1920mA PCIE_VDDC)

(1.8V@110mA VDD_CT)

55mA in BACO mode

110217 SB Add for DIS only

110217 SB BOM change

VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator

(1.8V@40mA PCIE_PVDD)

(120mA SPV10)

(For M97, Broadway, Madison and Park SPV10 = 1.0V)

(1.8V@75mA SPV18)

(M97, Broadway and Madison: 1.8V@150mA MPV18)

(Park: 1.8V@75mA MPV18)

PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

110218 SB change to short pad

ESD Proceted:2KV

have to use
Vgs(th):0.7~1.5 V
low Rds(on)

Vgs(th):1~1.8 V

MADISON-PRO-2-GP

DIS_PX

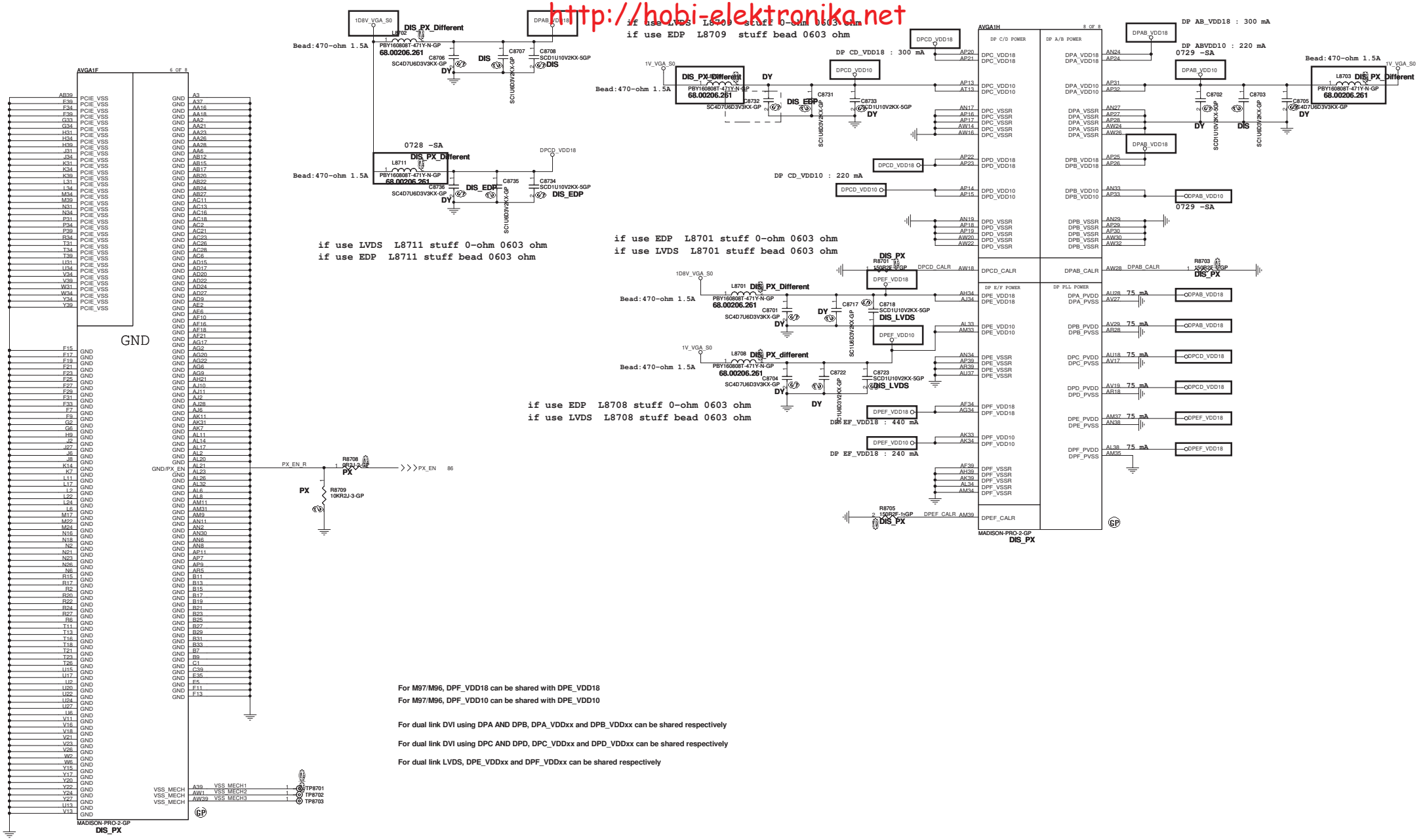
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size: A2 | Document Number: JE50_SB | Rev: SB

Date: Friday, April 01, 2011 | Sheet 86 of 102



For M97/M96, DPF_VDD18 can be shared with DPE_VDD18
For M97/M96, DPF_VDD10 can be shared with DPE_VDD10

For dual link DVI using DPA AND DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively

For dual link DVI using DPC AND DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively

For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively

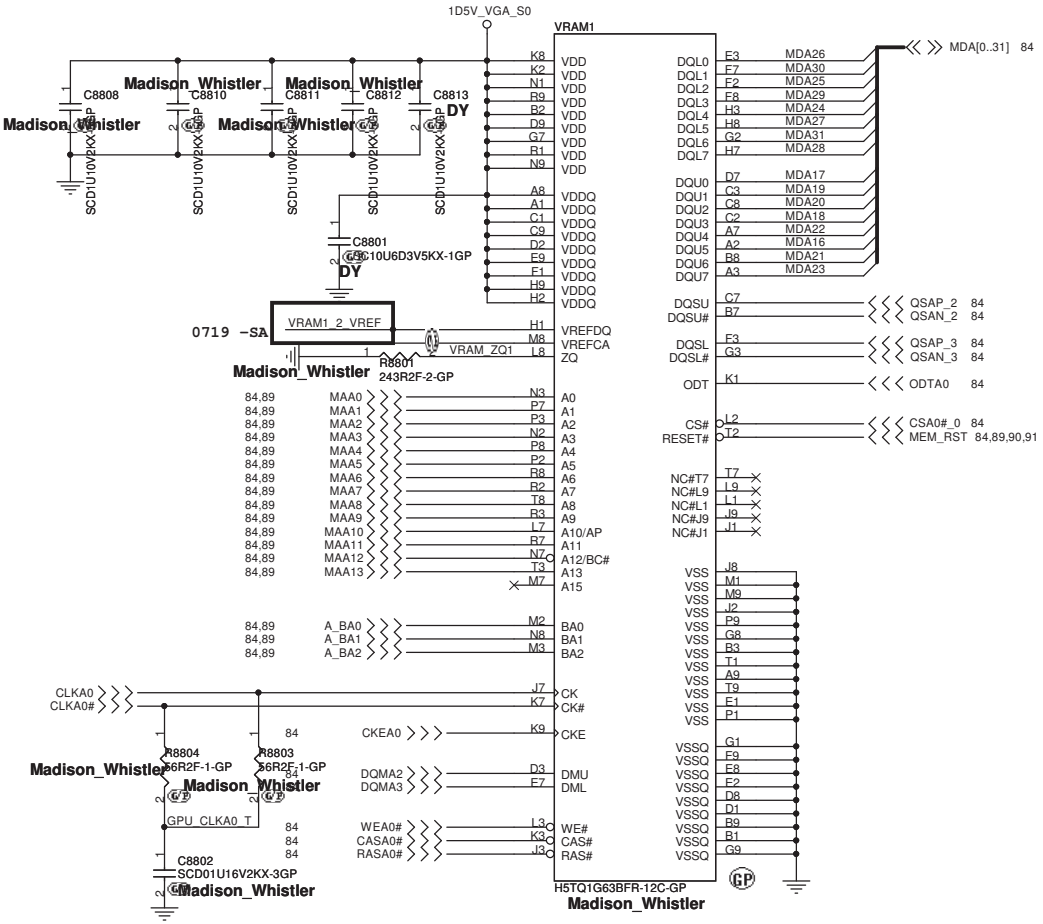
<Variant Name>

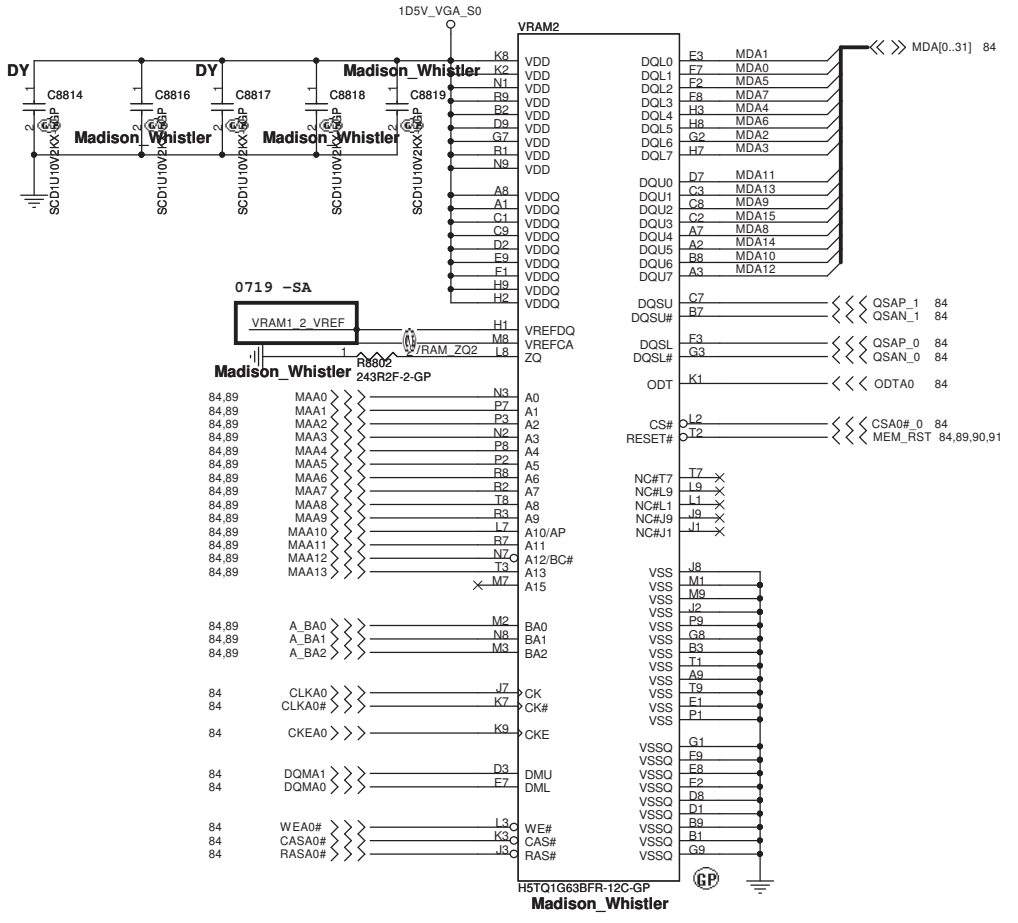
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

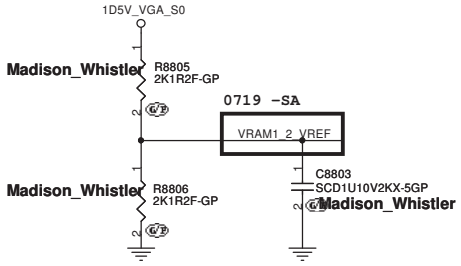
Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
A2	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 87 of 102

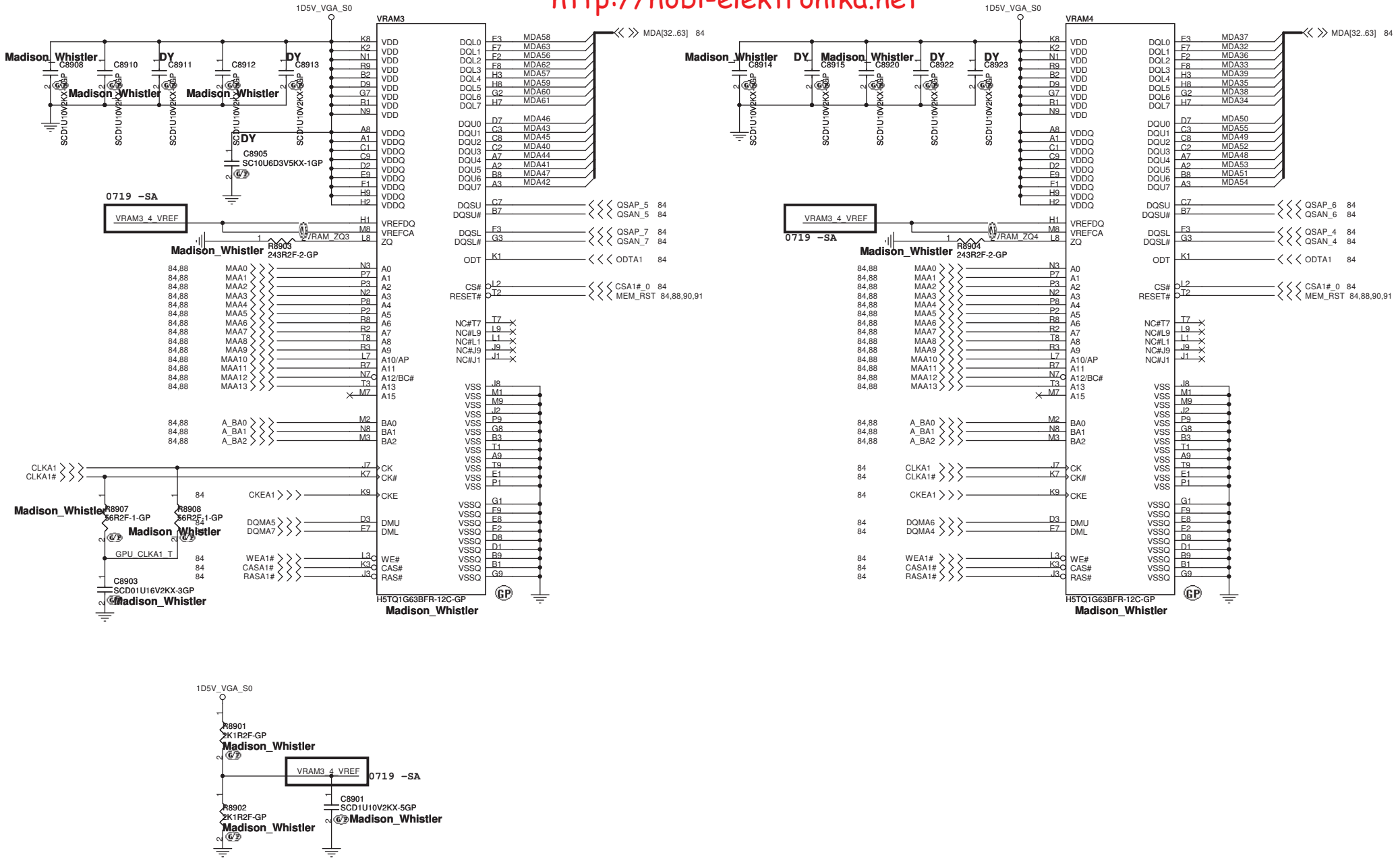






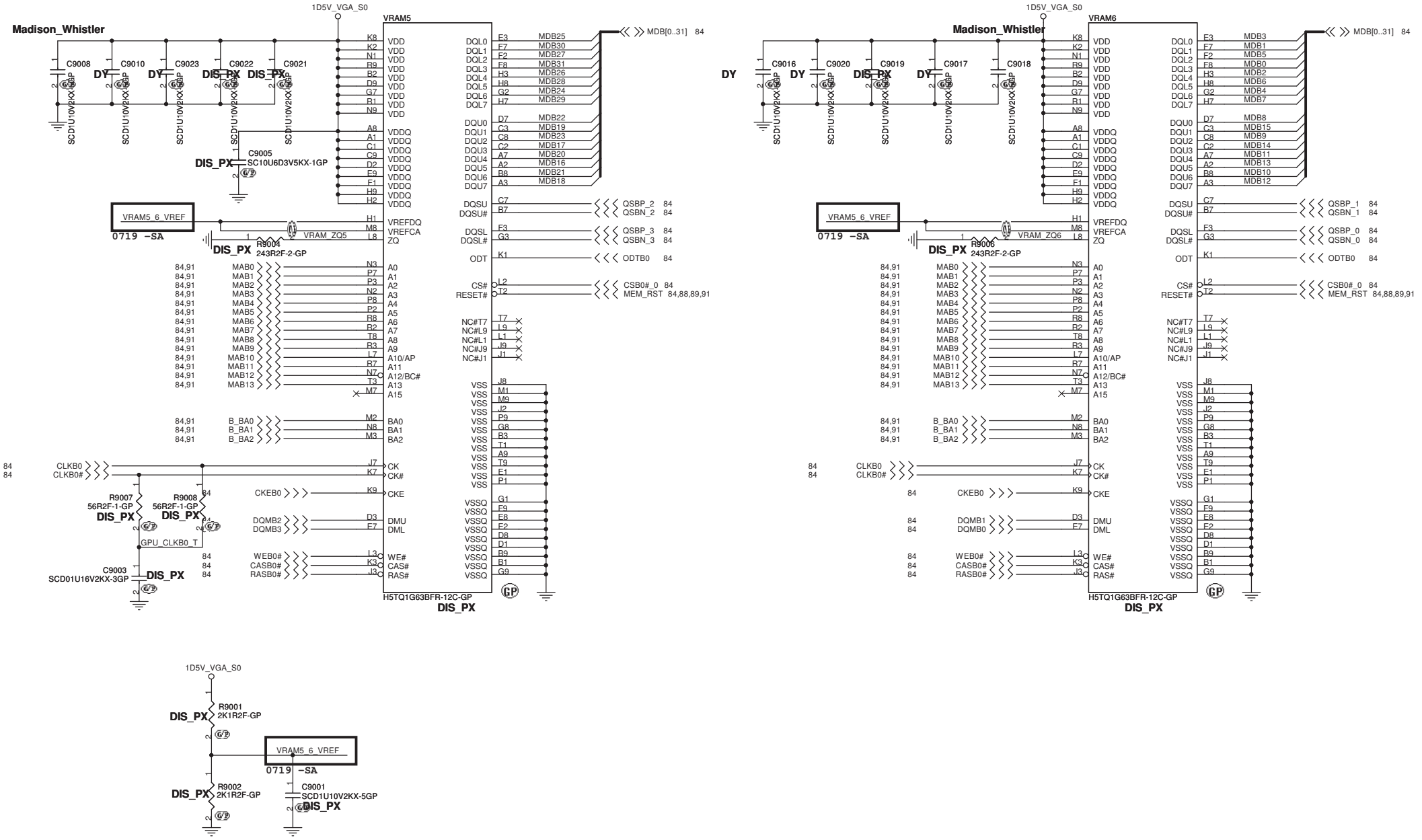
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU-VRAM1,2 (1/4)***
Size A3 / Document Number	**JE50_SB** / Rev **SB**
Date: Friday, April 01, 2011	Sheet 88 of 102



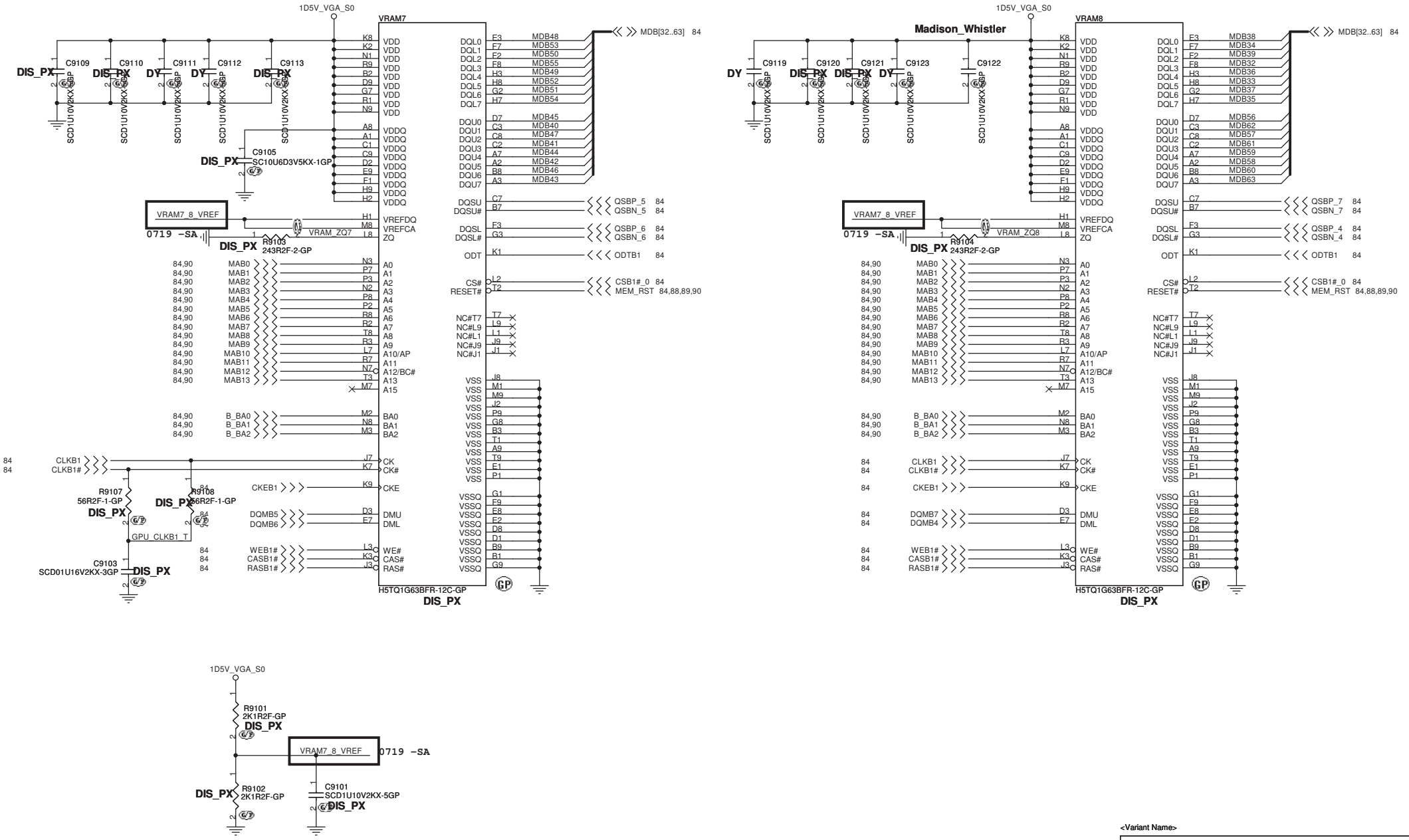
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU-VRAM3,4 (2/4)***
Size A3	Document Number **JE50_SB** Rev **SB**
Date: Friday, April 01, 2011	Sheet 89 of 102



<Variant Name>

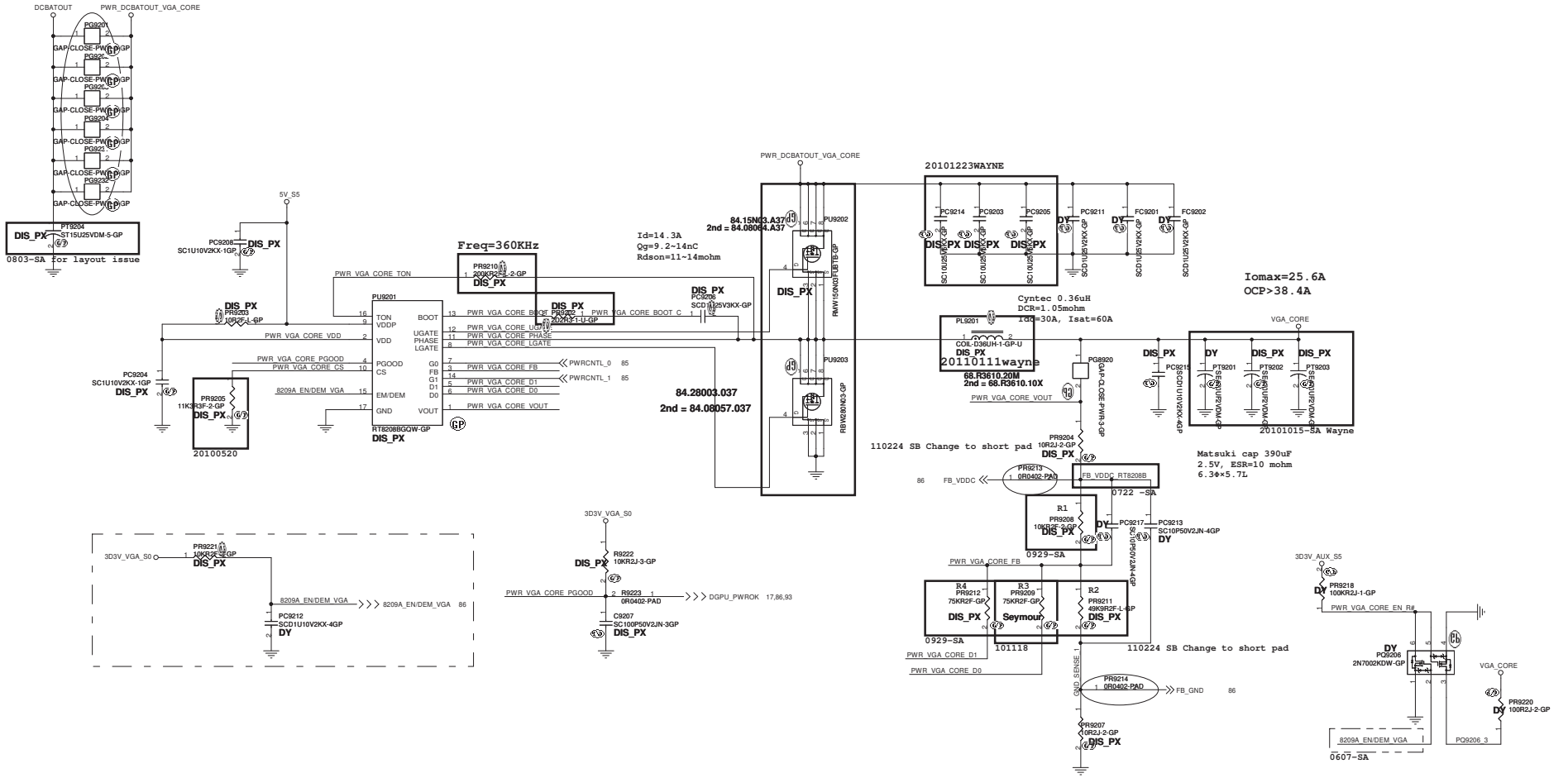
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU-VRAM5,6 (3/4)***
Size A3	Document Number **JE50_SB** Rev **SB**
Date: Friday, April 01, 2011	Sheet 90 of 102



<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU-VRAM7,8 (4/4)		
Size: A3	Document Number: JE50_SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 91 of 102	

110221 SB Change to short pad



PWR_VGA_CORE_D0	PWR_VGA_CORE_D1	Level	Whistler Pro	
H	L	High	1V	
H	L	Medium	1V	Vout = 0.75V * [1+R1/(R2//R4)]
H	H	Low	0.9V	Vout = 0.75V * (1+R1//R2)

PWR_VGA_CORE_D0	PWR_VGA_CORE_D1	Level	Seymour XT	
L	L	High	1.1V	Vout = 0.75V * [1+R1/(R2//R3//R4)]
L	H			
H	L	Medium	1V	Vout = 0.75V * [1+R1/(R2//R4)]
H	H	Low	0.9V	Vout = 0.75V * (1+R1//R2)

Field side feedback 3D mark,D2D low % error
Increase voltage to 1.15V for suffer weak VGA

1008-SA

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8208B +VGA_CORE		
Size: A2	Document Number: JE50_SB	Rev: SB
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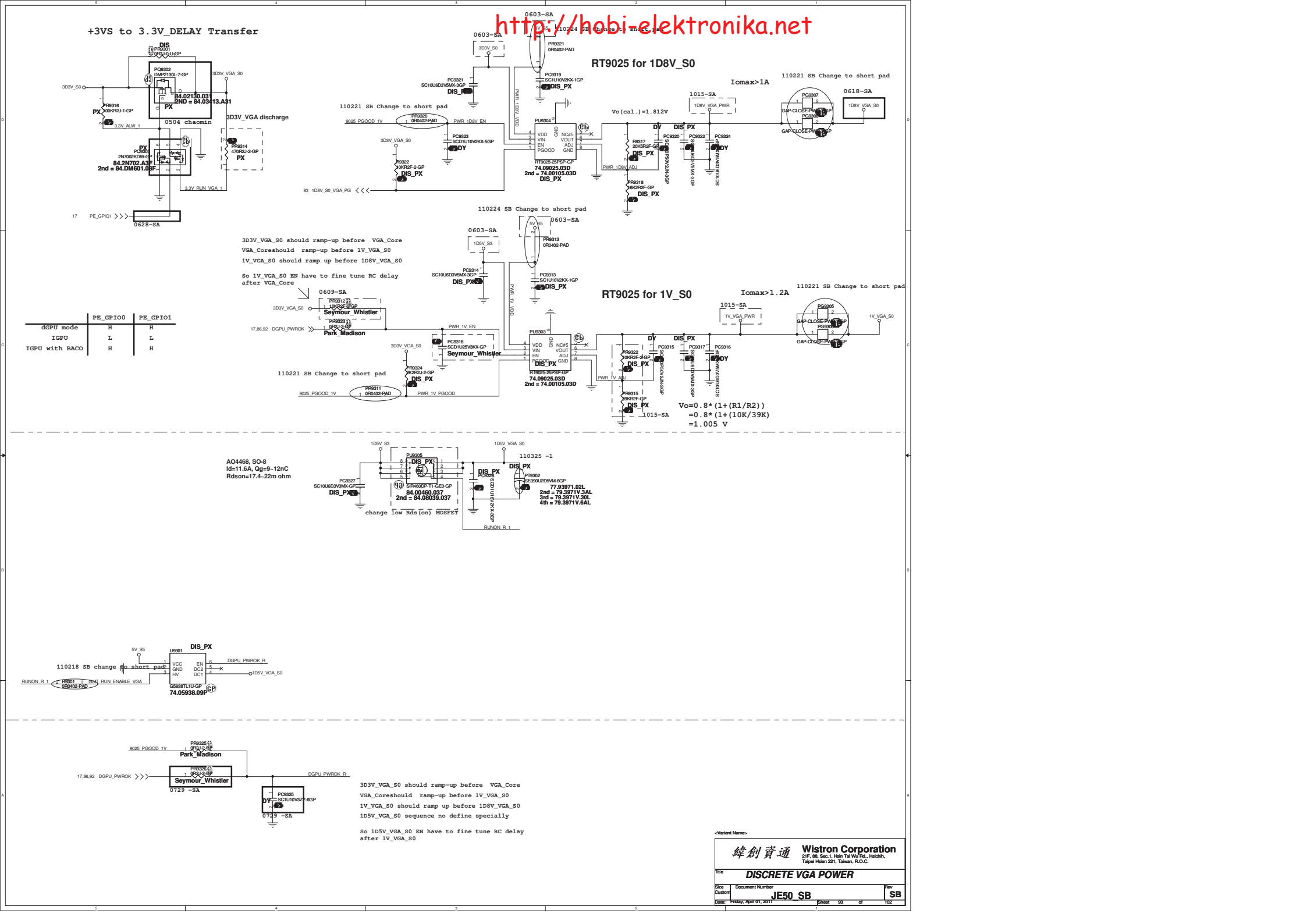

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size	Document Number	Rev
Custom	JE50_SB	SB

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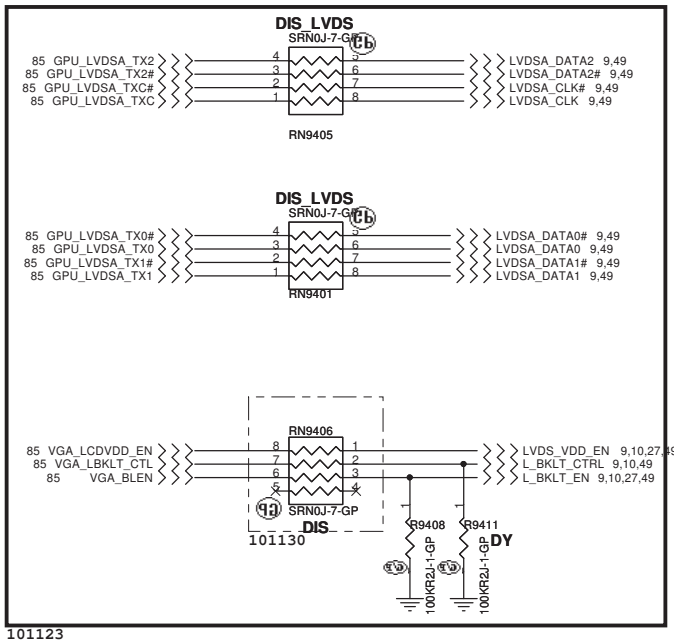
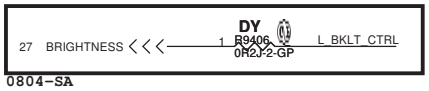
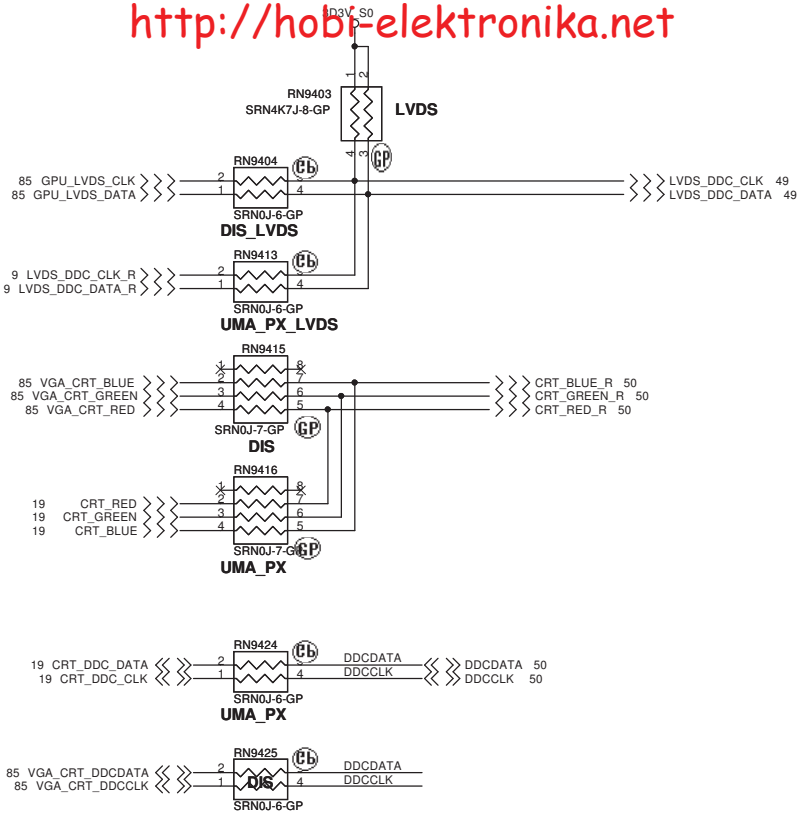
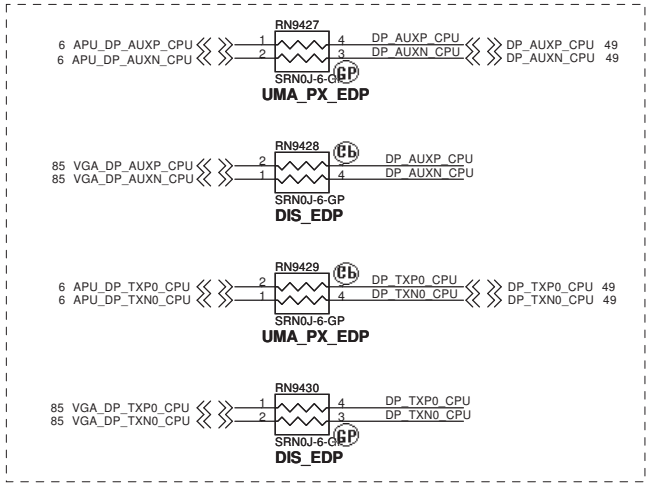


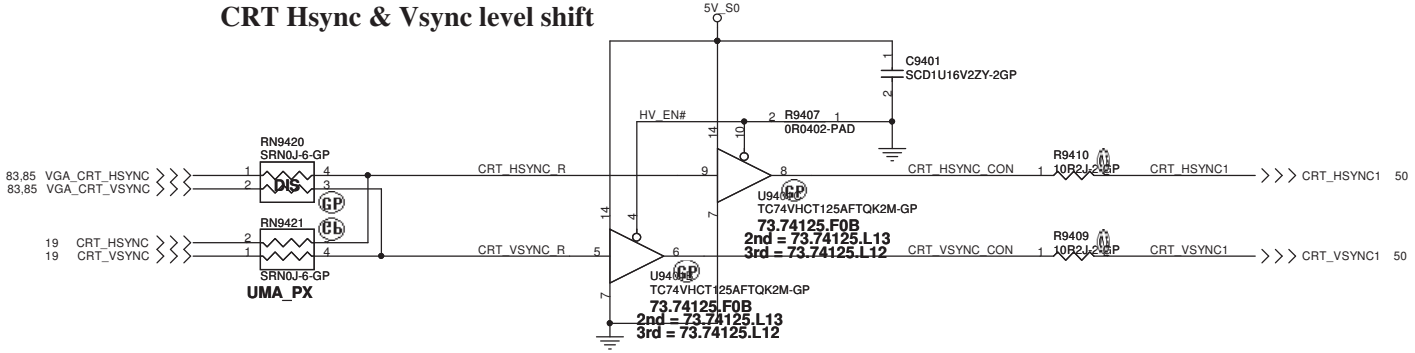






if Co-layout LVDS and EDP panel,
have to place Res near LVDS Cap
for Reflection Prevent

CRT Hsync & Vsync level shift



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LVDS_Switch***
Size: A3	Document Number: **JE50_SB**
Rev	**SB**
Date: Friday, April 01, 2011	Sheet 94 of 102

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<Variant Name>

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Title

Reserved

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(Blanking)

<Variant Name>

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Title: ***Reserved***

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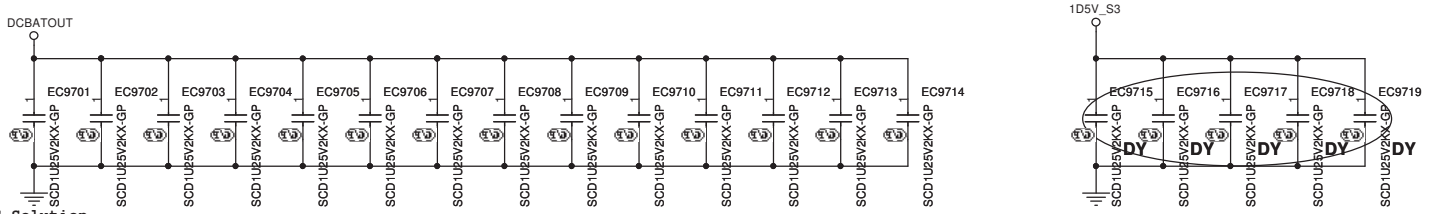
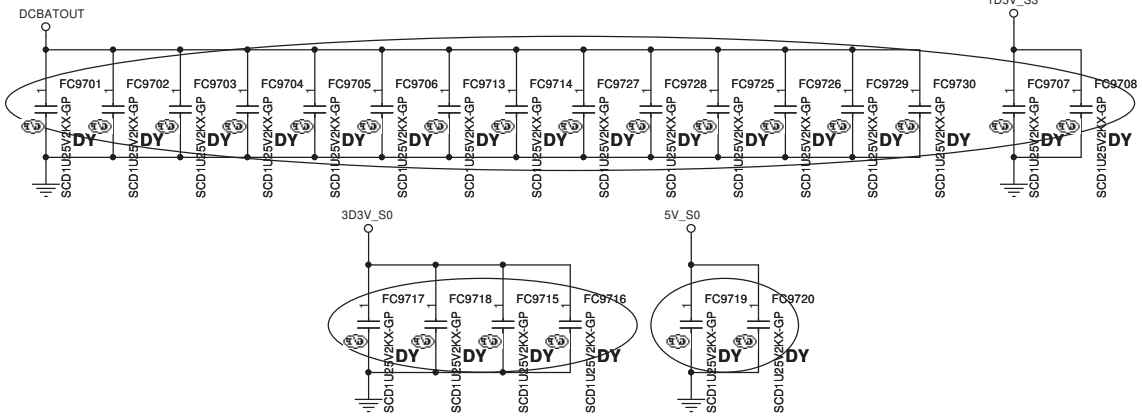
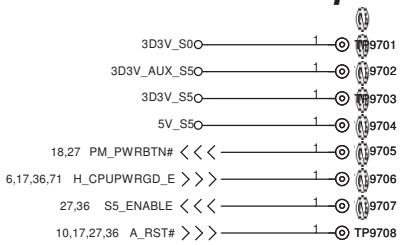
110223 SB RF Solution



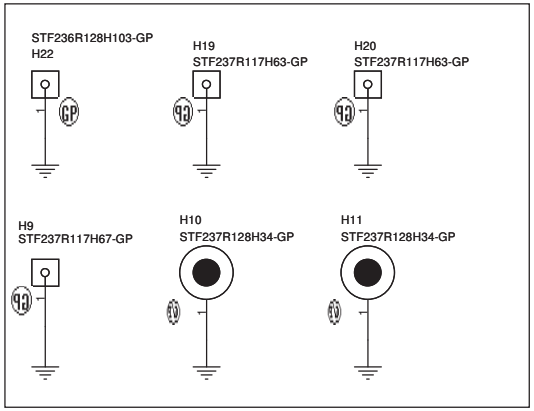
110218 SB RF Solution



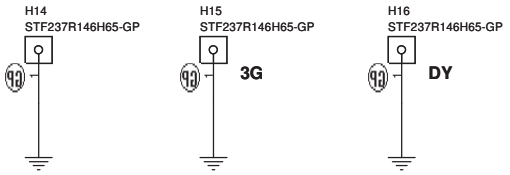
Check test point



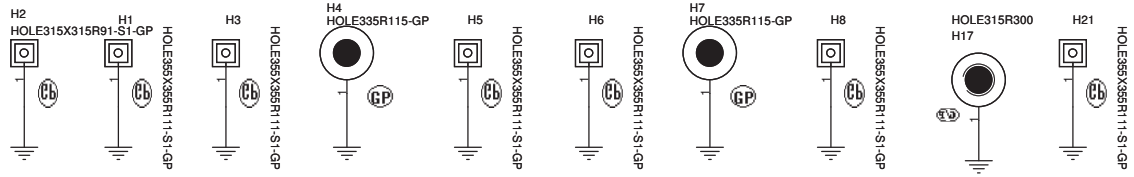
Test Point放在Dimm Door打開可量測處



SYSTEM THERMAL



WLAN WWAN



<Core Design>

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Title: ***UNUSED PARTS/CAP***

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Modify list

65 W: PR4007 -> 187K(64.18735.6DL)
90 W: PR4007 -> 121K (64.12135.6DL)

UMA and PX R5114 ~ R5121   -> 604-ohm (64.60405.6DL)
Diserete -> R5114 ~ R5121-> 499-ohm(64.49905.6DL)

R8332 stuff 1K   for Mannhatton VGA
      stuff 5.1K(64.51015.6DL) for Vancouver VGA

if use LVDS L8711,L8709 stuff 0-ohm 0603
if use LVDS L8701,L8708 stuff bead 0603

if use EDP L8711,L8709 stuff bead 0603 ohm
if use EDP L8701,L8708 stuff 0-ohm 0603

<Core Design>

緯創資通 Wistron Corporation
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Title: Change History

Size: A4 | Document Number: JE50_SB | Rev: SB

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POWER SEQUENCE

<Core Design>

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Title: POWER SEQUENCE

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<Core Design>

緯創資通 **Wistron Corporation**

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Title: ***Power Block Diagram***

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<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***SMBUS BLOCK DIAGRAM***

Size	Document Number	Rev
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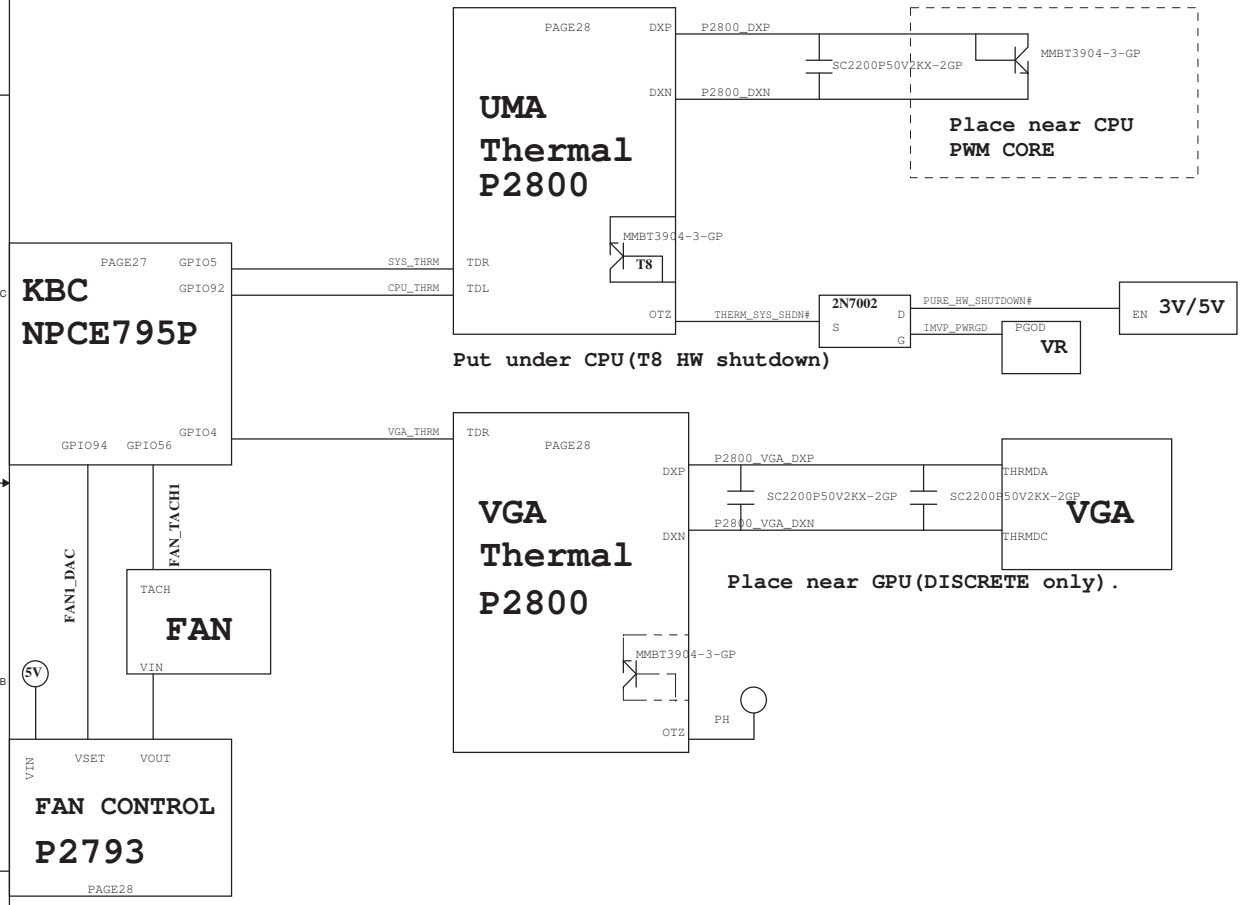
Thermal Block Diagram



Audio Block Diagram

<Core Design>

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Title	THERMAL/AUDIO BLOCK DIAGRAM	
Size: Custom	Document Number: JE50 SB	Rev: SB
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