1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2010-08-05

SCHEM,FLYING_CLOUD,MLB,K90i

"EVT3" 11/22/10

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8658	1	SCHEM,MLB,K90i	SCH	CRITICAL	
820-2936	1	PCBF,MLB,K90i	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Nov 22 19:21:11 2010

DRAWING TITLE: SCHEM,FLYING CLOUD,MLB,K90i

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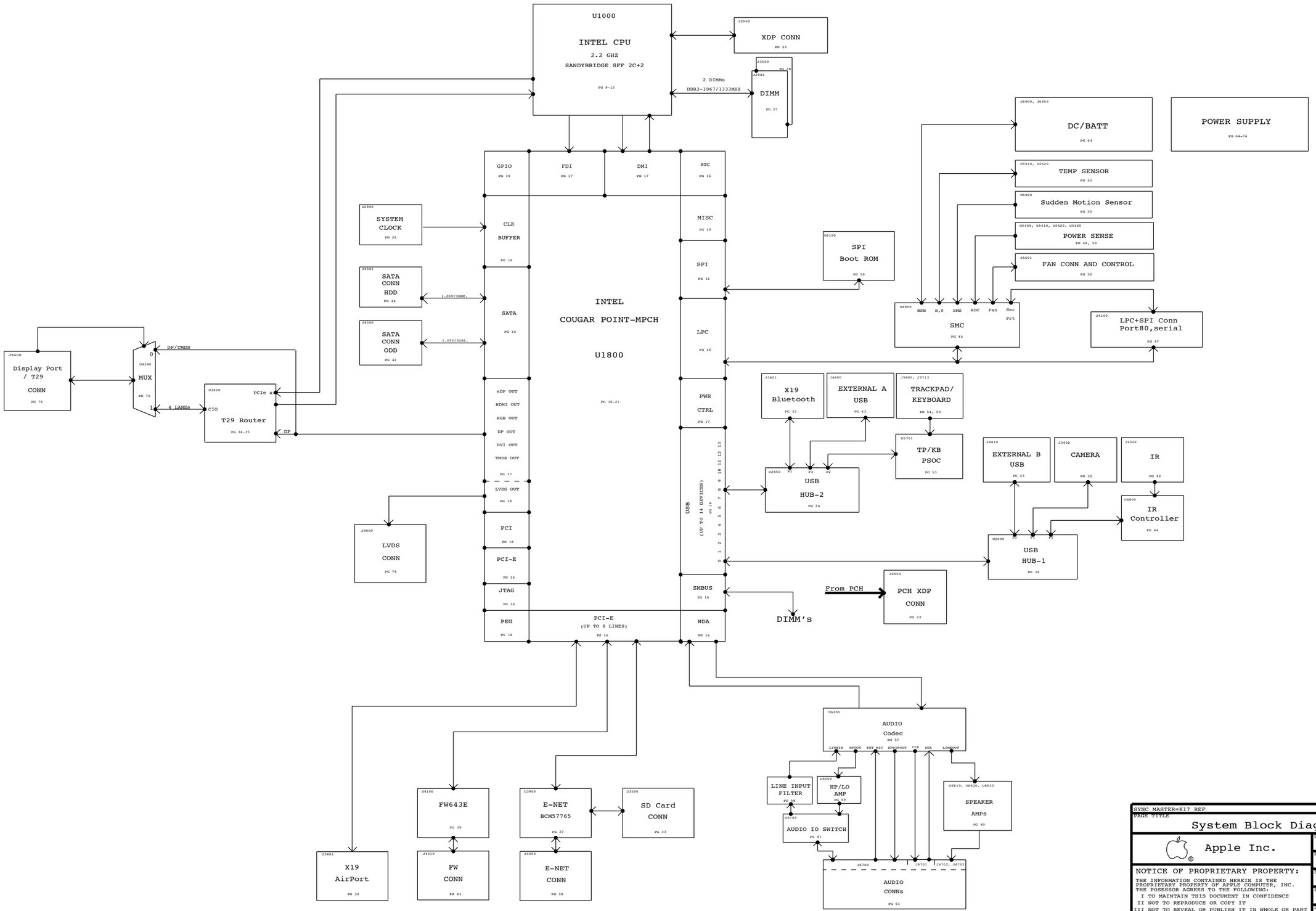

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SYNC DATE=06/30/2009

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System Block Diagram

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K9OI POWER SYSTEM ARCHITECTURE

J6900 AC ADAPTER IN
DCIN(16.5V)
F6905 6A FUSE
R7020 A
SMC_DCIN_ISENSE
U7000 ISL6259HRTZ PBUS SUPPLY/ BATTERY CHARGER (PAGE 64)
SMC_RESET_L
PPVBAT_G3H
F7040
PPBUS_G3H
R7050 A
SMC_BATT_ISENSE
J6950 3S2P (9 TO 12.6V)
PPVBATT_G3H_CONN
Q7055
CHGR_BGATE
PPVBAT_G3H_CHGR_R
PPDCIN_G3H
R6990
PPDCIN_S5_P3V42G3H
D6990
SMC_PBUS_VSENSE
R5400 A
SMC_CPU_HI_ISENSE
ENABLE 3.425V G3HOT PM6640 U6990 (PAGE 63)
PP3V42_G3H
SMC PWRGD SN0903048 U5010 (PAGE 44)
SMC_RESET_L
PP5V_S0_CPUVCCIOS0
CPUVCCIOS0_EN
1.05V ISL95870 U7600 (PAGE 70)
CPUVCCIOS0_PGOOD
R7640 A
PPCPUVCCIO_S0
SMC_CPU_FSB_ISENSE
TPS22924 U4202 (PAGE 38)
PP1V0_FW_FWPHY
FW_PWR_EN
SMC_CPU_VSENSE
CPU VCORE ISL95231 U7400 (PAGE 68)
CPUIMVP7_VR_ON
SMC_CPU_ISENSE
PPVCORE_S0_CPU
SMC_GFX_VSENSE
PPVCORE_S0_AXG
CPUIMVP_IMON
CPUIMVP_IMONG
CPUIMVP7_PGOOD
CPUIMVP7_AXG_PGOOD
DDRREG_EN
MEMVTT_EN
1.5V S5 / 0.75V S3 TPS51916 U7300 (PAGE 67)
PP1V5_S3
PP0V75_S0_DDRVTT
TP_DDRREG_PGOOD
PP5V_S0
PVCCSA_EN
ISL95870A U7100 (PAGE 65)
PPVCCSA_S0_CPU
PVCCSA_PGOOD
U2850
COUGAR-POINT (PCH) U1800 (PAGE 16~21)
PM_PCH_PWRGD
PM_PWRBTN_L
PM_SYSRST_L
PM_RSMRST_L
PLT_RERST_L
CPU_PWRGD
PM_MEM_PWRGD
CPU U1000 (PAGE 9~13)
SM_DRAMPWROK
UNCOREPWRGOOD
RESET*
SMC U4900
P60
SMC_PM_G2_EN
RC DELAY
P3V3S5_EN
(PAGE 44)
COUGAR-POINT (PCH) U1800 (PAGE 16~21)
SLP_S5#(E4)
SLP_S4#(H4)
SLP_S3#(F4)
PM_SLP_S5_L PG 17
PM_SLP_S4_L PG 17
PM_SLP_S3_L PG 17
P5VS3_EN PG71
DDRREG_EN PG71
P3V3S3_EN PG71
R7978 PG71
PM_SLP_S3_L_R PG71
P1V8S0_EN PG71
CPUVCCIOS0_EN PG71
P5VS0_EN
P3V3S0_EN
PBUSVSENS_EN
R5410 A
PPBUS_S5_HS_OTHER_ISNS
P5VS3_EN_L
P3V3S5_EN_L
VIN 5V (L/H) 3.3V (R/H) TPS51125 U7200 (PAGE 66)
PP5V_S3
PP3V3_S5
P5V3V3_PGOOD
Q7860
PP5V_S0
PM_SLP_S3_L_R
Q7922
PP3V3_ENET
BCM57765 U3900 CAESAR IV (PAGE 35)
PP1V2_ENET_PHY
PM_SLP_S3_L&&WOL_EN||SMC_ADAPTER_EN
TPS720105 U7740 (PAGE 71)
PP1V05_S5
F9700
Q9706
LCD_BKLT_EN
&& BKLT_PLT_RST_L
VIN LP8550 U9701 (PAGE 77)
PPBUS_SW_LCDBKLT_PWR
PPVOUT_SW_LCDBKLT
Q7810
PP3V3_S3
P3V3S3_EN
Q4260
F4260
PPVP_FW
PP3V3_S0 && FWPORT_PWR_EN
Q7830
PP3V3_S0
PM_SLP_S3_L_R
Q3880
T29_A_HV_EN
VIN LT3957 U3890 (PAGE 36)
PP24V_T29
P1V8_S0_EN
MAX15053EWL U7760 (PAGE 71)
PP1V8_S0
FW_PWR_EN
TPS22924 U4201 (PAGE 40)
PP3V3_FW_FWPHY
PP3V3_S5_PWRCTL
U7980
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
SMC U4900 (PAGE 43)
PWRGD(P12)
RSMRST_IN(P13)
PWR_BUTTON(P90)
RSMRST_OUT(P15)
99ms DLY
INVP_VR_ON(P16)
SYSRST(PA2)
P17(BTN_OUT)
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
RES*
CPUIMVP_VR_ON
CPUVCCIOS0_PGOOD
PVCCSA_PGOOD
P1V8S0_PGOOD
P5V3V3_PGOOD
S0PGOOD_PWROK
PP3V3_S5_VMON
Q7970 ASMCC0179 (PAGE 73)
PP3V3_S0
PP1V5_S3RS0
PP1V05_S0

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Revision History

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1294	PCBA,2.5G,K90i	K90i_COMMON,CPU_2_5GHZ,EEEE_DDRQ
639-1581	PCBA,2.7G,K90i	K90i_COMMON,CPU_2_7GHZ,EEEE_DH78
639-1698	PCBA,2.6G,K90i	K90i_COMMON,CPU_2_6GHZ,EEEE_DH8F
639-1699	PCBA,2.3G,K90i	K90i_COMMON,CPU_2_3GHZ,EEEE_DH8G
085-1998	K90i MLB DEVELOPMENT BOM	K90i_DEVEL:ENG

K90i BOM GROUPS

BOM GROUP	BOM OPTIONS
K90i_COMMON	ALTERNATE,COMMON,K90i_COMMON1,K90i_COMMON2,K90i_DEBUG:ENG,K90i_PROGPARTS,USBHUB_2513B,T29BST:Y
K90i_COMMON1	BATT_3S,CPUMEM_S0,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_3NONREM,T29:YES,DP_SDRV:A2,SDRV_PD,SDRVI2C:MCU
K90i_COMMON2	MIKEY,KB_BL
K90i_PROGPARTS	BOOTROM_PROG,SMC_PROG,TPAD_PROG,ENET_PROG,T29ROM:PROG,T29MCU:PROG
K90i_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,XDP_CPU:BPM,XDP_PCH,LPCPLUS,VREFMRGN,S0PGOOD_ISL,IMVPISNS_ENG
K90i_DEVEL:PVT	LPCPLUS,XDP_CONN,XDP_PCH
K90i_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K90i_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT
K90i_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT,LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3934	1	SNB,2C,QSXX,ES1,2.2,35W,R2,1M,GT1,BGA	U1000	CRITICAL	CPU_2_2GHZ
337S4058	1	SNB,Q1RA,QS,J1,2.5,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU_2_5GHZ
337S4057	1	SNB,Q1R3,QS,J1,2.7,35W,2+2,1.30,4M,BGA	U1000	CRITICAL	CPU_2_7GHZ
337S4024	1	SNB,Q1R9,QS,J1,2.3,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU_2_3GHZ
337S4064	1	SNB,Q1R7,QS,J1,2.6,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU_2_6GHZ
337S4029	1	IC,PCH,COUGARPOINT,SLH9D,PRQ,BD82HM65	U1800	CRITICAL	
343S0534	1	IC,BCM57765B0,ENET&SD,8X8	U3900	CRITICAL	
338S0753	1	IC,PM643-B2,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0921	1	IC,T29-C0,220 FCBGA,15x15MM	U3600	CRITICAL	T29:YES
353S3055	1	IC,PI3VEDP212,X2 DISPLAYPORT 2:1 MUX,QFN	U9390	CRITICAL	

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0663	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,8P,SOIC	U3990	CRITICAL	ENET_BLANK
341S3026	1	IC ENET,1!MBITFLAH,CIV REV01,K60/K62	U3990	CRITICAL	ENET_PROG
335S0777	1	IC,EEPROM,SERIAL,SPI,1Kx8,1.8V,MLP8,LF	U3690	CRITICAL	T29ROM:BLANK
341T0317	1	IC,T29 ASSY	U3690	CRITICAL	T29ROM:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2939	1	IC,PROGRMD,LPC1112A,T29 PORT MCU,HVQFN25	U9330	CRITICAL	T29MCU:PROG
338S0895	1	IC,SMC,HS8/2117/9MMx9MM,TLP	U4900	CRITICAL	SMC_BLANK
341T0300	1	IC,SMC,K90i	U4900	CRITICAL	SMC_PROG
335S0770	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
335S0769	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341T0299	1	IC,EFI ROM,K90i	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63803-LQXC	U4800	CRITICAL	
341S3024	1	IC,TP PSOC,K90,K90i,K91,K91F,K92	U5701	CRITICAL	TPAD_PROG

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1998	1	K90i MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DDRQ]	CRITICAL	EEEE_DDRQ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DH78]	CRITICAL	EEEE_DH78
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DH8F]	CRITICAL	EEEE_DH8F
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DH8G]	CRITICAL	EEEE_DH8G

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
516S0805	516S0806		ALL	Molex alt to Foxconn
128S0303	128S0282		ALL	Panasonic alt to Sanyo
138S0676	138S0691		ALL	Murata alt to Samsung
152S0778	152S0693		ALL	Cyntec alt to Vishay
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Rohm alt to Toshiba
376S0927	376S0966		ALL	Fairchild alt to Renesas
376S0927	376S0790		ALL	Fairchild alt to CICLON
376S0960	376S0801		ALL	Renesas alt to Renesas
376S0790	376S0928		ALL	CICLON alt to Fairchild
376S0928	376S0895		ALL	Fairchild alt to Renesas
376S0937	376S0845		ALL	Fairchild alt to Renesas
376S0777	376S0761		ALL	AON alt to Siliconix
376S0957	376S0958		ALL	Fairchild alt to Fairchild
376S0953	376S0958		ALL	Fairchild alt to Renesas
353S3085	353S1658		ALL	STMicro alt to LT

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BOM Configuration

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Functional Test Points

Fan Connectors

J11	TRUE	PP5V_S0	6 7 22 42 47 52 54 65 68 70 72 73 77
J10	TRUE	FAN_RT_PWM	52
J10	TRUE	FAN_RT_TACH	52

(NEED TO ADD 1 GND TP)

MIC FUNC_TEST

J530	TRUE	BI_MIC_LO	61 62
J530	TRUE	BI_MIC_HI	61 62
J530	TRUE	BI_MIC_SHIELD	61 62

(NEED TO ADD 1 GND TP)

SPEAKER FUNC_TEST

J223	TRUE	SPKRAMP_L_N_OUT	60 61 85
J224	TRUE	SPKRAMP_L_P_OUT	60 61 85
J225	TRUE	SPKRAMP_R_N_OUT	60 61 85
J230	TRUE	SPKRAMP_R_P_OUT	60 61 85
J229	TRUE	SPKRAMP_SUB_N_OUT	60 61 85
J231	TRUE	SPKRAMP_SUB_P_OUT	60 61 85

LVDS FUNC_TEST

J400	TRUE	PP3V3_LCDVDD_SW_F (NEED 2 TP)	6 74
J401	TRUE	PP3V3_S0_LCD_F	6 74
J402	TRUE	PPVOUT_SW_LCDBKLT (NEED 2 TP)	74 77
J403	TRUE	BKL_VSYNC	74 77
J404	TRUE	LVDS_DDC_CLK	8 18 74
J405	TRUE	LVDS_DDC_DATA	8 18 74
J406	TRUE	LVDS_IG_A_DATA_N<0>	18 74 80
J407	TRUE	LVDS_IG_A_DATA_P<0>	18 74 80
J408	TRUE	LVDS_IG_A_DATA_N<1>	18 74 80
J409	TRUE	LVDS_IG_A_DATA_P<1>	18 74 80
J410	TRUE	LVDS_IG_A_DATA_N<2>	18 74 80
J411	TRUE	LVDS_IG_A_DATA_P<2>	18 74 80
J412	TRUE	LVDS_CONN_A_CLK_F_N	74 85
J413	TRUE	LVDS_CONN_A_CLK_F_P	74 85
J414	TRUE	LED_RETURN_1	74 77
J415	TRUE	LED_RETURN_2	74 77
J416	TRUE	LED_RETURN_3	74 77
J417	TRUE	LED_RETURN_4	74 77
J418	TRUE	LED_RETURN_5	74 77
J419	TRUE	LED_RETURN_6	74 77

(NEED TO ADD 5 GND TP)

SATA ODD CONN

J240	TRUE	PP5V_SW_ODD (NEED 2 TP)	6 42
J241	TRUE	SMC_ODD_DETECT	42 45
J242	TRUE	SATA_ODD_D2R_UF_P	42 85
J243	TRUE	SATA_ODD_D2R_UF_N	42 85
J245	TRUE	SATA_ODD_R2D_P	42 80
J246	TRUE	SATA_ODD_R2D_N	42 80

(NEED TO ADD 3 GND TP)

SATA HDD/IR/SIL

J310	TRUE	PP5V_S0_HDD_FLT (NEED 2 TP)	6 42
J314	TRUE	SATA_HDD_R2D_P	42 80
J315	TRUE	SATA_HDD_R2D_N	42 80
J316	TRUE	SATA_HDD_D2R_C_P	42 80
J317	TRUE	SATA_HDD_D2R_C_N	42 80
J307	TRUE	SYS_LED_ANODE_R	42
J306	TRUE	IR_RX_OUT	42 44
J311	TRUE	PP5V_S3_IR_R	42

(NEED TO ADD 3 GND TP)

BATT POWER CONN

J320	TRUE	SMBUS_SMC_BSA_SCL	6 45 48 63 64 84
J321	TRUE	SMBUS_SMC_BSA_SDA	6 45 48 63 64 84
J325	TRUE	SYS_DETECT_L	63
J305	TRUE	PPVBAT_G3H_CONN (NEED 5 TP)	63 64

(NEED TO ADD 5 GND TP)

BIL CONN

J420	TRUE	PP3V42_G3H	6 7 26 43 45 46 47 48 53 63 64
J421	TRUE	SMBUS_SMC_BSA_SCL	6 45 48 63 64 84
J422	TRUE	SMBUS_SMC_BSA_SDA	6 45 48 63 64 84
J423	TRUE	SMC_BIL_BUTTON_L	45 46 63
J424	TRUE	SMC_LID_R	63

(NEED TO ADD 2 GND TP)

X19 CONN

J201	TRUE	PP3V3_WLAN (NEED 3 TP)	6 32 46
J202	TRUE	PCIE_AP_D2R_PI_P	32 81
J203	TRUE	PCIE_AP_D2R_PI_N	32 81
J204	TRUE	PCIE_AP_R2D_P	32 81
J205	TRUE	PCIE_AP_R2D_N	32 81
J206	TRUE	PCIE_CLK100M_AP_CONN_P	32 85
J207	TRUE	PCIE_CLK100M_AP_CONN_N	32 85
J208	TRUE	PP3V3_S3_BT_F	32
J209	TRUE	PCIE_WAKE_L	17 26 32
J210	TRUE	SMBUS_SMC_0_S0_SCL	32 45 48 51 84
J211	TRUE	SMBUS_SMC_0_S0_SDA	32 45 48 51 84
J212	TRUE	USB_BT_P	24 32 80
J213	TRUE	USB_BT_N	24 32 80
J214	TRUE	AP_CLKREQ_O_L	32
J215	TRUE	AP_RESET_CONN_L	32
J216	TRUE	AP_TEMP_SMB_SDA_R	32
J550	TRUE	AP_TEMP_SMB_SCL_R	32
J551	TRUE	WIFI_EVENT_L_R	32

(NEED TO ADD 5 GND TP)

IPD_FLEX_CONN

J370	TRUE	PP3V3_S5	76 85 6 7 8 17 19 20 22 23 24 26 30 24 30 46 56 66 72 73 74 76 85
J371	TRUE	PP18V5_S5	6 54
J372	TRUE	Z2_CS_L	53 54
J373	TRUE	Z2_DEBUG3	53 54
J374	TRUE	Z2_MOSI	53 54
J375	TRUE	Z2_MISO	53 54
J376	TRUE	Z2_SCLK	53 54
J377	TRUE	Z2_BOOST_EN	54
J378	TRUE	Z2_HOST_INTN	53 54
J379	TRUE	Z2_CLKIN	53 54
J380	TRUE	Z2_KEY_ACT_L	53 54
J381	TRUE	Z2_RESET	53 54
J382	TRUE	PSOC_MISO	53 54
J383	TRUE	PSOC_MOSI	53 54
J384	TRUE	PSOC_SCLK	53 54
J385	TRUE	SMBUS_SMC_A_S3_SDA	6 32 45 48 54 55 84
J386	TRUE	SMBUS_SMC_A_S3_SCL	6 32 45 48 54 55 84
J387	TRUE	PSOC_F_CS_L	53 54
J540	TRUE	PICKB_L	53 54

(NEED TO ADD 2 GND TP)

KEYBOARD CONN

J334	TRUE	PP3V3_S5	6 7 8 17 19 20 22 23 24 26 30 46 56 66 72 73 74 76 85
J335	TRUE	PP3V42_G3H	6 7 26 43 45 46 47 48 53 63 64 73
J344	TRUE	WS_KBD1	53
J345	TRUE	WS_KBD2	53
J346	TRUE	WS_KBD3	53
J347	TRUE	WS_KBD4	53
J348	TRUE	WS_KBD5	53
J349	TRUE	WS_KBD6	53
J350	TRUE	WS_KBD7	53
J351	TRUE	WS_KBD8	53
J352	TRUE	WS_KBD9	53
J353	TRUE	WS_KBD10	53
J354	TRUE	WS_KBD11	53
J355	TRUE	WS_KBD12	53
J356	TRUE	WS_KBD13	53
J357	TRUE	WS_KBD14	53
J358	TRUE	WS_KBD15_CAP	53
J359	TRUE	WS_KBD16_NUM	53
J360	TRUE	WS_KBD17	53
J361	TRUE	WS_KBD18	53
J362	TRUE	WS_KBD19	53
J363	TRUE	WS_KBD20	53
J364	TRUE	WS_KBD21	53
J365	TRUE	WS_KBD22	53
J366	TRUE	WS_KBD23	53
J367	TRUE	WS_KBD_ONOFF_L	53
J368	TRUE	WS_LEFT_SHIFT_KBD	53
J369	TRUE	WS_LEFT_OPTION_KBD	53
J333	TRUE	WS_CONTROL_KBD	53

(NEED TO ADD 2 GND TP)

KBD BACKLIGHT CONN

J356	TRUE	KBDLED_ANODE	54
J394	TRUE	SMC_KDBLED_PRESENT_L	54

(NEED TO ADD 1 GND TP)

CAMERA/ALS CONN

J400	TRUE	PP5V_S3_ALSCAMERA_F	32
J409	TRUE	SMBUS_SMC_A_S3_SCL	6 32 45 48 54 55 84
J410	TRUE	SMBUS_SMC_A_S3_SDA	6 32 45 48 54 55 84
J397	TRUE	USB_CAMERA_CONN_P	32 80
J396	TRUE	USB_CAMERA_CONN_N	32 80

(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

J185	TRUE	PPVCORE_S0_CPU	7 9 12 14 49
J186	TRUE	PPVCORE_S0_AXG	7 9 12 15 49 69
J414	TRUE	PP1V2_S3_ENET_INTREG	37 71
J188	TRUE	PP1V05_S0	45 48 70 73 7 9 10 12 14 16 17 20 22 23 36 40
J189	TRUE	PP1V5_S3RS0	7 10 12 15 30 72 73 85
J190	TRUE	PP1V8_S0	7 14 17 20 22 26 71
J191	TRUE	PP3V3_S0	29 33 36 37 40 48 6 7 8 12 16 17 50 18 19 20 22 23 26 27 51 52 54 57 61 65 74 75 77 85
J192	TRUE	PP5V_S0	7 8 18 24 26 30 31 32 33 48 50 54 55 72 73
J193	TRUE	PP3V3_S3	7 30 32 42 43 44 46 57 59 60 61 66 67 72
J194	TRUE	PP5V_S3	7 10 12 15 65
J410	TRUE	PPVCCSA_S0_CPU	16 6
J195	TRUE	PP3V3_S5	16 6
J196	TRUE	PP3V42_G3H	47 48 53 63 64 6 7 26 43 45 46 16 6
J197	TRUE	PPBUS_G3H	7 8 36 40 49 50 63 64 77
J411	TRUE	PP3V3_ENET	7 26 37 71 73
J192	TRUE	PP3V3_WLAN	6 32 46
J193	TRUE	PP5V_SW_ODD	6 42
J198	TRUE	PP5V_S0_HDD_FLT	6 42
J199	TRUE	PP18V5_S5	6 54
J418	TRUE	PP3V3_S0_LCD_F	6 74
J419	TRUE	PP3V3_LCDVDD_SW_F	6 74
J200	TRUE	PP4V5_AUDIO_ANALOG	57
J410	TRUE	PP1V5_S3	7 27 29 30 67 72
J201	TRUE	SMC_PM_G2_EN	45 73
J545	TRUE	PM_SLP_S4_L	17 30 45 73
J202	TRUE	PM_SLP_S3_L	17 30 45 73

(NEED TO ADD 6 GND TP)

DC POWER CONN

(NEED 3 TP)

J312	TRUE	PP18V5_DCIN_FUSE	63
J304	TRUE	ADAPTER_SENSE	63

(NEED TO ADD 4 GND TP)

LPC+SPI DEBUG_CONN

J530	TRUE	LPC_AD<0>	16 45 47 81
J531	TRUE	LPC_AD<1>	16 45 47 81
J532	TRUE	LPC_AD<2>	16 45 47 81
J533	TRUE	LPC_AD<3>	16 45 47 81
J600	TRUE	LPC_CLK33M_LPCPLUS	26 47 81
J601	TRUE	LPC_FRAME_L	16 45 47 81
J602	TRUE	LPC_PWRDWN_L	17 45 47
J603	TRUE	LPC_SERIRQ	16 45 47
J604	TRUE	LPCPLUS_GPIO	19 47
J605	TRUE	LPCPLUS_RESET_L	26 47 81
J606	TRUE	PM_CLKRUN_L	17 45 47
J607	TRUE	PP3V42_G3H	6 7 26 43 45 46 47 48 53 63 64 73
J608	TRUE	PP5V_S0	6 7 22 42 47 52 54 65 68 70 72 73 77
J609	TRUE	SMC_MD1	45 47
J610	TRUE	SMC_RX_L	43 45 46 47
J611	TRUE	SMC_TCK	45 46 47
J612	TRUE	SMC_TDI	45 46 47
J613	TRUE	SMC_TDO	45 46 47
J614	TRUE	SMC_TMS	45 46 47
J615	TRUE	SMC_TRST_L	45 47
J616	TRUE	SMC_TX_L	43 45 46 47
J617	TRUE	SPI_ALT_CLK	47
J618	TRUE	SPI_ALT_CS_L	47
J619	TRUE	SPI_ALT_MISO	47
J620	TRUE	SPI_ALT_MOSI	47
J621	TRUE	SPIROM_USE_MLB	19 47 56

(NEED TO ADD 2 GND TP)

NC NO_TESTs

NO_TEST

17 6	NC_CRT_IG_BLUE	TRUE MAKE_BASE=TRUE	NC_CRT_IG_BLUE	6 17
17 6	NC_CRT_IG_GREEN	TRUE MAKE_BASE=TRUE	NC_CRT_IG_GREEN	6 17
17 6	NC_CRT_IG_RED	TRUE MAKE_BASE=TRUE	NC_CRT_IG_RED	6 17
17 6	NC_CRT_IG_DDC_CLK	TRUE MAKE_BASE=TRUE	NC_CRT_IG_DDC_CLK	6 17
17 6	NC_CRT_IG_DDC_DATA	TRUE MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA	6 17
17 6	NC_CRT_IG_HSYNC	TRUE MAKE_BASE=TRUE	NC_CRT_IG_HSYNC	6 17
17 6	NC_CRT_IG_VSYNC	TRUE MAKE_BASE=TRUE	NC_CRT_IG_VSYNC	6 17
	NC_LVDS_IG_CTRL_CLK	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_CLK	6 18
	NC_LVDS_IG_CTRL_DATA	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA	6 18
	NC_PCH_LVDS_VBG	TRUE MAKE_BASE=TRUE	NC_PCH_LVDS_VBG	6 18
	NC_HDA_SDIN1	TRUE MAKE_BASE=TRUE	NC_HDA_SDIN1	6 16
	NC_HDA_SDIN2	TRUE MAKE_BASE=TRUE	NC_HDA_SDIN2	6 16
	NC_HDA_SDIN3	TRUE MAKE_BASE=TRUE	NC_HDA_SDIN3	6 16
18 6	NC_PCI_PME_L	TRUE MAKE_BASE=TRUE	NC_PCI_PME_L	6 18
18 6	NC_PCI_CLK33M_OUT3	TRUE MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3	6 18
16 6	NC_CLINK_CLK	TRUE MAKE_BASE=TRUE	NC_CLINK_CLK	6 16
16 6	NC_CLINK_DATA	TRUE MAKE_BASE=TRUE	NC_CLINK_DATA	6 16
16 6	NC_CLINK_RESET_L	TRUE MAKE_BASE=TRUE	NC_CLINK_RESET_L	6 16
16 6	NC_PCIE_CLK100M_PEBN	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBN	6 16
16 6	NC_PCIE_CLK100M_PEBP	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP	6 16
39 6	NC_FW643_SDA	TRUE MAKE_BASE=TRUE	NC_FW643_SDA	6 39
39 6	NC_FW643_SM	TRUE MAKE_BASE=TRUE	NC_FW643_SM	6 39
39 6	NC_FW643_TCK	TRUE MAKE_BASE=TRUE	NC_FW643_TCK	6 39
39 6	NC_FW643_TMS	TRUE MAKE_BASE=TRUE	NC_FW643_TMS	6 39
39 6	NC_FW643_FW620_L	TRUE MAKE_BASE=TRUE	NC_FW643_FW620_L	6 39
39 6	NC_FW643_VBUF	TRUE MAKE_BASE=TRUE	NC_FW643_VBUF	6 39
39 6	NC_FW643_OCR10_CTL	TRUE MAKE_BASE=TRUE	NC_FW643_OCR10_CTL	6 39
39 6	NC_FW643_AVREG	TRUE MAKE_BASE=TRUE	NC_FW643_AVREG	6 39
39 6	NC_FW643_TDI	TRUE MAKE_BASE=TRUE	NC_FW643_TDI	6 39
	TP_XDP_PCH_OBSFN_A<0..1>	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>	23 6
	TP_XDP_PCH_OBSFN_B<0..1>	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>	23 6
23 6	NC_TP_XDPPCH_HOOK2	TRUE MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK2	6 23
23 6	NC_TP_XDPPCH_HOOK3	TRUE MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK3	6 23
	TP_XDP_PCH_OBSFN_D<0..1>	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1>	23 6
23 6	NC_TP_XDP_PCH_HOOK4	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK4	6 23
23 6	NC_TP_XDP_PCH_HOOK5	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK5	6 23
16 6	NC_PCH_GPIO64_CLKOUTFLEX0	TRUE MAKE_BASE=TRUE	NC_PCH_GPIO64_CLKOUTFLEX0	6 16
16 6	NC_PCH_GPIO65_CLKOUTFLEX1	TRUE MAKE_BASE=TRUE	NC_PCH_GPIO65_CLKOUTFLEX1	6 16
16 6	NC_PCH_GPIO66_CLKOUTFLEX2	TRUE MAKE_BASE=TRUE	NC_PCH_GPIO66_CLKOUTFLEX2	6 16
16 6	NC_PCH_GPIO67_CLKOUTFLEX3	TRUE MAKE_BASE=TRUE	NC_PCH_GPIO67_CLKOUTFLEX3	6 16

NC NO_TESTs

NO_TEST

R600	TRUE	NC_FW2_TPBP	39 41
R599	TRUE	NC_FW2_TPBN	39 41
R598	TRUE	NC_FW2_TPBIAS	39 41
R597	TRUE	NC_FW2_TPAP	39 41
R595	TRUE	NC_FW2_TPAN	39 41
R596	TRUE	NC_FW0_TPBP	39 41 82
R594	TRUE	NC_FW0_TPBN	39 41 82
R593	TRUE	NC_FW0_TPAP	39 41 82
R492	TRUE	XDP_PCH_AP_PWR_EN	
R493	TRUE	XDP_PCH_USB_HUB_SOFT_RST_L	23
R494	TRUE	XDP_PCH_SDCONN_STATE_RST_L	23
R495	TRUE	XDP_PCH_ENET_PWR_EN	23
R496	TRUE	XDP_PCH_SDCONN_DET_L	23
R497	TRUE	XDP_PCH_S5_PWRGD	23
R498	TRUE	XDP_PCH_PWRBTN_L	23
R585	TRUE	XDP_PCH_ISOLATE_CPU_MEM_L	23
R586	TRUE	XDP_FW_CLKREQ_L	23
R588	TRUE	XDP_AP_CLKREQ_L	23
R587	TRUE	XDP_PCH_AUD_IPHS_SWITCH_EN	23

17 6	NC_SDVO_TVCLKINN	TRUE MAKE_BASE=TRUE	NC_SDVO_TVCLKINN	6 17
17 6	NC_SDVO_TVCLKINP	TRUE MAKE_BASE=TRUE	NC_SDVO_TVCLKINP	6 17
17 6	NC_SDVO_STALLN	TRUE MAKE_BASE=TRUE	NC_SDVO_STALLN	6 17
17 6	NC_SDVO_STALLP	TRUE MAKE_BASE=TRUE	NC_SDVO_STALLP	6 17
17 6	NC_SDVO_INTN	TRUE MAKE_BASE=TRUE	NC_SDVO_INTN	6 17
17 6	NC_SDVO_INTP	TRUE MAKE_BASE=TRUE	NC_SDVO_INTP	6 17

9 6	NC_EDP_TXP<0..3>	TRUE MAKE_BASE=TRUE	TP_EDP_TX_P<0..3>	6 9
9 6	NC_EDP_TXN<0..3>	TRUE MAKE_BASE=TRUE	TP_EDP_TX_N<0..3>	6 9
9 6	NC_EDP_AUXP	TRUE MAKE_BASE=TRUE	NC_EDP_AUXP	6 9
9 6	NC_EDP_AUXN	TRUE MAKE_BASE=TRUE	NC_EDP_AUXN	6 9
6	NC_CPU_THERMDA	TRUE MAKE_BASE=TRUE	NC_CPU_THERMDA	6
6	NC_CPU_THERMDC	TRUE MAKE_BASE=TRUE	NC_CPU_THERMDC	6
	NC_CPU_RSVD<30..45>	TRUE MAKE_BASE=TRUE	TP_CPU_RSVD<30..45>	
	NC_CPU_RSVD<8..27>	TRUE MAKE_BASE=TRUE	TP_CPU_RSVD<8..27>	
	NC_PEG_R2D_CP<0..7>	TRUE MAKE_BASE=TRUE	=PEG_R2D_C_P<0..7>	9
	NC_PEG_R2D_CN<0..7>	TRUE MAKE_BASE=TRUE	=PEG_R2D_C_N<0..7>	9
	NC_PEG_D2RP<0..7>	TRUE MAKE_BASE=TRUE	=PEG_D2R_P<0..7>	9
	NC_PEG_D2RN<0..7>	TRUE MAKE_BASE=TRUE	=PEG_D2R_N<0..7>	9
	NC_PEG_R2D_CP<12..15>	TRUE MAKE_BASE=TRUE	=PEG_R2D_C_P<12..15>	
	NC_PEG_R2D_CN<12..15>	TRUE MAKE_BASE=TRUE	=PEG_R2D_C_N<12..15>	
9	NC_PEG_D2RP<12..15>	TRUE MAKE_BASE=TRUE	=PEG_D2R_P<12..15>	
9	NC_PEG_D2RN<12..15>	TRUE MAKE_BASE=TRUE	=PEG_D2R_N<12..15>	
6	NC_PCIE_CLK100M_PE4N	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4N	6
6	NC_PCIE_CLK100M_PE4P	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P	6
16 6	NC_PCIE_CLK100M_PE5N	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N	6 16
16 6	NC_PCIE_CLK100M_PE5P	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P	6 16
19 6	NC_PCIE_CLK100M_PE6N	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N	6 19
19 6	NC_PCIE_CLK100M_PE6P	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P	6 19
19 6	NC_PCIE_CLK100M_PE7N	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7N	6 19
19 6	NC_PCIE_CLK100M_PE7P	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7P	6 19
53 6	NC_PSOC_P1_3	TRUE MAKE_BASE=TRUE	NC_PSOC_P1_3	6 53
16 6	NC_SATA_B_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_B_D2RN	6 16
16 6	NC_SATA_B_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_B_D2RP	6 16
16 6	NC_SATA_B_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_B_R2D_CN	6 16
16 6	NC_SATA_B_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_B_R2D_CP	6 16
16 6	NC_SATA_D_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_D_D2RN	6 16
16 6	NC_SATA_D_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_D_D2RP	6 16
16 6	NC_SATA_D_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_D_R2D_CN	6 16
16 6	NC_SATA_D_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_D_R2D_CP	6 16
16 6	NC_SATA_E_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_E_D2RN	6 16
16 6	NC_SATA_E_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_E_D2RP	6 16
16 6	NC_SATA_E_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_E_R2D_CN	6 16
16 6	NC_SATA_E_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_E_R2D_CP	6 16
16 6	NC_SATA_F_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_F_D2RN	6 16
16 6	NC_SATA_F_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_F_D2RP	6 16
16 6	NC_SATA_F_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_F_R2D_CN	6 16
16 6	NC_SATA_F_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_F_R2D_CP	6 16
6	NC_PCH_TP18	TRUE MAKE_BASE=TRUE	NC_PCH_TP18	6
6	NC_PCH_TP17	TRUE MAKE_BASE=TRUE	NC_PCH_TP17	6
6	NC_PCH_TP16	TRUE MAKE_BASE=TRUE	NC_PCH_TP16	6
6	NC_PCH_TP15	TRUE MAKE_BASE=TRUE	NC_PCH_TP15	6
6	NC_PCH_TP14	TRUE MAKE_BASE=TRUE	NC_PCH_TP14	6
6	NC_PCH_TP13	TRUE MAKE_BASE=TRUE	NC_PCH_TP13	6
6	NC_PCH_TP12	TRUE MAKE_BASE=TRUE	NC_PCH_TP12	6
6	NC_PCH_TP10	TRUE MAKE_BASE=TRUE	NC_PCH_TP10	6
6	NC_PCH_TP9	TRUE MAKE_BASE=TRUE	NC_PCH_TP9	6
6	NC_PCH_TP8	TRUE MAKE_BASE=TRUE	NC_PCH_TP8	6
6	NC_PCH_TP7	TRUE MAKE_BASE=TRUE	NC_PCH_TP7	6
6	NC_PCH_TP6	TRUE MAKE_BASE=TRUE	NC_PCH_TP6	6
6	NC_PCH_TP5	TRUE MAKE_BASE=TRUE	NC_PCH_TP5	6
6	NC_PCH_TP4	TRUE MAKE_BASE=TRUE	NC_PCH_TP4	6
6	NC_PCH_TP3	TRUE MAKE_BASE=TRUE	NC_PCH_TP3	6
6	NC_PCH_TP2	TRUE MAKE_BASE=TRUE	NC_PCH_TP2	6
6	NC_PCH_TP1	TRUE MAKE_BASE=TRUE	NC_PCH_TP1	6
1522	PCH_VSS_NCTF<1>	TRUE	PCH_VSS_NCTF<15>	1542 81
1523	PCH_VSS_NCTF<2>	TRUE	PCH_VSS_NCTF<17>	1543 81
1520	PCH_VSS_NCTF<5>	TRUE	PCH_VSS_NCTF<19>	1544 6 81
1519	PCH_VSS_NCTF<9>	TRUE	PCH_VSS_NCTF<19>	1544 6 81
1518	PCH_VSS_NCTF<11>	TRUE	PCH_VSS_NCTF<21>	1545 81
1517	PCH_VSS_NCTF<12>	TRUE	PCH_VSS_NCTF<25>	1546 81
			PCH_VSS_NCTF<27>	1547 81
			PCH_VSS_NCTF<29>	1548 81
80 18 9	TP_LVDS_IG_B_CLKN	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKN	
80 18 9	TP_LVDS_IG_B_CLKP	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP	
6	NC_LVDS_IG_BKL_PWM	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM	6
6	NC_SMC_BS_ALRT_L	TRUE MAKE_BASE=TRUE	NC_SMC_BS_ALRT_L	6

SYNC MASTER=K24 MLB
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FUNC TEST

Apple Inc.

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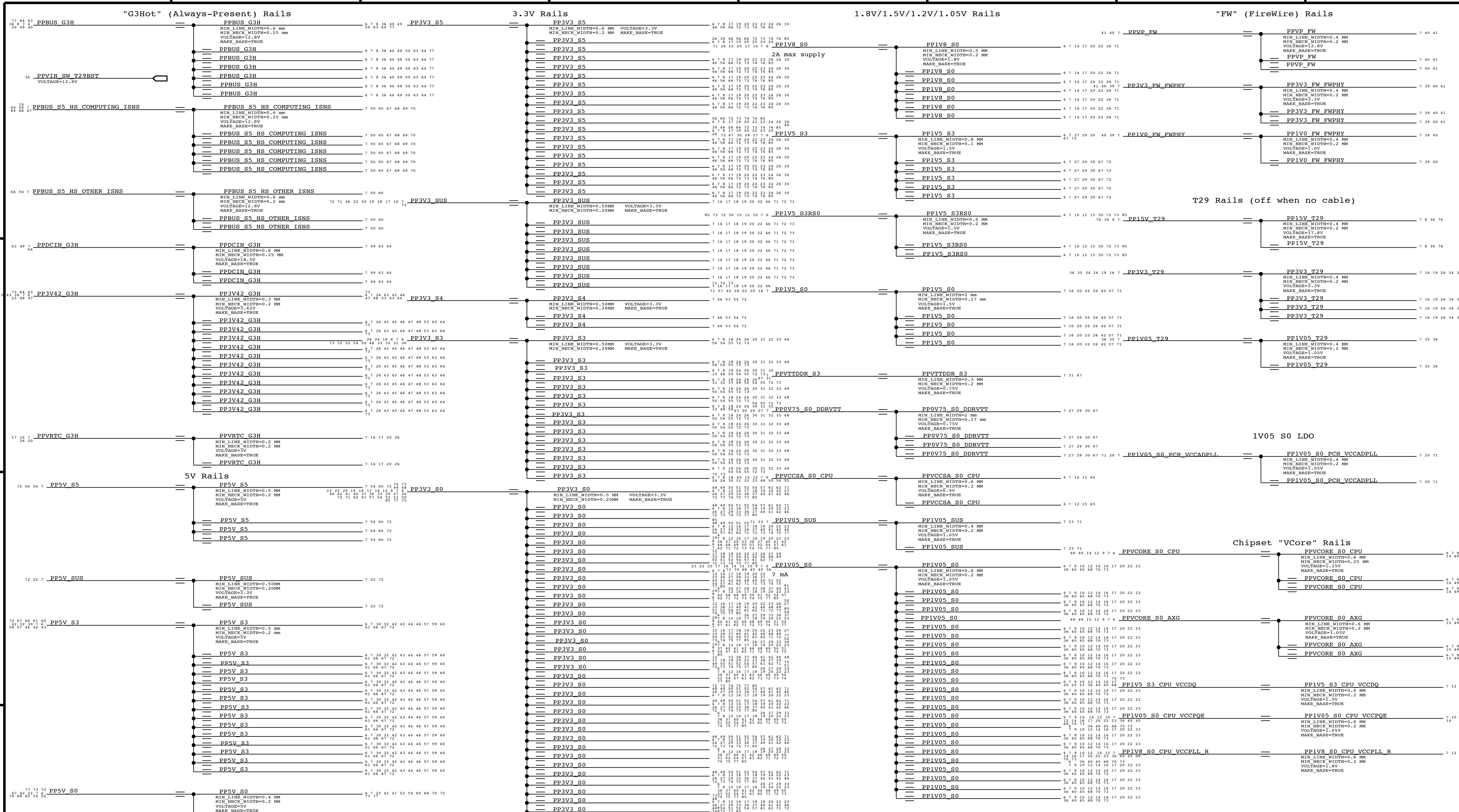

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010

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Power Aliases

Apple Inc.

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HEATSINK STANDOFFS

Z0902
STDOFF-4.5OD.98H-1.1-3.48-TH

Z0904
STDOFF-4.5OD.98H-1.1-3.48-TH

BELOW CPU

Z0920
STDOFF-4.5OD.98H-1.1-3.48-TH

LEFT OF CPU

FAN STANDOFF

Z0905
STDOFF-4.5OD.98H-1.1-3.48-TH

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

OMIT Z0906 3R2P5

OMIT Z0907 3R2P5

MLB MOUNTING (TO TOPCASE) SCREW HOLES

OMIT Z0908 3R2P5

OMIT Z0909 3R2P5

OMIT Z0910 3R2P5

OMIT Z0911 3R2P5

OMIT Z0912 3R2P5

EMI IO (SHORT) POGO PINS

ZS0900 1.4DIA-SHORT-EMI-MLB-K19-K24

ZS0901 1.4DIA-SHORT-EMI-MLB-K19-K24

ZS0902 1.4DIA-SHORT-EMI-MLB-K19-K24

ZS0903 1.4DIA-SHORT-EMI-MLB-K19-K24

ZS0908 1.4DIA-SHORT-EMI-MLB-K19-K24

ZS0909 1.4DIA-SHORT-EMI-MLB-K19-K24

EMI TALL POGO PINS

ZS0904 2.0DIA-TALL-EMI-MLB-M97-M98

ZS0905 2.0DIA-TALL-EMI-MLB-M97-M98

ZS0906 2.0DIA-TALL-EMI-MLB-M97-M98

ZS0907 2.0DIA-TALL-EMI-MLB-M97-M98

Heat Spreader Holes for T29, PCH

Z0950 STDOFF-4.0OD1.85H-SM

Z0951 STDOFF-4.0OD1.85H-SM

Z0952 STDOFF-4.0OD1.85H-SM

CPU signals

MEMVTT_EN — MEMVTT_EN

DP_EXTA_ML_C_P<3..0> — DP_IG_ML_P<3..0> — TP_DP_IG_B_MLP<3..0>

DP_EXTA_ML_C_N<3..0> — DP_IG_ML_N<3..0> — TP_DP_IG_B_MLN<3..0>

DP_EXTA_AUXCH_C_P — DP_EXTA_AUXCH_C_P

DP_EXTA_AUXCH_C_N — DP_EXTA_AUXCH_C_N

=PEG_R2D_C_P<11..8> — PEG_R2D_C_P<11..8> — PCIE_T29_R2D_C_P<3..0>

=PEG_R2D_C_N<11..8> — PEG_R2D_C_N<11..8> — PCIE_T29_R2D_C_N<3..0>

=PEG_D2R_P<11..8> — PEG_D2R_P<11..8> — PCIE_T29_D2R_P<3..0>

=PEG_D2R_N<11..8> — PEG_D2R_N<11..8> — PCIE_T29_D2R_N<3..0>

FW_PLUG_DET_L — FW_PLUG_DET_L

FW643_WAKE_L — FW643_WAKE_L

TP_SMC_EXCARD_PWR_EN — TP_SMC_EXCARD_PWR_EN

NC_PCIE_EXCARD_D2RN — NC_PCIE_EXCARD_D2RN

NC_PCIE_EXCARD_D2RP — NC_PCIE_EXCARD_D2RP

NC_PCIE_EXCARD_R2D_CN — NC_PCIE_EXCARD_R2D_CN

NC_PCIE_EXCARD_R2D_CP — NC_PCIE_EXCARD_R2D_CP

NC_PCIE_CLK100M_EXCARDN — NC_PCIE_CLK100M_EXCARDN

NC_PCIE_CLK100M_EXCARDP — NC_PCIE_CLK100M_EXCARDP

PCIE_PCH_D2R_N<5..8> — NC_PCIE_PCH_D2RN<5..8>

PCIE_PCH_D2R_P<5..8> — NC_PCIE_PCH_D2RP<5..8>

PCIE_PCH_R2D_C_N<5..8> — NC_PCIE_PCH_R2D_CN<5..8>

PCIE_PCH_R2D_C_P<5..8> — NC_PCIE_PCH_R2D_CP<5..8>

NC_PEG_CLK100MP — NC_PEG_CLK100MP

NC_PEG_CLK100MN — NC_PEG_CLK100MN

NC_PCH_CLKOUT_DPN — NC_PCH_CLKOUT_DPN

NC_PCH_CLKOUT_DPP — NC_PCH_CLKOUT_DPP

TP_ISSP_SCLK_P1_1 — TP_ISSP_SCLK_P1_1

TP_ISSP_SDATA_P1_0 — TP_ISSP_SDATA_P1_0

NC_FSB_CLK133M_PCH_P — NC_FSB_CLK133M_PCH_P

NC_FSB_CLK133M_PCH_N — NC_FSB_CLK133M_PCH_N

T29BST:N
R0960 0 5% 1/8W MF-LF 805
PPBUS_G3H — PP15V_T29

T29_A_BIAS — C0960 0.01UF 10% 10V X5R 201

DP_A_BIAS0 — C0962 0.01UF 10% 10V X5R 201

DP_A_BIAS2 — C0964 0.01UF 10% 10V X5R 201

T29_A_BIAS_R2DP1

T29_A_BIAS_R2DN0

T29_A_BIAS — R0970 51 1/20W MF VOLTAGE=3.3V — T29_A_BIAS_R2DP0

C0970 0.01UF 10% 10V X5R 201

R0971 51 1/20W MF VOLTAGE=3.3V — T29_A_BIAS_R2DN1

C0971 0.01UF 10% 10V X5R 201

R0973 51 1/20W MF VOLTAGE=3.3V — T29_A_BIAS_D2RN1

R0972 51 1/20W MF VOLTAGE=3.3V — T29_A_BIAS_D2RP1

C0972 0.01UF 10% 10V X5R 201

C0973 0.01UF 10% 10V X5R 201

T29 JTAG

JTAG_ISP_TCK — JTAG_ISP_TCK

JTAG_ISP_TDI — JTAG_ISP_TDI

JTAG_ISP_TDO — JTAG_ISP_TDO

PP3V3_S0

R0920 2.2K 5% 1/16W MF-LF 402
R0921 2.2K 5% 1/16W MF-LF 402
R0922 2.2K 5% 1/16W MF-LF 402
R0923 2.2K 5% 1/16W MF-LF 402

DP_IG_C_CTRL_CLK — DP_IG_C_CTRL_CLK

DP_IG_C_CTRL_DATA — DP_IG_C_CTRL_DATA

DP_IG_D_CTRL_CLK — DP_IG_D_CTRL_CLK

DP_IG_D_CTRL_DATA — DP_IG_D_CTRL_DATA

PP3V3_S0

R0924 2.2K 5% 1/16W MF-LF 402
R0925 2.2K 5% 1/16W MF-LF 402

DP_EXTA_DDC_CLK — DP_EXTA_DDC_CLK

DP_EXTA_DDC_DATA — DP_EXTA_DDC_DATA

DP_EXTA_HPD — DP_EXTA_HPD

R0908 100K 5% 1/16W MF-LF 402

R0910 0 5% 1/16W MF-LF 402
PPBUS_SW_LCDBKLT_PWR — PPBUS_SW_BKL — PPBUS_SW_BKL
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=12.6V

NC_USB_HUB1_OCS4 — NC_USB_HUB1_OCS4

NC_USB_HUB2_OCS4 — NC_USB_HUB2_OCS4

PU_USB_HUB2_PRT4_P — PU_USB_HUB2_PRT4_P

PU_USB_HUB2_PRT4_N — PU_USB_HUB2_PRT4_N

Unused T29 Ports

T29_D2R_P<2..3> — NC_T29_D2RP<2..3>

T29_D2R_N<2..3> — NC_T29_D2RN<2..3>

T29_R2D_C_P<2..3> — NC_T29_R2D_CP<2..3>

T29_R2D_C_N<2..3> — NC_T29_R2D_CN<2..3>

T29_LSEO<2> — T29_LSOE<2>

T29_LSEO<3> — T29_LSOE<3>

Unused PGOOD signal

TP_P1V5S3RS0_RAMP_DONE — TP_P1V5S3RS0_RAMP_DONE

TP_DDRREG_PGOOD — TP_DDRREG_PGOOD

T29 DP Ports

DP_T29SNK0_HPD — DP_T29SNK0_HPD

TP_DP_IG_C_MLP<3..0> — DP_T29SNK0_ML_C_P<3..0>

TP_DP_IG_C_MLN<3..0> — DP_T29SNK0_ML_C_N<3..0>

DP_T29SNK0_AUXCH_C_P — DP_T29SNK0_AUXCH_C_P

DP_T29SNK0_AUXCH_C_N — DP_T29SNK0_AUXCH_C_N

DP_T29SNK1_HPD — DP_T29SNK1_HPD

TP_DP_IG_D_MLP<3..0> — DP_T29SNK1_ML_C_P<3..0>

TP_DP_IG_D_MLN<3..0> — DP_T29SNK1_ML_C_N<3..0>

DP_T29SNK1_AUXCH_C_P — DP_T29SNK1_AUXCH_C_P

DP_T29SNK1_AUXCH_C_N — DP_T29SNK1_AUXCH_C_N

TP_BCM57765_TRAFFICLED_L — TP_BCM57765_TRAFFICLED_L

NC_BCM57765_CE_L_MS_INS_L — NC_BCM57765_CE_L_MS_INS_L

TP_LVDS_IG_B_CLKP — TP_LVDS_IG_B_CLKP

TP_LVDS_IG_B_CLKN — TP_LVDS_IG_B_CLKN

NC_LVDS_IG_B_DATAP<0..3> — LVDS_IG_B_DATA_P<0..3>

NC_LVDS_IG_B_DATAN<0..3> — LVDS_IG_B_DATA_N<0..3>

NC_LVDS_IG_A_DATAP<3> — NC_LVDS_IG_A_DATAP<3>

NC_LVDS_IG_A_DATAN<3> — NC_LVDS_IG_A_DATAN<3>

LVDS_DDC_CLK — LVDS_DDC_CLK

LVDS_DDC_DATA — LVDS_DDC_DATA

LCD_BKLT_PWM — LCD_BKLT_PWM

LCD_IG_PWR_EN — LCD_IG_PWR_EN

LCD_BKLT_EN — LCD_BKLT_EN

DPA PWR SW : Nostuff, Backup

U0950 TPS2553 SOT-23 NOSTUFF
PP3V3_S5 — IN
SMC_S4_WAKESRC_EN — EN
GND
OUT — PP3V3_SW_DPAPWR
ILIM — DPAPWR_ILIM
FAULT* — T29_A_HV_EN

NOSTUFF R0950 20K 5% 1/16W MF-LF 402

PP3V3_S3

R0915 10K 5% 1/16W MF-LF 402 NO STUFF
R0916 10K 5% 1/16W MF-LF 402
R0903 10K 5% 1/16W MF-LF 402 NO STUFF
R0904 10K 5% 1/16W MF-LF 402 NO STUFF
R0905 10K 5% 1/16W MF-LF 402 NO STUFF
R0906 10K 5% 1/16W MF-LF 402 NO STUFF

T29_A_RSVD_N — R0917 0 1/20W MF — USB_T29A_N

T29_A_RSVD_P — R0918 0 1/20W MF — USB_T29A_P

NO STUFF

USB_EXTC_N

USB_EXTC_P

PU_USB_HUB2_PRT4_N

PU_USB_HUB2_PRT4_P

TP_CPU_VTT_SELECT — TP_CPU_VTT_SELECT

Digital Ground

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

SYNC MASTER=K91 MLB — SYNC DATE=05/15/2010

PAGE TITLE: Signal Aliases

Apple Inc.

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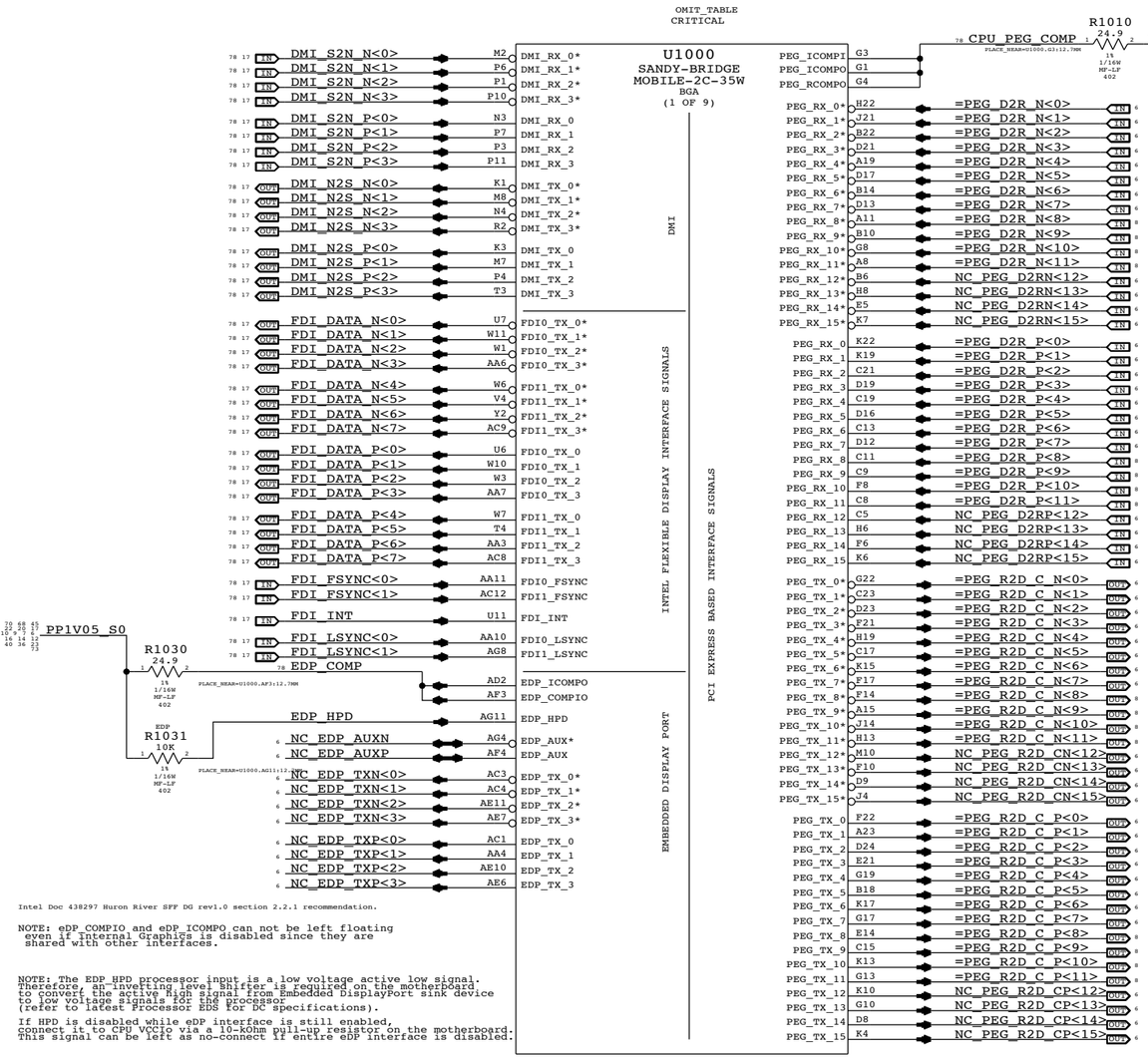

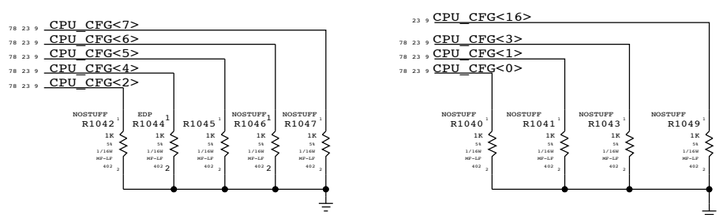

FOR SANDYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT)	10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

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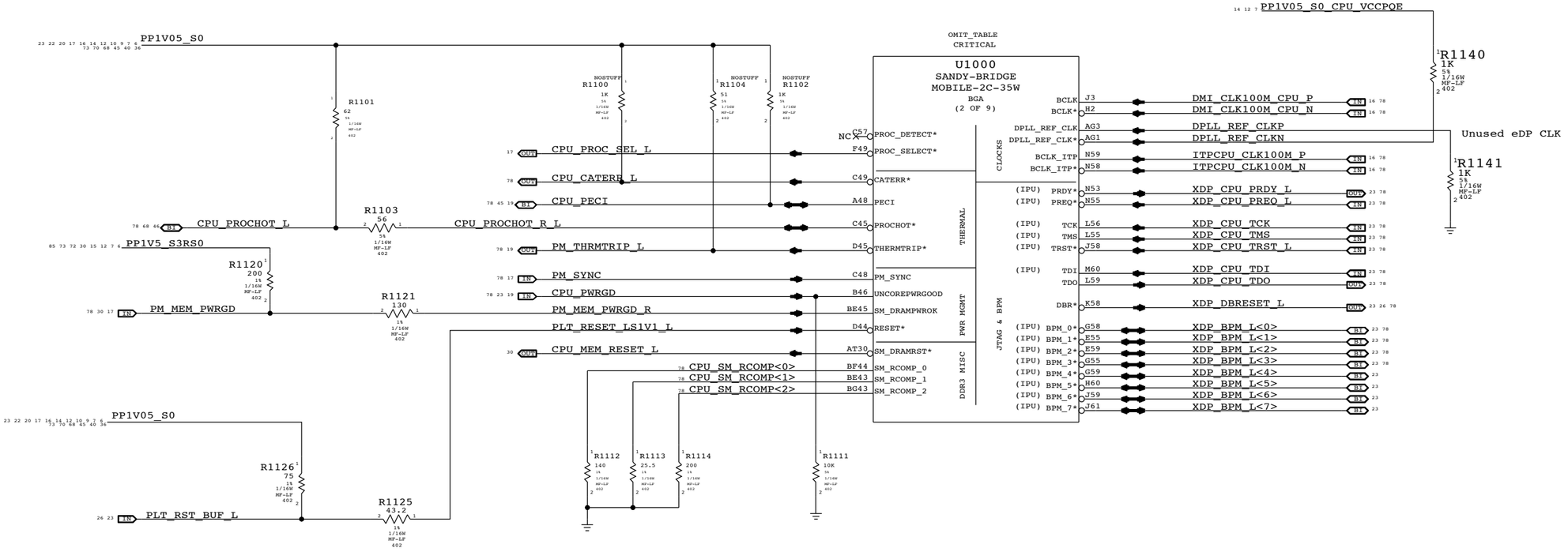

PAGE TITLE
CPU CLOCK/MISC/JTAG

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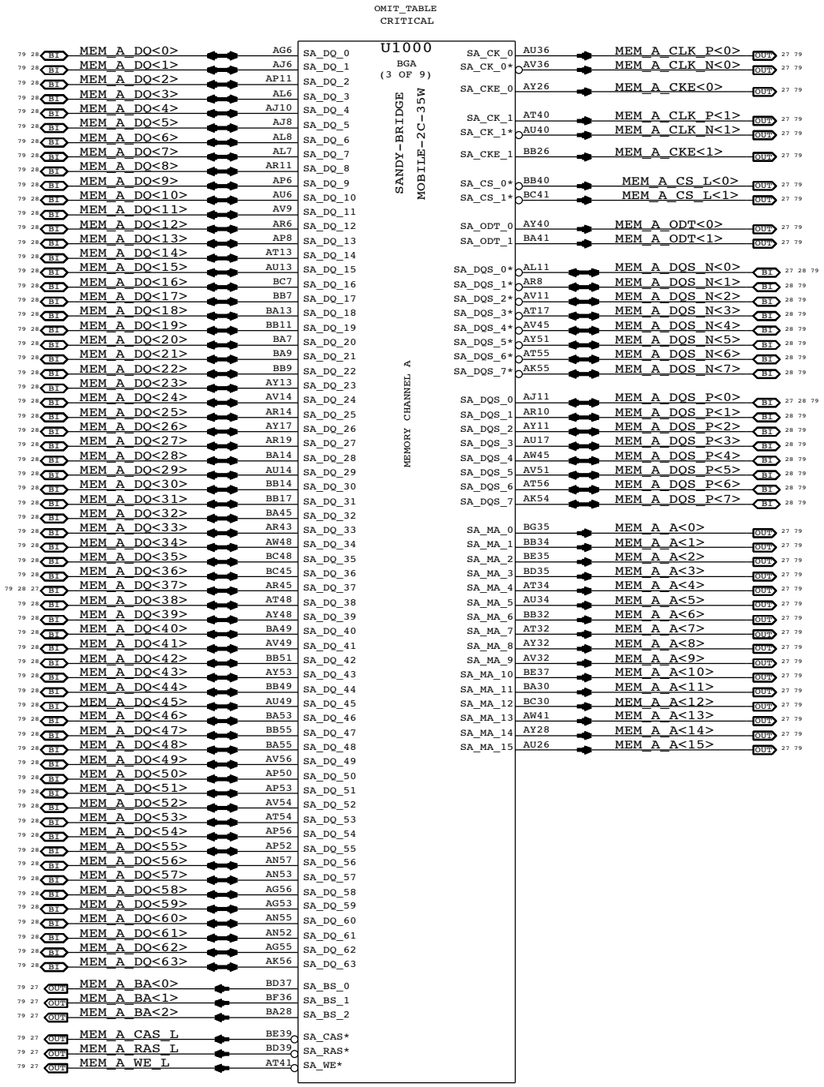

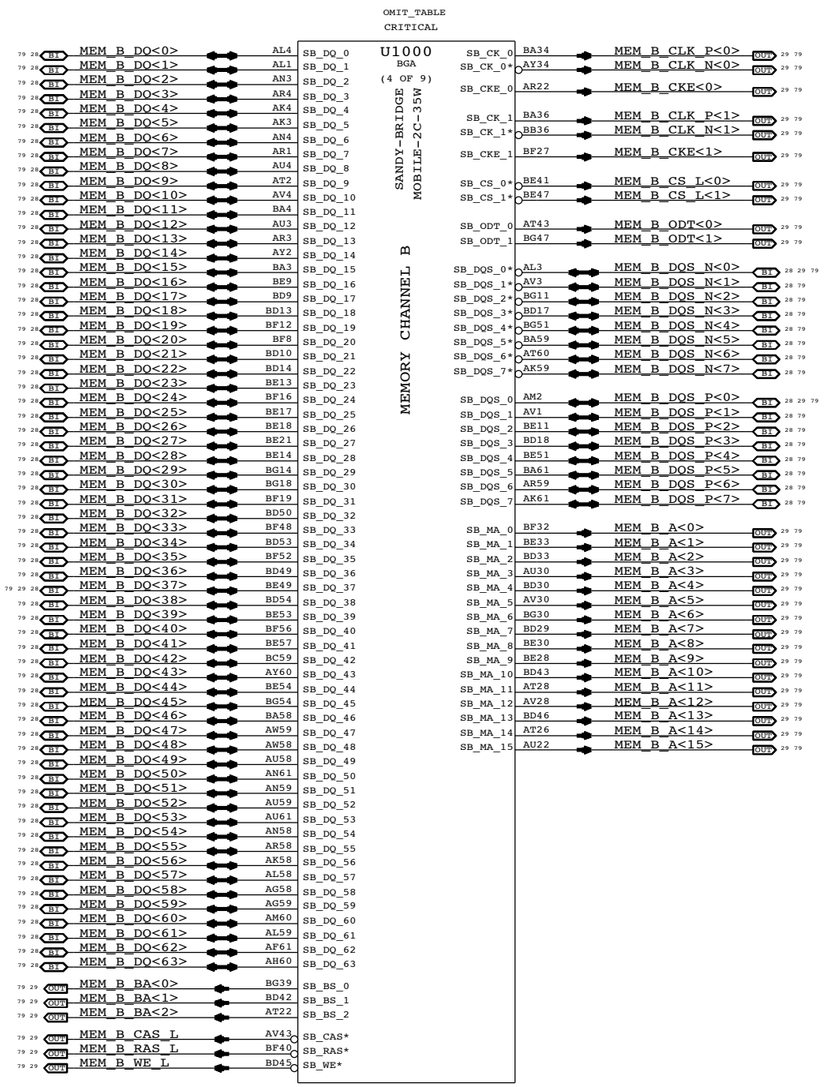

SYNC DATE=06/18/2010

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

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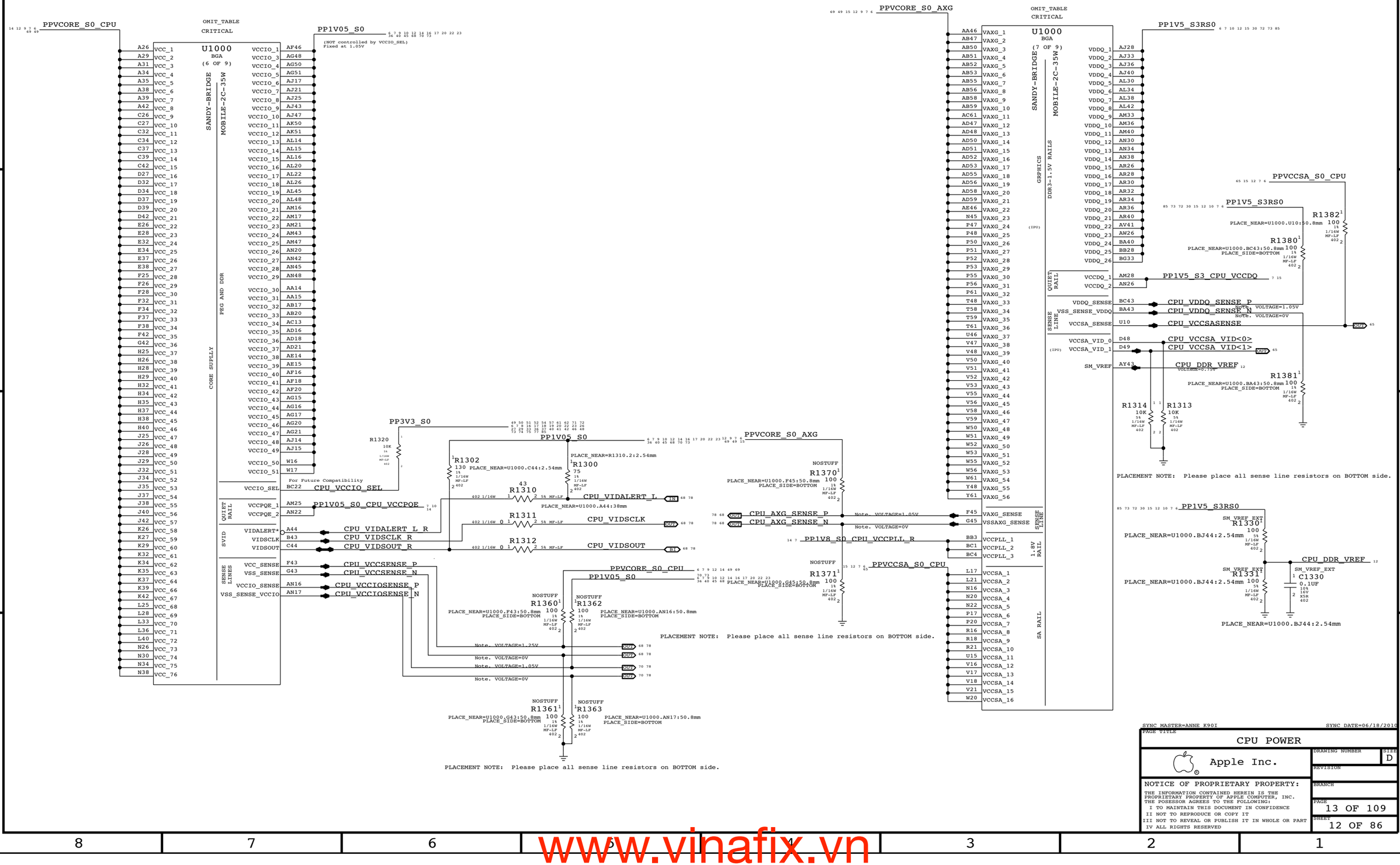

SYNC MASTER=ANNE K90I SYNC DATE=06/18/2010

PAGE TITLE

CPU POWER

Apple Inc.

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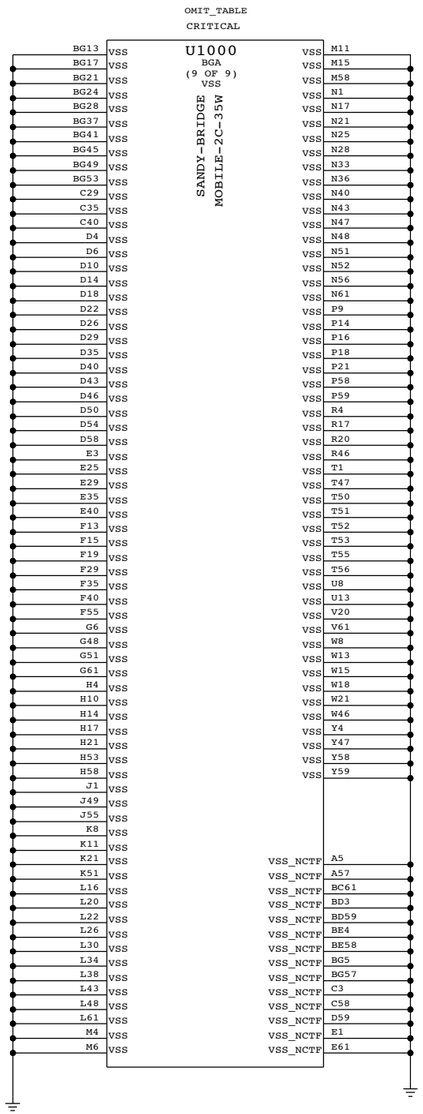

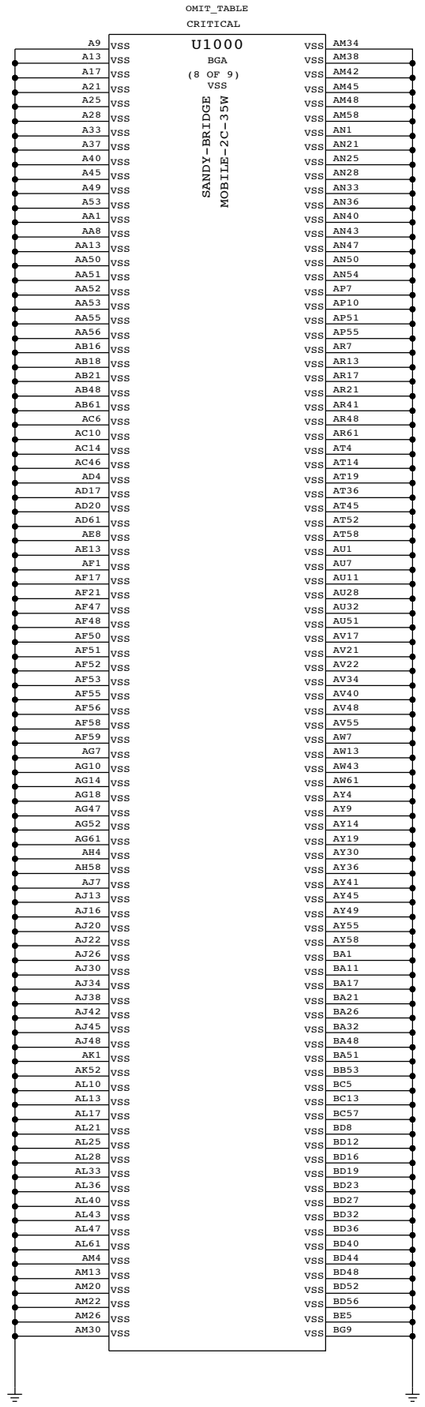

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CPU GROUNDS

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All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Intel recommendation (Section 6.2): 35x 2.2uF, 25x 22uF, 4x 470uF

69 49 12 9 7 6 PPVCORE_S0_CPU

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619 C1620 C1621 C1622 C1623 C1624
C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639 C1640 C1641 C1642 C1643 C1644 C1645 C1646 C1647 C1648 C1649
C1650 C1651 C1652 C1653 C1654
2.2UF 20% 4V X5R 402

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

C1655 C1656 C1657 C1658 C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666
22UF 20% 6.3V X5R-CERM-1 603

PLACEMENT_NOTE (C1667-C1679):
Place close to U1000 on bottom side.

C1667 C1668 C1669 C1670 C1671 C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679
22UF 20% 6.3V X5R-CERM-1 603

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

C1680 C1681 C1682 C1683
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	16	CAP,CER,X5R,22uF,20%,6.3V,0603,SAMSUNG		CRITICAL	
		C1655,C1660,C1661,C1662,C1663,C1664,C1665,C1666,C1667,C1670,C1671,C1674,C1676,C1677,C1678,C1679			

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000

45 40 36 23 12 10 8 3 PP1V05_S0
22 20 17 14 73 70 68

C1684 C1685 C1686 C1687 C1688 C1689 C1690 C1691 C1692 C1693 C1694 C1695 C1696
C1697 C1698 C1699 C169A C169B C169C C169D C169E C169F C161A C161B C161C C161D
1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C161E C161F C162A C162B C162C C162D C162E C167A C167B C167C
10UF 20% 6.3V CERM-X5R 0402-1

C167D C167E
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603
PP1V05_S0_CPU_VCCPQE 7 10 12
C167F 1UF 10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):
Place near U1000 on top side

71 26 22 20 17 7 6 PP1VR_S0
R1600 0 5% 1/16W MF-LF 402
PP1VR_S0_CPU_VCCPLL_R 7 12
PLACE_NEAR=U1000.AK61:5mm
C160X 1UF 10% 10V X5R 402
C160Y 1UF 10% 10V X5R 402
C160Z 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA
PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

CPU VCCPLL Low pass filter

SYNC MASTER=JACK K90I SYNC DATE=06/28/2010

PAGE TITLE: CPU DECOUPLING-I

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VAXG DECOUPLING

Intel recommendation (section 6.3): 21x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

69 49 12 9 7 6 PPVCORE_S0_AXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL C1700 1UF 10% 10V X5R 402
CRITICAL C1701 1UF 10% 10V X5R 402
CRITICAL C1702 1UF 10% 10V X5R 402
CRITICAL C1703 1UF 10% 10V X5R 402
CRITICAL C1704 1UF 10% 10V X5R 402
CRITICAL C1705 1UF 10% 10V X5R 402
CRITICAL C1706 1UF 10% 10V X5R 402
CRITICAL C1707 1UF 10% 10V X5R 402
CRITICAL C1708 1UF 10% 10V X5R 402
CRITICAL C1709 1UF 10% 10V X5R 402
CRITICAL C1710 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL C1711 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1712 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1713 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1714 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1715 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1716 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL OMIT C1717 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1718 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1719 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1720 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1721 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1722 22UF 20% 6.3V X5R-CERM-1 603

PLACEMENT_NOTE (C1723-C1724):

Place near inductors on bottom side.

C1723 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
C1724 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	6	CAP,CER,X5R,22uF,20%,6.3V,0603,SAMSUNG	C1717,C1718,C1719,C1720,C1721,C1722	CRITICAL	

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.5): 10x 1uF, 8x 10uF, 1x 330uF

85 73 72 30 12 10 7 6 PP1V5_S3RS0

PLACEMENT_NOTE (C1738-C1747):

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V CERM-X5R 0402-1

C1756 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702 0.010 1% 1/4W MF 0603

PP1V5_S3_RS0_VCCDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 6x 1uf, 5x 10uf, 1x 330uf

65 12 7 6 PPVCCSA_S0_CPU

PLACEMENT_NOTE (C1758-C1762):

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

C1768 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

SYNC MASTER=JACK K90I SYNC DATE=06/28/2010

PAGE TITLE: CPU DECOUPLING-II

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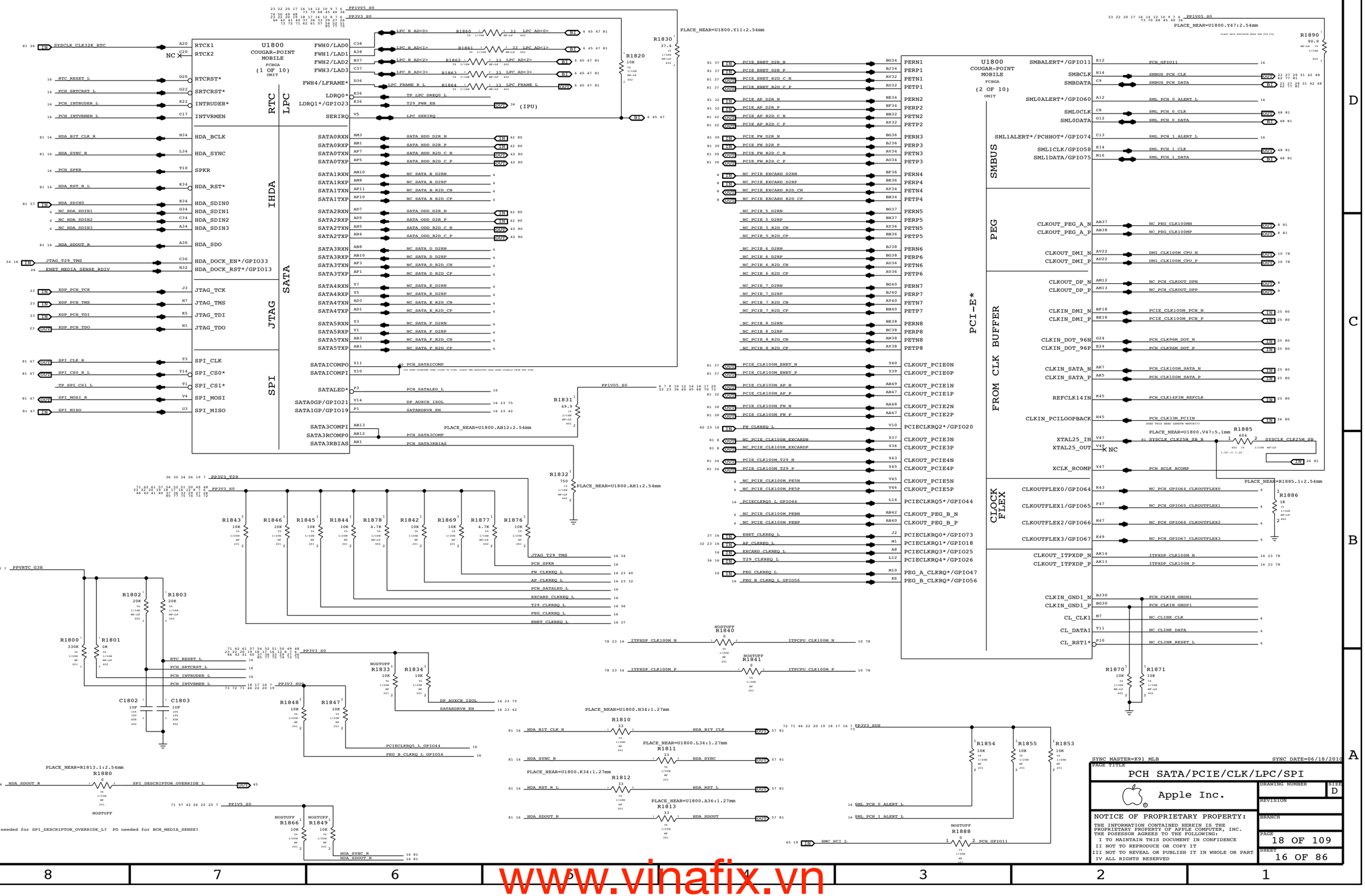
U1800
COUGAR-POINT
MOBILE
FCBGA
(1 OF 10)
OMIT
RTC
LPC
IHDA
SATA
JTAG
SPI
PCI-E*
SMBUS
PEG
FROM CLK BUFFER
CLOCK FLEX
SYSCLK_CLK32K_RTC
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
HDA_BIT_CLK_R
HDA_SYNC_R
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
NC_HDA_SDIN1
NC_HDA_SDIN2
NC_HDA_SDIN3
HDA_SDOUT_R
JTAG_T29_TMS
ENET_MEDIA_SENSE_RDIV
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
SPI_MOSI_R
SPI_MISO
LPC_R_AD<0>
LPC_R_AD<1>
LPC_R_AD<2>
LPC_R_AD<3>
LPC_FRAME_R_L
TP_LPC_DREQ0_L
T29_PWR_EN
LPC_SERIRQ
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
NC_SATA_B_D2RN
NC_SATA_B_D2RP
NC_SATA_B_R2D_CN
NC_SATA_B_R2D_CP
SATA_ODD_D2R_N
SATA_ODD_D2R_P
SATA_ODD_R2D_C_N
SATA_ODD_R2D_C_P
NC_SATA_D_D2RN
NC_SATA_D_D2RP
NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP
NC_SATA_E_D2RN
NC_SATA_E_D2RP
NC_SATA_E_R2D_CN
NC_SATA_E_R2D_CP
NC_SATA_F_D2RN
NC_SATA_F_D2RP
NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP
PCH_SATAICOMP
DP_AUXCH_ISOL
PCH_SATALED_L
SATARDRVR_EN
PCH_SATA3COMP
PCH_SATA3RBIAS
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_FW_D2R_N
PCIE_FW_D2R_P
PCIE_FW_R2D_C_N
PCIE_FW_R2D_C_P
NC_PCIE_EXCARD_D2RN
NC_PCIE_EXCARD_D2RP
NC_PCIE_EXCARD_R2D_CN
NC_PCIE_EXCARD_R2D_CP
NC_PCIE_5_D2RN
NC_PCIE_5_D2RP
NC_PCIE_5_R2D_CN
NC_PCIE_5_R2D_CP
NC_PCIE_6_D2RN
NC_PCIE_6_D2RP
NC_PCIE_6_R2D_CN
NC_PCIE_6_R2D_CP
NC_PCIE_7_D2RN
NC_PCIE_7_D2RP
NC_PCIE_7_R2D_CN
NC_PCIE_7_R2D_CP
NC_PCIE_8_D2RN
NC_PCIE_8_D2RP
NC_PCIE_8_R2D_CN
NC_PCIE_8_R2D_CP
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_FW_N
PCIE_CLK100M_FW_P
FW_CLKREQ_L
NC_PCIE_CLK100M_EXCARDN
NC_PCIE_CLK100M_EXCARDP
PCIE_CLK100M_T29_N
PCIE_CLK100M_T29_P
NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P
PCIECLKRQ5_L GPIO44
NC_PCIE_CLK100M_PEBN
NC_PCIE_CLK100M_PEBP
ENET_CLKREQ_L
AP_CLKREQ_L
EXCARD_CLKREQ_L
T29_CLKREQ_L
PEG_CLKREQ_L
PEG_B_CLKRQ_L GPIO56
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKIN_GND1_N
CLKIN_GND1_P
CL_CLK1
CL_DATA1
CL_RST1*
R1800 330K
R1801 1M
R1802 20K
R1803 20K
C1802 1UF
C1803 1UF
R1810 33
R1811 33
R1812 33
R1813 33
R1820 10K
R1830 37.4
R1831 49.9
R1832 750
R1840 0
R1841 0
R1843 10K
R1844 10K
R1845 10K
R1846 10K
R1848 10K
R1847 10K
R1833 10K
R1834 10K
R1854 10K
R1855 10K
R1853 10K
R1866 10K
R1849 10K
R1870 10K
R1871 10K
R1878 4.7K
R1842 10K
R1869 10K
R1877 4.7K
R1876 10K
R1880 0
R1888 0
R1890 90.9
R1885 604
R1886 1K
PLACE_NEAR=U1800.Y11:2.54mm
PLACE_NEAR=U1800.Y47:2.54mm
PLACE_NEAR=U1800.AB12:2.54mm
PLACE_NEAR=U1800.AH1:2.54mm
PLACE_NEAR=U1800.N34:1.27mm
PLACE_NEAR=U1800.L34:1.27mm
PLACE_NEAR=U1800.K34:1.27mm
PLACE_NEAR=U1800.A36:1.27mm
PLACE_NEAR=U1800.V47:5.1mm
PLACE_NEAR=R1813.1:2.54mm
PLACE_NEAR=R1885.1:2.54mm
PP1V05_S0
PP3V3_S0
PP3V3_T29
PP3V3_SUS
PPVRTC_G3H
PP1V5_S0
SYNC MASTER=K91 MLB
SYNC DATE=06/18/2010
PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI
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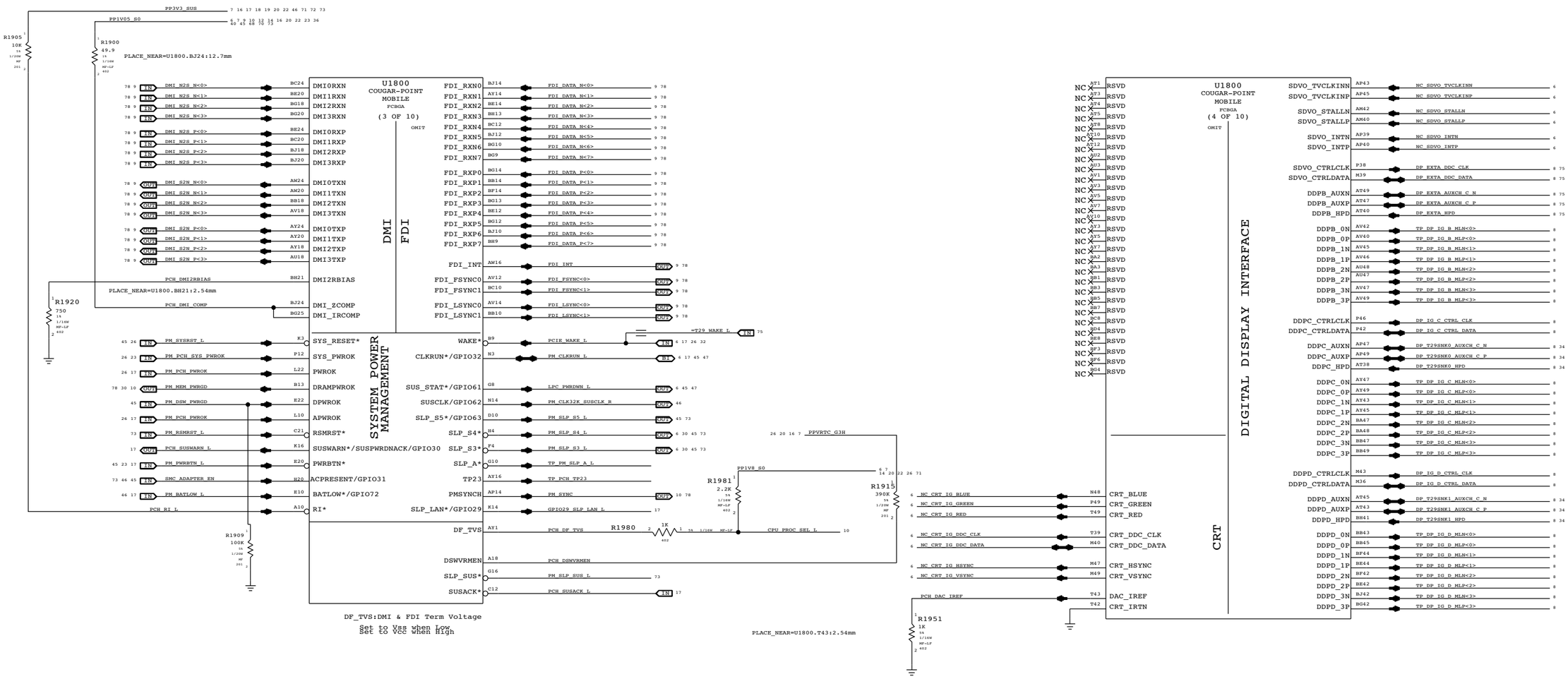
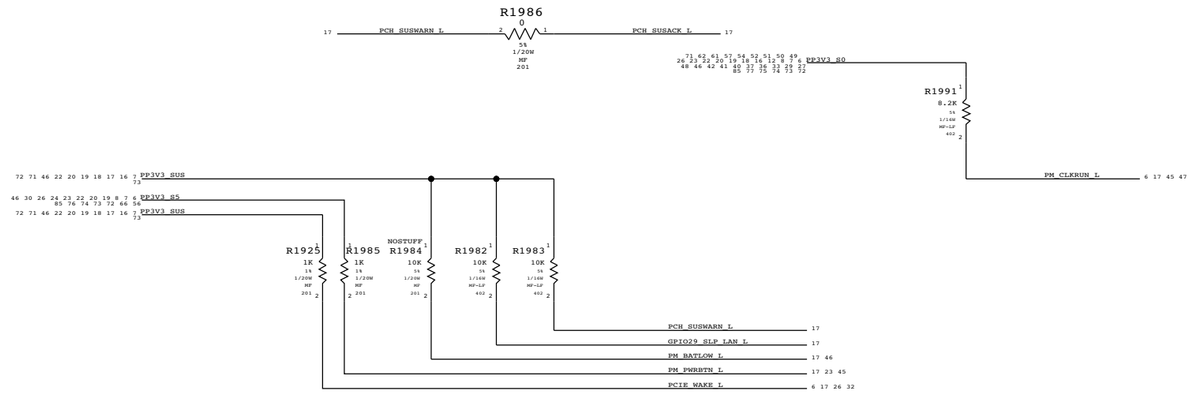
Pullup needed for SPI_DESCRIPTOR_OVERRIDE_L? PD needed for BCM_MEDIA_SENSE?
www.vinafix.vn





PAGE TITLE
PCH DMI/FDI/GRAPHICS

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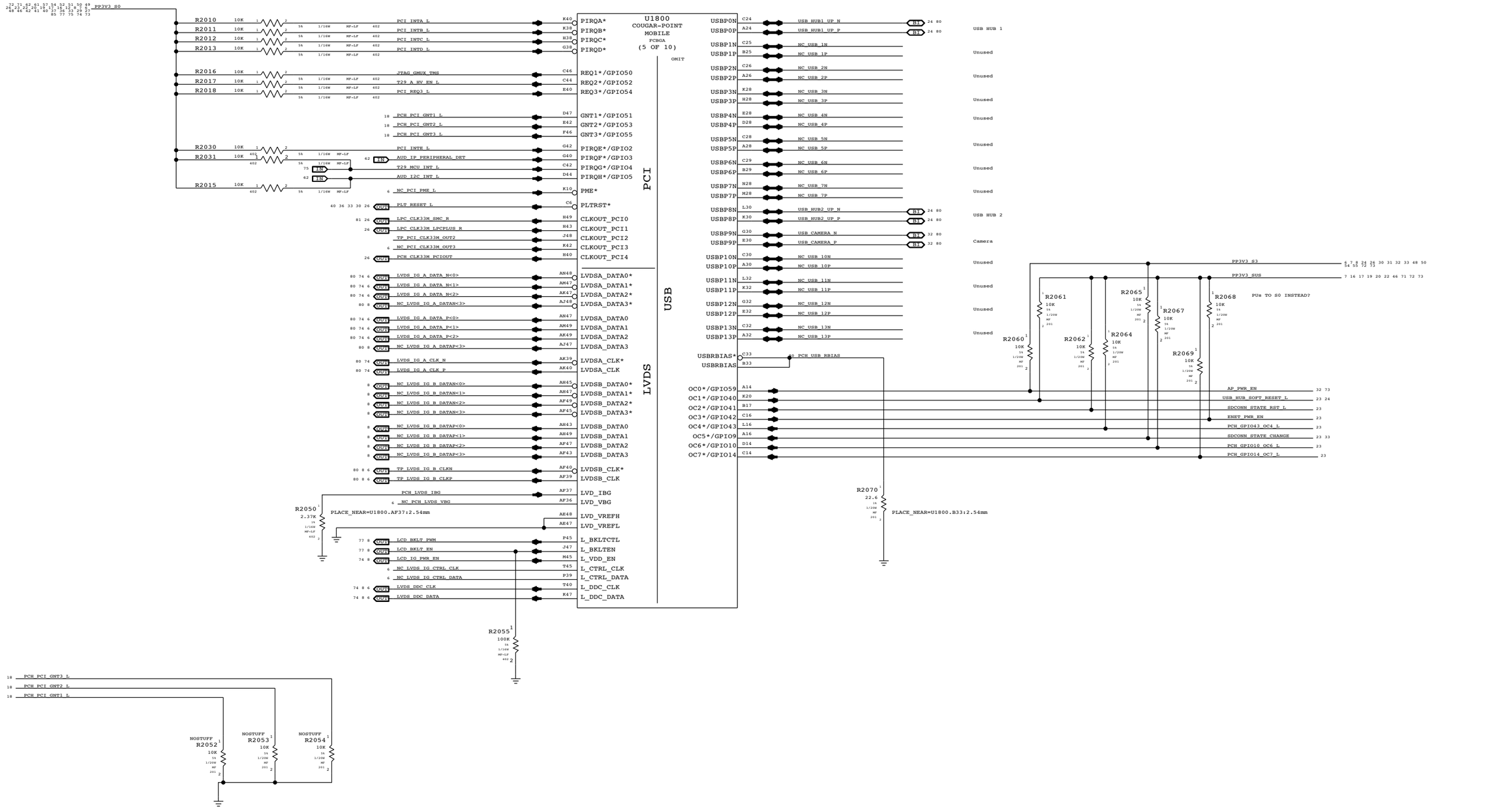

SYNC MASTER=K91 MLB SYNC DATE=06/10/2010

PAGE TITLE

PCH PCI/FLASHCACHE/USB

Apple Inc.

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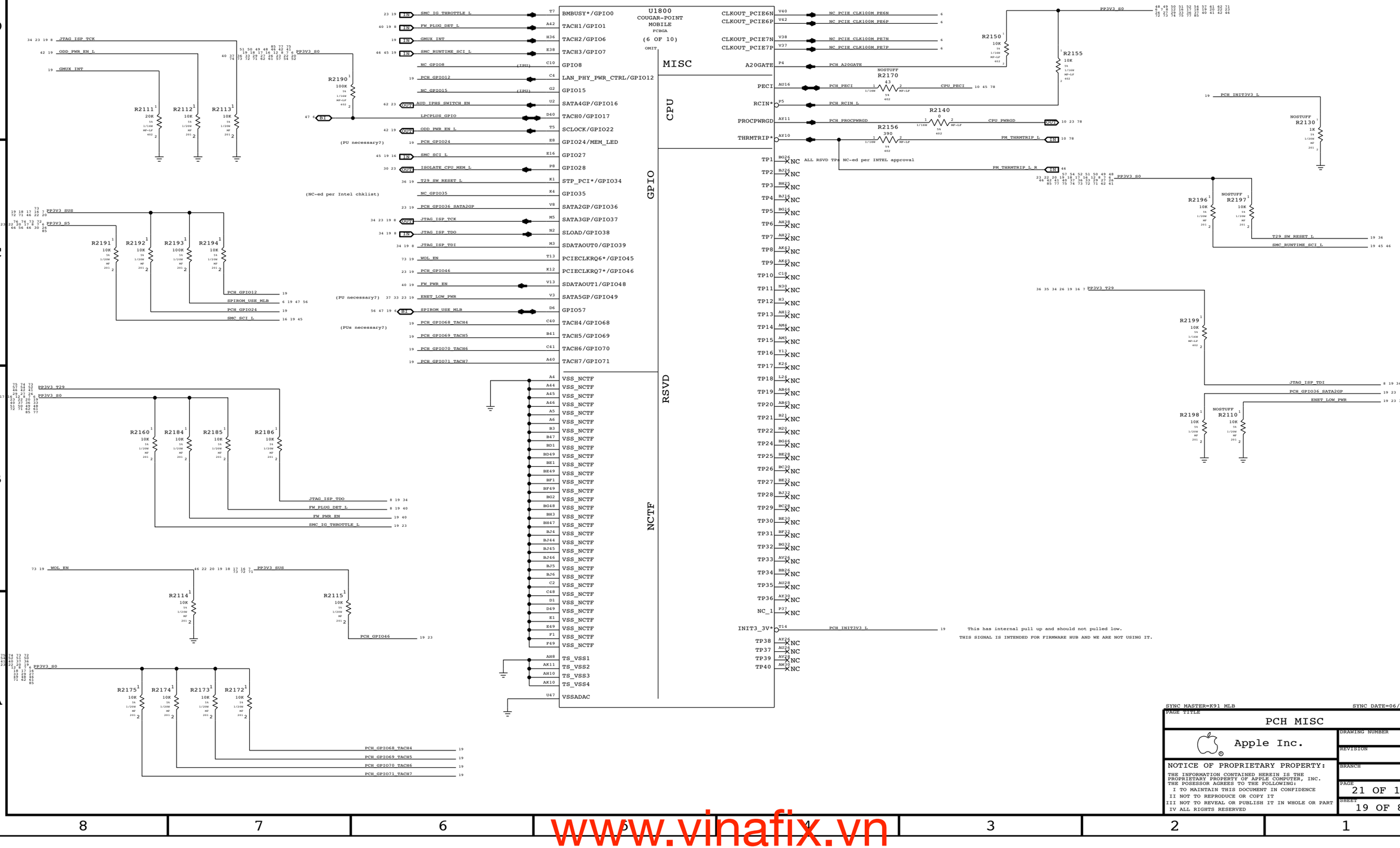

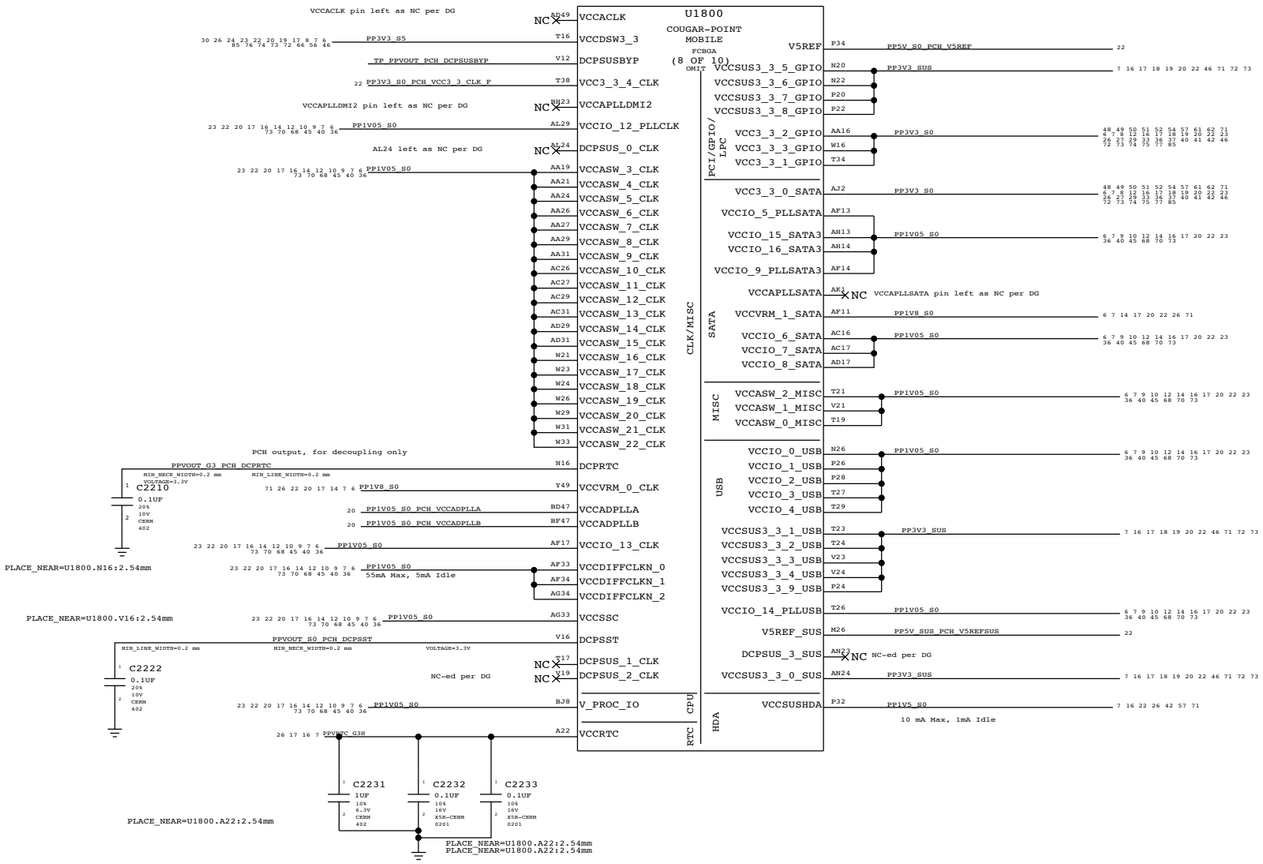

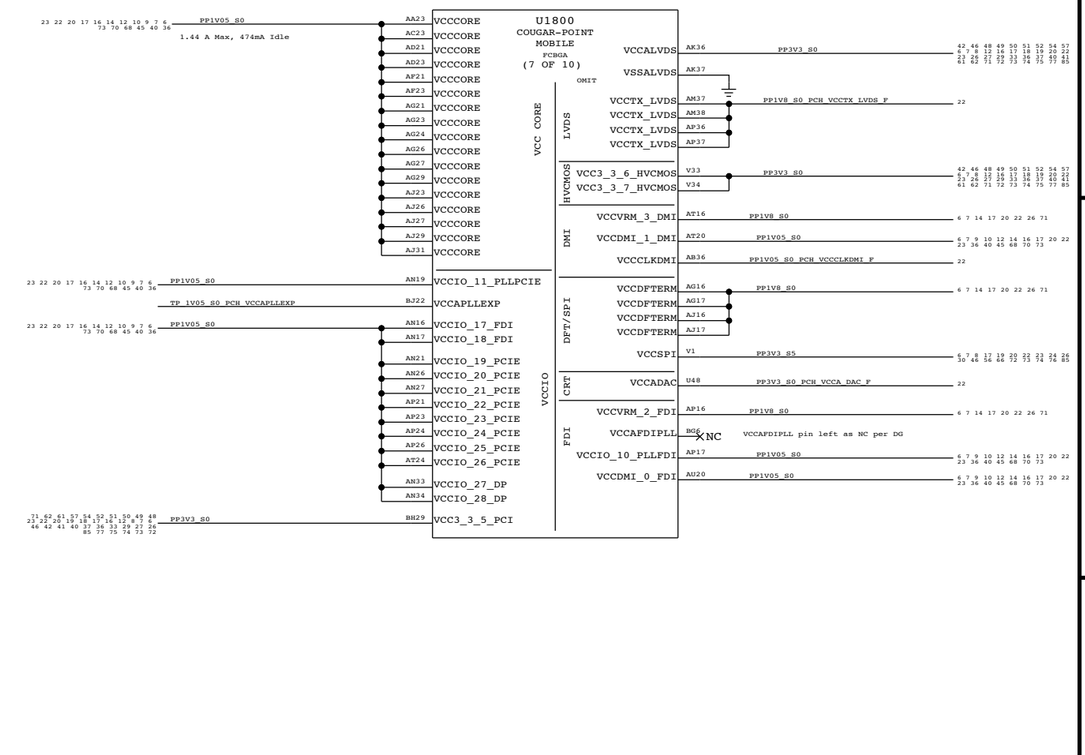

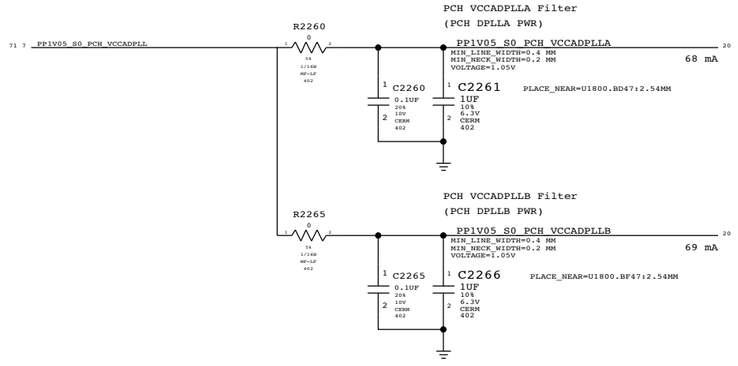

PAGE TITLE: PCH POWER

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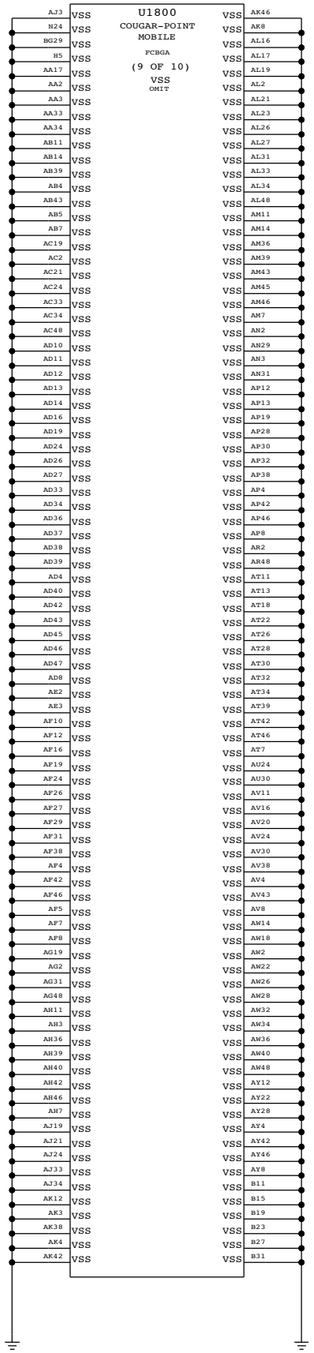

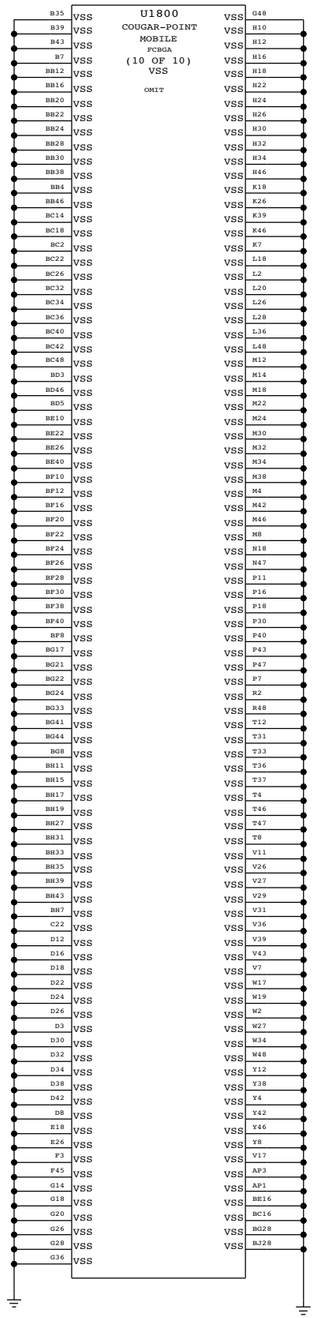

SYNC MASTER=K91 MLB SYNC DATE=05/27/2010

PAGE TITLE

PCH GROUNDS

Apple Inc.

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L2406
10UH-0.12A-0.36OHM
0603
R2415
PP1V05_S0_PCH_VCCCLKDMI_R
PP1V05_S0_PCH_VCCCLKDMI_F
C2411 10UF
PLACE_NEAR=U1800.AB36:2.54mm

L2407
0.1UH
0805
PP1V8_S0
PP1V05_S0_PCH_VCCTX_LVDS_F
C2400 22UF
C2406 0.01UF
C2408 0.01UF
PLACE_NEAR=U1800.AM37:2.54mm
PLACE_NEAR=U1800.AM37:2.54mm
PLACE_NEAR=U1800.AM37:2.54mm

R2450
PP3V3_S0
PP3V3_S0_PCH_VCCA_DAC_F
C2450 10UF
C2451 0.1UF
C2455 0.01UF
PLACE_NEAR=U1800.U48:2.54mm
PLACE_NEAR=U1800.U48:2.54mm
PLACE_NEAR=U1800.U48:2.54mm

PCH V5REF Filter & Follower
(PCH Reference for 5V Tolerance on PCI)
R2405 100
D2400 BAT54DW-X-G
PP3V3_S0
PP5V_S0
1 mA
NEED PWR CONSTRAINT
PP5V_S0_PCH_V5REF
<1 MA
C2439 1UF
PLACE_NEAR=U1800.P34:2.54mm

PCH V5REF_SUS Filter & Follower
(PCH Reference for 5V Tolerance on USB)
R2404 10
D2400 BAT54DW-X-G
PP3V3_SUS
PP5V_SUS
1 mA S0-S5
NEED PWR CONSTRAINT
PP5V_SUS_PCH_V5REFSUS
<1 MA S0-S5
C2438 0.1UF
PLACE_NEAR=U1800.M26:2.54mm

C2421 0.1UF
PLACE_NEAR=U1800.BH29:2.54mm

C2423 0.1UF
PLACE_NEAR=U1800.AJ2:2.54mm

C2424 0.1UF
PLACE_NEAR=U1800.V33:2.54mm

C2486 0.1UF
C2485 0.1UF
PLACE_NEAR=U1800.T34:2.54mm
PLACE_NEAR=U1800.AA16:2.54mm

PCH VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)
PP3V3_SUS
C2484 0.1UF
C2413 0.1UF
PLACE_NEAR=U1800.P24:2.54mm
PLACE_NEAR=U1800.V24:2.54mm

PCH VCCSUSHDA BYPASS
(PCH HD Audio 3.3V/1.5V PWR)
PP1V5_S0
C2416 4.7UF
C2417 0.1UF
C2430 0.1UF
PLACE_NEAR=U1800.BJ8:2.54mm
PLACE_NEAR=U1800.BJ8:2.54mm
PLACE_NEAR=U1800.BJ8:2.54mm

PCH VCCIO BYPASS
C2419 1UF
PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)
PLACE_NEAR=U1800.AT20:2.54mm

R2451
PP3V3_S0_PCH_VCC3_3_CLK_R
L2451
10UH-0.12A-0.36OHM
PP3V3_S0_PCH_VCC3_3_CLK_F
C2453 10UF
C2454 1UF
PLACE_NEAR=U1800.T38:2.54mm
PLACE_NEAR=U1800.T38:2.54mm

C2429 1UF
C2414 1UF
C2407 1UF
C2463 1UF
C2401 10UF
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm

C2426 1UF
C2456 1UF
C2496 1UF
C2428 22UF
C2420 22UF
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm

C2440 0.1UF
PLACE_NEAR=U1800.AJ16:2.54mm

C2441 0.1UF
PLACE_NEAR=U1800.P32:2.54mm

C2442 1UF
PLACE_NEAR=U1800.V1:2.54mm

C2499 0.1UF
PLACE_NEAR=U1800.T16:2.54mm

C2444 1UF
C2452 1UF
PLACE_NEAR=U1800.AC17:2.54mm
PLACE_NEAR=U1800.AH13:2.54mm

C2475 1UF
C2476 1UF
PLACE_NEAR=U1800.AG33:2.54mm
PLACE_NEAR=U1800.P22:2.54mm

C2434 1UF
PLACE_NEAR=U1800.AF34:2.54mm

PCH VCCIO BYPASS
(PCH USB 1.05V PWR)
C2446 1UF
PLACE_NEAR=U1800.P28:2.54mm

PCH VCCCORE BYPASS
(PCH 1.05V CORE PWR)
C2481 1UF
C2482 1UF
C2483 1UF
C2460 10UF
PLACE_NEAR=U1800.AD21:2.54mm
PLACE_NEAR=U1800.AG24:2.54mm
PLACE_NEAR=U1800.AJ27:2.54mm
PLACE_NEAR=U1800.AG26:2.54mm

C2469 1UF
PLACE_NEAR=U1800.AF17:2.54mm

SYNC MASTER=K91 MLB
SYNC DATE=06/25/2010
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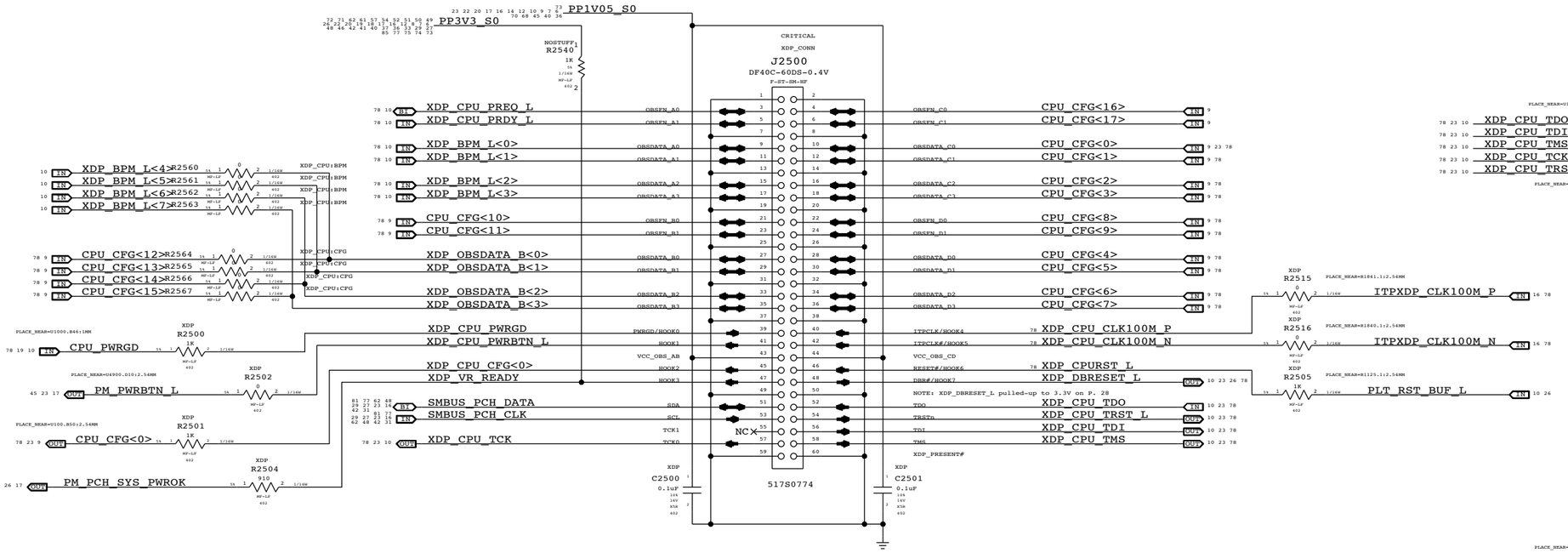
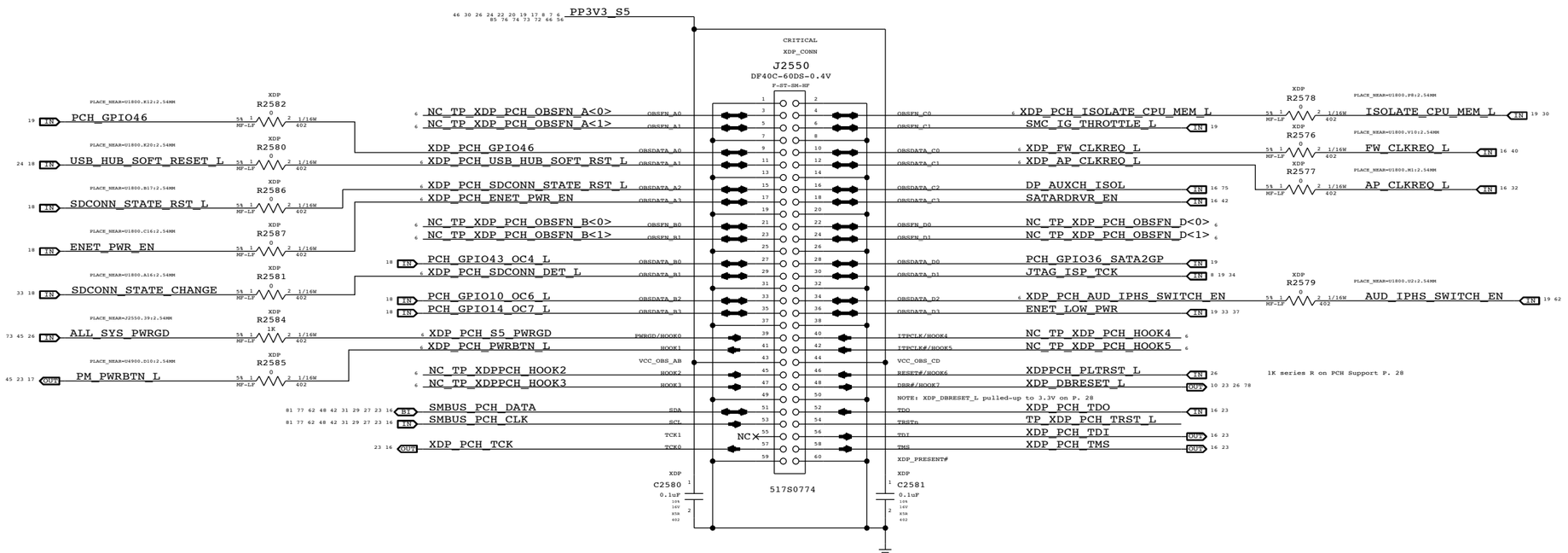
PROCESSOR MINI XDP



PCH MINI XDP



SYNC MASTER=ANNE K90I SYNC DATE=06/22/2010

PAGE TITLE

CPU & PCH XDP

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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0923	2	SMSC USX2513B	U2600,U2650	CRITICAL	USBHUB_2513B

SYNC_MASTER=K91_MLB SYNC_DATE=06/08/2010

PAGE TITLE: USB HUBS

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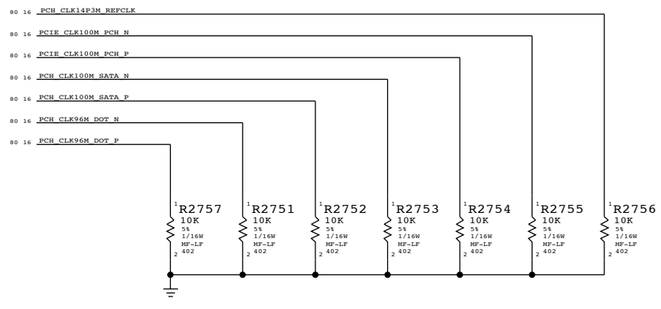
UNUSED clock terminations for FCIM MODE



SYNC_MASTER=K91_MLB SYNC_DATE=06/21/2011

PAGE TITLE

Clock (CK505)

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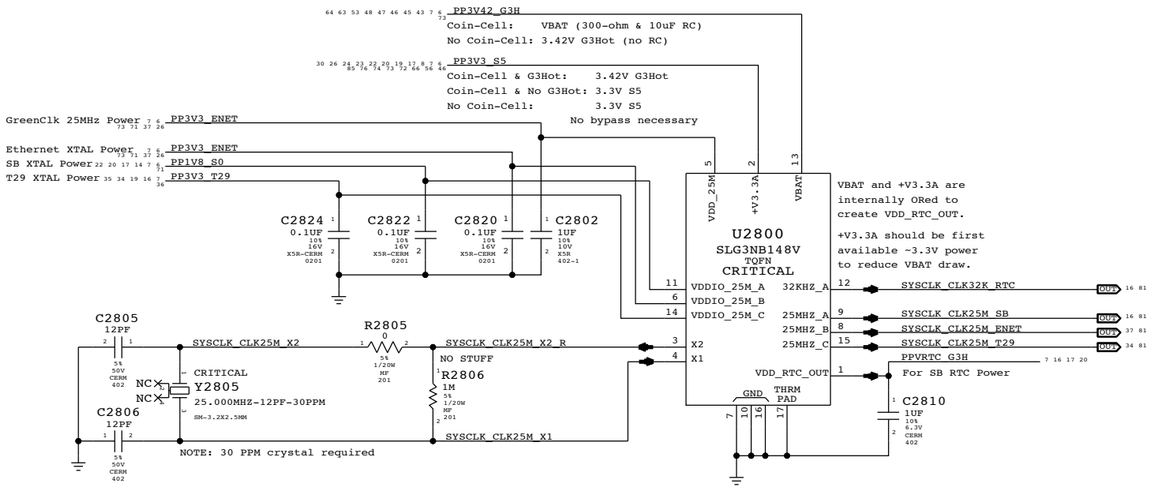
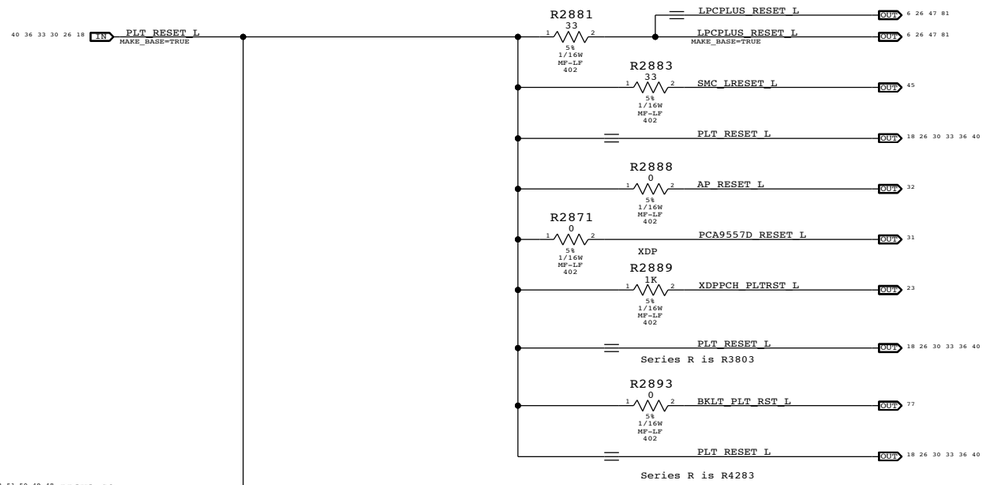
System RTC Power Source & 32kHz / 25MHz Clock Generator

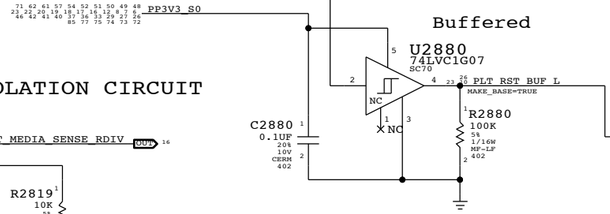


Platform Reset Connections

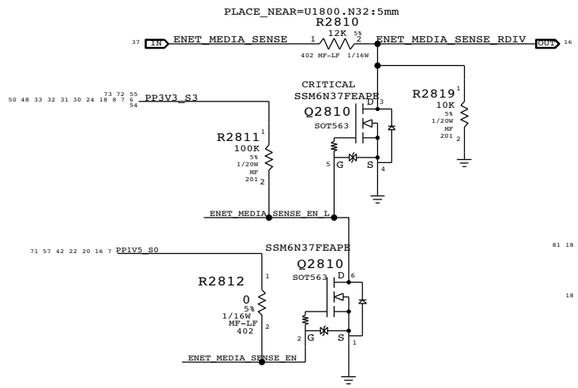
Unbuffered



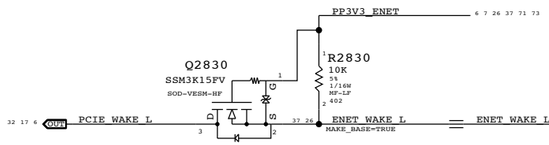
Buffered



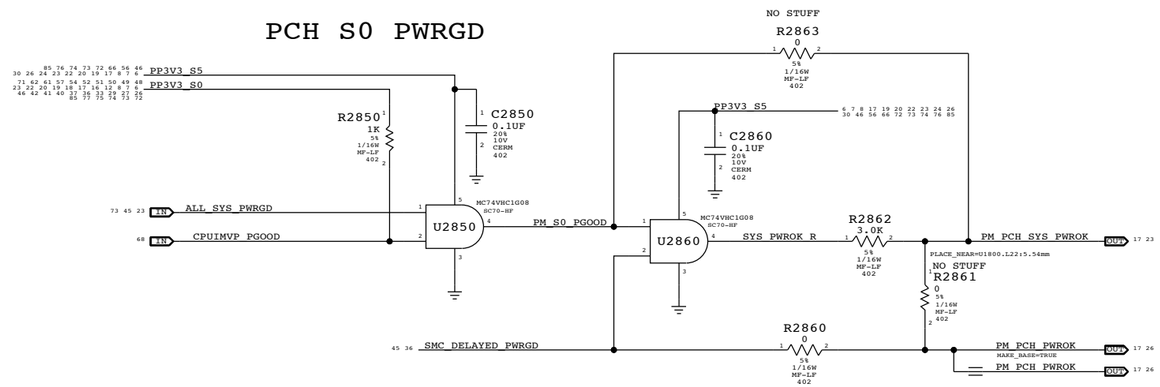
ENET_MEDIA_SENSE ISOLATION CIRCUIT



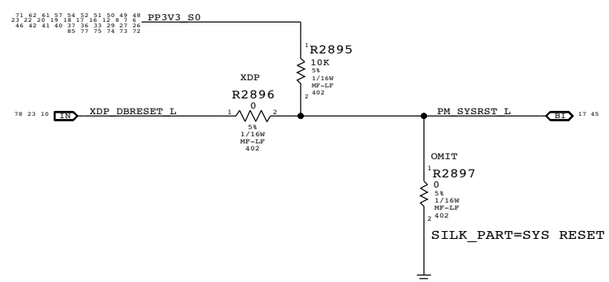
Ethernet WAKE# Isolation



PCH S0 PWRGD

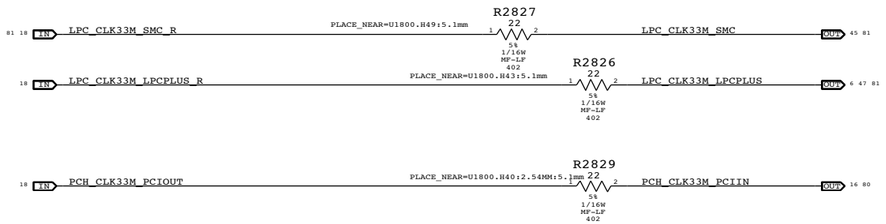


PCH Reset Button



Platform Reset Connections

Series R



DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPDDR_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

72 67 30 29 7 6 PP1V5_S3

C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402

C2900 10UF 20% 6.3V X5R 603
C2901 10UF 20% 6.3V X5R 603

31 9 PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

J2900 DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2) F-RT-THB

79 11 IN	MEM_A_CKE<0>	73	CKE0	CKE1	74	MEM_A_CKE<1>	IN 11 79
	NC	75	VDD	VDD	76		
	NC	77	NC	A15	78	MEM_A_A<15>	IN 11 79
79 11 IN	MEM_A_BA<2>	79	BA2	A14	80	MEM_A_A<14>	IN 11 79
		81	VDD	VDD	82		
79 11 IN	MEM_A_A<12>	83	A12/BC*	A11	84	MEM_A_A<11>	IN 11 79
79 11 IN	MEM_A_A<9>	85	A9	A7	86	MEM_A_A<7>	IN 11 79
		87	VDD	VDD	88		
79 11 IN	MEM_A_A<8>	89	A8	A6	90	MEM_A_A<6>	IN 11 79
79 11 IN	MEM_A_A<5>	91	A5	A4	92	MEM_A_A<4>	IN 11 79
		93	VDD	VDD	94		
79 11 IN	MEM_A_A<3>	95	A3	A2	96	MEM_A_A<2>	IN 11 79
79 11 IN	MEM_A_A<1>	97	A1	A0	98	MEM_A_A<0>	IN 11 79
		99	VDD	VDD	100		
79 11 IN	MEM_A_CLK_P<0>	101	CK0	CK1	102	MEM_A_CLK_P<1>	IN 11 79
79 11 IN	MEM_A_CLK_N<0>	103	CK0*	CK1*	104	MEM_A_CLK_N<1>	IN 11 79
		105	VDD	VDD	106		
79 11 IN	MEM_A_A<10>	107	A10/AP	BA1	108	MEM_A_BA<1>	IN 11 79
79 11 IN	MEM_A_BA<0>	109	BA0	RAS*	110	MEM_A_RAS_L	IN 11 79
		111	VDD	VDD	112		
79 11 IN	MEM_A_WE_L	113	WE*	S0*	114	MEM_A_CS_L<0>	IN 11 79
79 11 IN	MEM_A_CAS_L	115	CAS*	ODT0	116	MEM_A_ODT<0>	IN 11 79
		117	VDD	VDD	118		
79 11 IN	MEM_A_A<13>	119	A13	ODT1	120	MEM_A_ODT<1>	IN 11 79
79 11 IN	MEM_A_CS_L<1>	121	S1*	NC	122	NC	
		123	VDD	VDD	124		
NC		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
28 BI	=MEM_A_DQ<32>	129	DQ32	DQ36	130	=MEM_A_DQ<36>	BI 28
28 BI	=MEM_A_DQ<33>	131	DQ33	DQ37	132	MEM_A_DQ<37>	BI 11 28 79
		133	VSS	VSS	134		
28 BI	=MEM_A_DQS_N<4>	135	DQS4*	DM4	136	GND	IN
28 BI	=MEM_A_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	=MEM_A_DQ<38>	BI 28
28 BI	=MEM_A_DQ<34>	141	DQ34	DQ39	142	=MEM_A_DQ<39>	BI 28
28 BI	=MEM_A_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	=MEM_A_DQ<44>	BI 28
28 BI	=MEM_A_DQ<40>	147	DQ40	DQ45	148	=MEM_A_DQ<45>	BI 28
28 BI	=MEM_A_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	=MEM_A_DQS_N<5>	BI 28
IN GND		153	DM5	DQS5	154	=MEM_A_DQS_P<5>	BI 28
		155	VSS	VSS	156		
28 BI	=MEM_A_DQ<42>	157	DQ42	DQ46	158	=MEM_A_DQ<46>	BI 28
28 BI	=MEM_A_DQ<43>	159	DQ43	DQ47	160	=MEM_A_DQ<47>	BI 28
		161	VSS	VSS	162		
28 BI	=MEM_A_DQ<48>	163	DQ48	DQ52	164	=MEM_A_DQ<52>	BI 28
28 BI	=MEM_A_DQ<49>	165	DQ49	DQ53	166	=MEM_A_DQ<53>	BI 28
		167	VSS	VSS	168		
28 BI	=MEM_A_DQS_N<6>	169	DQS6*	DM6	170	GND	IN
28 BI	=MEM_A_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	=MEM_A_DQ<54>	BI 28
28 BI	=MEM_A_DQ<50>	175	DQ50	DQ55	176	=MEM_A_DQ<55>	BI 28
28 BI	=MEM_A_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	=MEM_A_DQ<60>	BI 28
28 BI	=MEM_A_DQ<56>	181	DQ56	DQ61	182	=MEM_A_DQ<61>	BI 28
28 BI	=MEM_A_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	=MEM_A_DQS_N<7>	BI 28
IN GND		187	DM7	DQS7	188	=MEM_A_DQS_P<7>	BI 28
		189	VSS	VSS	190		
28 BI	=MEM_A_DQ<58>	191	DQ58	DQ62	192	=MEM_A_DQ<62>	BI 28
28 BI	=MEM_A_DQ<59>	193	DQ59	DQ63	194	=MEM_A_DQ<63>	BI 28
		195	VSS	VSS	196		
MEM_A_SA<0>		197	SA0	EVENT*	198	MEM_EVENT_L	OD 29 45
		199	VDDSPD	SDA	200	SMBUS_PCH_DATA	BI 16 23 29 31 42 48 62 77 81
MEM_A_SA<1>		201	SA1	SCL	202	SMBUS_PCH_CLK	IN 16 23 29 31 42 48 62 77 81
		203	VTT	VTT	204	PP0V75_S0_DDRVTT	7 29 30 67

KEY

516-0229

SPD ADDR=0xA0(WR)/0xA1(RD)

73 72 71 62 61 42 41 40 72 34 PP3V3_S0
33 29 28 23 22 20 19 18 44 57 54 52 51 49 48 46 85 77 75 74

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

J2900 DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2) F-RT-THB CRITICAL

		1	VREFDQ	VSS	2		
		3	VSS	DQ4	4	=MEM_A_DQ<4>	BI 28
28 BI	=MEM_A_DQ<0>	5	DQ0	DQ5	6	=MEM_A_DQ<5>	BI 28
28 BI	=MEM_A_DQ<1>	7	DQ1	VSS	8		
		9	VSS	DQS0*	10	MEM_A_DQS_N<0>	BI 11 28 79
IN GND		11	DM0	DQS0	12	MEM_A_DQS_P<0>	BI 11 28 79
		13	VSS	VSS	14		
28 BI	=MEM_A_DQ<2>	15	DQ2	DQ6	16	=MEM_A_DQ<6>	BI 28
28 BI	=MEM_A_DQ<3>	17	DQ3	DQ7	18	=MEM_A_DQ<7>	BI 28
		19	VSS	VSS	20		
28 BI	=MEM_A_DQ<8>	21	DQ8	DQ12	22	=MEM_A_DQ<12>	BI 28
28 BI	=MEM_A_DQ<9>	23	DQ9	DQ13	24	=MEM_A_DQ<13>	BI 28
		25	VSS	VSS	26		
28 BI	=MEM_A_DQS_N<1>	27	DQS1*	DM1	28	GND	IN
28 BI	=MEM_A_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 29 30
		31	VSS	VSS	32		
28 BI	=MEM_A_DQ<10>	33	DQ10	DQ14	34	=MEM_A_DQ<14>	BI 28
28 BI	=MEM_A_DQ<11>	35	DQ11	DQ15	36	=MEM_A_DQ<15>	BI 28
		37	VSS	VSS	38		
28 BI	=MEM_A_DQ<16>	39	DQ16	DQ20	40	=MEM_A_DQ<20>	BI 28
28 BI	=MEM_A_DQ<17>	41	DQ17	DQ21	42	=MEM_A_DQ<21>	BI 28
		43	VSS	VSS	44		
28 BI	=MEM_A_DQS_N<2>	45	DQS2*	DM2	46	GND	IN
28 BI	=MEM_A_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	=MEM_A_DQ<22>	BI 28
28 BI	=MEM_A_DQ<18>	51	DQ18	DQ23	52	=MEM_A_DQ<23>	BI 28
28 BI	=MEM_A_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	=MEM_A_DQ<28>	BI 28
28 BI	=MEM_A_DQ<24>	57	DQ24	DQ29	58	=MEM_A_DQ<29>	BI 28
28 BI	=MEM_A_DQ<25>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	=MEM_A_DQS_N<3>	BI 28
IN GND		63	DM3	DQS3	64	=MEM_A_DQS_P<3>	BI 28
		65	VSS	VSS	66		
28 BI	=MEM_A_DQ<26>	67	DQ26	DQ30	68	=MEM_A_DQ<30>	BI 28
28 BI	=MEM_A_DQ<27>	69	DQ27	DQ31	70	=MEM_A_DQ<31>	BI 28
		71	VSS	VSS	72		

KEY

516-0229

31 PP0V75_S3_MEM_VREFCA_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

C2950 1UF 10% 10V X5R 402
C2951 1UF 10% 10V X5R 402
C2952 1UF 10% 10V X5R 402
C2953 1UF 10% 10V X5R 402

"Factory" (top) slot

SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

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BRANCH:
PAGE: 29 OF 109
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CPU CHANNEL A DQS 0 -> DIMM A DQS 0

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=	MEM_A_DQS_N<0>	
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=	MEM_A_DQS_P<0>	
	MAKE_BASE=TRUE	=	GND	
MEM_A_DQ<7>	MAKE_BASE=TRUE	=	=MEM_A_DQ<3>	
MEM_A_DQ<6>	MAKE_BASE=TRUE	=	=MEM_A_DQ<6>	
MEM_A_DQ<5>	MAKE_BASE=TRUE	=	=MEM_A_DQ<1>	
MEM_A_DQ<4>	MAKE_BASE=TRUE	=	=MEM_A_DQ<5>	
MEM_A_DQ<3>	MAKE_BASE=TRUE	=	=MEM_A_DQ<2>	
MEM_A_DQ<2>	MAKE_BASE=TRUE	=	=MEM_A_DQ<7>	
MEM_A_DQ<1>	MAKE_BASE=TRUE	=	=MEM_A_DQ<0>	
MEM_A_DQ<0>	MAKE_BASE=TRUE	=	=MEM_A_DQ<4>	
	MAKE_BASE=TRUE	=		

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<1>	
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<1>	
	MAKE_BASE=TRUE	=	GND	
MEM_A_DQ<15>	MAKE_BASE=TRUE	=	=MEM_A_DQ<11>	
MEM_A_DQ<14>	MAKE_BASE=TRUE	=	=MEM_A_DQ<10>	
MEM_A_DQ<13>	MAKE_BASE=TRUE	=	=MEM_A_DQ<12>	
MEM_A_DQ<12>	MAKE_BASE=TRUE	=	=MEM_A_DQ<9>	
MEM_A_DQ<11>	MAKE_BASE=TRUE	=	=MEM_A_DQ<15>	
MEM_A_DQ<10>	MAKE_BASE=TRUE	=	=MEM_A_DQ<14>	
MEM_A_DQ<9>	MAKE_BASE=TRUE	=	=MEM_A_DQ<13>	
MEM_A_DQ<8>	MAKE_BASE=TRUE	=	=MEM_A_DQ<8>	
	MAKE_BASE=TRUE	=		

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<2>	
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<2>	
	MAKE_BASE=TRUE	=	GND	
MEM_A_DQ<23>	MAKE_BASE=TRUE	=	=MEM_A_DQ<23>	
MEM_A_DQ<22>	MAKE_BASE=TRUE	=	=MEM_A_DQ<22>	
MEM_A_DQ<21>	MAKE_BASE=TRUE	=	=MEM_A_DQ<21>	
MEM_A_DQ<20>	MAKE_BASE=TRUE	=	=MEM_A_DQ<20>	
MEM_A_DQ<19>	MAKE_BASE=TRUE	=	=MEM_A_DQ<18>	
MEM_A_DQ<18>	MAKE_BASE=TRUE	=	=MEM_A_DQ<19>	
MEM_A_DQ<17>	MAKE_BASE=TRUE	=	=MEM_A_DQ<16>	
MEM_A_DQ<16>	MAKE_BASE=TRUE	=	=MEM_A_DQ<17>	
	MAKE_BASE=TRUE	=		

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<3>	
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<3>	
	MAKE_BASE=TRUE	=	GND	
MEM_A_DQ<31>	MAKE_BASE=TRUE	=	=MEM_A_DQ<26>	
MEM_A_DQ<30>	MAKE_BASE=TRUE	=	=MEM_A_DQ<24>	
MEM_A_DQ<29>	MAKE_BASE=TRUE	=	=MEM_A_DQ<28>	
MEM_A_DQ<28>	MAKE_BASE=TRUE	=	=MEM_A_DQ<25>	
MEM_A_DQ<27>	MAKE_BASE=TRUE	=	=MEM_A_DQ<31>	
MEM_A_DQ<26>	MAKE_BASE=TRUE	=	=MEM_A_DQ<27>	
MEM_A_DQ<25>	MAKE_BASE=TRUE	=	=MEM_A_DQ<30>	
MEM_A_DQ<24>	MAKE_BASE=TRUE	=	=MEM_A_DQ<29>	
	MAKE_BASE=TRUE	=		

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<4>	
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<4>	
	MAKE_BASE=TRUE	=	GND	
MEM_A_DQ<39>	MAKE_BASE=TRUE	=	=MEM_A_DQ<38>	
MEM_A_DQ<38>	MAKE_BASE=TRUE	=	=MEM_A_DQ<39>	
MEM_A_DQ<37>	MAKE_BASE=TRUE	=	MEM_A_DQ<37>	
MEM_A_DQ<36>	MAKE_BASE=TRUE	=	=MEM_A_DQ<33>	
MEM_A_DQ<35>	MAKE_BASE=TRUE	=	=MEM_A_DQ<34>	
MEM_A_DQ<34>	MAKE_BASE=TRUE	=	=MEM_A_DQ<35>	
MEM_A_DQ<33>	MAKE_BASE=TRUE	=	=MEM_A_DQ<32>	
MEM_A_DQ<32>	MAKE_BASE=TRUE	=	=MEM_A_DQ<36>	

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<5>	
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<5>	
	MAKE_BASE=TRUE	=	GND	
MEM_A_DQ<47>	MAKE_BASE=TRUE	=	=MEM_A_DQ<46>	
MEM_A_DQ<46>	MAKE_BASE=TRUE	=	=MEM_A_DQ<43>	
MEM_A_DQ<45>	MAKE_BASE=TRUE	=	=MEM_A_DQ<45>	
MEM_A_DQ<44>	MAKE_BASE=TRUE	=	=MEM_A_DQ<41>	
MEM_A_DQ<43>	MAKE_BASE=TRUE	=	=MEM_A_DQ<47>	
MEM_A_DQ<42>	MAKE_BASE=TRUE	=	=MEM_A_DQ<42>	
MEM_A_DQ<41>	MAKE_BASE=TRUE	=	=MEM_A_DQ<40>	
MEM_A_DQ<40>	MAKE_BASE=TRUE	=	=MEM_A_DQ<44>	
	MAKE_BASE=TRUE	=		

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<6>	
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<6>	
	MAKE_BASE=TRUE	=	GND	
MEM_A_DQ<55>	MAKE_BASE=TRUE	=	=MEM_A_DQ<51>	
MEM_A_DQ<54>	MAKE_BASE=TRUE	=	=MEM_A_DQ<54>	
MEM_A_DQ<53>	MAKE_BASE=TRUE	=	=MEM_A_DQ<49>	
MEM_A_DQ<52>	MAKE_BASE=TRUE	=	=MEM_A_DQ<53>	
MEM_A_DQ<51>	MAKE_BASE=TRUE	=	=MEM_A_DQ<50>	
MEM_A_DQ<50>	MAKE_BASE=TRUE	=	=MEM_A_DQ<55>	
MEM_A_DQ<49>	MAKE_BASE=TRUE	=	=MEM_A_DQ<48>	
MEM_A_DQ<48>	MAKE_BASE=TRUE	=	=MEM_A_DQ<52>	
	MAKE_BASE=TRUE	=		

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<7>	
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<7>	
	MAKE_BASE=TRUE	=	GND	
MEM_A_DQ<63>	MAKE_BASE=TRUE	=	=MEM_A_DQ<58>	
MEM_A_DQ<62>	MAKE_BASE=TRUE	=	=MEM_A_DQ<59>	
MEM_A_DQ<61>	MAKE_BASE=TRUE	=	=MEM_A_DQ<60>	
MEM_A_DQ<60>	MAKE_BASE=TRUE	=	=MEM_A_DQ<57>	
MEM_A_DQ<59>	MAKE_BASE=TRUE	=	=MEM_A_DQ<63>	
MEM_A_DQ<58>	MAKE_BASE=TRUE	=	=MEM_A_DQ<62>	
MEM_A_DQ<57>	MAKE_BASE=TRUE	=	=MEM_A_DQ<61>	
MEM_A_DQ<56>	MAKE_BASE=TRUE	=	=MEM_A_DQ<56>	
	MAKE_BASE=TRUE	=		

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=	MEM_B_DQS_N<0>	
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=	MEM_B_DQS_P<0>	
	MAKE_BASE=TRUE	=	GND	
MEM_B_DQ<7>	MAKE_BASE=TRUE	=	=MEM_B_DQ<3>	
MEM_B_DQ<6>	MAKE_BASE=TRUE	=	=MEM_B_DQ<2>	
MEM_B_DQ<5>	MAKE_BASE=TRUE	=	=MEM_B_DQ<0>	
MEM_B_DQ<4>	MAKE_BASE=TRUE	=	=MEM_B_DQ<4>	
MEM_B_DQ<3>	MAKE_BASE=TRUE	=	=MEM_B_DQ<7>	
MEM_B_DQ<2>	MAKE_BASE=TRUE	=	=MEM_B_DQ<6>	
MEM_B_DQ<1>	MAKE_BASE=TRUE	=	=MEM_B_DQ<5>	
MEM_B_DQ<0>	MAKE_BASE=TRUE	=	=MEM_B_DQ<1>	
	MAKE_BASE=TRUE	=		

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<1>	
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<1>	
	MAKE_BASE=TRUE	=	GND	
MEM_B_DQ<15>	MAKE_BASE=TRUE	=	=MEM_B_DQ<15>	
MEM_B_DQ<14>	MAKE_BASE=TRUE	=	=MEM_B_DQ<14>	
MEM_B_DQ<13>	MAKE_BASE=TRUE	=	=MEM_B_DQ<13>	
MEM_B_DQ<12>	MAKE_BASE=TRUE	=	=MEM_B_DQ<8>	
MEM_B_DQ<11>	MAKE_BASE=TRUE	=	=MEM_B_DQ<11>	
MEM_B_DQ<10>	MAKE_BASE=TRUE	=	=MEM_B_DQ<10>	
MEM_B_DQ<9>	MAKE_BASE=TRUE	=	=MEM_B_DQ<12>	
MEM_B_DQ<8>	MAKE_BASE=TRUE	=	=MEM_B_DQ<9>	
	MAKE_BASE=TRUE	=		

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<2>	
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<2>	
	MAKE_BASE=TRUE	=	GND	
MEM_B_DQ<23>	MAKE_BASE=TRUE	=	=MEM_B_DQ<23>	
MEM_B_DQ<22>	MAKE_BASE=TRUE	=	=MEM_B_DQ<18>	
MEM_B_DQ<21>	MAKE_BASE=TRUE	=	=MEM_B_DQ<16>	
MEM_B_DQ<20>	MAKE_BASE=TRUE	=	=MEM_B_DQ<17>	
MEM_B_DQ<19>	MAKE_BASE=TRUE	=	=MEM_B_DQ<22>	
MEM_B_DQ<18>	MAKE_BASE=TRUE	=	=MEM_B_DQ<19>	
MEM_B_DQ<17>	MAKE_BASE=TRUE	=	=MEM_B_DQ<21>	
MEM_B_DQ<16>	MAKE_BASE=TRUE	=	=MEM_B_DQ<20>	
	MAKE_BASE=TRUE	=		

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<3>	
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<3>	
	MAKE_BASE=TRUE	=	GND	
MEM_B_DQ<31>	MAKE_BASE=TRUE	=	=MEM_B_DQ<26>	
MEM_B_DQ<30>	MAKE_BASE=TRUE	=	=MEM_B_DQ<30>	
MEM_B_DQ<29>	MAKE_BASE=TRUE	=	=MEM_B_DQ<28>	
MEM_B_DQ<28>	MAKE_BASE=TRUE	=	=MEM_B_DQ<29>	
MEM_B_DQ<27>	MAKE_BASE=TRUE	=	=MEM_B_DQ<27>	
MEM_B_DQ<26>	MAKE_BASE=TRUE	=	=MEM_B_DQ<31>	
MEM_B_DQ<25>	MAKE_BASE=TRUE	=	=MEM_B_DQ<25>	
MEM_B_DQ<24>	MAKE_BASE=TRUE	=	=MEM_B_DQ<24>	
	MAKE_BASE=TRUE	=		

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<4>	
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<4>	
	MAKE_BASE=TRUE	=	GND	
MEM_B_DQ<39>	MAKE_BASE=TRUE	=	=MEM_B_DQ<38>	
MEM_B_DQ<38>	MAKE_BASE=TRUE	=	=MEM_B_DQ<39>	
MEM_B_DQ<37>	MAKE_BASE=TRUE	=	MEM_B_DQ<37>	
MEM_B_DQ<36>	MAKE_BASE=TRUE	=	=MEM_B_DQ<37>	
MEM_B_DQ<35>	MAKE_BASE=TRUE	=	=MEM_B_DQ<34>	
MEM_B_DQ<34>	MAKE_BASE=TRUE	=	=MEM_B_DQ<35>	
MEM_B_DQ<33>	MAKE_BASE=TRUE	=	=MEM_B_DQ<32>	
MEM_B_DQ<32>	MAKE_BASE=TRUE	=	=MEM_B_DQ<36>	

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<5>	
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<5>	
	MAKE_BASE=TRUE	=	GND	
MEM_B_DQ<47>	MAKE_BASE=TRUE	=	=MEM_B_DQ<43>	
MEM_B_DQ<46>	MAKE_BASE=TRUE	=	=MEM_B_DQ<46>	
MEM_B_DQ<45>	MAKE_BASE=TRUE	=	=MEM_B_DQ<40>	
MEM_B_DQ<44>	MAKE_BASE=TRUE	=	=MEM_B_DQ<45>	
MEM_B_DQ<43>	MAKE_BASE=TRUE	=	=MEM_B_DQ<47>	
MEM_B_DQ<42>	MAKE_BASE=TRUE	=	=MEM_B_DQ<42>	
MEM_B_DQ<41>	MAKE_BASE=TRUE	=	=MEM_B_DQ<41>	
MEM_B_DQ<40>	MAKE_BASE=TRUE	=	=MEM_B_DQ<44>	
	MAKE_BASE=TRUE	=		

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<6>	
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<6>	
	MAKE_BASE=TRUE	=	GND	
MEM_B_DQ<55>	MAKE_BASE=TRUE	=	=MEM_B_DQ<54>	
MEM_B_DQ<54>	MAKE_BASE=TRUE	=	=MEM_B_DQ<55>	
MEM_B_DQ<53>	MAKE_BASE=TRUE	=	=MEM_B_DQ<53>	
MEM_B_DQ<52>	MAKE_BASE=TRUE	=	=MEM_B_DQ<49>	
MEM_B_DQ<51>	MAKE_BASE=TRUE	=	=MEM_B_DQ<51>	
MEM_B_DQ<50>	MAKE_BASE=TRUE	=	=MEM_B_DQ<50>	
MEM_B_DQ<49>	MAKE_BASE=TRUE	=	=MEM_B_DQ<48>	
MEM_B_DQ<48>	MAKE_BASE=TRUE	=	=MEM_B_DQ<52>	
	MAKE_BASE=TRUE	=		

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<7>	
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<7>	
	MAKE_BASE=TRUE	=	GND	
MEM_B_DQ<63>	MAKE_BASE=TRUE	=	=MEM_B_DQ<56>	
MEM_B_DQ<62>	MAKE_BASE=TRUE	=	=MEM_B_DQ<59>	
MEM_B_DQ<61>	MAKE_BASE=TRUE	=	=MEM_B_DQ<61>	
MEM_B_DQ<60>	MAKE_BASE=TRUE	=	=MEM_B_DQ<60>	
MEM_B_DQ<59>	MAKE_BASE=TRUE	=	=MEM_B_DQ<63>	
MEM_B_DQ<58>	MAKE_BASE=TRUE	=	=MEM_B_DQ<58>	
MEM_B_DQ<57>	MAKE_BASE=TRUE	=	=MEM_B_DQ<57>	
MEM_B_DQ<56>	MAKE_BASE=TRUE	=	=MEM_B_DQ<62>	
	MAKE_BASE=TRUE	=		

NOTE: Sandybridge does not use DM signals per doc 438297 Huron River SFF DG rev1.0 Section 2.6.13

SYNC MASTER=ANNE K90I SYNC DATE=06/22/2010

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_S
- =PP1V5_S3_MEM_S
- =PP0V75_S0_MEM_VTT_S
- =PPEFO_S0_MEM_S (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

ROM options provided by this page:
(NONE)

72 67 30 27 7 6 PP1V5_S3

C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603

31 9 PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 DDR3-SODIMM (2 OF 2) F-RT-BGA6

79 11 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 11 79
	NC	75	VDD	VDD	76		
		77	NC	A15	78	MEM_B_A<15>	IN 11 79
79 11 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 11 79
		81	VDD	VDD	82		
79 11 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 11 79
79 11 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 11 79
		87	VDD	VDD	88		
79 11 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 11 79
79 11 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 11 79
		93	VDD	VDD	94		
79 11 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 11 79
79 11 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 11 79
		99	VDD	VDD	100		
79 11 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 11 79
79 11 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 11 79
		105	VDD	VDD	106		
79 11 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 11 79
79 11 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 11 79
		111	VDD	VDD	112		
79 11 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 11 79
79 11 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 11 79
		117	VDD	VDD	118		
79 11 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 11 79
79 11 IN	MEM_B_CS_L<1>	121	S1*	NC	122	NC	
		123	VDD	VDD	124		
NC		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
28 BI	=MEM_B_DQ<32>	129	DQ32	DQ36	130	=MEM_B_DQ<36>	BI 28
79 28 11 BI	MEM_B_DQ<37>	131	DQ33	DQ37	132	=MEM_B_DQ<37>	BI 28
		133	VSS	VSS	134		
28 BI	=MEM_B_DQS_N<4>	135	DQS4*	DM4	136	GND	IN
28 BI	=MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	=MEM_B_DQ<38>	BI 28
28 BI	=MEM_B_DQ<34>	141	DQ34	DQ39	142	=MEM_B_DQ<39>	BI 28
28 BI	=MEM_B_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	=MEM_B_DQ<44>	BI 28
28 BI	=MEM_B_DQ<40>	147	DQ40	DQ45	148	=MEM_B_DQ<45>	BI 28
28 BI	=MEM_B_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	=MEM_B_DQS_N<5>	BI 28
IN	GND	153	DM5	DQS5	154	=MEM_B_DQS_P<5>	BI 28
		155	VSS	VSS	156		
28 BI	=MEM_B_DQ<42>	157	DQ42	DQ46	158	=MEM_B_DQ<46>	BI 28
28 BI	=MEM_B_DQ<43>	159	DQ43	DQ47	160	=MEM_B_DQ<47>	BI 28
		161	VSS	VSS	162		
28 BI	=MEM_B_DQ<48>	163	DQ48	DQ52	164	=MEM_B_DQ<52>	BI 28
28 BI	=MEM_B_DQ<49>	165	DQ49	DQ53	166	=MEM_B_DQ<53>	BI 28
		167	VSS	VSS	168		
28 BI	=MEM_B_DQS_N<6>	169	DQS6*	DM6	170	GND	IN
28 BI	=MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	=MEM_B_DQ<54>	BI 28
28 BI	=MEM_B_DQ<50>	175	DQ50	DQ55	176	=MEM_B_DQ<55>	BI 28
28 BI	=MEM_B_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	=MEM_B_DQ<60>	BI 28
28 BI	=MEM_B_DQ<56>	181	DQ56	DQ61	182	=MEM_B_DQ<61>	BI 28
28 BI	=MEM_B_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	=MEM_B_DQS_N<7>	BI 28
IN	GND	187	DM7	DQS7	188	=MEM_B_DQS_P<7>	BI 28
		189	VSS	VSS	190		
28 BI	=MEM_B_DQ<58>	191	DQ58	DQ62	192	=MEM_B_DQ<62>	BI 28
28 BI	=MEM_B_DQ<59>	193	DQ59	DQ63	194	=MEM_B_DQ<63>	BI 28
		195	VSS	VSS	196		
	MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	OUT 27 45
		199	VDDSPD	SDA	200	SMBUS_PCH_DATA	BI 16 23 27 31 42 48 62 77 81
	MEM_B_SA<1>	201	SA1	SCL	202	SMBUS_PCH_CLK	IN 16 23 27 31 42 48 62 77 81
		203	VTT	VTT	204		
	MTG PINS	205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

516S0806
SPD ADDR=0xA4(WR)/0xA5(RD)

J3100 DDR3-SODIMM (1 OF 2) F-RT-BGA6

		1	VREFDQ	VSS	2		
28 BI	=MEM_B_DQ<0>	3	VSS	DQ4	4	=MEM_B_DQ<4>	BI 28
28 BI	=MEM_B_DQ<1>	5	DQ0	DQ5	6	=MEM_B_DQ<5>	BI 28
		7	DQ1	VSS	8		
IN	GND	9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 11 28 79
		11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 11 28 79
		13	VSS	VSS	14		
28 BI	=MEM_B_DQ<2>	15	DQ2	DQ6	16	=MEM_B_DQ<6>	BI 28
28 BI	=MEM_B_DQ<3>	17	DQ3	DQ7	18	=MEM_B_DQ<7>	BI 28
		19	VSS	VSS	20		
28 BI	=MEM_B_DQ<8>	21	DQ8	DQ12	22	=MEM_B_DQ<12>	BI 28
28 BI	=MEM_B_DQ<9>	23	DQ9	DQ13	24	=MEM_B_DQ<13>	BI 28
		25	VSS	VSS	26		
28 BI	=MEM_B_DQS_N<1>	27	DQS1*	DM1	28	GND	IN
28 BI	=MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 27 30
		31	VSS	VSS	32		
28 BI	=MEM_B_DQ<10>	33	DQ10	DQ14	34	=MEM_B_DQ<14>	BI 28
28 BI	=MEM_B_DQ<11>	35	DQ11	DQ15	36	=MEM_B_DQ<15>	BI 28
		37	VSS	VSS	38		
28 BI	=MEM_B_DQ<16>	39	DQ16	DQ20	40	=MEM_B_DQ<20>	BI 28
28 BI	=MEM_B_DQ<17>	41	DQ17	DQ21	42	=MEM_B_DQ<21>	BI 28
		43	VSS	VSS	44		
28 BI	=MEM_B_DQS_N<2>	45	DQS2*	DM2	46	GND	IN
28 BI	=MEM_B_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	=MEM_B_DQ<22>	BI 28
28 BI	=MEM_B_DQ<18>	51	DQ18	DQ23	52	=MEM_B_DQ<23>	BI 28
28 BI	=MEM_B_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	=MEM_B_DQ<28>	BI 28
28 BI	=MEM_B_DQ<24>	57	DQ24	DQ29	58	=MEM_B_DQ<29>	BI 28
28 BI	=MEM_B_DQ<25>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	=MEM_B_DQS_N<3>	BI 28
IN	GND	63	DM3	DQS3	64	=MEM_B_DQS_P<3>	BI 28
		65	VSS	VSS	66		
28 BI	=MEM_B_DQ<26>	67	DQ26	DQ30	68	=MEM_B_DQ<30>	BI 28
28 BI	=MEM_B_DQ<27>	69	DQ27	DQ31	70	=MEM_B_DQ<31>	BI 28
		71	VSS	VSS	72		

KEY

516S0806

PP0V75_S3_MEM_VREFCA_B 31

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

85 77 75 74 73 49 48 46 42 41 40 PP3V3_S0
32 30 23 21 19 18 16 14 12 8 7 6
72 71 62 61 57 54 52 51 50

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

PP0V75_S0_DDRVTT 7 27 30 67

C3150 1UF 10% 10V X5R 402
C3151 1UF 10% 10V X5R 402
C3152 1UF 10% 10V X5R 402
C3153 1UF 10% 10V X5R 402

"Expansion" (bottom) slot

SYNC MASTER=MASTER SYNC DATE=MASTER
PAGE TITLE
DDR3 SO-DIMM Connector B

Apple Inc.

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SIZE D
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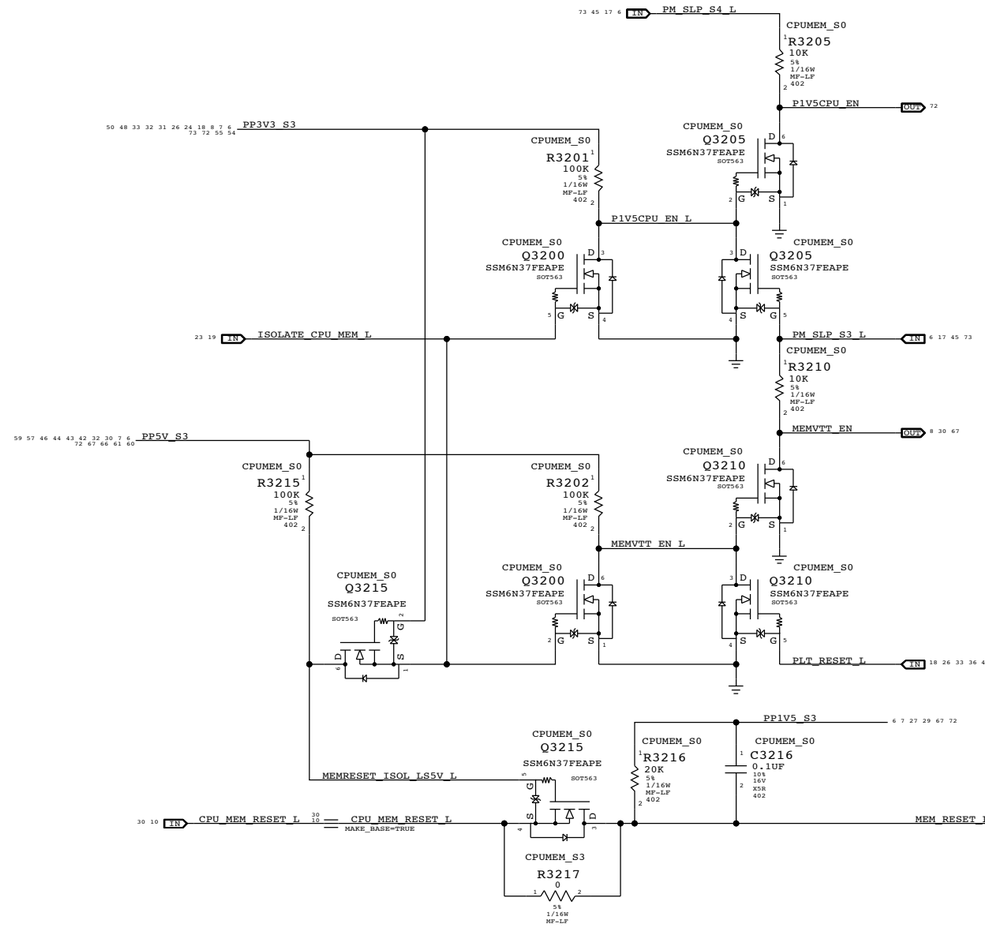
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well
as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN   = (ISOLATE_CPU_MEM_L + PLT_RST_L)   * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

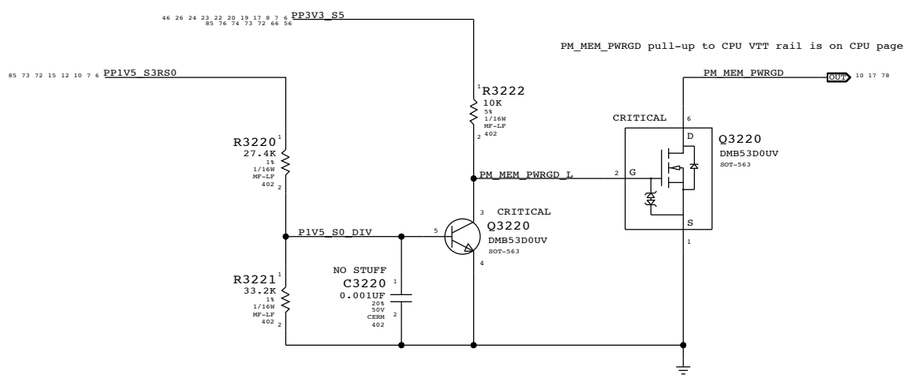


	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
to	3	0	0	0	1	X	1	0	0
S0	4	0	0	1	1	X	1	0	1
	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

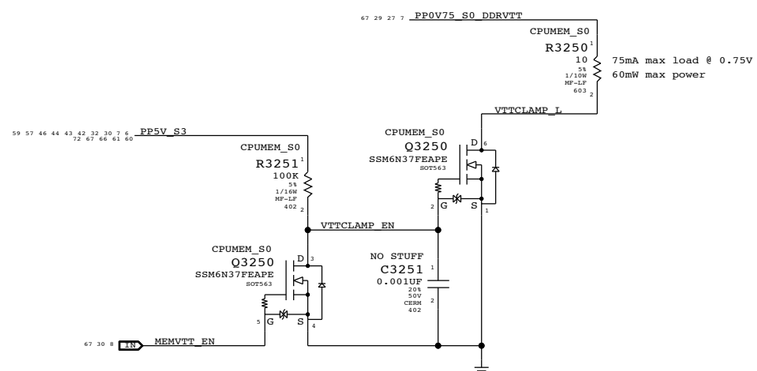
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC MASTER=ANNE K90I SYNC DATE=06/22/2010

PAGE TITLE

CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

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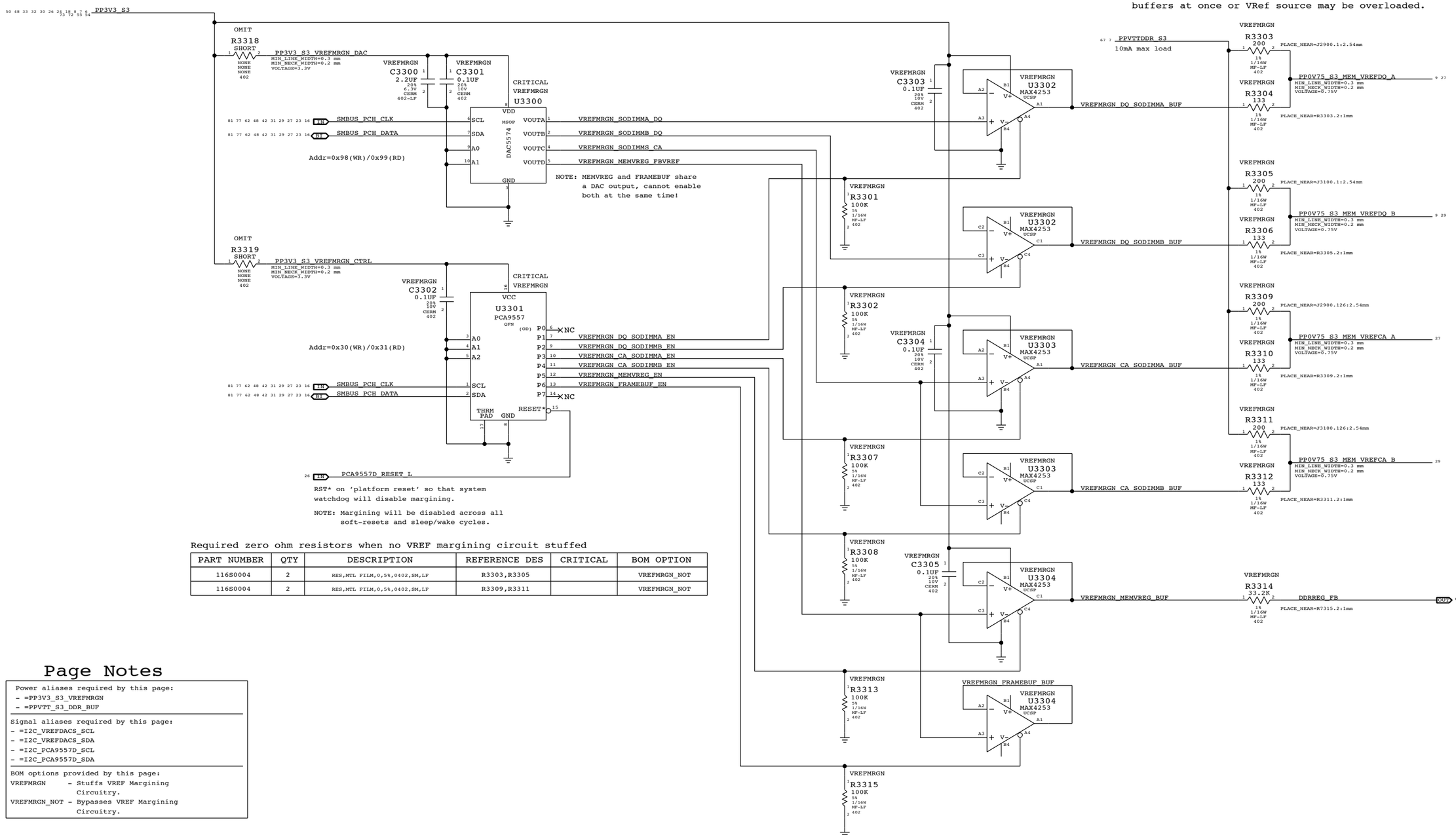

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=K91 MLB
SYNC DATE=06/01/2010
PAGE TITLE
FSB/DDR3/FRAMEBUF Vref Margining
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SIZE D
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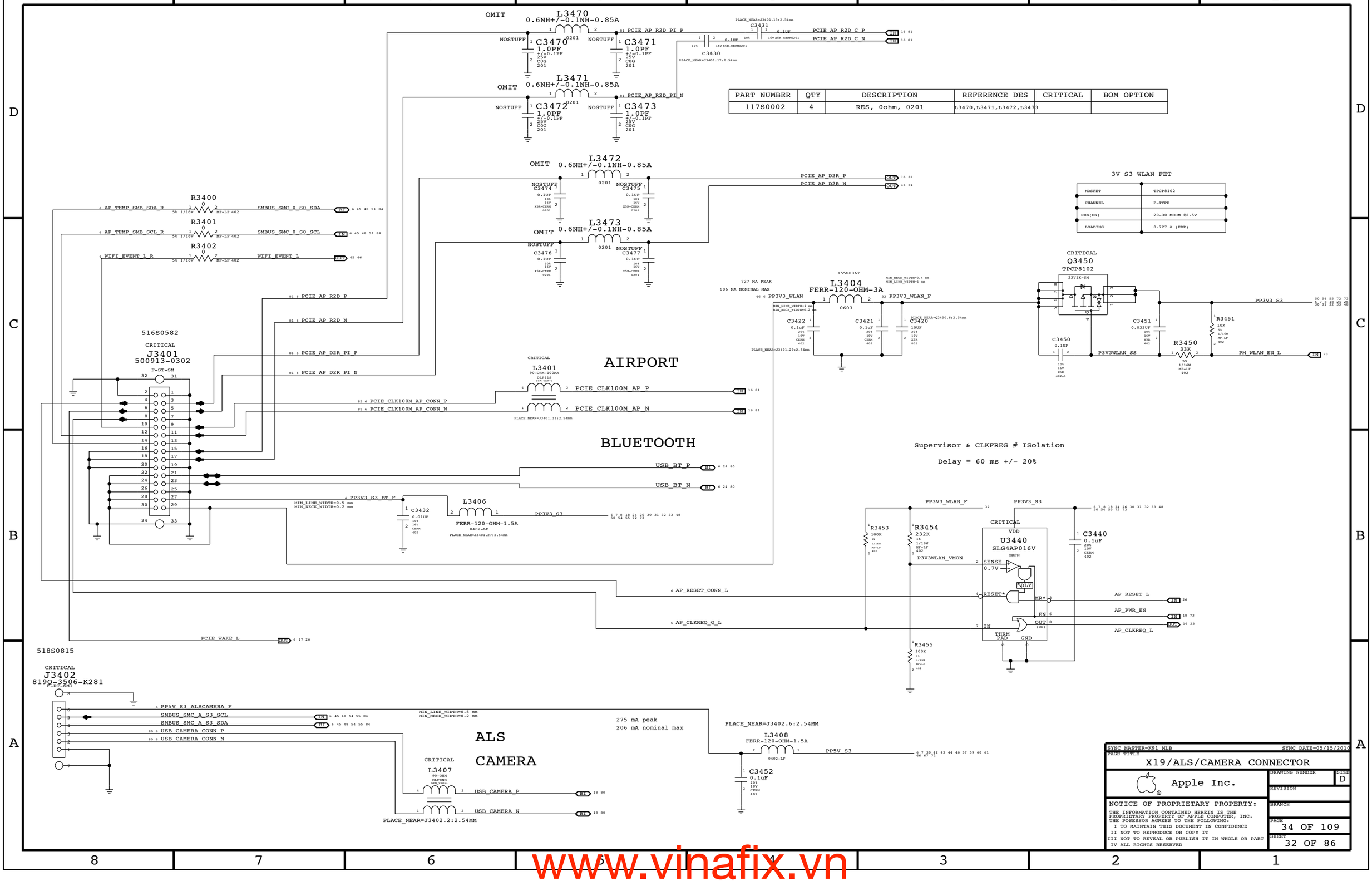
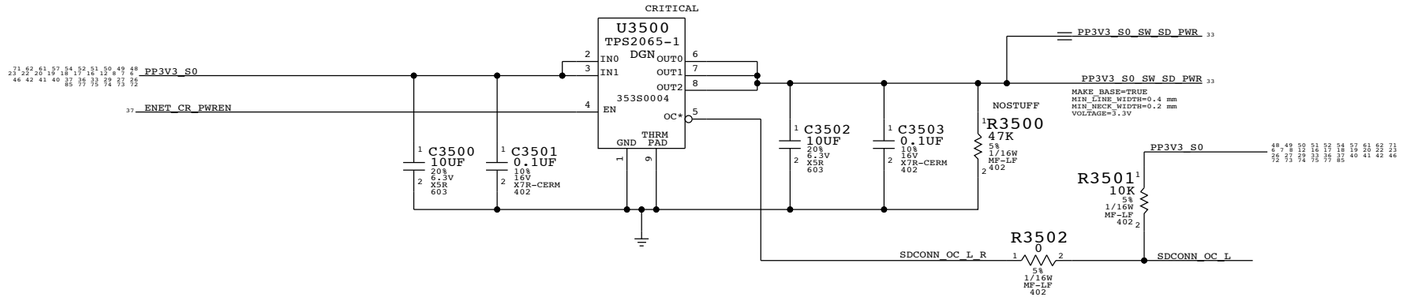


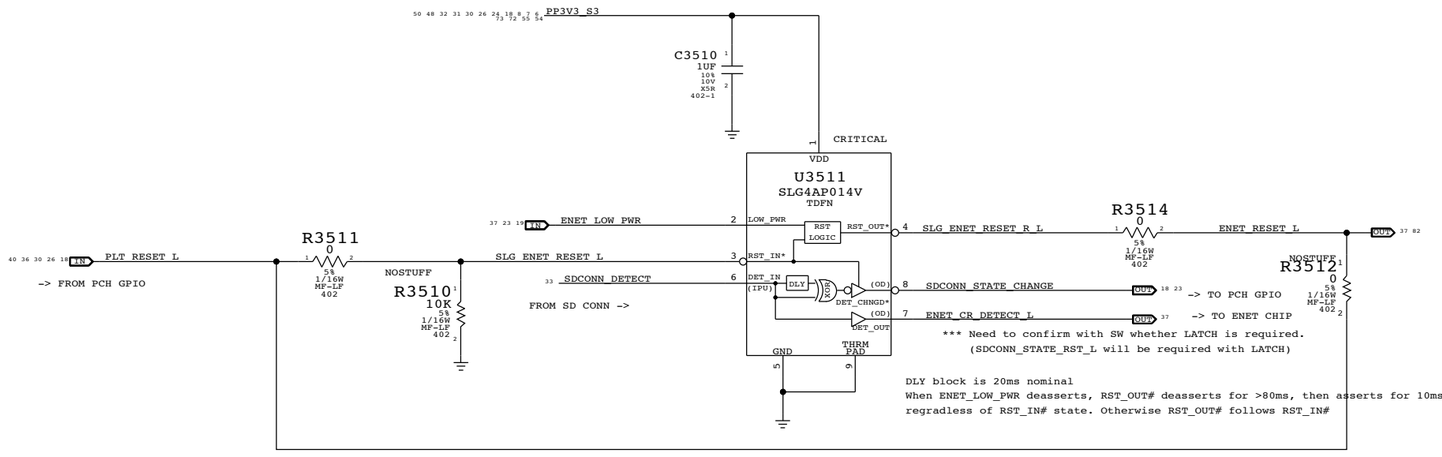
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0ohm, 0201	L3470,L3471,L3472,L3473		

SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

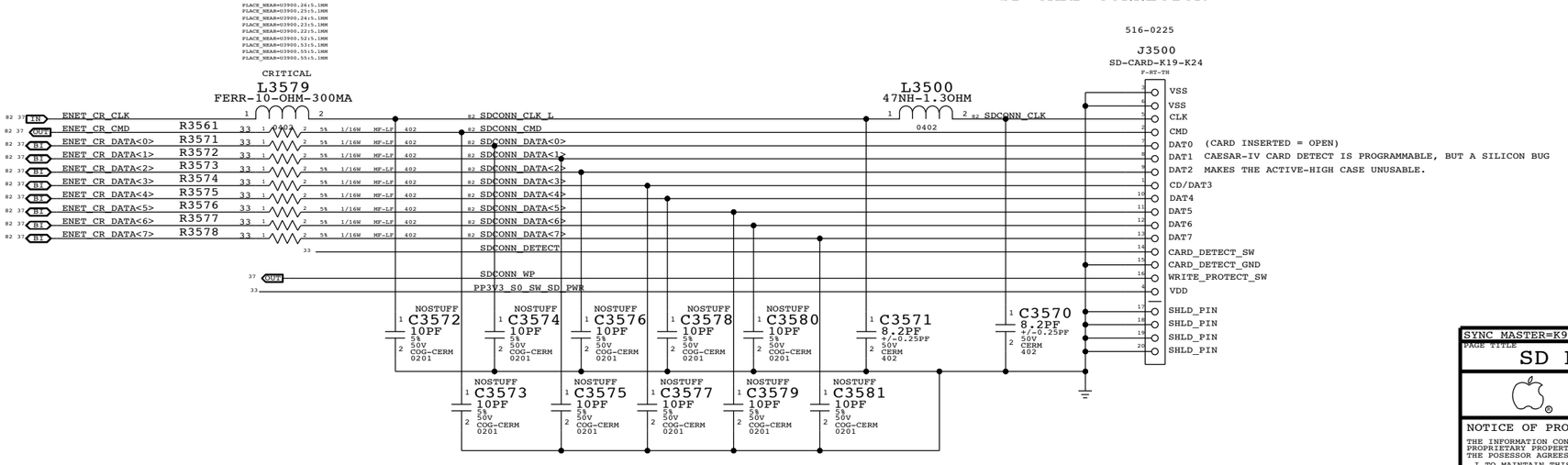
TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SD CARD CONNECTOR



SYNC_MASTER=K91_MLB SYNC_DATE=05/26/2010

PAGE TITLE: SD READER CONNECTOR

Apple Inc.

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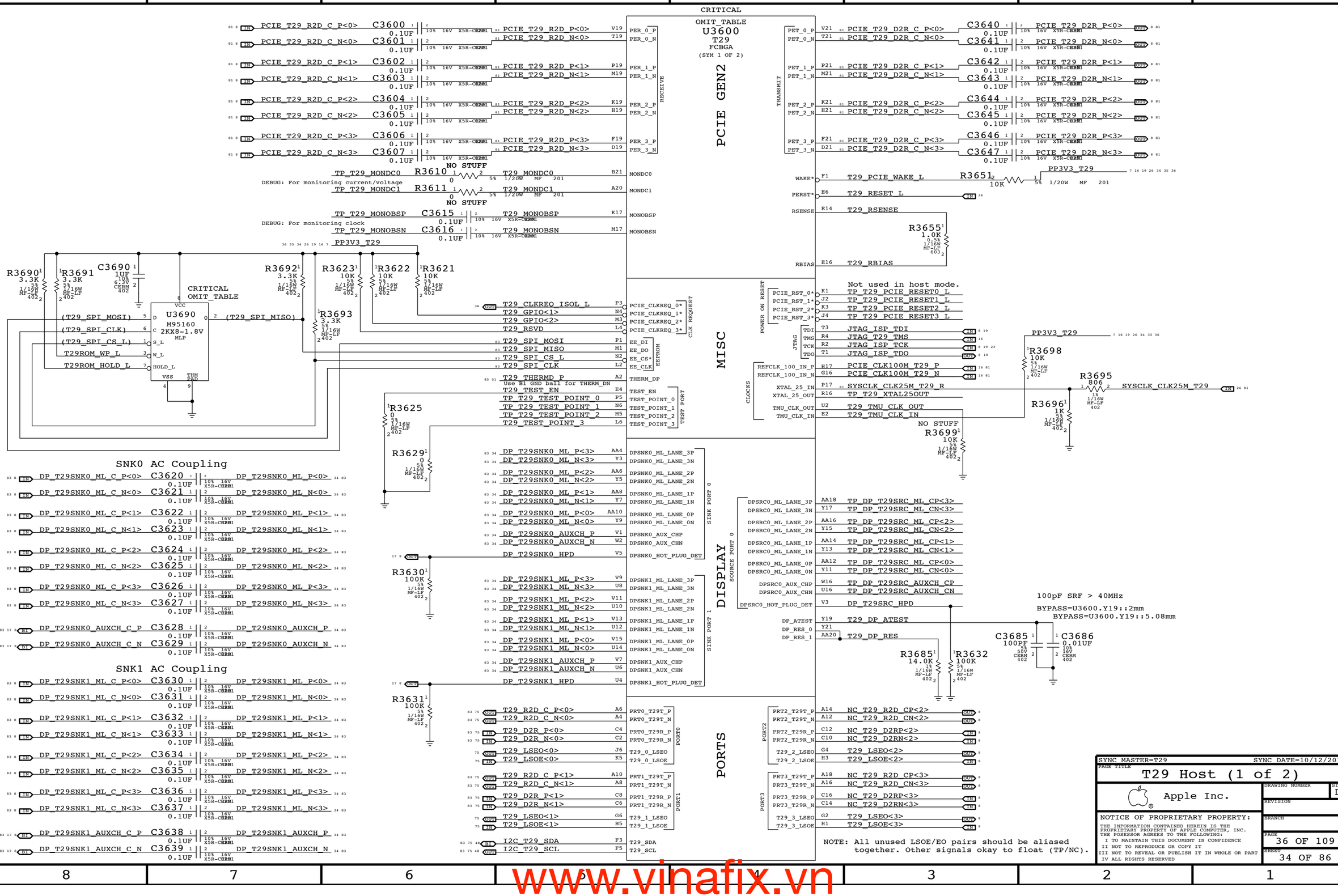

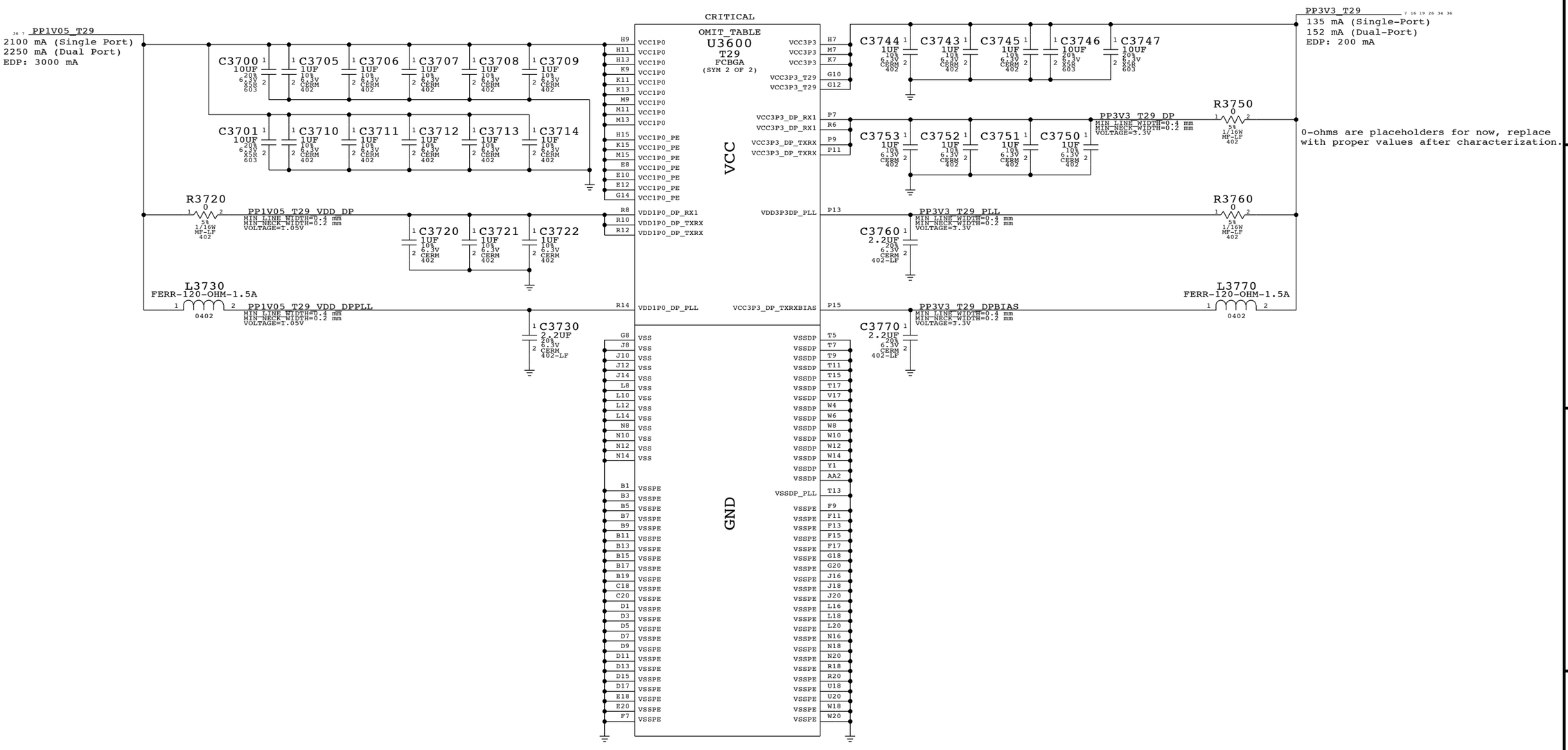

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29 SYNC_DATE=10/12/2010

PAGE TITLE: T29 Host (2 of 2)

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

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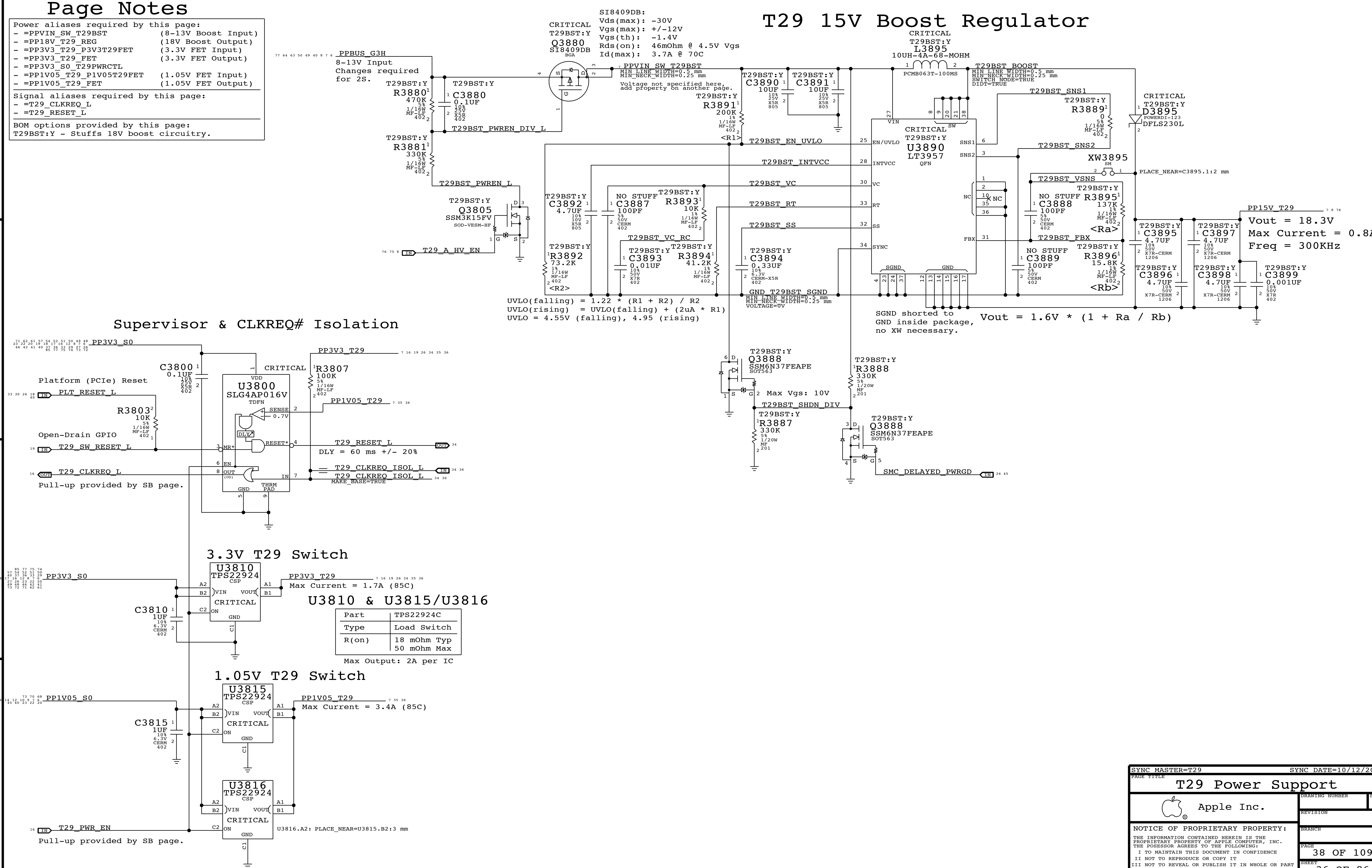
Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

T29 15V Boost Regulator



U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

SYNC_MASTER=T29 SYNC_DATE=10/12/2010

T29 Power Support

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:

SIZE D

BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

73 71 37 26 7 6 PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
37 PP3V3R1V8_ENET_LR_OUT_REG

CRITICAL L3900 FERR-600-OHM-0.5A
PP3V3_S3_ENET_PHY_XTALVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C3900 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3905 FERR-600-OHM-0.5A
PP3V3_S3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3910 FERR-600-OHM-0.5A
PP3V3_S3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 402
C3911 0.1UF 10% 16V X7R-CERM 402

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

72 71 62 61 57 54 52 51 50 49 23 22 20 19 18 17 16 12 8 7 5 48 46 42 41 40 36 33 29 27 26 85 77 75 74 73 PP3V3_S0

R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

C3950 0.1uF 10% 16V X5R 402
C3951 0.1uF 10% 16V X5R 402
C3955 0.1uF 10% 16V X5R 402
C3956 0.1uF 10% 16V X5R 402

81 16 OUT PCIE_ENET_D2R_N
81 16 OUT PCIE_ENET_D2R_P
81 16 IN PCIE_ENET_R2D_C_P
81 16 IN PCIE_ENET_R2D_C_N

R3943 0 5% 1/16W MF-LF 402
26 OUT ENET_WAKE_L
(See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

BCM57765_VMAIN_PRSNT → 58 VMAIN_PRSNT (IPD)
81 PCIE_ENET_D2R_C_N → 27 PCIE_TXD_N
81 PCIE_ENET_D2R_C_P → 28 PCIE_TXD_P
81 PCIE_ENET_R2D_P → 33 PCIE_RXD_P
81 PCIE_ENET_R2D_N → 34 PCIE_RXD_N
81 16 IN PCIE_CLK100M_ENET_P → 31 PCIE_REFCLK_P
81 16 IN PCIE_CLK100M_ENET_N → 30 PCIE_REFCLK_N
82 33 IN ENET_RESET_L → 11 PERST* (IPD)
16 OUT ENET_CLKREQ_L → 12 CLKREQ* (OD)
BCM57765_WAKE_R_L → 3 WAKE* (OD)
33 23 19 IN ENET_LOW_PWR → 4 LOW_PWR (IPD)
BCM57765_SMB_CLK → 6 SMB_CLK
BCM57765_SMB_DATA → 10 SMD_DATA (IPD)
37 BI BCM57765_SCLK → 66 SCLK
37 IN BCM57765_MISO → 64 SI/LINKLED*
37 BI BCM57765_MOSI → 65 SO
37 BI BCM57765_CS_L → 63 CS*
TP_BCM57765_SPD100LED_L → 2 SPD100LED*/SERIAL_DO (OD)
8 OUT TP_BCM57765_TRAFFICLED_L → 67 TRAFFICLED*/SERIAL_DI (OD)
81 24 IN SYSCLK_CLK25M_ENET → 18 XTALI
NC → 19 XTALO
BCM57765_RDAC → 38 RDAC

R3965 1.24K 1% 1/16W MF-LF 402

ENET_SR_LX 71
ENET_SR_VFB 71

Internal 1.2V Switching Regulator pins.

OMIT
U3900
BCM57765
QFN-8X8

AVDDH 42 48
BIASVDDH 37
XTALVDDH 17
VDDO 7 20 56 62
SR_VDD 14
SR_VDDP 15
SR_LX 16
SR_VFB 13
AVDDL 39 45 51
PCIE_PLLVDDL 29 32
GPHY_PLLVDDL 36
VDDC 35 61
THRM_PAD 69

PP1V2_S3_ENET_INTREG 6 71
???mA (1000base-T, Caesar V)

CRITICAL L3920 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3921 0.1UF 10% 16V X7R-CERM 402
C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3925 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3926 0.1UF 10% 16V X7R-CERM 402
C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3930 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3931 0.1UF 10% 16V X7R-CERM 402
C3930 4.7UF 10% 6.3V X5R-CERM 603

C3936 0.1UF 10% 16V X7R-CERM 402
C3935 10UF 10% 6.3V X5R 805

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

PP3V3R1V8_ENET_LR_OUT_REG 37
PP3V3R1V8_ENET_LR_OUT_REG 37
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V MAKE_TRACE=BLUE
C3970 4.7UF 10% 6.3V X5R-CERM 603
C3971 0.1UF 10% 16V X7R-CERM 402
C3972 0.1UF 10% 16V X7R-CERM 402

TRD0_P 40 ENET_MDI_P<0> BI 38 82
TRD0_N 41 ENET_MDI_N<0> BI 38 82
TRD1_P 44 ENET_MDI_P<1> BI 38 82
TRD1_N 43 ENET_MDI_N<1> BI 38 82
TRD2_P 46 ENET_MDI_P<2> BI 38 82
TRD2_N 47 ENET_MDI_N<2> BI 38 82
TRD3_P 50 ENET_MDI_P<3> BI 38 82
TRD3_N 49 ENET_MDI_N<3> BI 38 82

(IPD) GPIO_0 5 NC
GPIO_1/CR_BUS_PWR 8
RE*/GPIO_2 9 ENET_MEDIA_SENSE OUT 26
(IPU) SD_DETECT/WE* 1 ENET_CR_DETECT_L IN 33
(IPU) CR_CMD/CLE 26 ENET_CR_CMD IN 33 82
CR_CLK/RY_BY* 21 ENET_CR_CLK OUT 33 82

(IPD)
CR_DATA0 25 ENET_CR_DATA<0> BI 33 82
CR_DATA1 24 ENET_CR_DATA<1> BI 33 82
CR_DATA2 23 ENET_CR_DATA<2> BI 33 82
CR_DATA3 22 ENET_CR_DATA<3> BI 33 82
CR_DATA4 52 ENET_CR_DATA<4> BI 33 82
CR_DATA5 53 ENET_CR_DATA<5> BI 33 82
CR_DATA6 54 ENET_CR_DATA<6> BI 33 82
CR_DATA7 55 ENET_CR_DATA<7> BI 33 82

(IPU) CE*/MS_INS* 59 NC_BCM57765_CE_L_MS_INS_L NO_TEST=TRUE
CR_LED/ALE 60 ENET_CR_PWREN OUT 33
CR_WP*/XD_WP* 57 SDCONN_WP IN 33
XD_DETECT 68 BDM57765_SR_DISABLE R3980 1K 5% 1/16W MF-LF 402

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT can only be used active low due to errata.

ENET 1.2V SR IS ENABLED IF SR_DISABLE is PULLed-DOWN.

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET supports both active-levels for WP.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.
(Required ROM size TBD)

73 71 37 26 7 6 PP3V3_ENET

U3990 AT45DB011D SOIC-8S1 OMIT
VCC 8
SCK 2
CS* 4
WP* 5
RESET* 3
GND 7
SI 1
SO 8

C3990 0.1UF 10% 16V X7R-CERM 402

37 IN BCM57765_SCLK
37 IN BCM57765_CS_L
BCM57765_MOSI IN 37
BCM57765_MISO OUT 37

NOSTUFF
R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

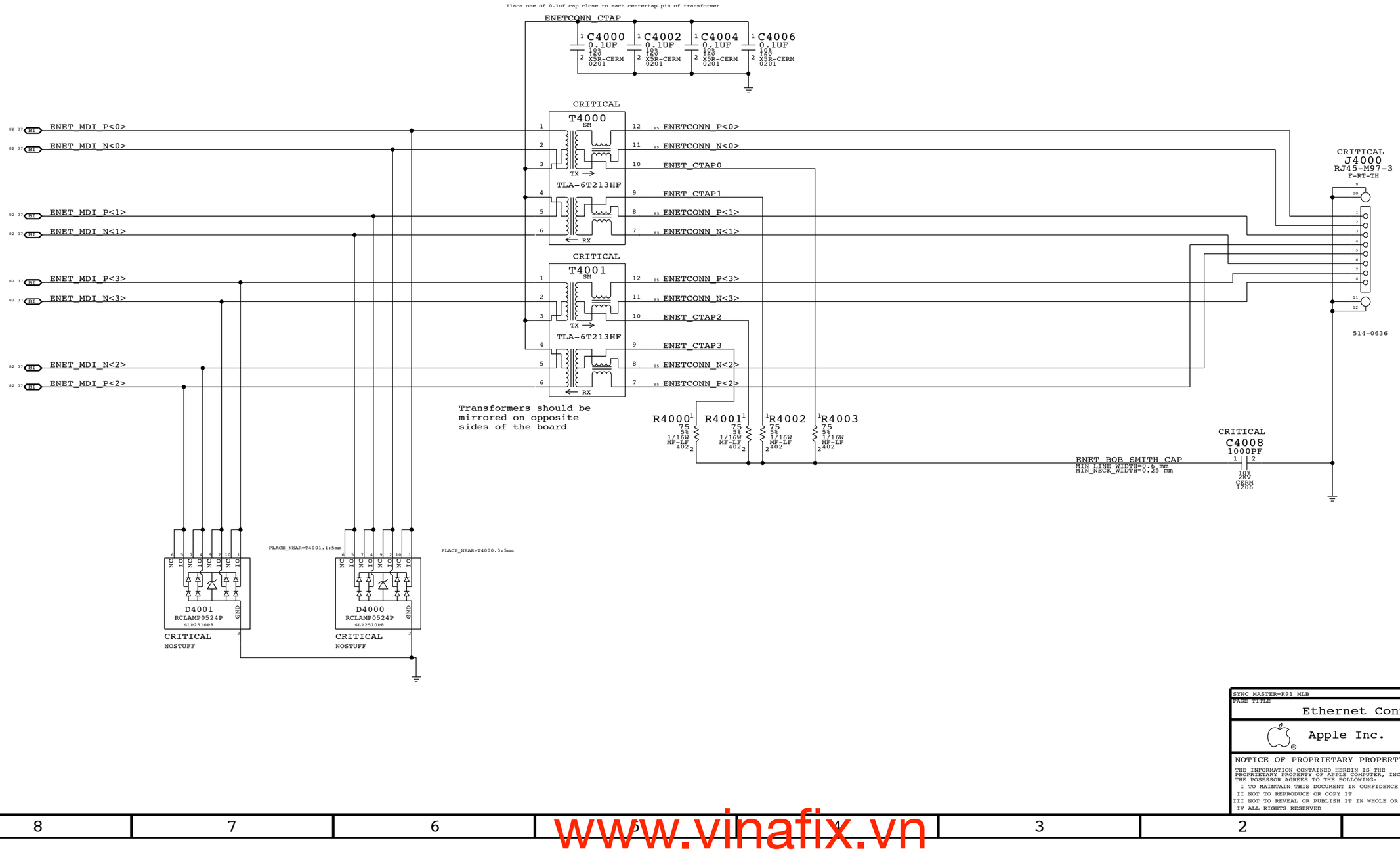
SYNC MASTER=K91_MLB SYNC DATE=05/26/2010
PAGE TITLE
ETHERNET PHY (CAESAR IV)
Apple Inc.
DRAWING NUMBER SIZE D
REVISION
BRANCH
PAGE 39 OF 109
SHEET 37 OF 86

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=K91 MLB — SYNC DATE=05/26/2010

PAGE TITLE: Ethernet Connector

Apple Inc.

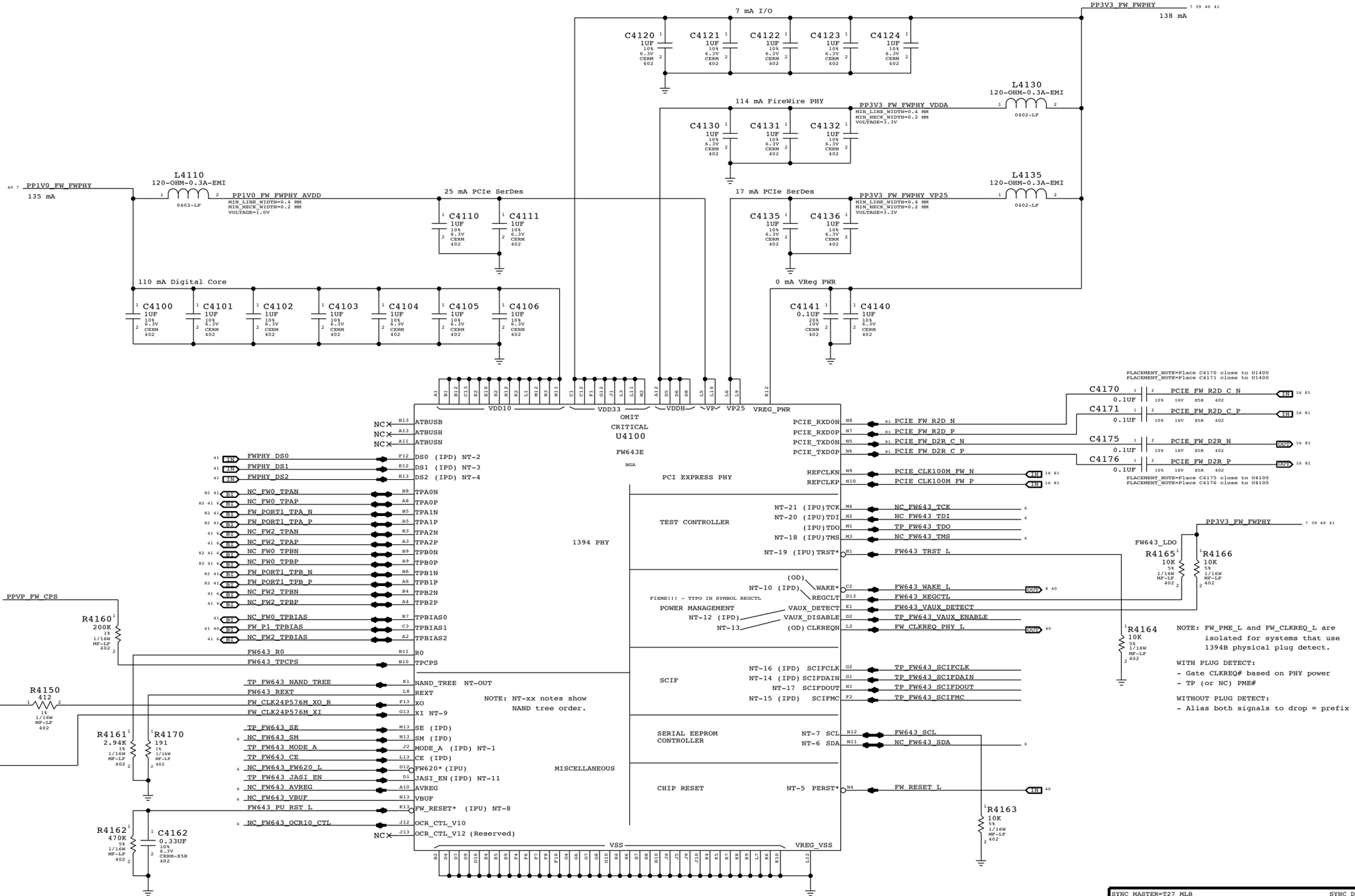
DRAWING NUMBER — SIZE: D

REVISION

BRANCH

PAGE: 40 OF 109

SHEET: 38 OF 86



SYNC MASTER=T27 MLB
SYNC DATE=07/20/2005

PAGE TITLE

FireWire LLC/PHY (FW643E)

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 41 OF 109
SHEET 39 OF 86

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_SO_FWLATEVG
- =PP3V3_SO_FWPWRCTL
- =PP1V05_SO_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)

FireWire Port Power Switch

Q4262 provides for fast-off of Q4260 in S0 (Late-VG detection)

PPBUS_G3H

CRITICAL Q4260 FDC638P_G SM

R4262 10K 5% 1/16W MF-LF 402

R4263 10 5% 1/16W MF-LF 402

FWPORT_FASTOFF_L_DIV

FWPORT_FASTOFF_L

Q4262 BSS8402DW SOT-363 SOT-363

R4260 300K 5% 1/16W MF-LF 402

C4260 0.1UF 10% 25V X5R 402

FWPORT_PWREN_L_DIV

R4261 470K 5% 1/16W MF-LF 402

FWPORT_PWREN_L

PP3V3_S0

Q4261 SSM3K15FV SOD-VESM-HF

NO STUFF C4261 0.1UF 10% 25V X5R 402

41 IN FWPORT_PWR_EN

PPBUS_FW_FWPWRSW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

CRITICAL F4260 1.1A-24V MINISMDC110H24

PPBUS_FW_FWPWRSW_D
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

CRITICAL D4260 SM CRS08-1.5A-30V

PPVP_FW 7 41

Supervisor & CLKREQ# Isolation

PP3V3_S0

C4290 0.1UF 10% 25V X5R 402

CRITICAL U4290 SLG4AP016V TDFN

R4290 100K 5% 1/16W MF-LF 402

PP1V0_FW_FWPHY 7 39 40

36 33 30 26 18 IN PLT_RESET_L

R4283 10K 5% 1/16W MF-LF 402

FW_RESET_R_L

FW_RESET_L OUT 39
DLY = 60 ms +/- 20%

40 19 IN FW_PWR_EN

23 18 OUT FW_CLKREQ_L

FW_CLKREQ_PHY_L IN 39 40
FW_CLKREQ_PHY_L 39 40
MAKE_BASE=TRUE

Pull-up provided by another page.

3.3V FW Switch

PP3V3_S0

C4201 1UF 10% 6.3V CERM 402

U4201 TPS22924 CSP CRITICAL

PP3V3_FW_FWPHY 7 39 40 41
EDP = 0.14A (85C)

U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch

PP1V05_S0

C4202 1UF 10% 6.3V CERM 402

U4202 TPS22924 CSP CRITICAL

PP1V05_FW_FET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

R4202 0.549 1% 1/16W MF 402

PP1V0_FW_FWPHY 7 39 40

LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.

PP1V05_S0

R4275 1K 5% 1/16W MF-LF 402

FW_PWR_EN_L

40 19 IN FW_PWR_EN

CRITICAL Q4275 DMB53D0UV SOT-563

R4270 330K 5% 1/16W MF-LF 402

R4271 56K 5% 1/16W MF-LF 402

CRITICAL Q4270 BC847CDXV6TXG SOT563

FWDET_MIRROR

FW_5KPD_DET_RC

FW_5KPD_DET_L
MAKE_BASE=TRUE

CRITICAL Q4275 DMB53D0UV SOT-563

C4270 0.1UF 10% 16V X5R 402

FW_P1_TPBIAS_R

FWDET_EMIT

R4272 1K 5% 1/16W MF-LF 402

R4273 12K 5% 1/16W MF-LF 402

PLACE_NEAR=C4360.1:2 mm

41 39 IN FW_P1_TPBIAS

FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

41 40 39 7 PP3V3_FW_FWPHY

R4277 10K 5% 1/16W MF-LF 402

R4276 100K 5% 1/16W MF-LF 402

FW_WAKE

NO STUFF C4276 0.1UF 10% 16V X5R 402

40 39 8 IN FW643_WAKE_L FW643_WAKE_L
MAKE_BASE=TRUE

CRITICAL Q4276 DMB53D0UV SOT-563

Dual-purpose output:

1) 5K Pull-down Detect when FW_PWR_EN is low.
2) FW643 WAKE# (PME#) when PHY is powered.

FW_PLUG_DET_L 8 19 OUT
Pull-up provided on another page.

CRITICAL Q4276 DMB53D0UV SOT-563

TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

SYNC_MASTER=T27_MLB SYNC_DATE=12/15/2009

PAGE TITLE
FireWire Port & PHY Power

Apple Inc.

DRAWING NUMBER — SIZE D
REVISION
BRANCH
PAGE 42 OF 109
SHEET 40 OF 86

Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

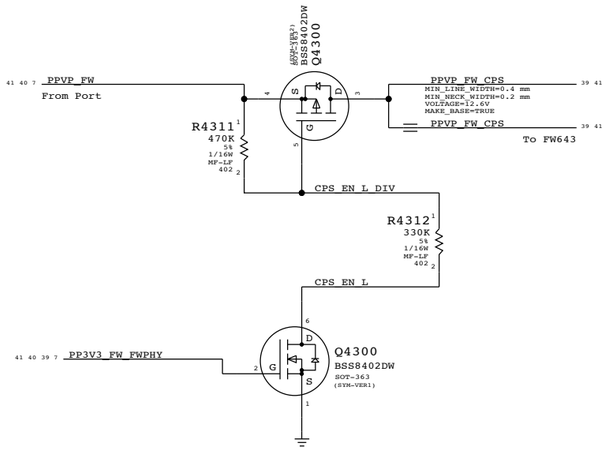
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

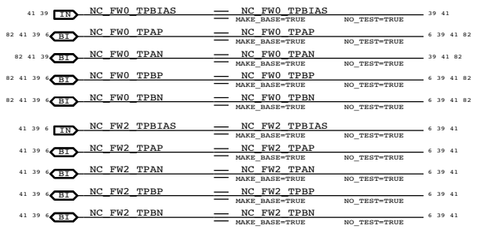
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



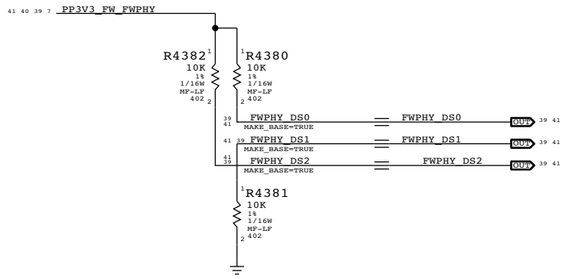
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



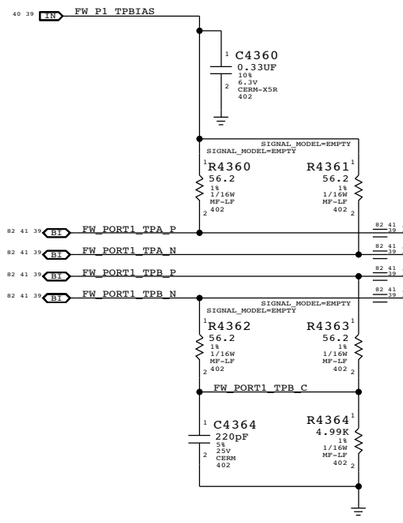
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

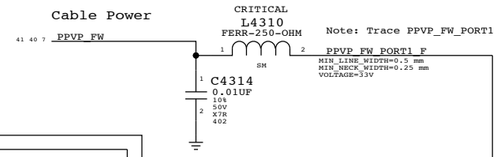


Termination

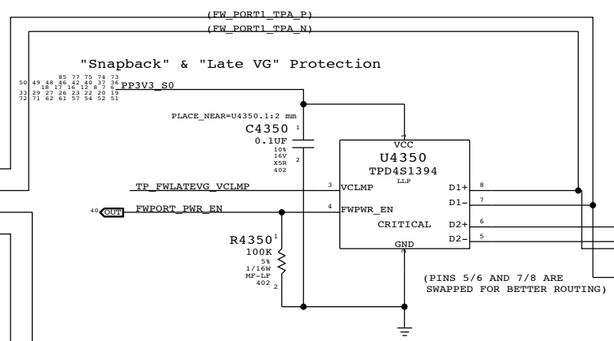
Place close to FireWire PHY

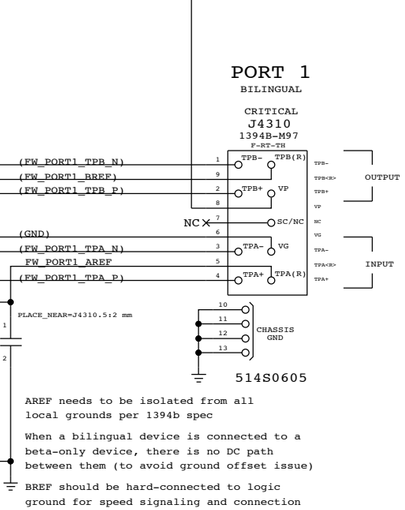


Cable Power



Note: Trace PPVP_FW_PORT1 must handle up to 5A





AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

SYNC MASTER=T27 MLB SYNC DATE=07/28/2009

PAGE TITLE: FireWire Connector

Apple Inc.

DRAWING NUMBER | SIZE: D

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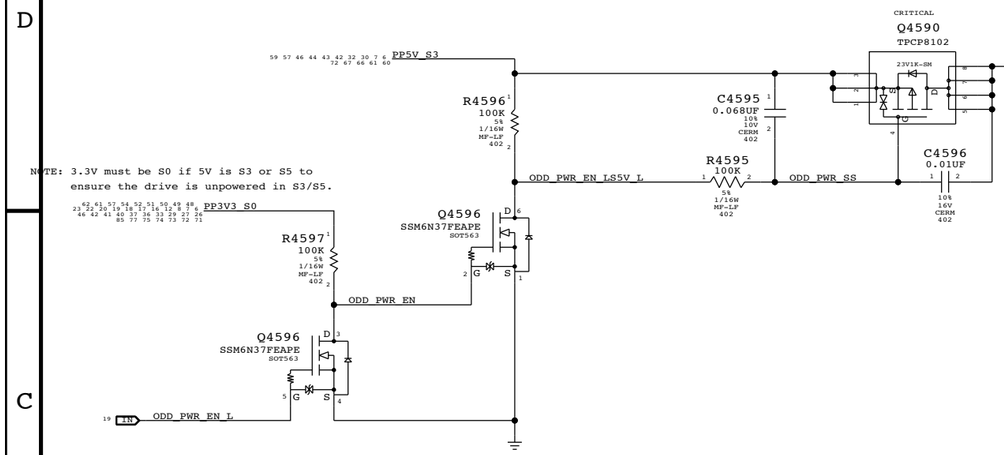
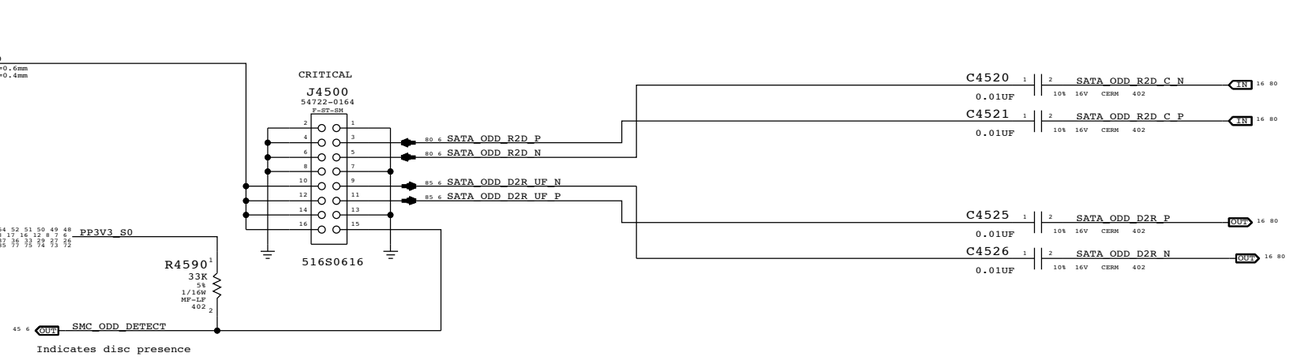
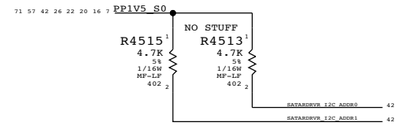
ODD Power Control



SATA ODD Connector

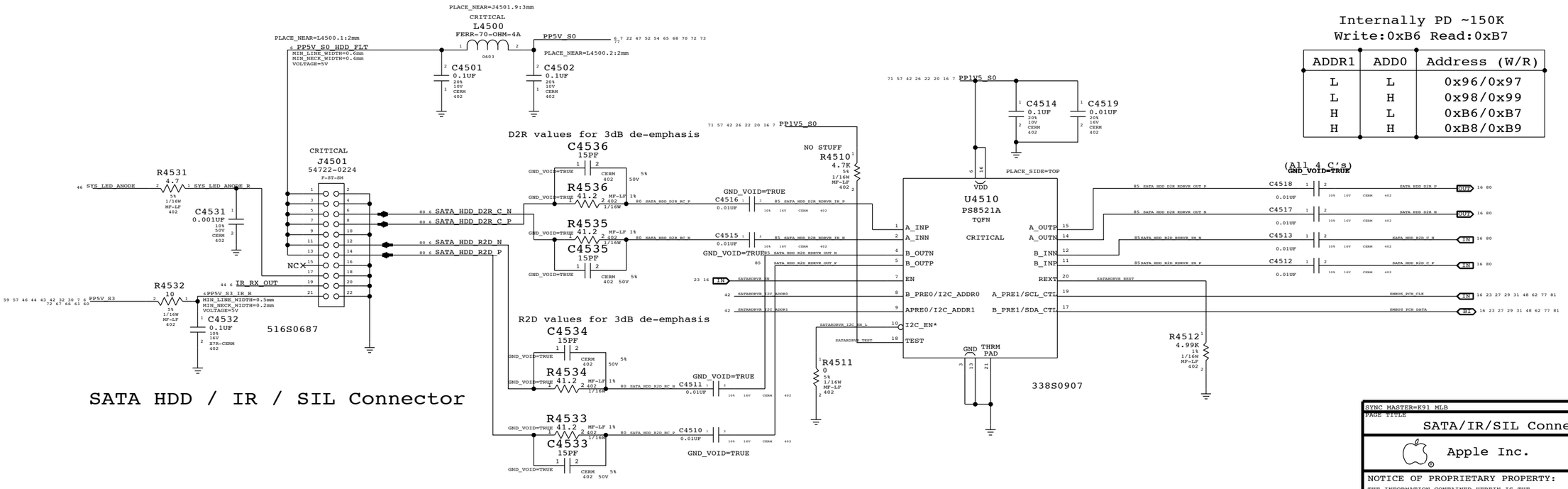




Internally PD ~150K
Write:0xB6 Read:0xB7

ADDR1	ADD0	Address (W/R)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SATA HDD / IR / SIL Connector



SYNC MASTER=K91 MLB	SYNC DATE=05/15/2010
PAGE TITLE	SATA/IR/SIL Connectors
Apple Inc.	DRAWING NUMBER: D; SIZE: D
	REVISION
	BRANCH
	PAGE: 45 OF 109
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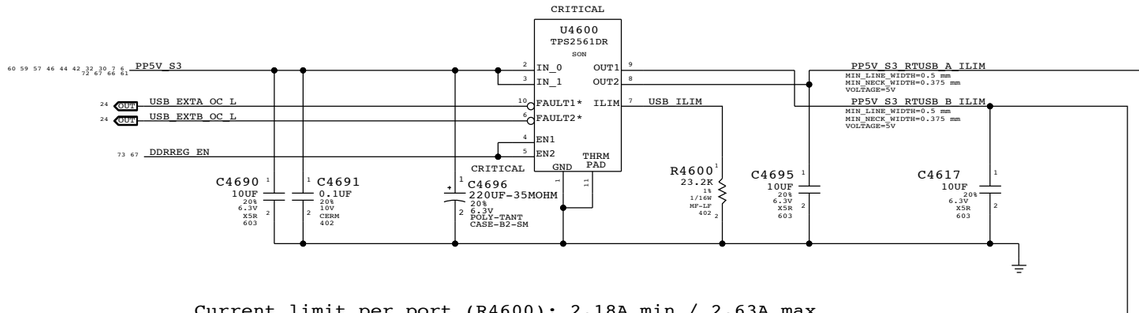
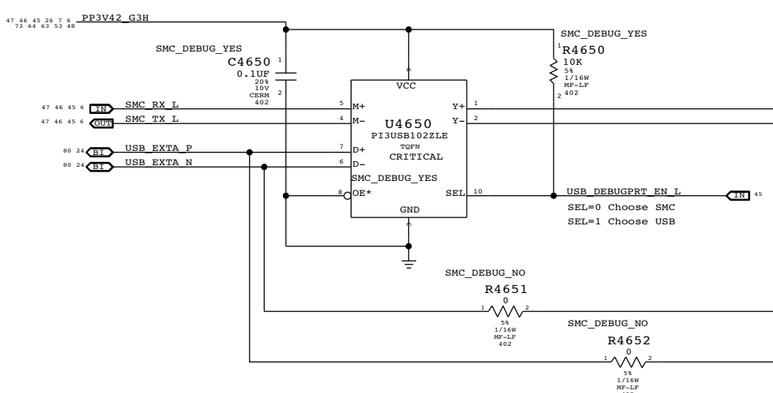
USB Port Power Switch

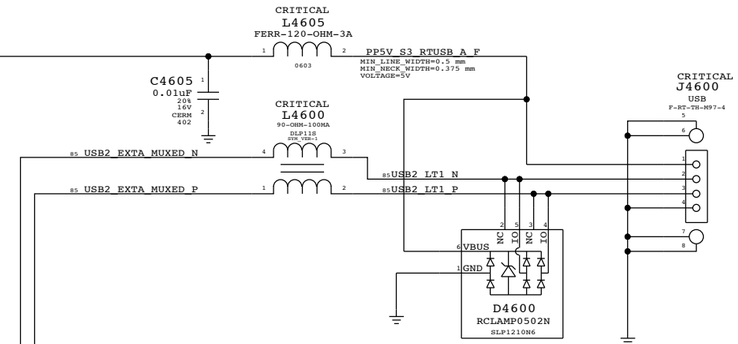


Current limit per port (R4600): 2.18A min / 2.63A max

USB/SMC Debug Mux



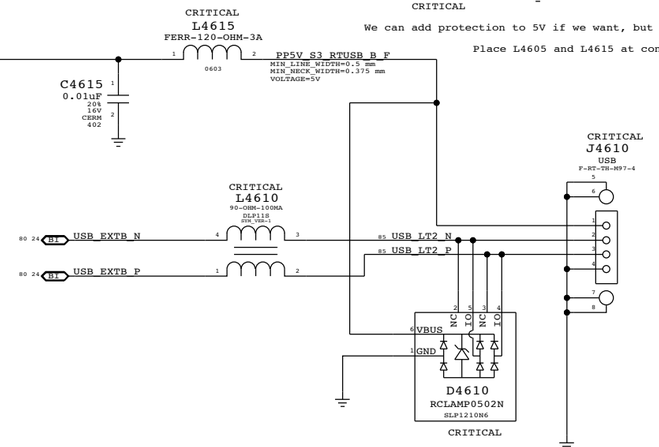
Left USB Port A



CRITICAL

We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin



Left USB Port B

SYNC MASTER=K91 MLB — SYNC DATE=06/01/2010

PAGE TITLE

External USB Connectors

Apple Inc.

DRAWING NUMBER — SIZE D

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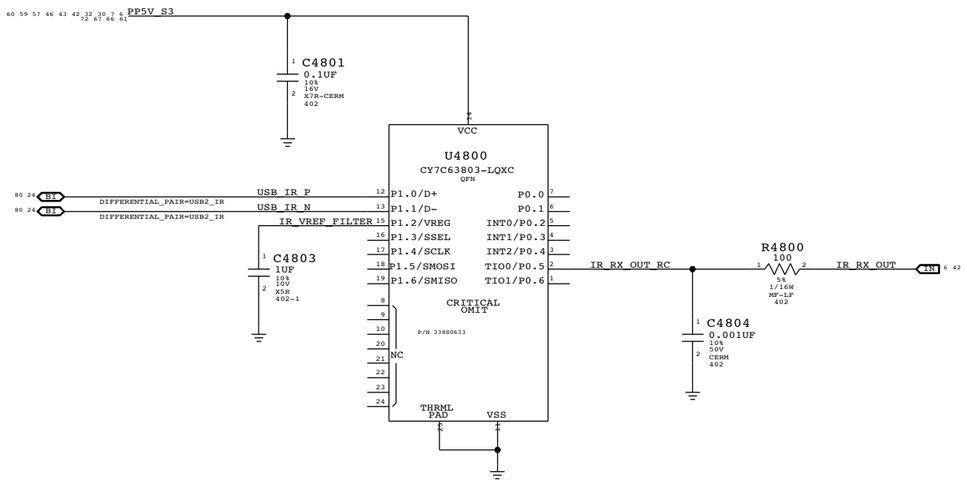
IR SUPPORT



SYNC MASTER=K91 MLB SYNC DATE=05/15/2010

PAGE TITLE

Front Flex Support

Apple Inc.

DRAWING NUMBER

SIZE D

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BRANCH

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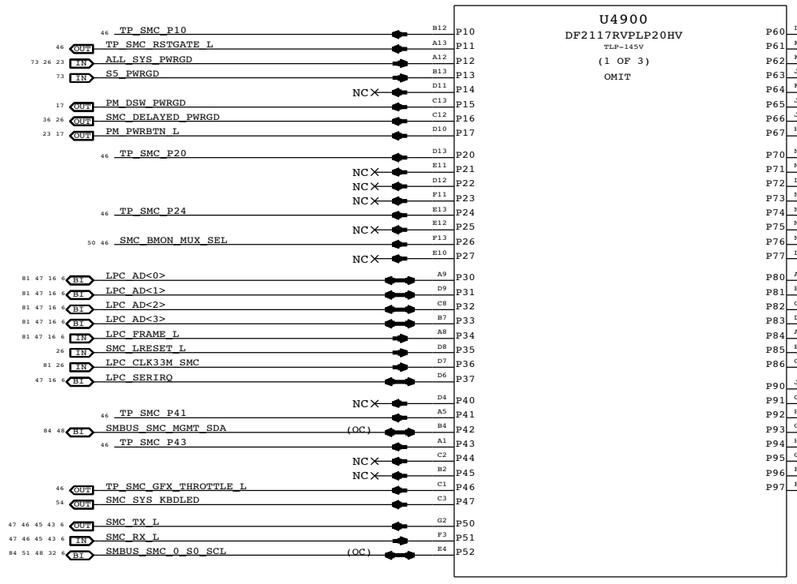
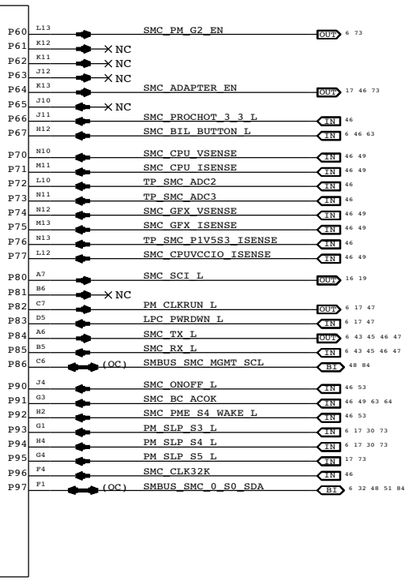
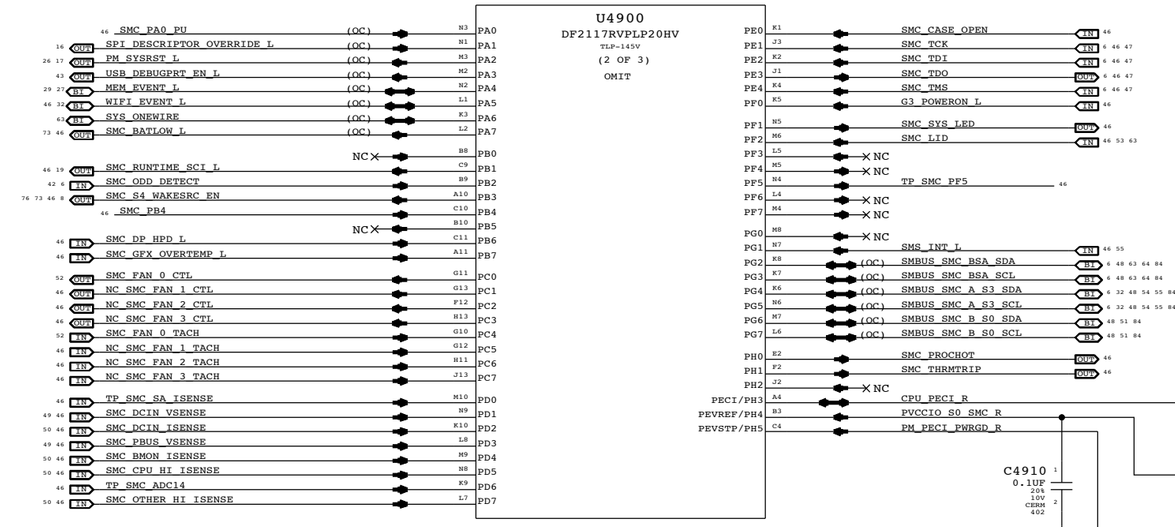
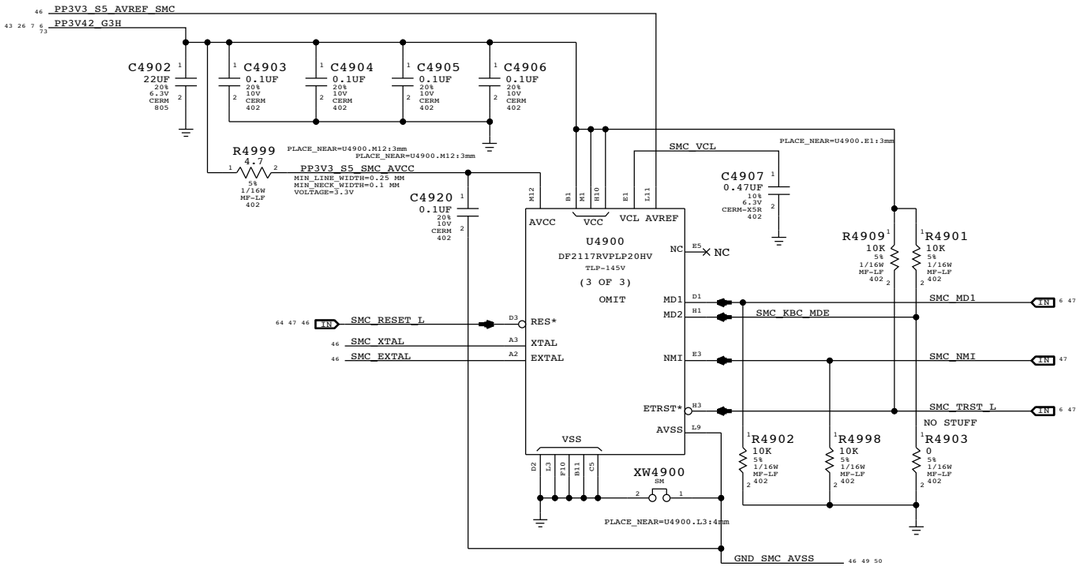
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

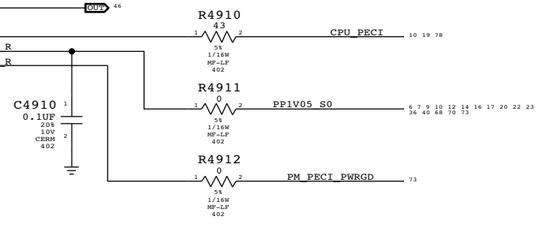






NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.





SYNC MASTER=LINDA_K90I SYNC DATE=07/07/2010

PAGE TITLE

SMC

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

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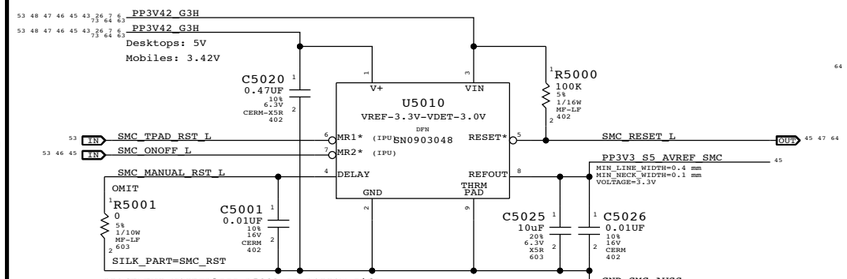
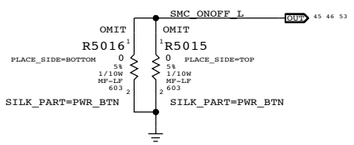
SMC Reset "Button", Supervisor & AVREF Supply



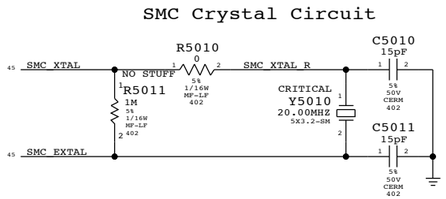
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

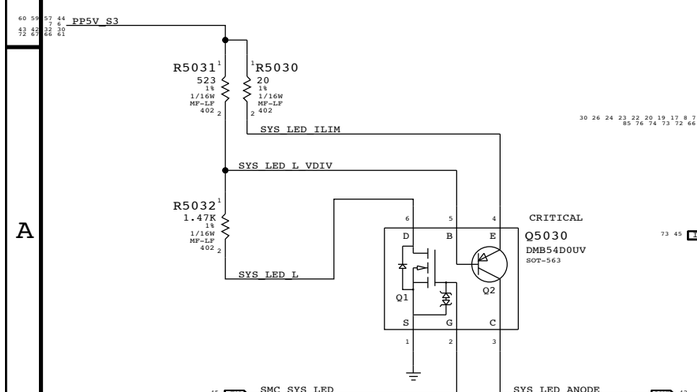
Debug Power "Buttons"



SMC Crystal Circuit

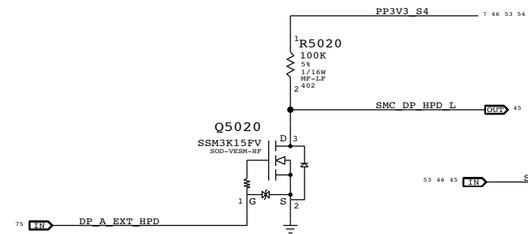


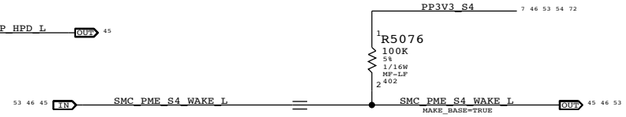
System (Sleep) LED Circuit



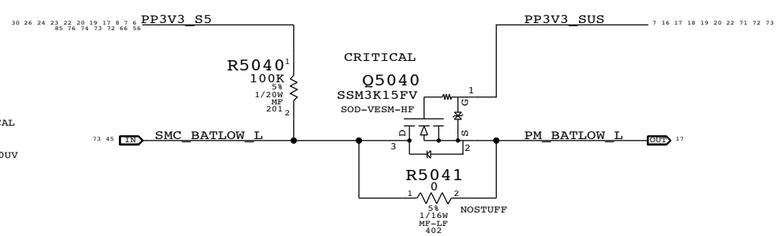
NC_SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	MAKE_BASE=TRUE	
NC_SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH	MAKE_BASE=TRUE	
NC_SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	MAKE_BASE=TRUE	
NC_SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH	MAKE_BASE=TRUE	
SMC_BC_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE	
SMS_INT_L	SMS_INT_L	MAKE_BASE=TRUE	
SMC_CPU_VSENSE	SMC_CPU_VSENSE	MAKE_BASE=TRUE	
SMC_CPU_ISENSE	SMC_CPU_ISENSE	MAKE_BASE=TRUE	
SMC_GFX_VSENSE	SMC_GFX_VSENSE	MAKE_BASE=TRUE	
SMC_GFX_ISENSE	SMC_GFX_ISENSE	MAKE_BASE=TRUE	
TP_SMC_P1V5S3_ISENSE	TP_SMC_P1V5S3_ISENSE	MAKE_BASE=TRUE	
SMC_CPUVCCIO_ISENSE	SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE	
TP_SMC_SA_ISENSE	TP_SMC_SA_ISENSE	MAKE_BASE=TRUE	
SMC_DCIN_VSENSE	SMC_DCIN_VSENSE	MAKE_BASE=TRUE	
SMC_DCIN_ISENSE	SMC_DCIN_ISENSE	MAKE_BASE=TRUE	
SMC_PBUS_VSENSE	SMC_PBUS_VSENSE	MAKE_BASE=TRUE	
SMC_BMON_ISENSE	SMC_BMON_ISENSE	MAKE_BASE=TRUE	
SMC_CPU_HI_ISENSE	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE	
SMC_OTHER_HI_ISENSE	SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE	
TP_SMC_P10	TP_SMC_P10	MAKE_BASE=TRUE	
TP_SMC_P20	TP_SMC_P20	MAKE_BASE=TRUE	
TP_SMC_P24	TP_SMC_P24	MAKE_BASE=TRUE	
SMC_BMON_MUX_SEL	SMC_BMON_MUX_SEL	MAKE_BASE=TRUE	
TP_SMC_P41	TP_SMC_P41	MAKE_BASE=TRUE	
TP_SMC_P43	TP_SMC_P43	MAKE_BASE=TRUE	
TP_SMC_PF5	TP_SMC_PF5	MAKE_BASE=TRUE	
TP_SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE	

R5012 22 5% 1/16W MF-LF 402
PM_CLK32K_SUSCLK_R — PLACE_NEAR=U1800.N14:5.1mm — SMC_CLK32K



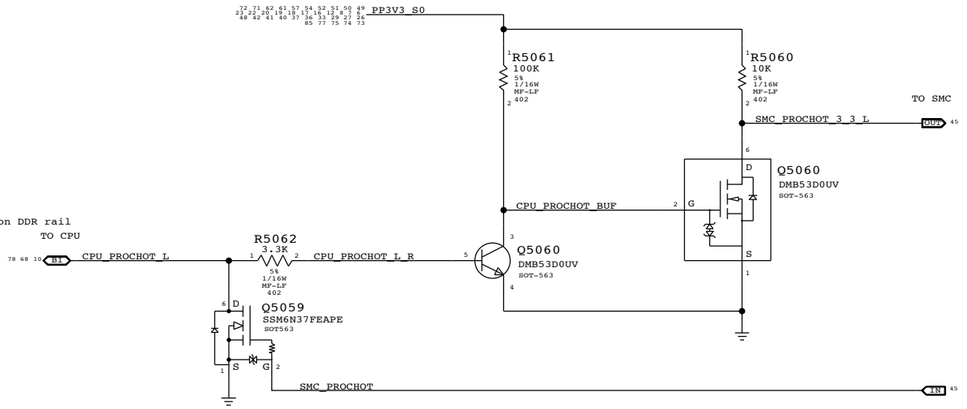


BATLOW# Isolation



Internal 20K pull-up on PM_BATLOW_L in PCH.

SMC FSB to 3.3V Level Shifting

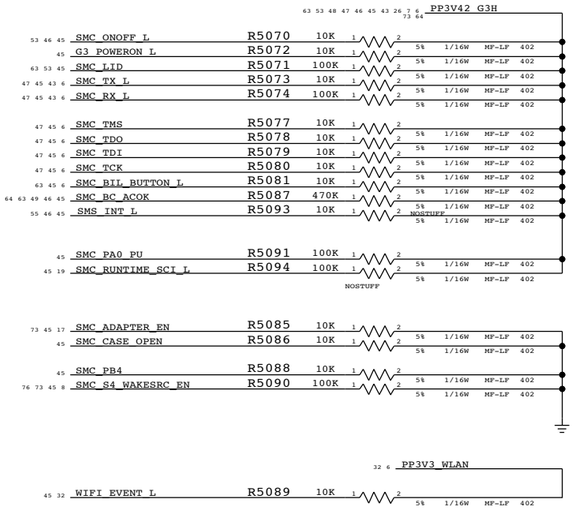


confirm if K90 needs Isense on DDR rail

Below connections are different from K91

NC_SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE	
NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE	
TP_SMC_ADC2	TP_SMC_ADC2	MAKE_BASE=TRUE	
TP_SMC_ADC3	TP_SMC_ADC3	MAKE_BASE=TRUE	
TP_SMC_ADC14	TP_SMC_ADC14	MAKE_BASE=TRUE	
TP_SMC_GFX_THROTTLE_L	TP_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	

SMC_GFX_OVERTEMP_L — R5095 10K 5% 1/16W MF-LF 402



SYNC MASTER=LINDA K90I	SYNC DATE=07/08/2010	
PAGE TITLE	SMC Support	
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	BRANCH	
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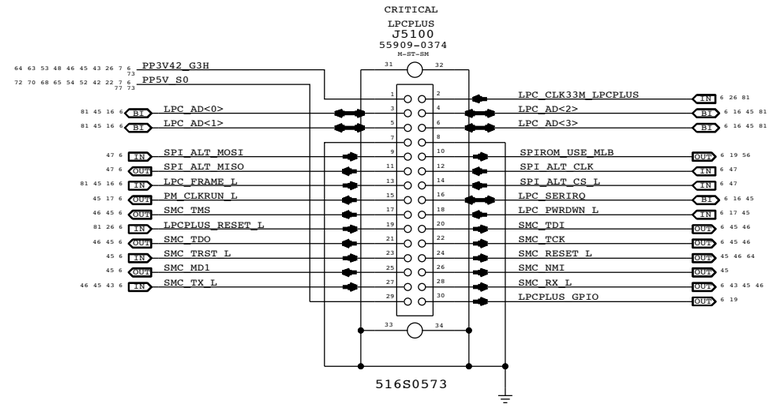
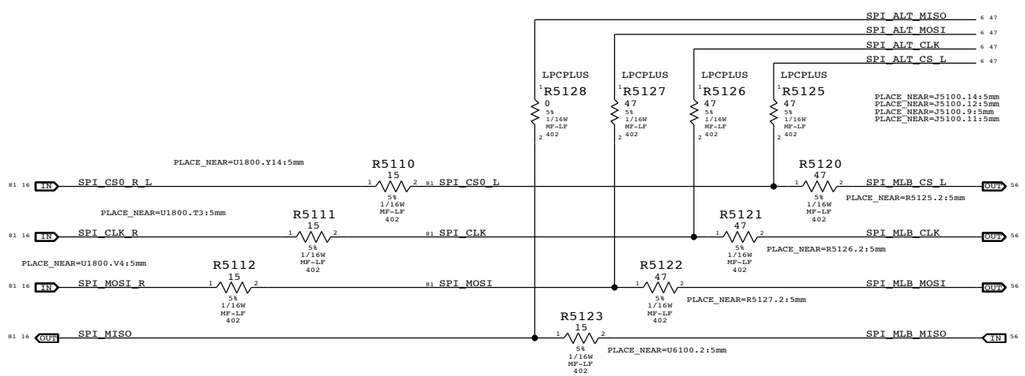
LPC+SPI Connector



SPI Bus Series Termination



SYNC MASTER=K91 MLB | SYNC DATE=05/15/2010

PAGE TITLE: LPC+SPI Debug Connector

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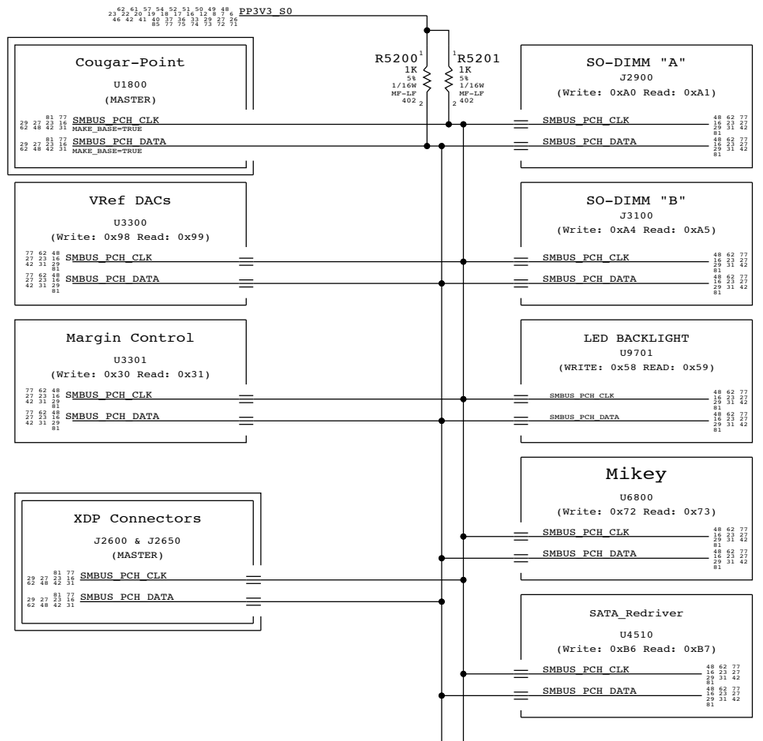
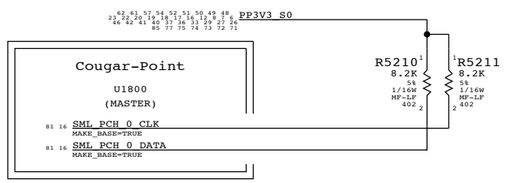
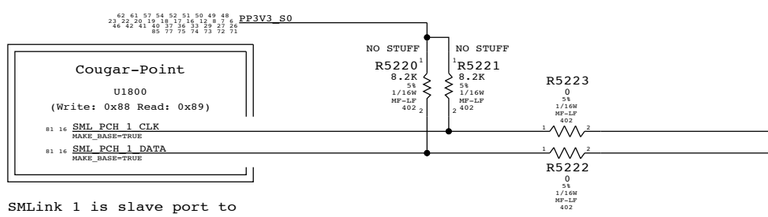
PCH SMBus "0" Connections



PCH "SMLink 0" Connections

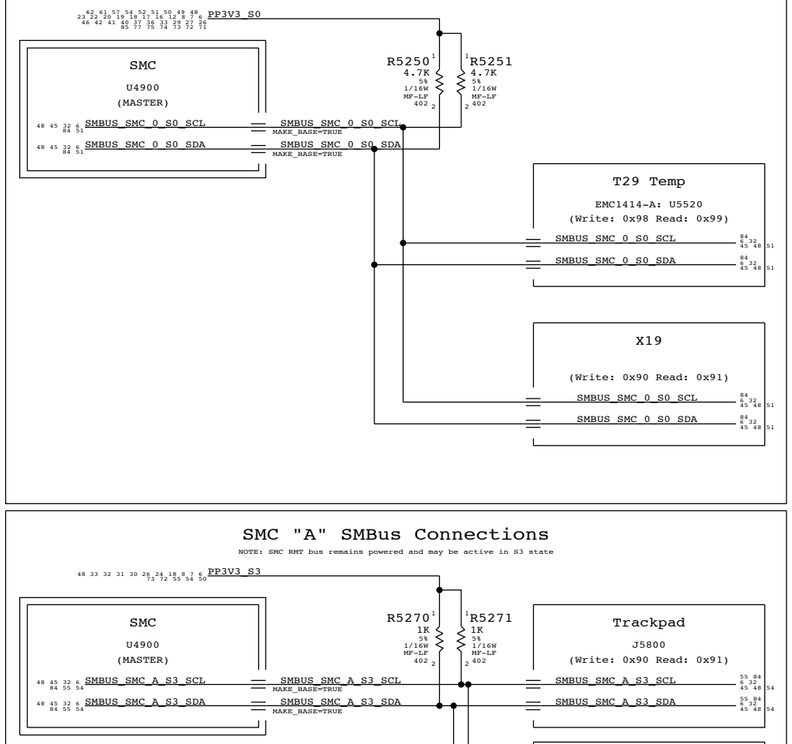


PCH "SMLink 1" Connections



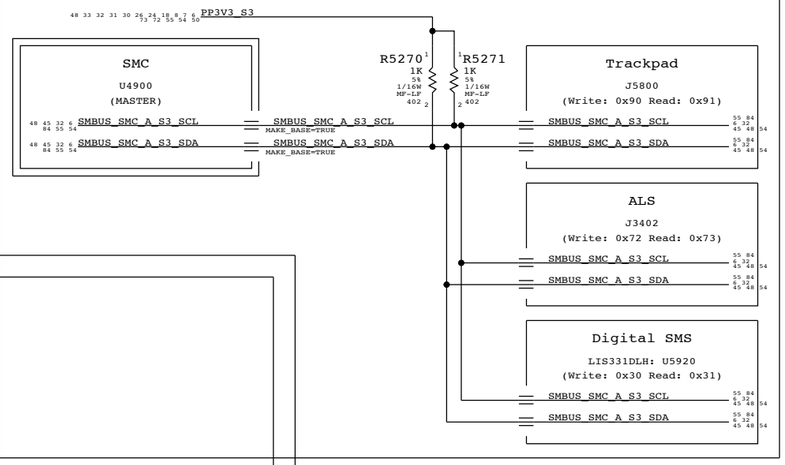
SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

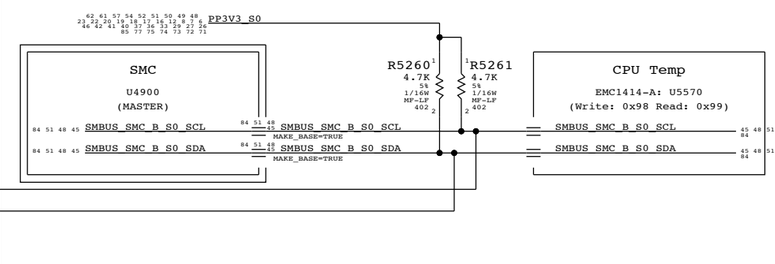


SMC "A" SMBus Connections

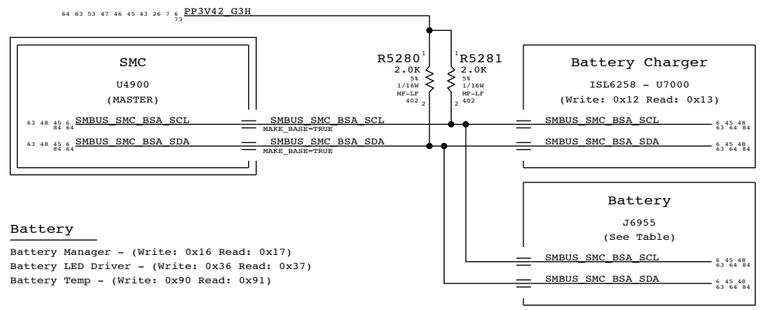
NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "B" SMBus Connections



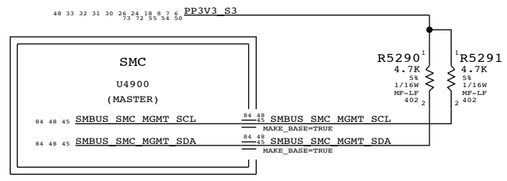
SMC "Battery A" SMBus Connections



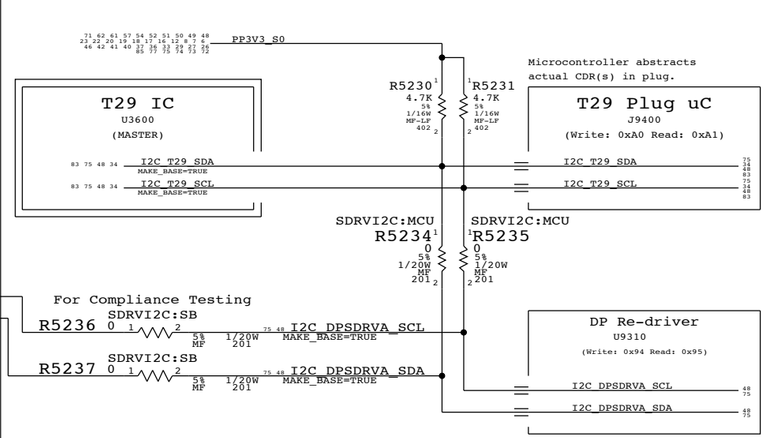
Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections



T29 I2C Connections



SYNC MASTER=K91 MLB
SYNC DATE=05/26/2010

PAGE TITLE
SMBus Connections

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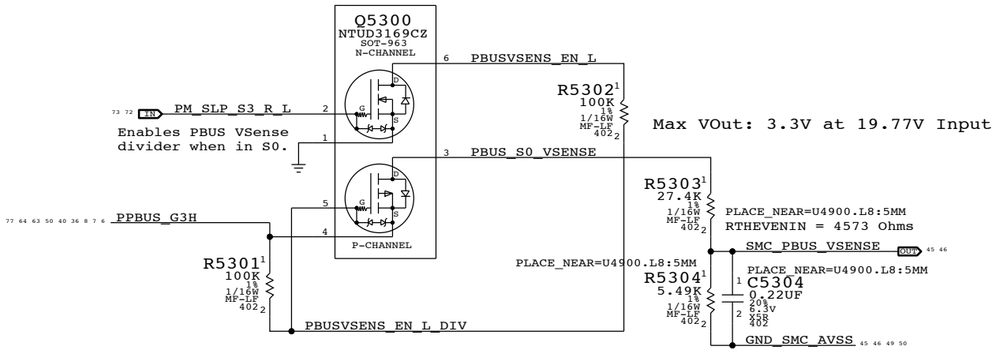
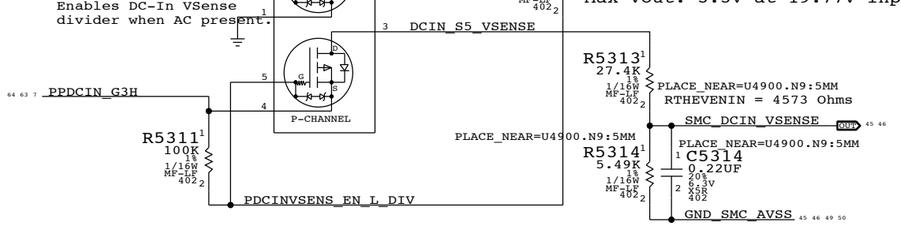
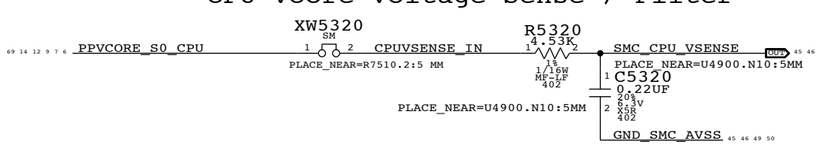
PBUS Voltage Sense Enable & Filter



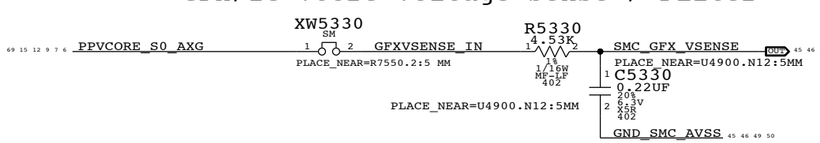
DC-In Voltage Sense Enable & Filter



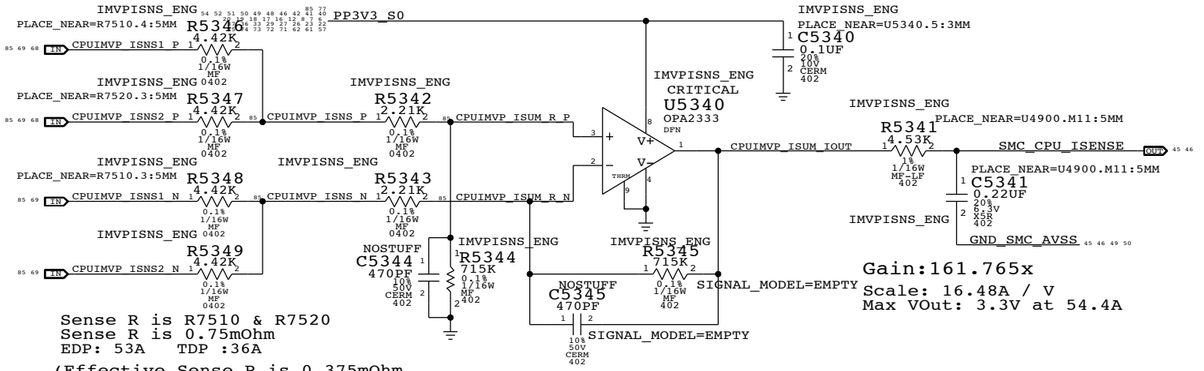
CPU Vcore Voltage Sense / Filter



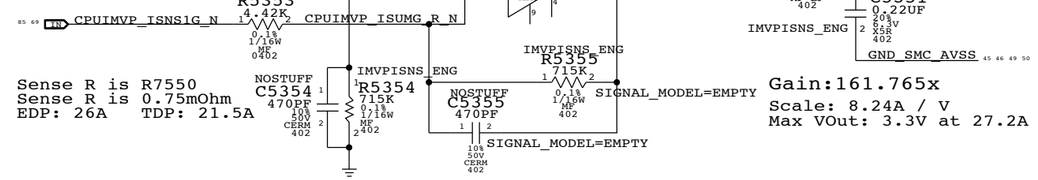
GFX/IG Vcore Voltage Sense / Filter



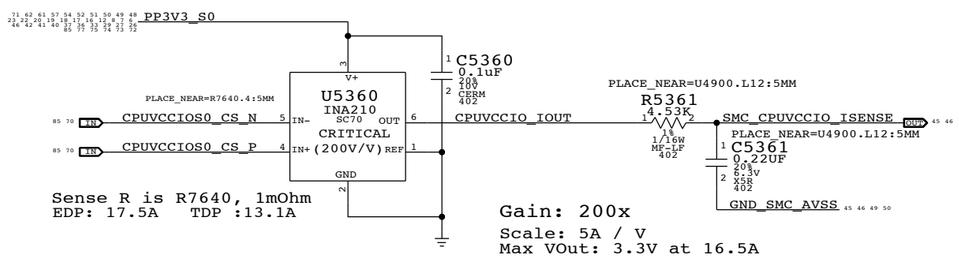
CPU VCore Load Side Current Sense / Filter



GFX/IG VCore Load Side Current Sense / Filter



CPU 1.05V VCCIO Current Sense / Filter



SYNC_MASTER=LINDA K90I SYNC_DATE=10/22/2010

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

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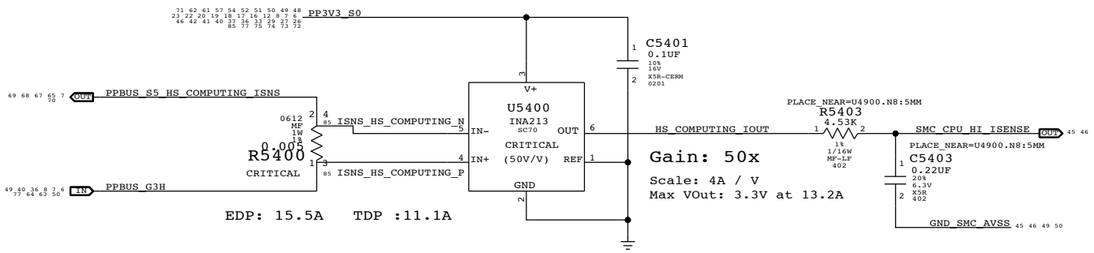
COMPUTING High Side Current Sense / Filter



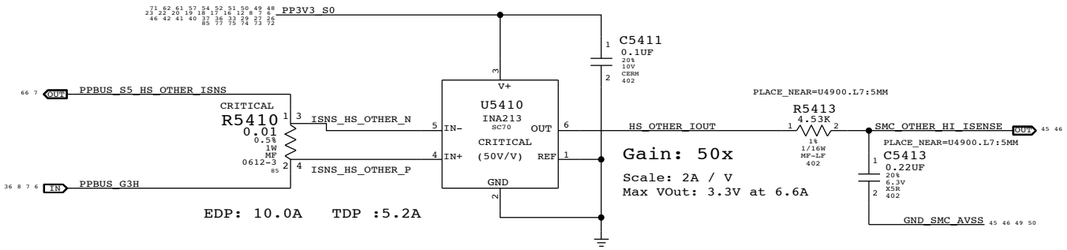
EDP: 15.5A TDP :11.1A

Gain: 50x

Scale: 4A / V

Max VOut: 3.3V at 13.2A

OTHER High Side Current Sense / Filter



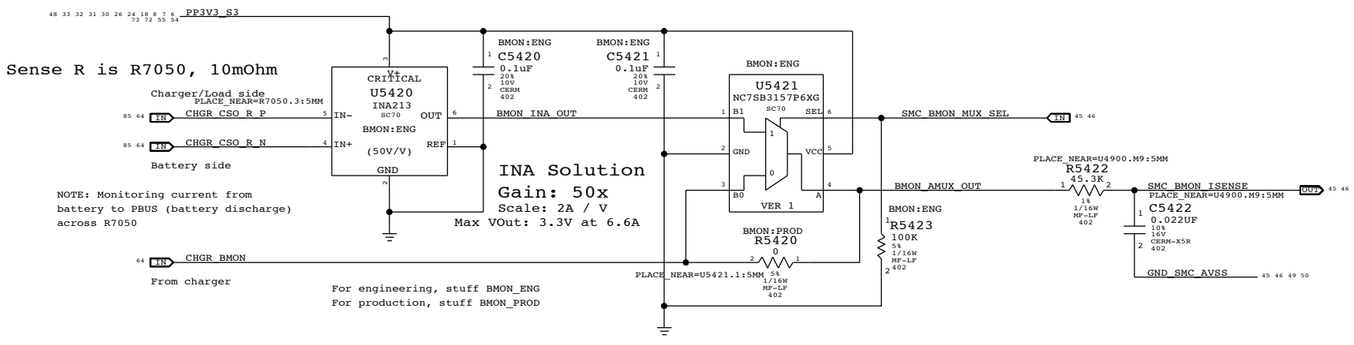
EDP: 10.0A TDP :5.2A

Gain: 50x

Scale: 2A / V

Max VOut: 3.3V at 6.6A

CHARGER BMON High Side (BATTERY DISCHAEGE) Current Sense, MUX & Filter



INA Solution

Gain: 50x

Scale: 2A / V

Max VOut: 3.3V at 6.6A

INA (Engineering) Solution

Gain: 50x

Scale: 2A / V

Max VOut: 3.3V at 6.6A

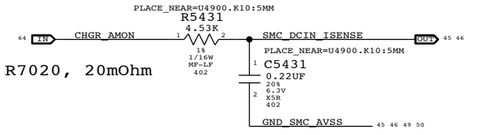
Charger BMON (Production) Solution

ISL6259 Gain: 36x

Scale: 2.78A / V

Max VOut: 3.3V at 9.167A

DC-IN (AMON) Current Sense Filter



Sense R is R7020, 20mOhm

DC-In AMON

ISL6259 Gain: 20x

Scale: 2.5A / V

Max VOut: 3.3V at 8.25A

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High Side Current Sensing

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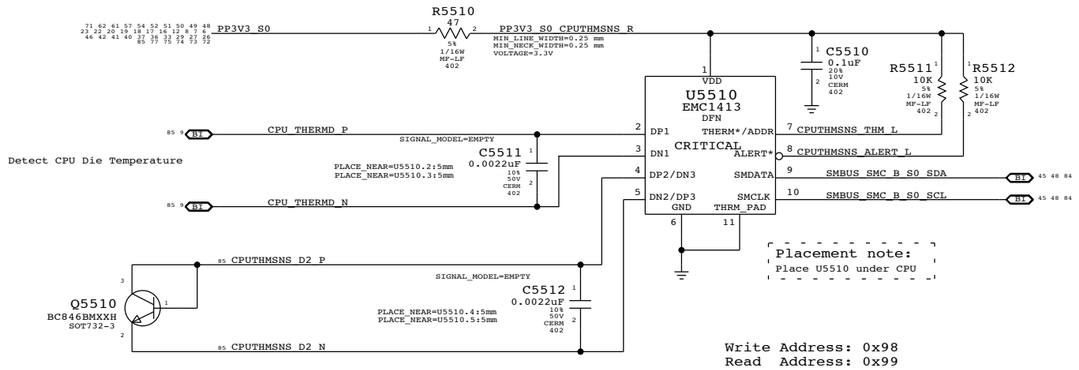
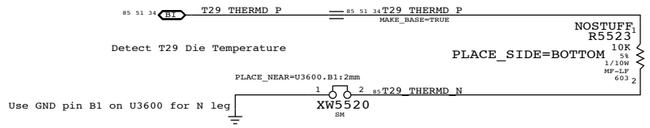
CPU Proximity/CPU Die/5V-3.3V Proximity

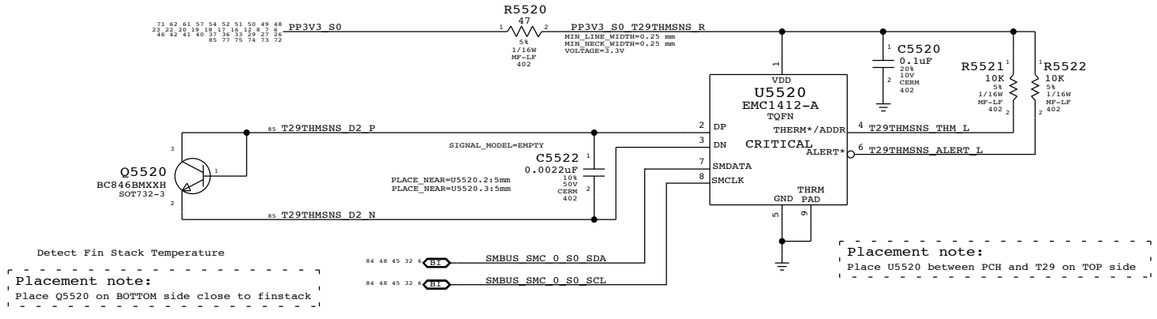


Write Address: 0x98
Read Address: 0x99

T29 Die



PCH-T29 Proximity/FinStack



Write Address: 0x98
Read Address: 0x99

SYNC MASTER=LINDA K90I SYNC DATE=10/22/2010

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Thermal Sensors

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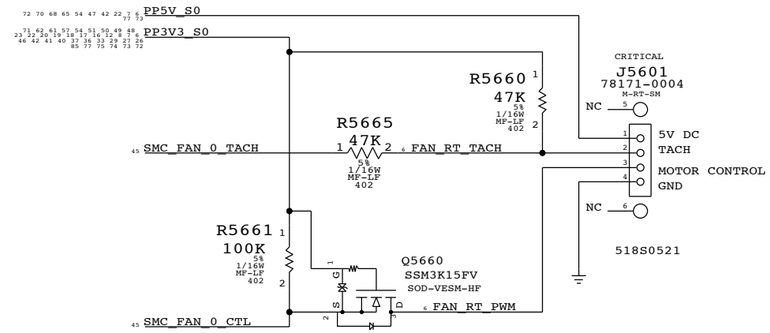

SYNC MASTER=K24 MLB	SYNC DATE=07/20/2009
PAGE TITLE: Fan	
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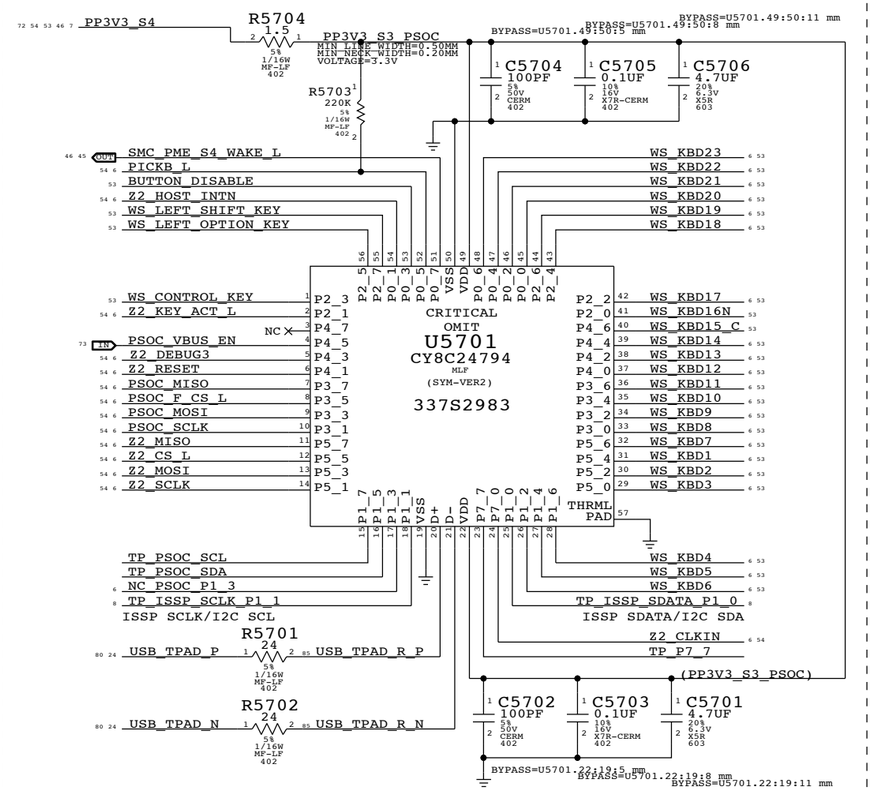
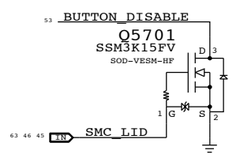
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable

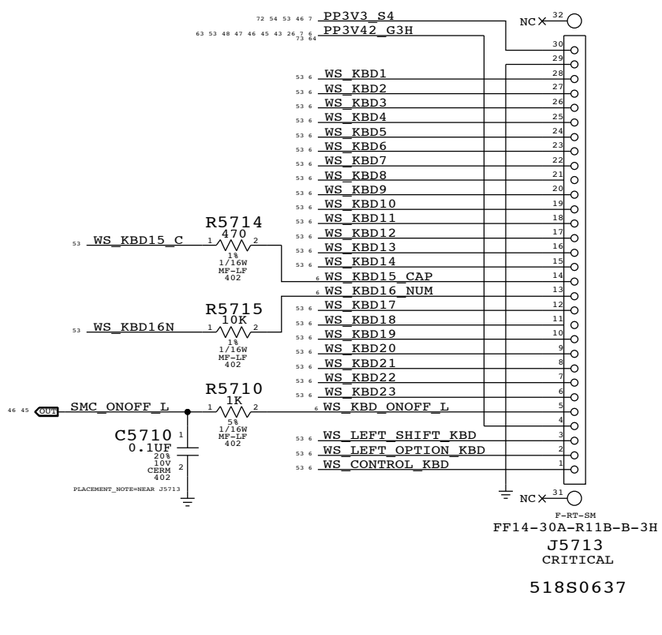


PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

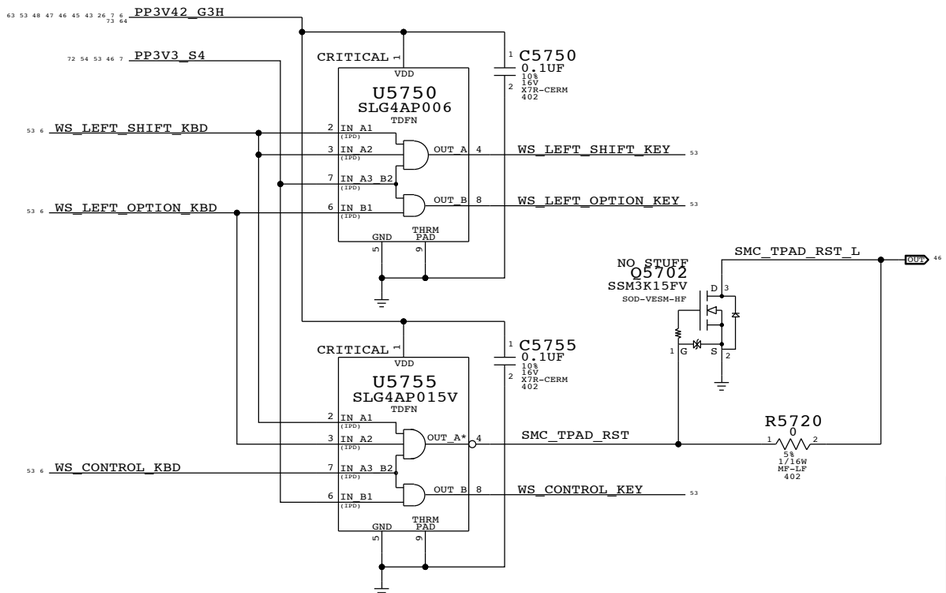
Keyboard Connector



518S0637

SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



SYNC_MASTER=LINDA K90I SYNC_DATE=07/12/2010

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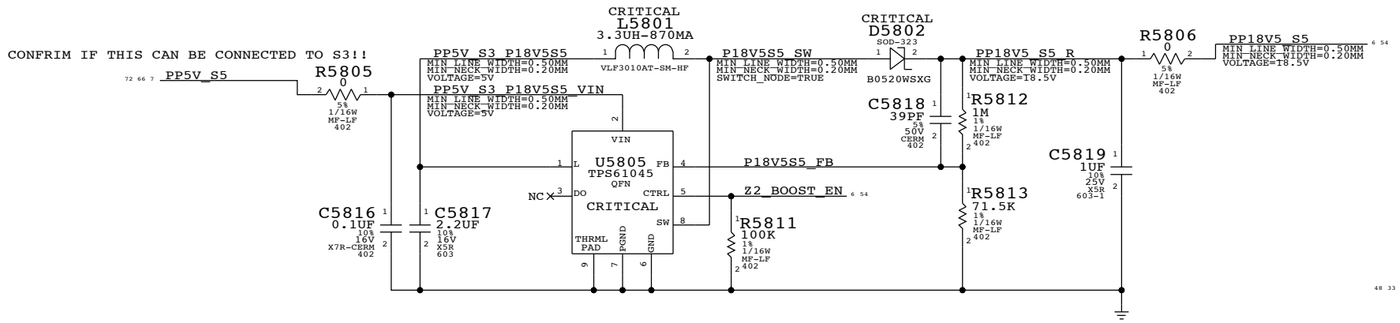
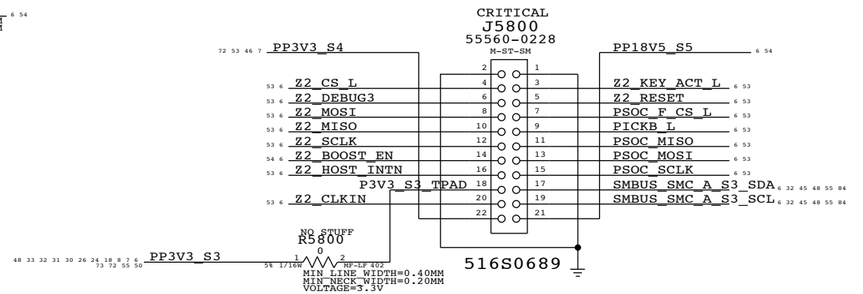
BOOSTER +18.5VDC FOR SENSORS

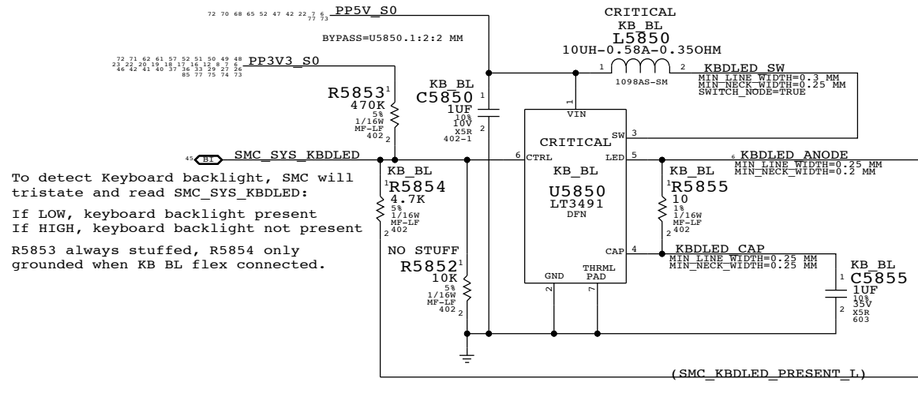
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



Keyboard Backlight Driver & Detection

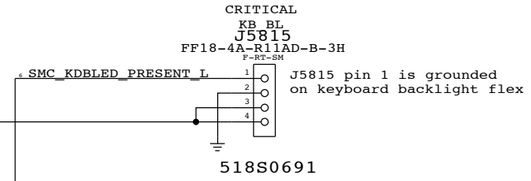


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



K6 NOTES : C5850 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC_MASTER=LINDA_K90I SYNC_DATE=07/12/2010

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

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PAGE: 58 OF 109

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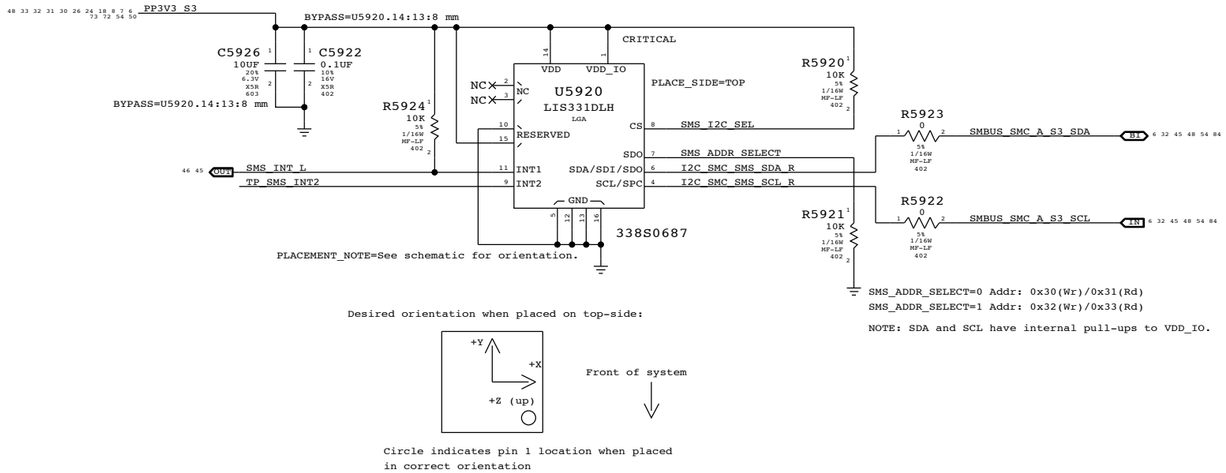

SYNC MASTER=LINDA K90I SYNC DATE=07/08/2010

PAGE TITLE

Digital Accelerometer

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

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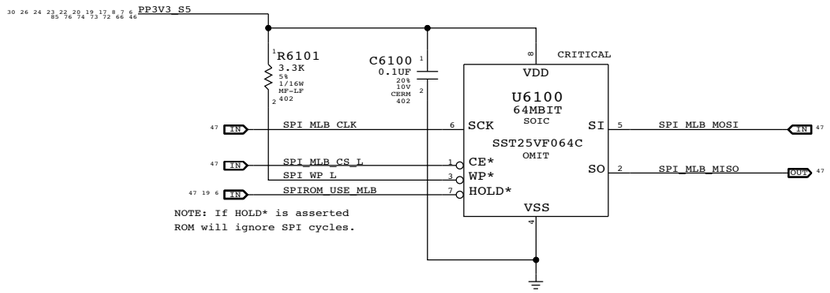
SHEET 55 OF 86



SYNC MASTER=K91 MLB SYNC DATE=05/15/2010

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER

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REVISION

BRANCH

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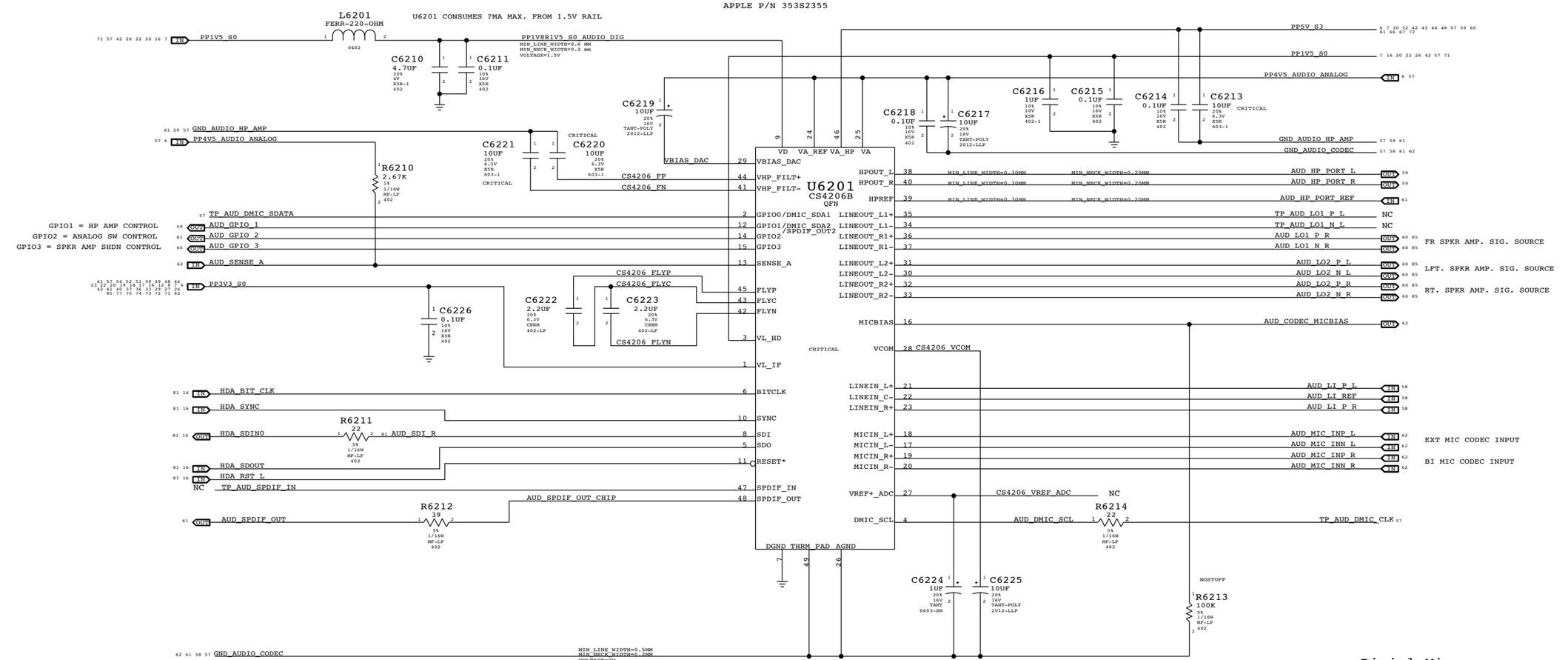
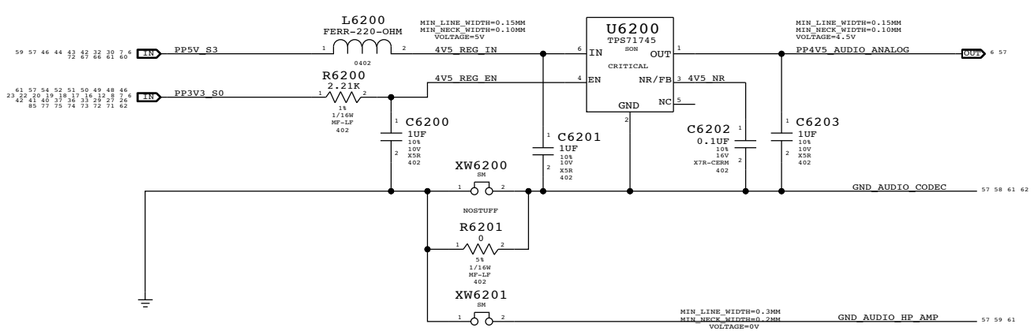
AUDIO CODEC

APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

Digial Mic

TP_AUD_DMIC_CLK == TP_AUD_DMIC_CLK (MAKE_BASE=TRUE)
TP_AUD_DMIC_SDATA == TP_AUD_DMIC_SDATA (MAKE_BASE=TRUE)

SYNC MASTER=LENG K90I | SYNC DATE=08/10/2010

PAGE TITLE: AUDIO: CODEC/REGULATOR

Apple Inc.

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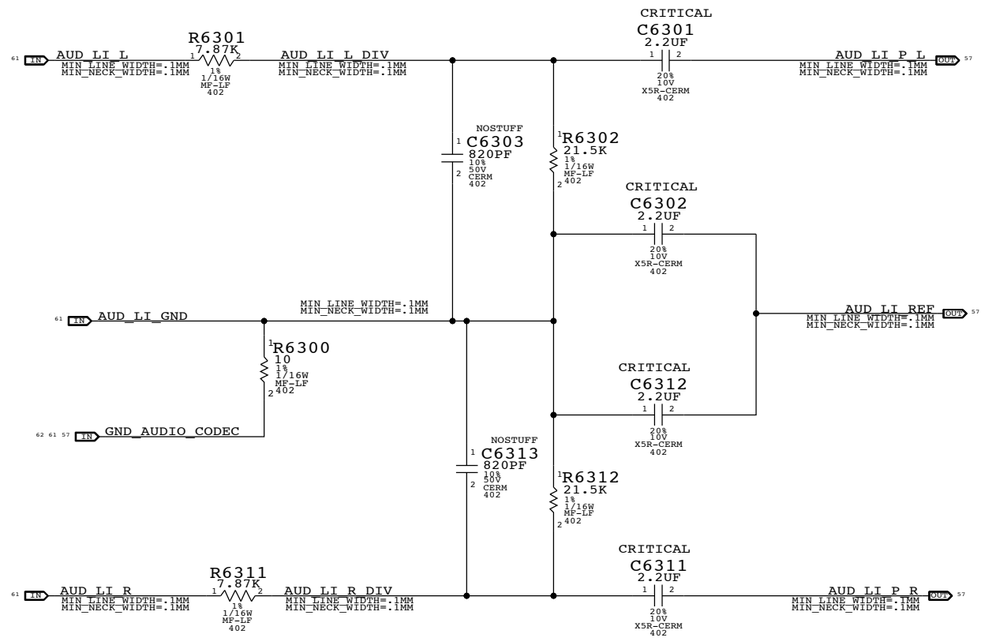
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

DRAWING NUMBER
SIZE D
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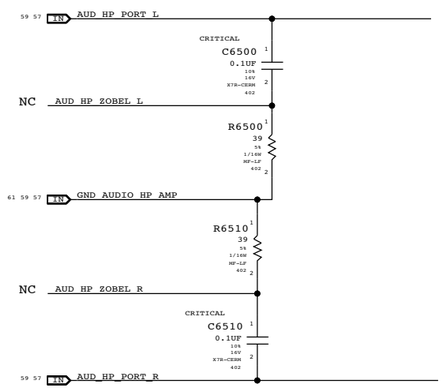
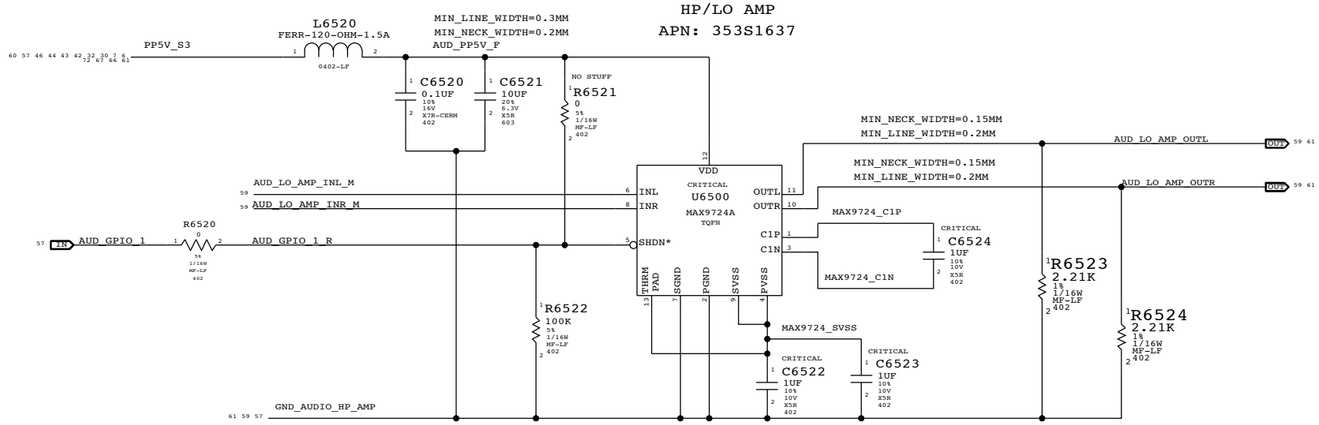
BRANCH
PAGE 63 OF 109
SHEET 58 OF 86

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



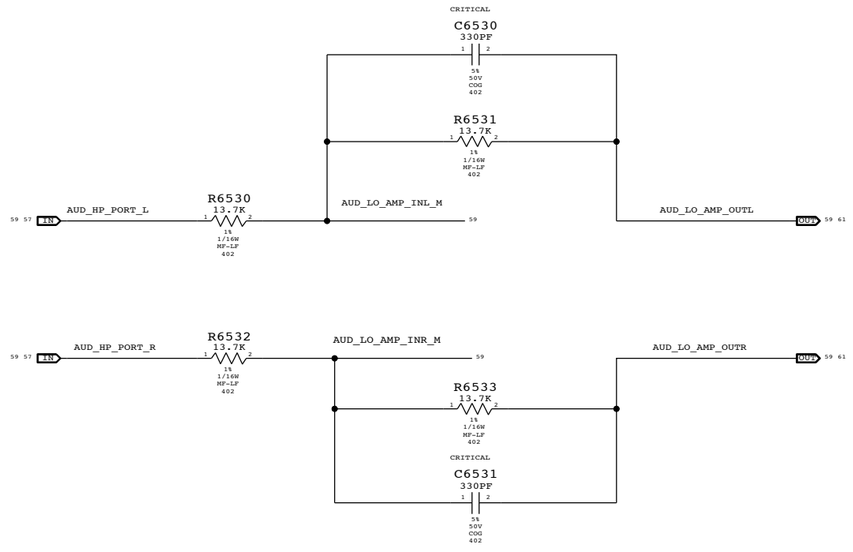
FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL
RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

HP/LO AMP
APN: 353S1637



MAX9724 GAIN/FILTER COMPONENTS

AV_PB = -1V/V, FC_LPF = 35.2KHZ



SYNC MASTER=LENG K90I SYNC DATE=08/10/2010

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

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SIZE D

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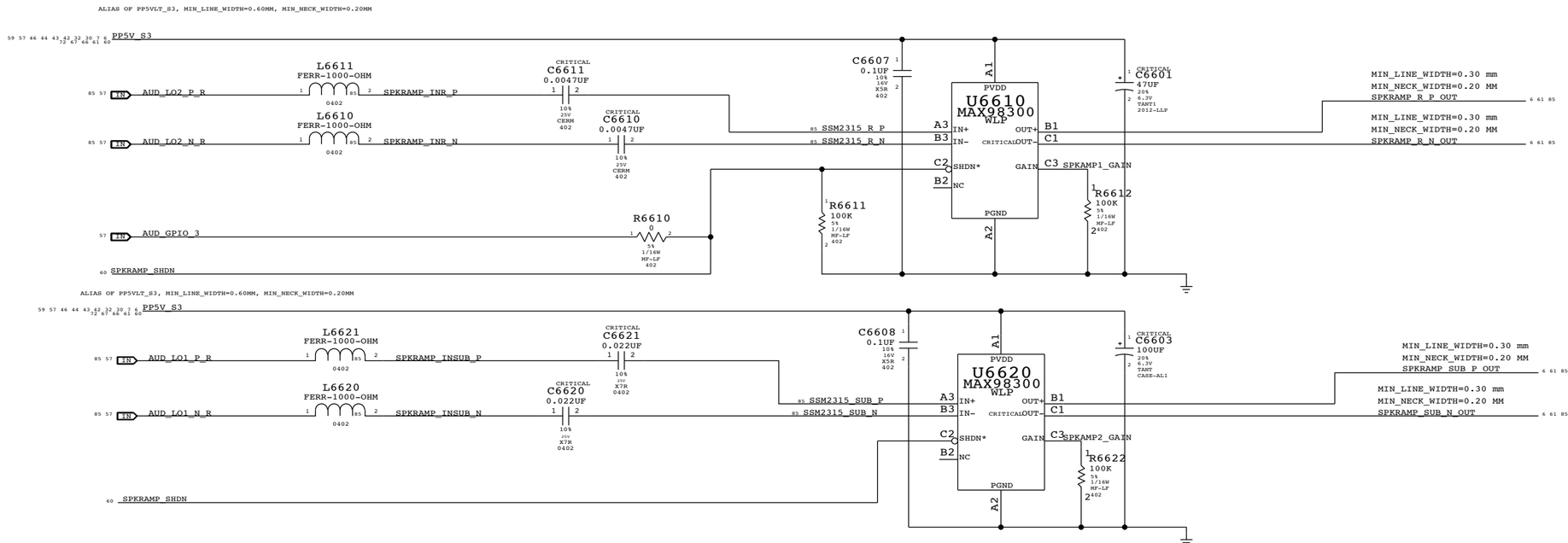
SATELLITE & SUB TWEETER AMPLIFIER

APN:353S2888

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	3DB



SYNC MASTER=LENG K90I SYNC DATE=08/10/2010

PAGE TITLE

AUDI0: SPEAKER AMP

Apple Inc.

DRAWING NUMBER

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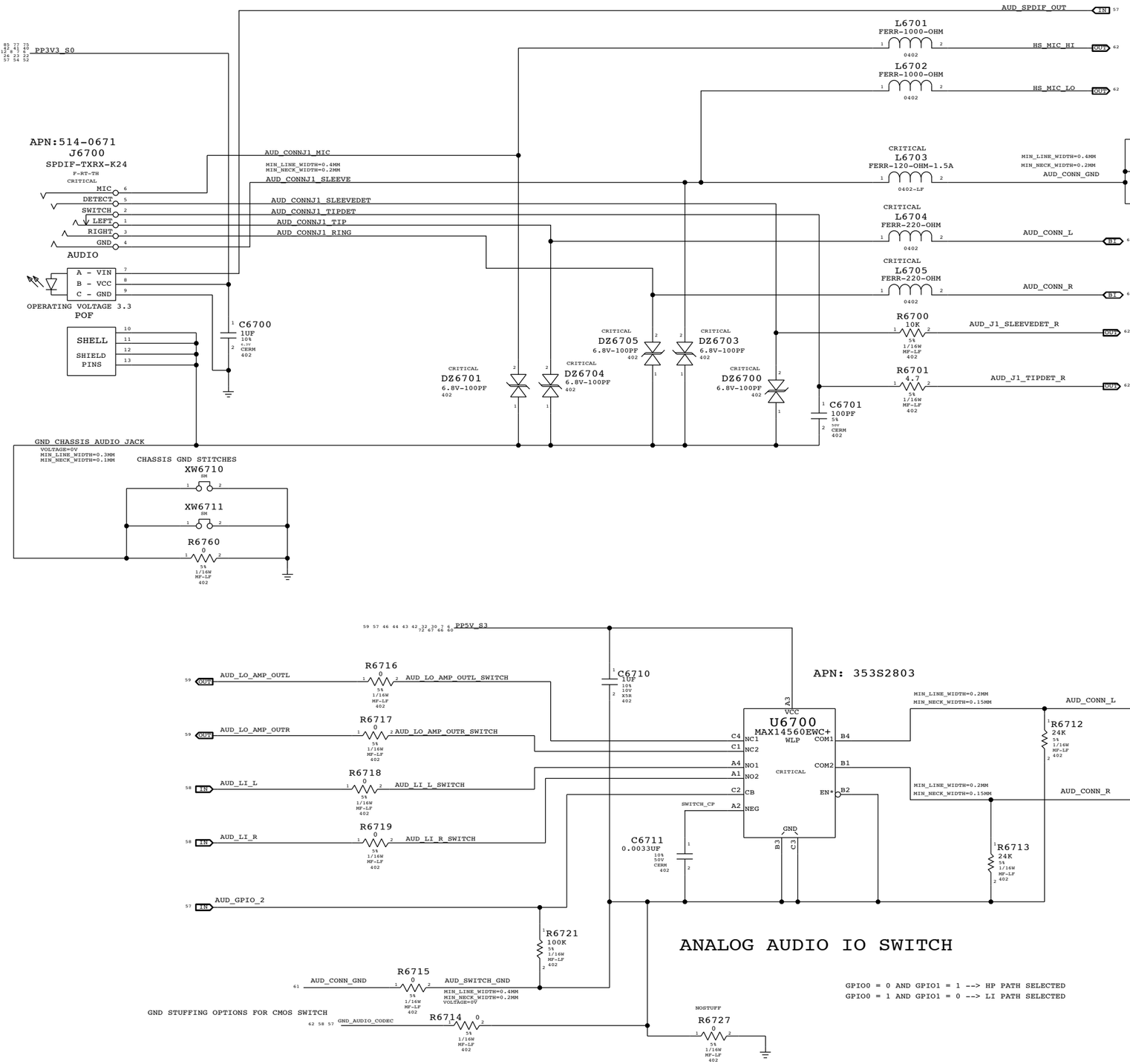
AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



SYNC MASTER=LENG K90I SYNC DATE=08/10/2010

PAGE TITLE

AUDIO: JACK

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_2 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_2 AND GPIO_1	0X09 (A)AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

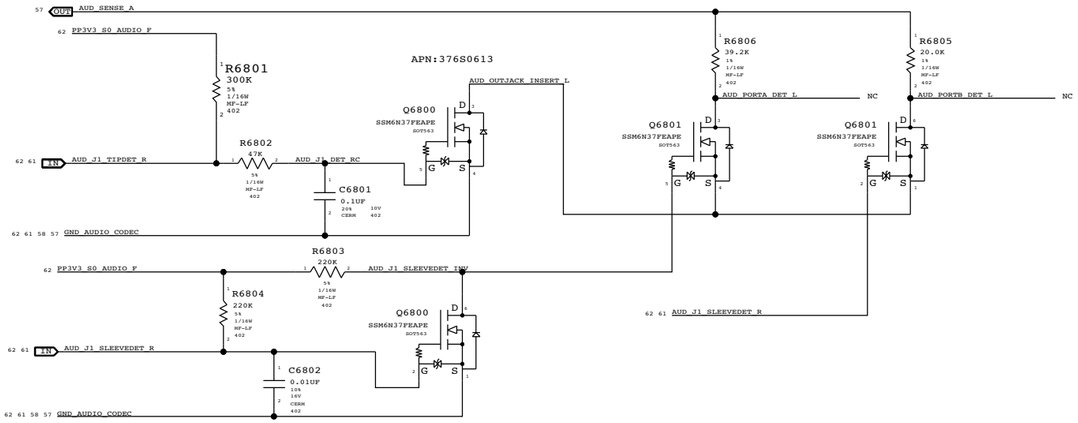
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

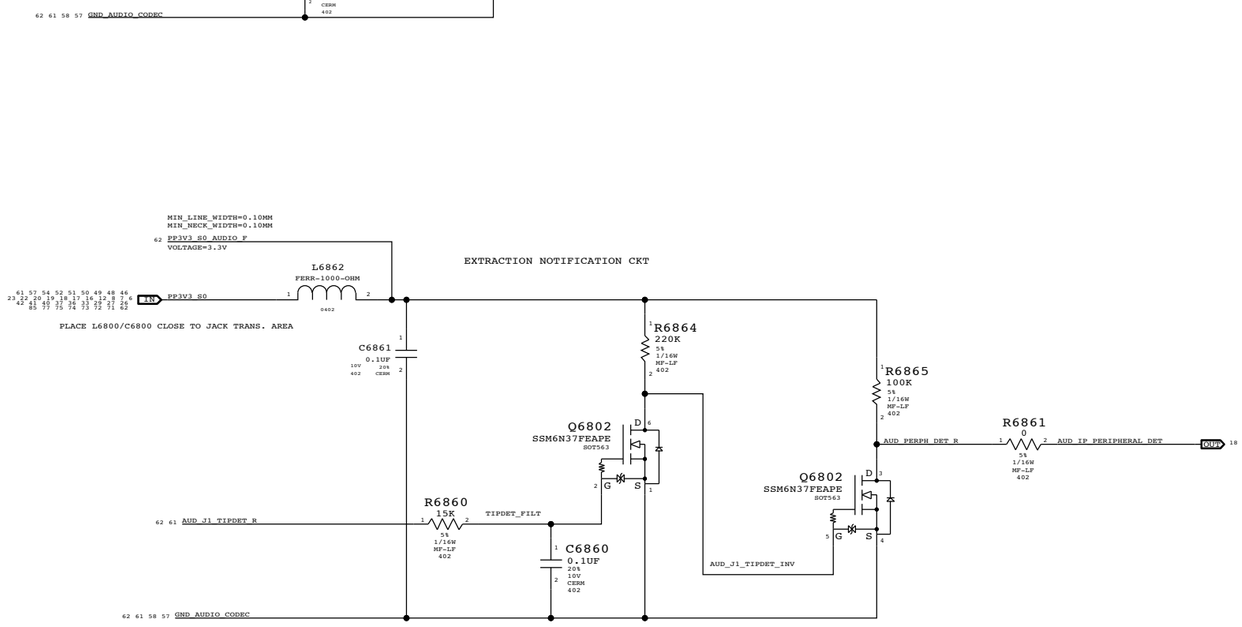
SOUTHBRIDGE RESOURCES

FUNCTION	SYSTEM GPIO	SYSTEM INTERRUPT
AUD_IPHS_SWITCH_EN	COUGAR_POINT GPIO16	N/A
AUD_I2C_INT_L	N/A	COUGAR_POINT GPIO5/PIRQH
AUD_IP_PERIPHERAL_DET	N/A	COUGAR_POINT GPIO3/PIRQH

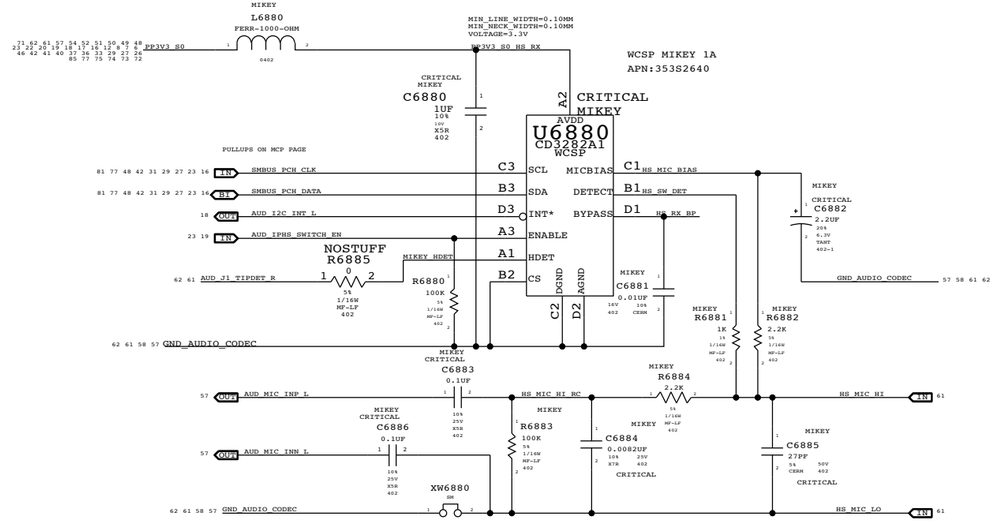
PORT A DETECT (HEADPHONES)

PORT B DETECT(SPDIF DELEGATE)

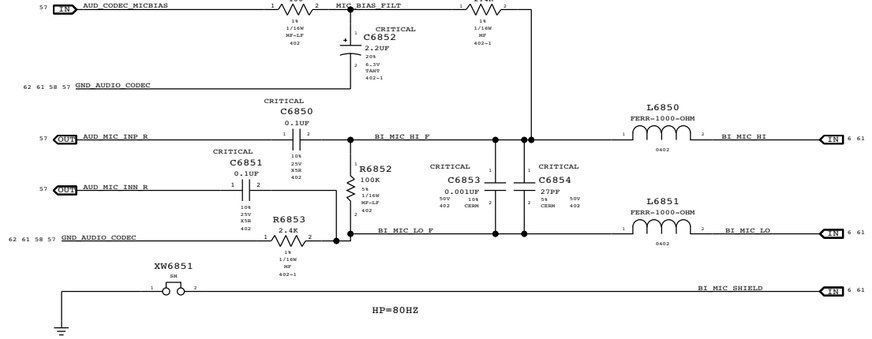




PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ



PORT B RIGHT(BUILT-IN MIC)



SYNC MASTER=LENG K90I SYNC DATE=08/10/2010

PAGE TITLE

AUDIO: JACK TRANSLATORS

Apple Inc.

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SIZE D

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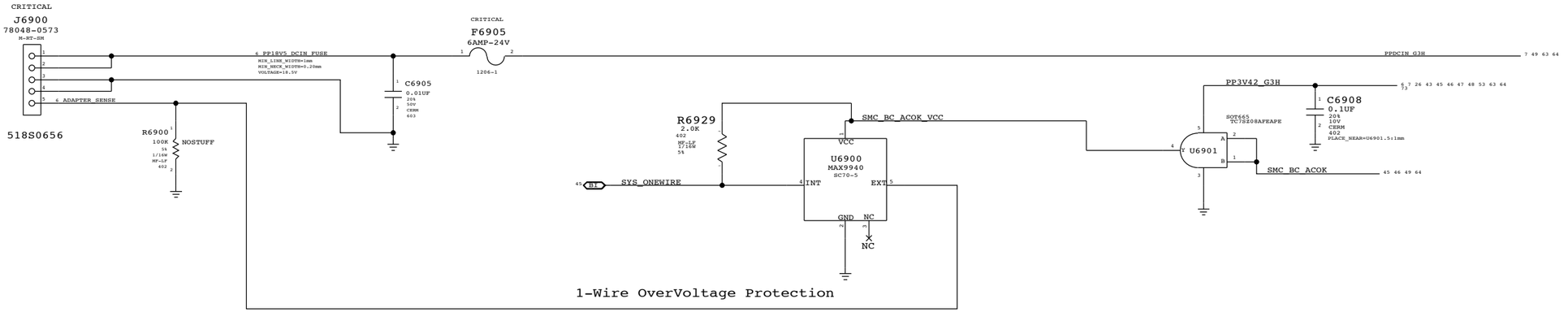
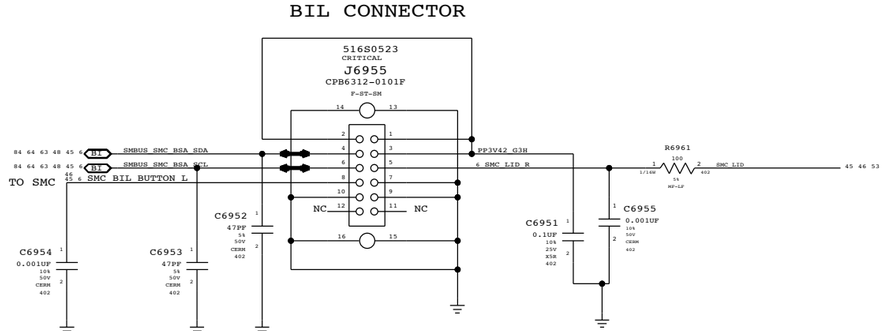
MagSafe DC Power Jack

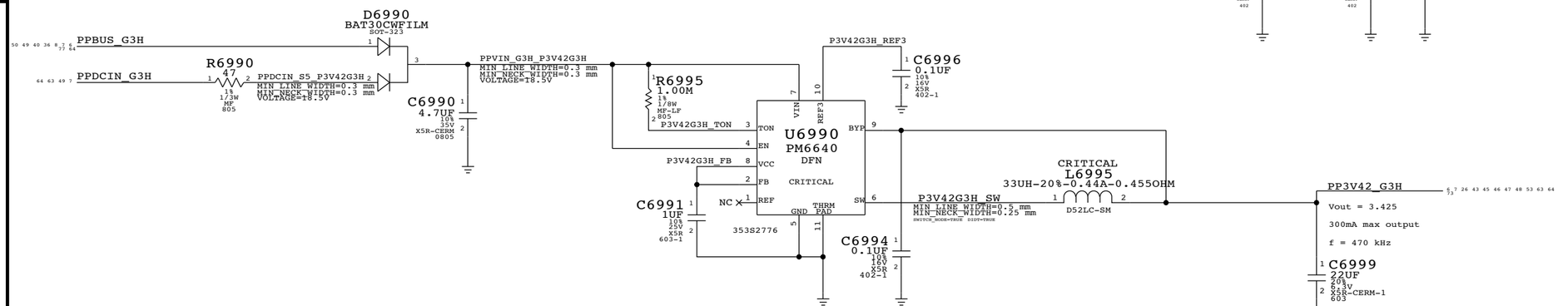


BIL CONNECTOR

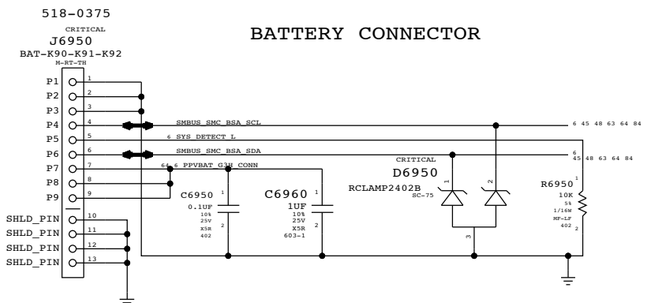


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



SYNC MASTER=JACK K90I SYNC DATE=08/20/2010

PAGE TITLE

DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER | SIZE D

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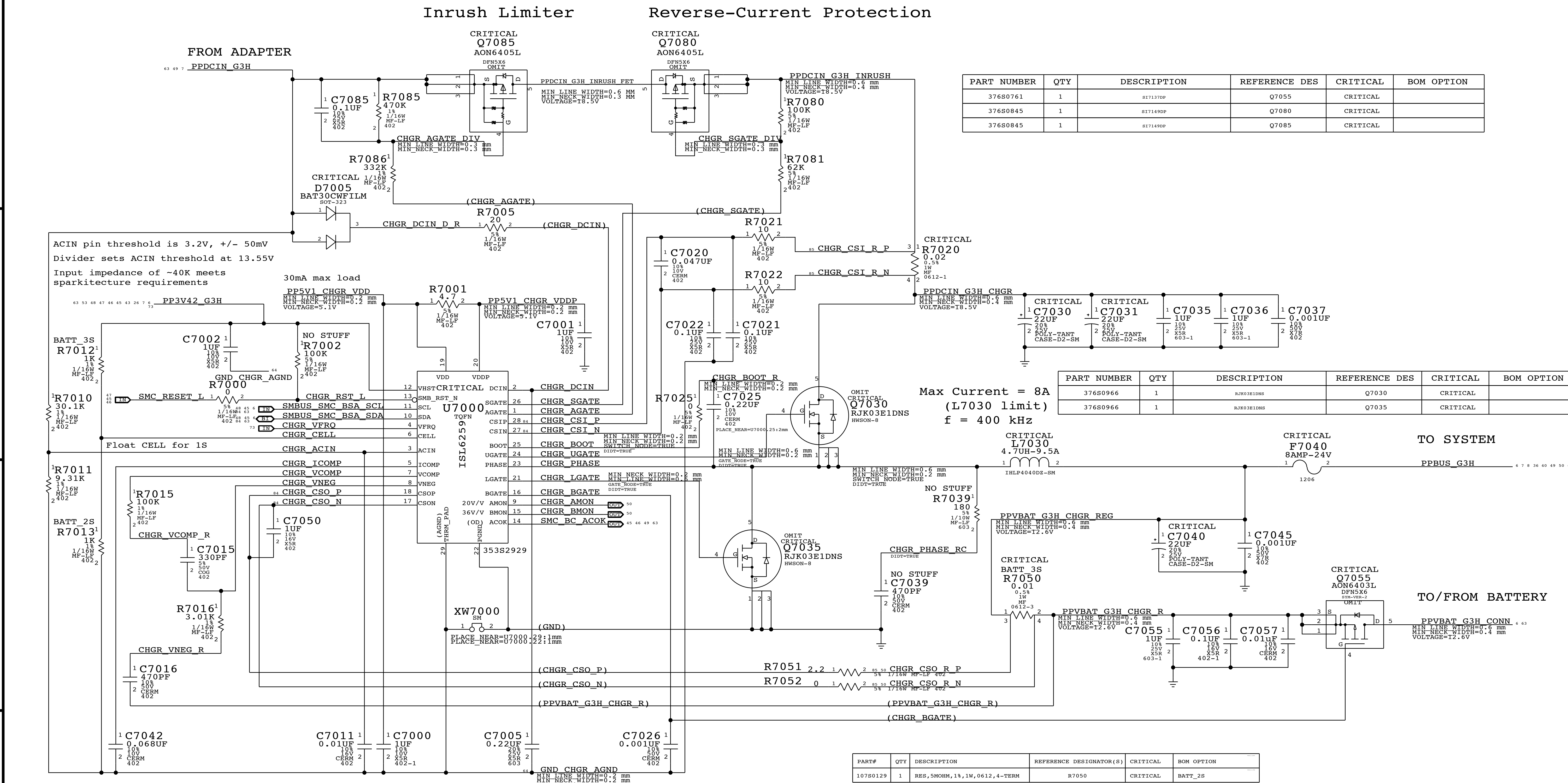


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0761	1	SI7137DP	Q7055	CRITICAL	
376S0845	1	SI7149DP	Q7080	CRITICAL	
376S0845	1	SI7149DP	Q7085	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DNS	Q7030	CRITICAL	
376S0966	1	RJK03E1DNS	Q7035	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0129	1	RES,5MOHM,1%,1W,0612,4-TERM	R7050	CRITICAL	BATT_2S

K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT

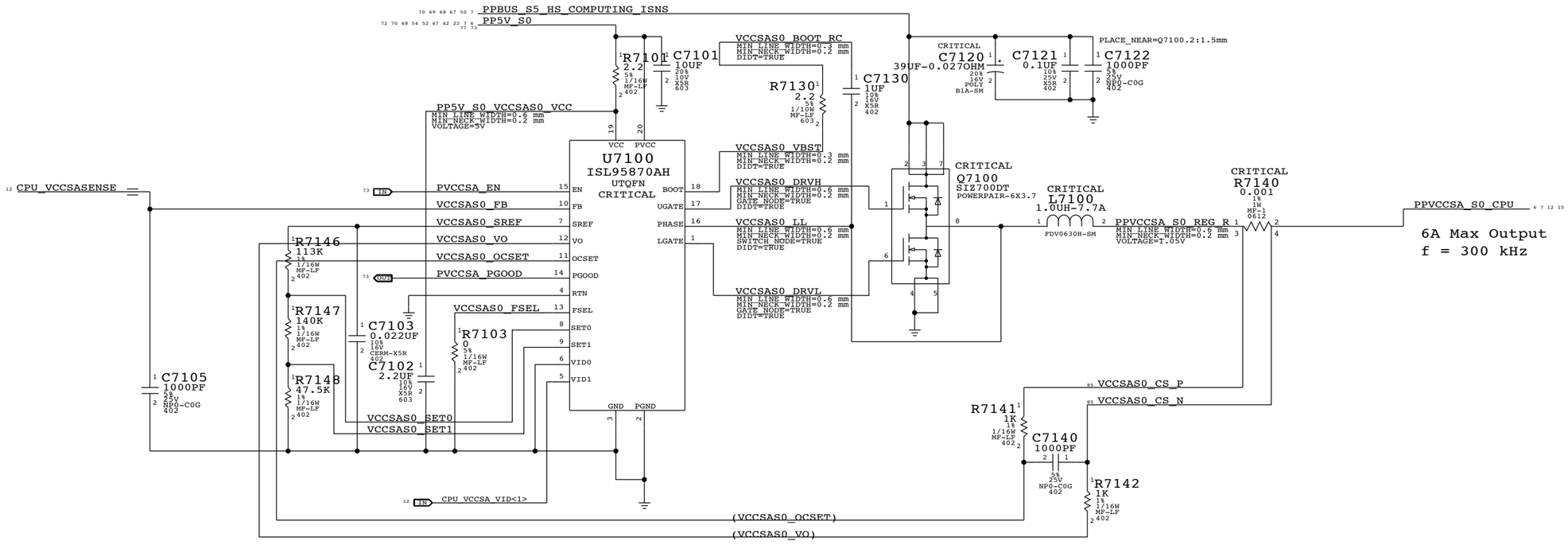
SYNC_MASTER=JACK_K90I SYNC_DATE=10/11/2010

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER — SIZE D — REVISION — BRANCH

System Agent Power Supply



SYNC MASTER=JACK K90I	SYNC DATE=08/19/2010
PAGE TITLE: System Agent Supply	
Apple Inc.	DRAWING NUMBER / SIZE: D
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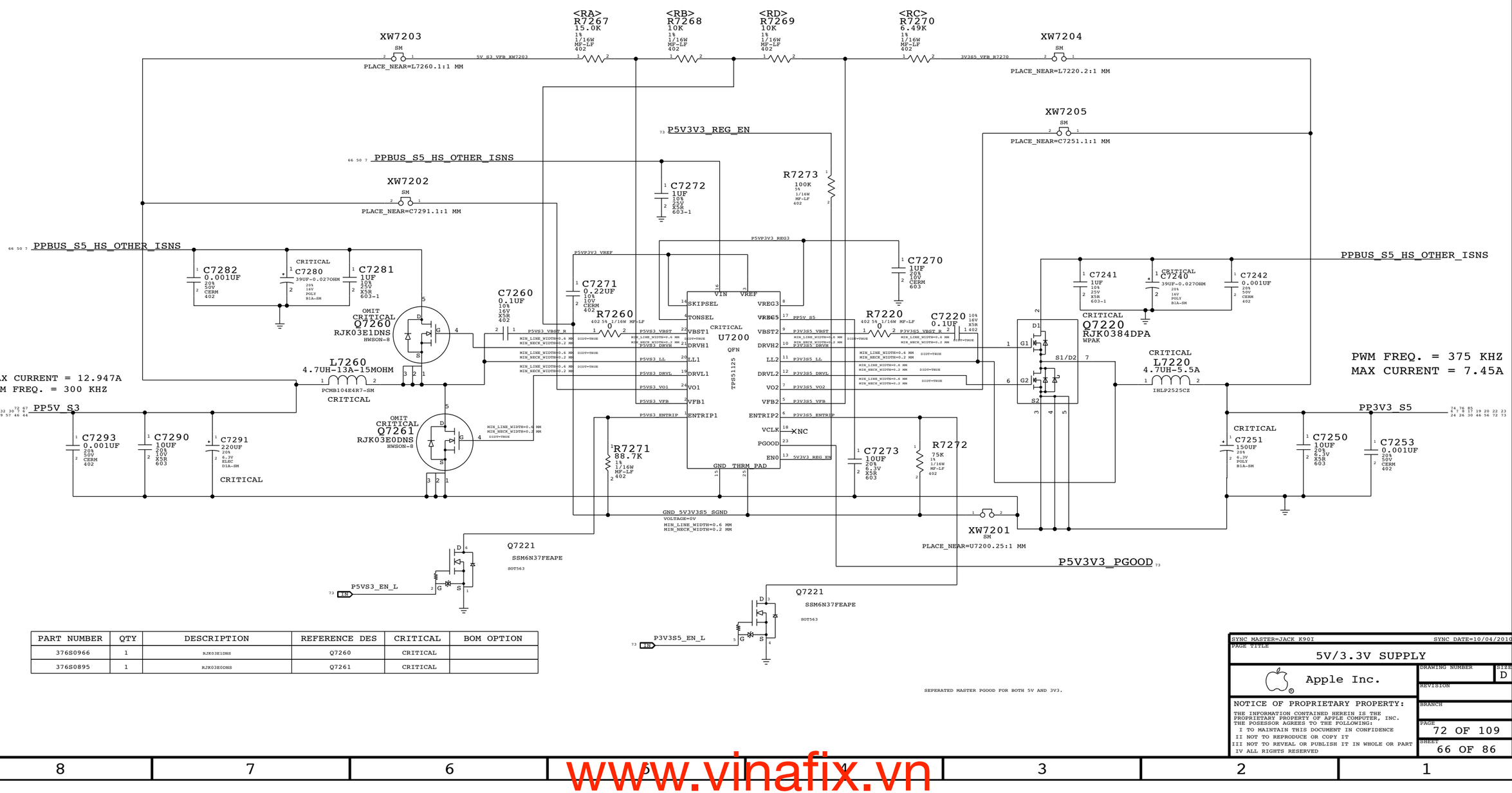
	SHEET: 65 OF 86

5V_S3/3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DNS	Q7260	CRITICAL	
376S0895	1	RJK03E0DNS	Q7261	CRITICAL	

SYNC MASTER=JACK K90I SYNC DATE=10/04/2010

PAGE TITLE

5V/3.3V SUPPLY

Apple Inc.

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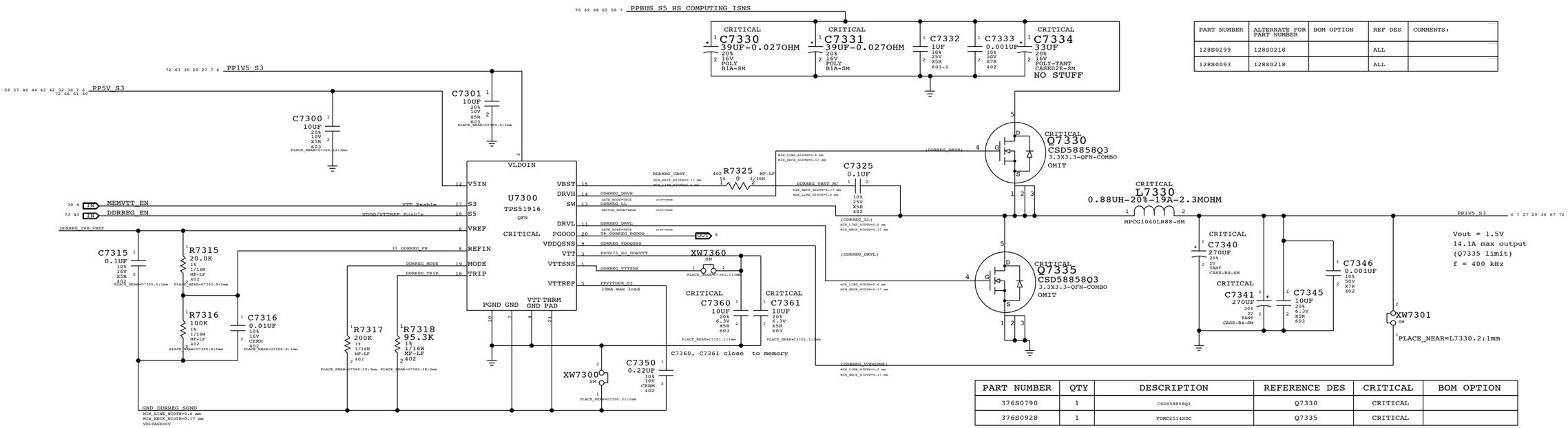

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0299	128S0218		ALL	
128S0093	128S0218		ALL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0790	1	CSD58858Q3	Q7330	CRITICAL	
376S0928	1	FDMC2514SDC	Q7335	CRITICAL	

SYNC_MASTER=JACK_K90I SYNC_DATE=10/11/2010

PAGE TITLE: 1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER | SIZE: D

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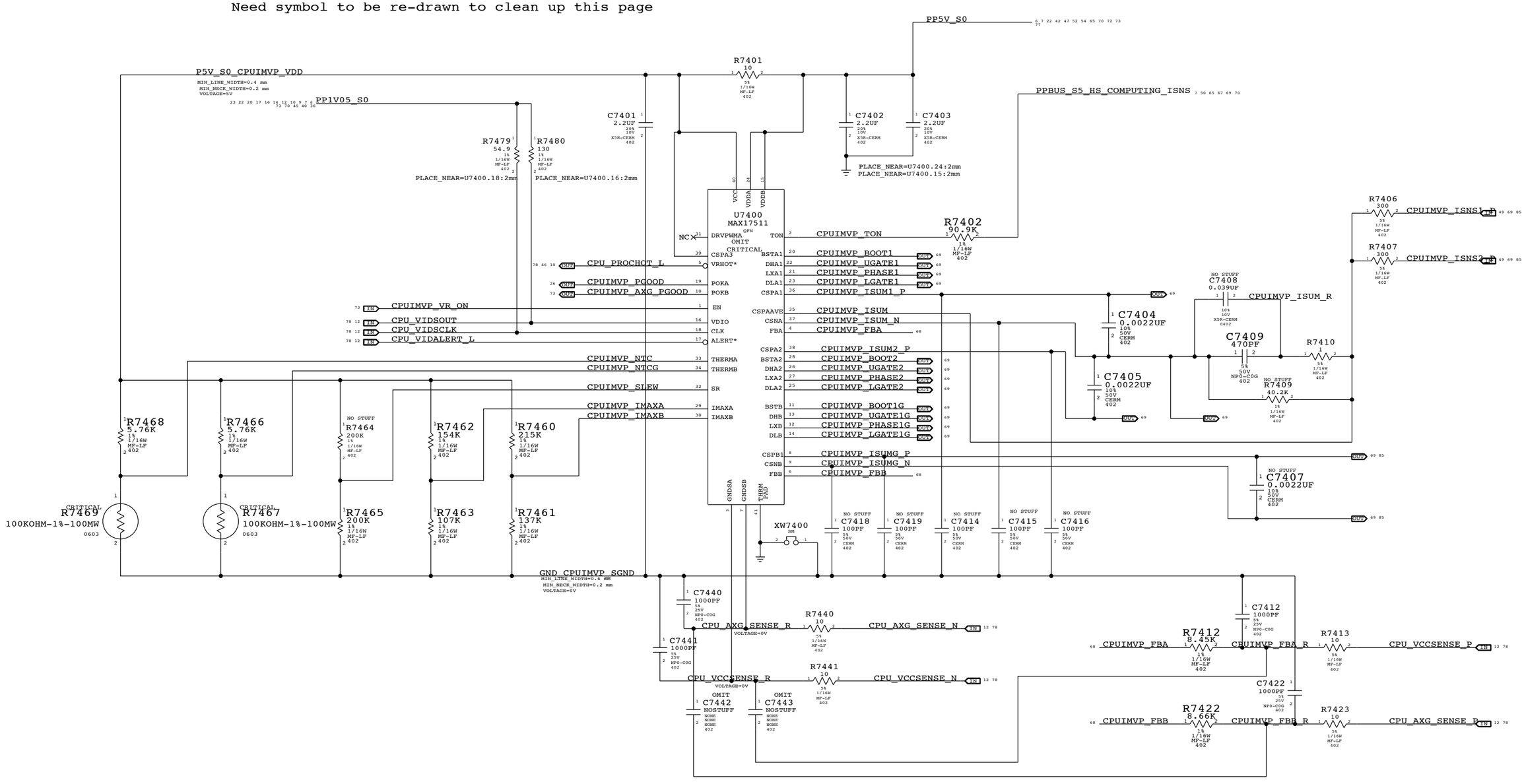
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3259	1	IC,MAX15092,3+1PH CPU REG,IMVP7,5X5QFN40	U7400	CRITICAL	

Need symbol to be re-drawn to clean up this page



SYNC_MASTER=JACK_K90I	SYNC_DATE=10/14/2011
PAGE TITLE	CPU IMVP7 & AXG VCore Regulator
Apple Inc.	DRAWING NUMBER: D; SIZE: D
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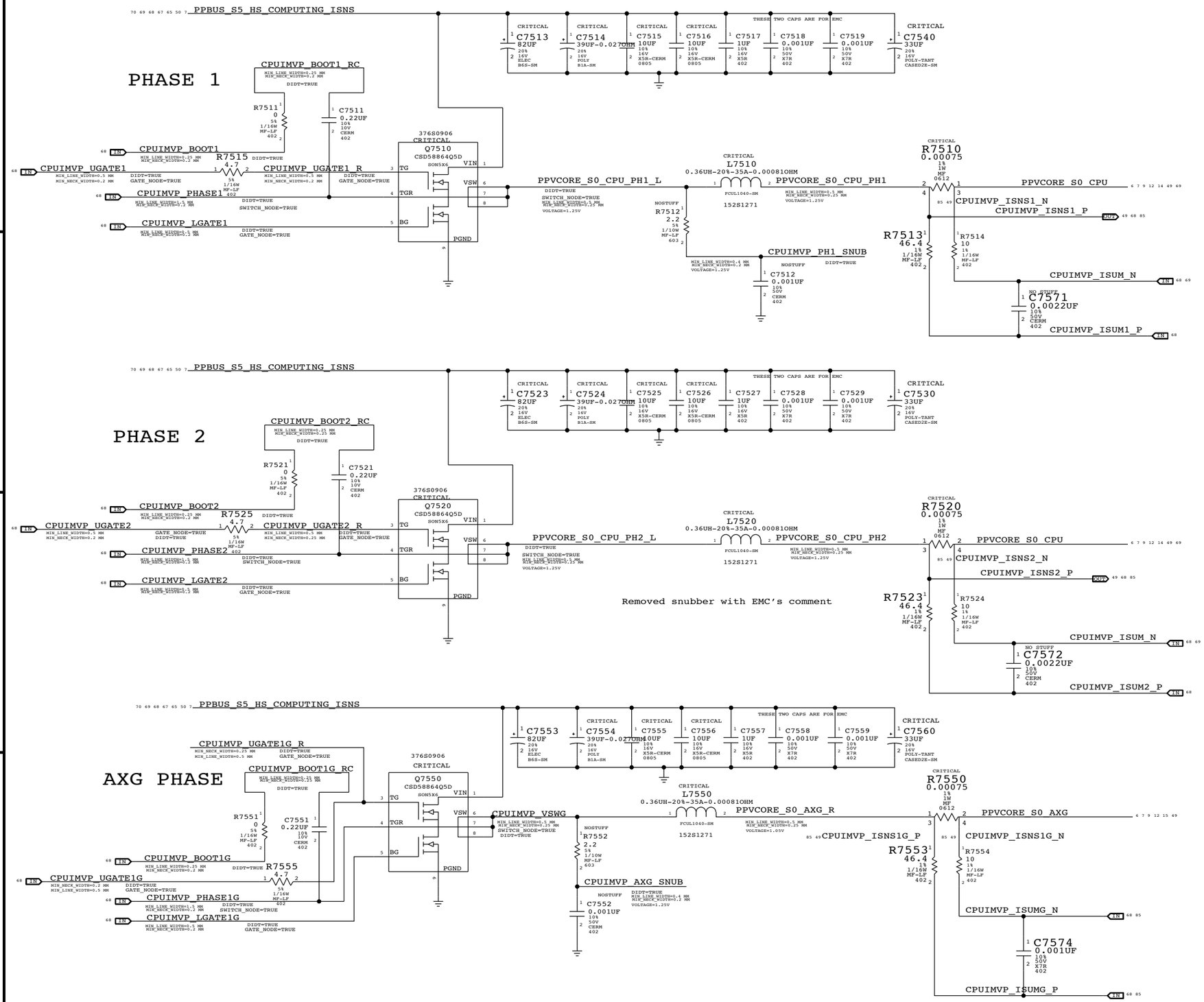
	PAGE: 74 OF 109
	SHEET: 68 OF 86



SYNC_MASTER=JACK_K90I	SYNC_DATE=09/03/2010
PAGE TITLE	CPU IMVP7 & AXG VCore Output
Apple Inc.	DRAWING NUMBER: — SIZE: D
	REVISION:
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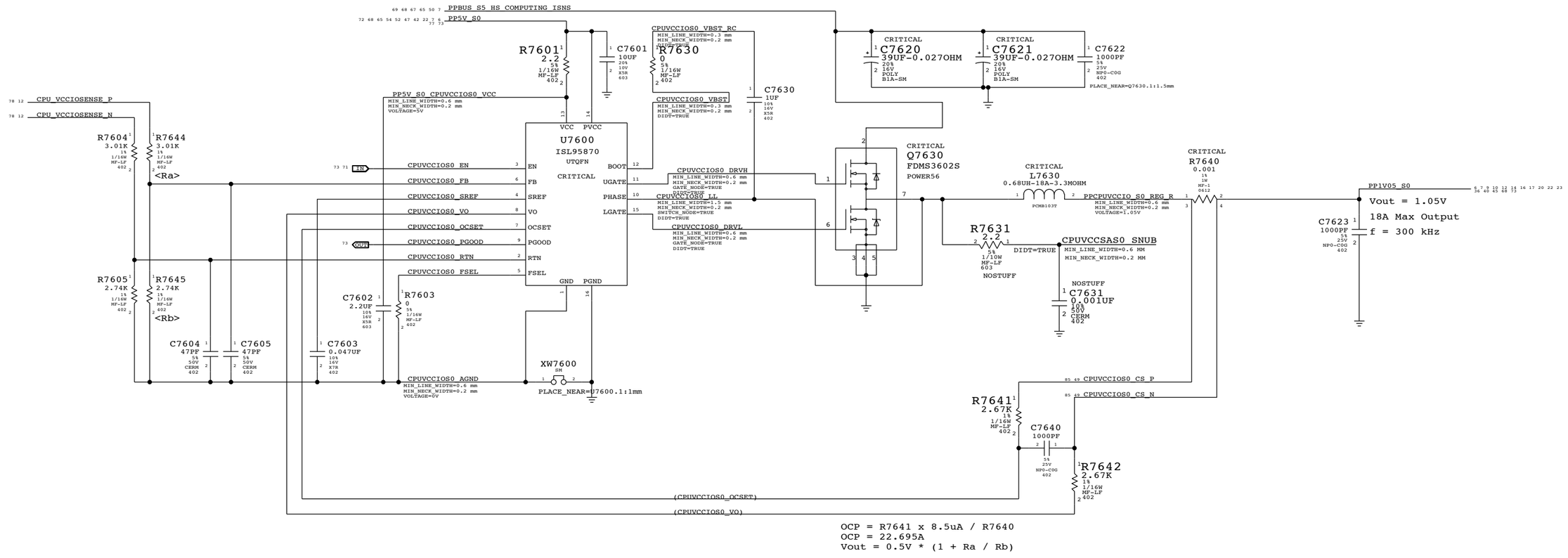
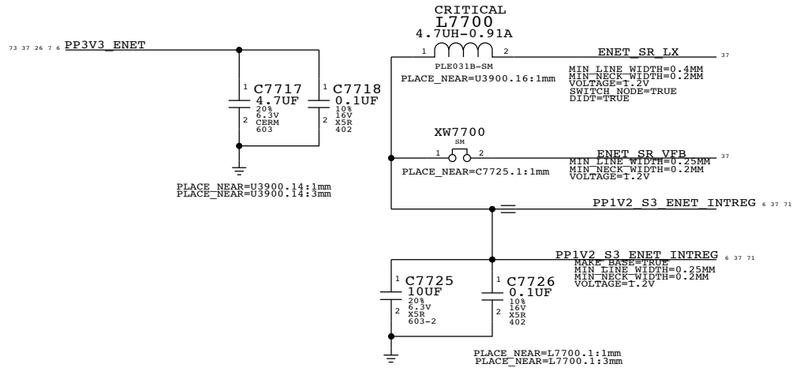
CPU VCCIO (1.05V S0) Regulator



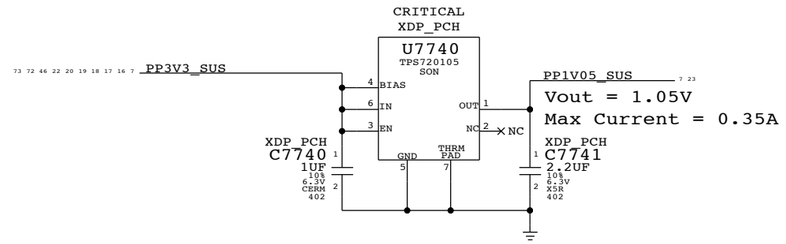
SYNC MASTER=JACK K90I	SYNC DATE=08/19/2010
PAGE TITLE	CPUVCCIO (1.05V) Power Supply
Apple Inc.	DRAWING NUMBER: 076-2000 SIZE: D
	REVISION:
	BRANCH:
	PAGE: 76 OF 109
	SHEET: 70 OF 86

CAESAR IV 1.2V INT.VR CMPTS

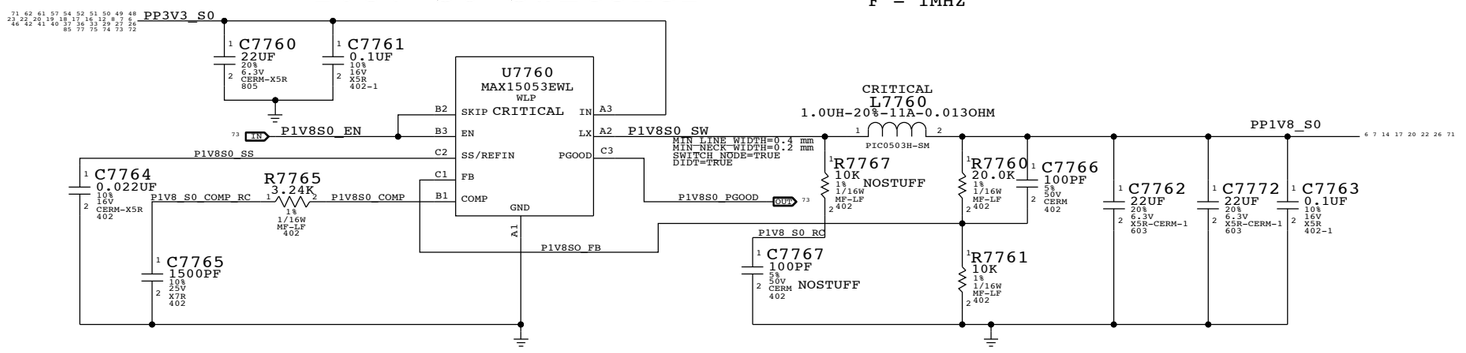


1.05V S5 LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in S5.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

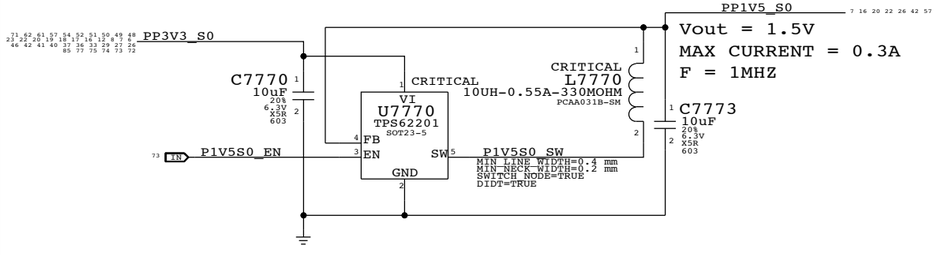


1.8V S0 Switcher

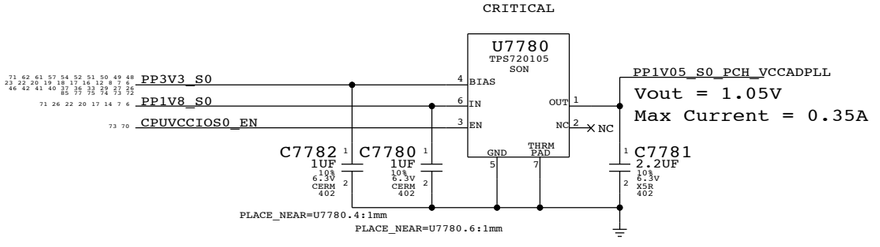


Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ

1.5V S0 Switcher



1.05V S0 LDO



SYNC_MASTER=JACK K90I SYNC_DATE=08/19/2010

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER | SIZE: D

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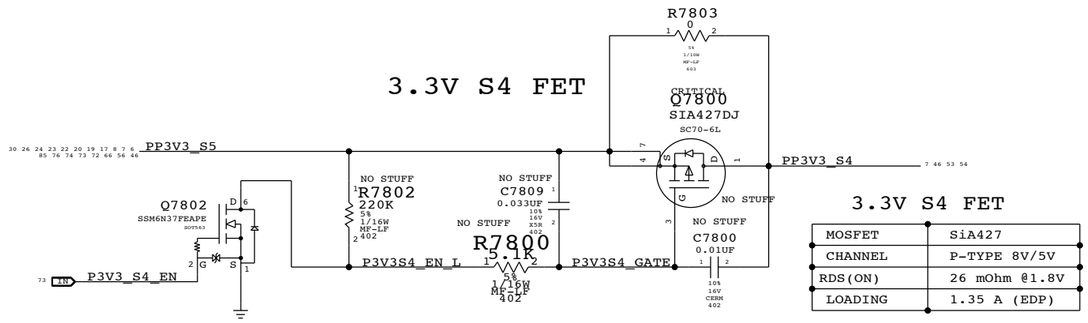
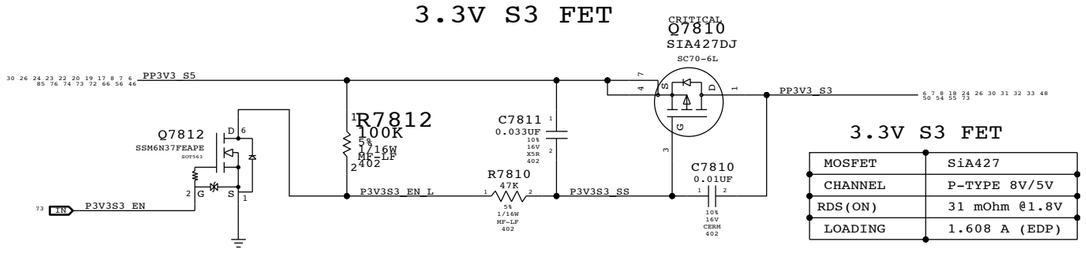
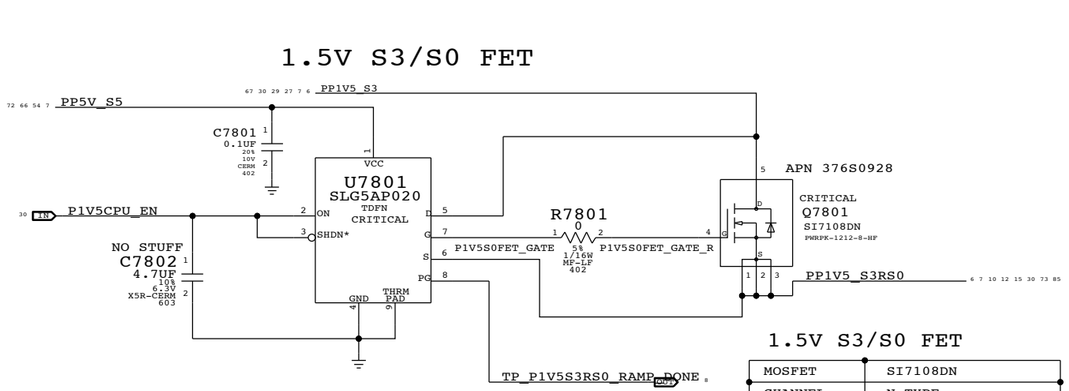


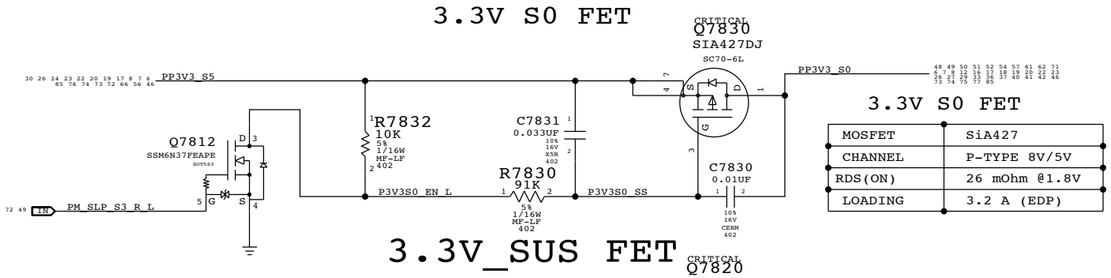
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.35 A (EDP)



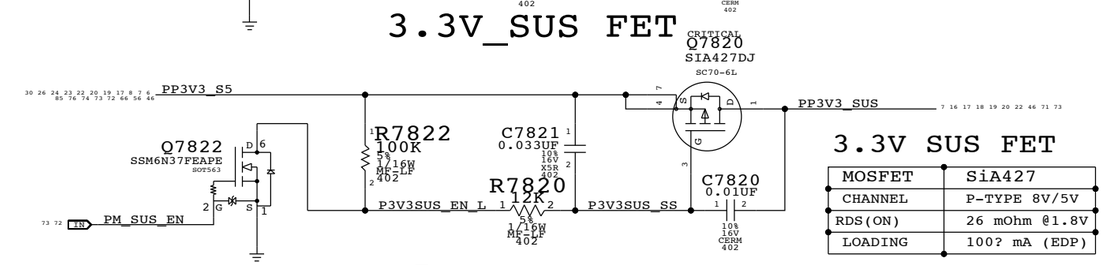
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)



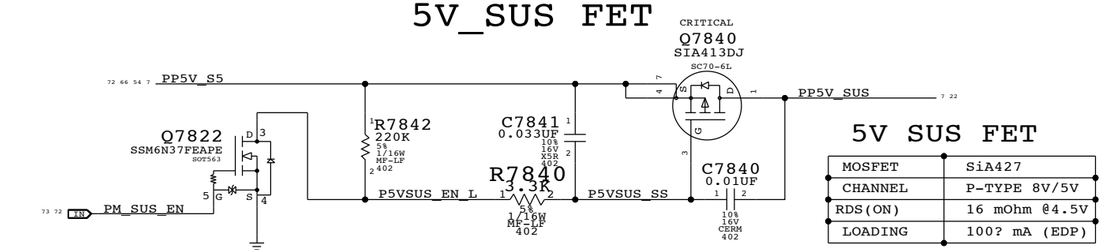
1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)



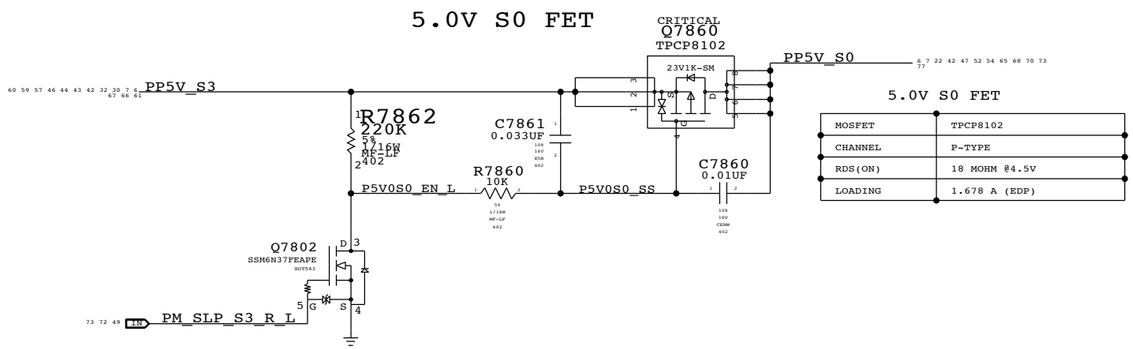
3.3V S0 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)



3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)



5V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	16 mOhm @4.5V
LOADING	100? mA (EDP)



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC MASTER=JACK K90I SYNC DATE=10/22/2010

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S5 Rail Enables & PGOOD

Internal pull-ups 100K +/- 20%

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

PP3V42_G3H
C7940 0.1uF 20% 10V CERM 402
U7941 SLG4AP012 TDFN (CRITICAL, VDD 343S0497)
SMC_PM_G2_EN (IN) MAKE_BASE=TRUE
PP3V3_S5
Threshold: ??
DLY > 10 ms
S5PGOOD_DLY
C7941 220PF 5% 25V CERM 402
R7941 100 5% 1/16W MF-LF 402
C7942 0.033UF 10% 16V X5R 402 NO STUFF
P3V3S5_EN_L (IN) MAKE_BASE=TRUE
P3V3S5_EN_L_R
P5V3V3_REG_EN
S5_PWRGD (OUT) MAKE_BASE=TRUE
S5_PWRGD (old name RSMRST_PWRGD)-->SMC
SMC-->PM_DSW_PWRGD

3.3V S4 ENABLE

NO STUFF
R7916 0 5% 1/16W MF-LF 402
PM_SLP_S5_L (IN)
P3V3_S4_EN (OUT) MAKE_BASE=TRUE
R7915 100K 5% 1/16W MF-LF 402
PLACE_NEAR=U1800.G18:5mm
Delete R when pull-down added to PCH page
SMC_S4_WAKESRC_EN
NO STUFF R7919 0 5% 1/16W MF-LF 402 PLACE_NEAR=U1800.G18:5mm

3.3V,5V S3 ENABLE

R7913 68K 5% 1/16W MF-LF 402
PP3V42_G3H
P5V3S3_EN_L (OUT) MAKE_BASE=TRUE
NO STUFF C7913 0.068UF 10% 10V CERM 402
R7914 3.3K 5% 1/16W MF-LF 402
PM_SLP_S4_L (IN) MAKE_BASE=TRUE
PSOC_VBUS_EN (OUT) MAKE_BASE=TRUE
R7910 100K 5% 1/16W MF-LF 402
Delete R when pull-down added to PCH page
R7911 5.1K 5% 1/16W MF-LF 402
R7912 9.1K 5% 1/16W MF-LF 402
PLACE_NEAR=Q7812.2:6mm
Q7911 SSM3K15FV SOD-VESM-HF
PLACE_NEAR=U7300.16:6mm
P3V3S3_EN (OUT) MAKE_BASE=TRUE
DDRREG_EN (OUT) MAKE_BASE=TRUE
C7910 0.47UF 10% 6.3V CERM-X5R 402
C7912 0.47UF 10% 6.3V CERM-X5R 402
PLACE_NEAR=U7300.16:6mm
PLACE_NEAR=Q7812.2:6mm

CPUVCORE ENABLE

ALL_SYS_PWRGD
R7974 0 5% 1/16W MF-LF 402
PLACE_NEAR=U7400.7:5mm
CPUIMVP_VR_ON (OUT)
NO STUFF
R7976 0 5% 1/16W MF-LF 402
R7975 0 5% 1/16W MF-LF 402
CPUVCCIOS0_PGOOD
PM_PECI_PWRGD (OUT)

S0 ENABLE

R7978 100 5% 1/16W MF-LF 402
PM_SLP_S3_L (IN)
R7979 100K 5% 1/16W MF-LF 402
Delete R when pull-down added to PCH page
PLACE_NEAR=U1800.P12:5mm
(PM_SLP_S3_R_L)
PM_SLP_S3_R_L MAKE_BASE=TRUE
R7987 33K 5% 1/16W MF-LF 402
R7981 20K 5% 1/16W MF-LF 402
R7988 39K 5% 1/16W MF-LF 402
R7986 5.1K 5% 1/16W MF-LF 402
PM_SLP_S3_R_L (OUT)
P1V8S0_EN (OUT) MAKE_BASE=TRUE
P1V5S0_EN (OUT) MAKE_BASE=TRUE
CPUVCCIOS0_EN (OUT) MAKE_BASE=TRUE
PVCCSA_EN (OUT) MAKE_BASE=TRUE
C7987 0.47UF 10% 6.3V CERM-X5R 402
C7981 0.47UF 10% 6.3V CERM-X5R 402
C7988 0.47UF 10% 6.3V CERM-X5R 402
C7986 0.47UF 10% 6.3V CERM-X5R 402

S0 Rail PGOOD (BJT Version)

PP3V3_S5
PP3V3_S0
R7951 15.0K 1% 1/16W MF-LF 402
R7952 7.15K 1% 1/16W MF-LF 402
R7956 150K 1% 1/16W MF-LF 402
R7953 1K 5% 1/16W MF-LF 402
R7954 1K 5% 1/16W MF-LF 402
R7955 1K 5% 1/16W MF-LF 402
VMON_3V3_DIV
VMON_Q2_BASE
VMON_Q3_BASE
PP1V5_S3RS0
PP1V05_S0
S0PGD_C
Q7950 ASMCC0179 DFN2015H4-8 (Q1 Q2 Q3 CRITICAL Q4)
NC
353S2809 S0PGD_BJT_GND_R
R7957 100 5% 1/16W MF-LF 402
Worst-Case Thresholds:
Q2: 0.XXXV
Q3: 0.640V
3.3.V w/Divider: 2.345V
Q4: 0.660V

3.3V/5.0V Sus ENABLE

PP3V3_S5
C7943 0.1uF 20% 10V CERM 402
SMC_BATLOW_L:100K pull up on SMC page
SMC_BATLOW_L (IN)
U7940 74AUP1G32GS SOT891 (VCC A B C Y GND)
ALL_SYS_PWRGD
PM_SLP_SUS_L (IN)
PM_SUS_EN (OUT) MAKE_BASE=TRUE
PLACE_NEAR=U1800.G16:5mm
R7918 100K 5% 1/16W MF-LF 402
Delete R when pull-down added to PCH page
NO STUFF R7917 0 5% 1/16W MF-LF 402

3.3V SUS Detect

PP3V3_S5
PLACE_NEAR=U7930.6:2.3mm
C7930 0.1uF 20% 10V CERM 402
No stuff C7931, 12ms Min delay time
U7930 Sense input threhold is 3.07V
PP3V3_SUS
R7933 100K 5% 1/16W MF-LF 402
CRITICAL U7930 TPS3808G33DBVRG4 SOT23-6 (VDD SENSE RESET* CT GND MR*)
PM_RSMRST_L (OUT)
PM_RSMRST_L goes to U1800.C21
S4_PGOOD
C7931 0.001UF 20% 50V CERM 402 NO STUFF

CHGR VFRQ Generation

PP3V42_G3H
R7931 10K 5% 1/16W MF-LF 402
CHGR_VFRQ (OUT)
Q7931 SSM3K15FV SOD-VESM-HF
VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

3.3V ENET FET

CRITICAL Q7922 NTR4101P SOT-23-HF
PP3V3_S3
PP3V3_ENET
R7921 10K 5% 1/16W MF-LF 402
C7921 0.033UF 10% 16V X5R 402
R7922 100K 5% 1/16W MF-LF 402
C7922 0.01UF 10% 16V CERM 402
P3V3ENET_SS
PM_ENET_EN_L

S0 Rail PGOOD Circuitry

Thresholds: (ISL Version in development)
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

PP5V_S0
PP3V3_S0
PP1V5_S3RS0
PP1V05_S0
S0PGOOD_ISL
C7960 0.1uF 20% 10V CERM 402
R7960 6.04K 1% 1/16W MF-LF 402
R7970 10K 1% 1/16W MF-LF 402
R7972 6.04K 1% 1/16W MF-LF 402
U7960 ISL88042IRTEZ TDFN (CRITICAL) (VDD V2MON V3MON V4MON RST* GND THRM_PAD)
P5V_DIV_VMON
P1V5_DIV_VMON
P1V05_DIV_VMON
R7961 15.0K 1% 1/16W MF-LF 402
R7971 10K 1% 1/16W MF-LF 402
R7973 15.0K 1% 1/16W MF-LF 402
ALL_SYS_PWRGD_R
353S2310
R7962 330 5% 1/16W MF-LF 402
R7967 10K 5% 1/16W MF-LF 402
R7968 100 5% 1/16W MF-LF 402 NO STUFF
R7966 100 5% 1/16W MF-LF 402
R7965 100 5% 1/16W MF-LF 402
R7964 100 5% 1/16W MF-LF 402
R7963 100 5% 1/16W MF-LF 402
CPUIMVP_AXG_PGOOD
P1V8S0_PGOOD
P5V3V3_PGOOD
CPUVCCIOS0_PGOOD
PVCCSA_PGOOD
P1V5S0_PGOOD from U7710

DP S4 Power Enable

SMC_S4_WAKESRC_EN
MAKE_BASE=TRUE

PSOC USB Power Enable

SMC_ADAPTER_EN (IN)

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

WOL_EN (IN)
Q7925 2N7002DW-X-G SOT-363
Q7921 SSM3K15FV SOD-VESM-HF
PM_WLAN_EN_L (OUT)
AP_PWR_EN (IN)
PM_SLP_S3_L (IN)
AC_EN_L
(AC_EN_L)
(PM_SLP_S3_L)
Q7920 2N7002DW-X-G SOT-363
NO STUFF R7929 0 5% 1/16W MF-LF 402

SYNC MASTER=JACK K90I SYNC DATE=10/22/2010
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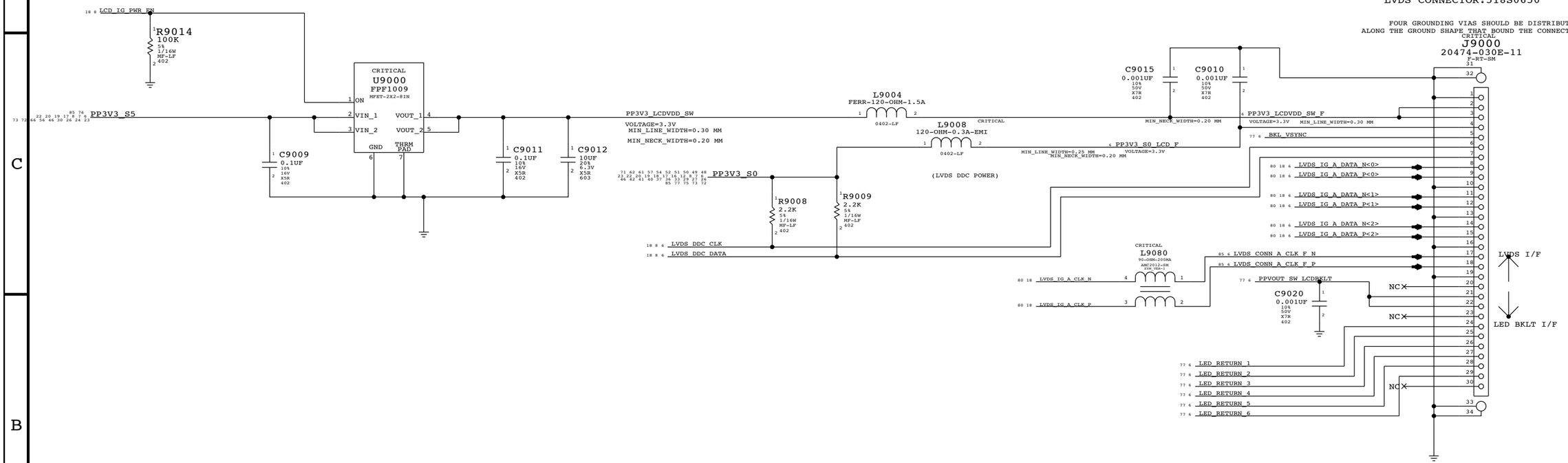
LCD CONNECTOR

LVDS CONNECTOR:518S0650

FOUR GROUNDING VIAS SHOULD BE DISTRIBUTED
ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY



SYNC MASTER=K24 MLB	SYNC DATE=07/20/2009
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T29 A High-Speed Signals

DP_EXTA_ML_C_P<0> C9300 0.1UF DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1UF DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1UF DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1UF DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1UF DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1UF DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1UF DP_EXTA_ML_P<3>
DP_EXTA_ML_C_N<3> C9307 0.1UF DP_EXTA_ML_N<3>
DP_EXTA_AUXCH_C_P C9308 0.1UF DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1UF DP_EXTA_AUXCH_N

PP3V3_S0
R9309 1M 5% MF 1/20W 201 DP_EXTA_AUXCH_P
R9308 1M 5% MF 1/20W 201 DP_EXTA_AUXCH_N

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

T29 signals are P/N-swapped after AC caps to improve layout.

T29_A_BIAS_R2DP0
T29_A_BIAS_R2DN0
GND_VOID=TRUE (C9370/C9371)
C9370 0.47UF
C9371 0.47UF

T29_D2R_N<0> T29_D2R_P<0>
OVERSIZE_PAD=0.875 mm^2 (Both L's)
L9372 1.0NH+/-0.1NH 0201-1
L9373 1.0NH+/-0.1NH 0201-1
T29_R2D_C_N<0> T29_R2D_C_P<0>
T29_R2D_C_F_N<0> T29_R2D_C_F_P<0>
C9372 0.47UF (C9372.2)
C9373 0.47UF (C9373.2)
GND_VOID=TRUE

R9372 1.5K 5% MF 1/20W 201 T29_R2D_P<0>
R9373 1.5K 5% MF 1/20W 201 T29_R2D_N<0>

D9364 BAR90-02LRH TSLP-2-7 GND_VOID=TRUE (D9364.2)
D9372 BAR90-02LRH TSLP-2-7
D9373 BAR90-02LRH TSLP-2-7
D9365 BAR90-02LRH TSLP-2-7
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY

T29: TX_0
T29DPA_ML_C_P<0> T29DPA_ML_C_N<0>
GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)
R9374 1.5K 5% MF 1/20W 201
R9375 1.5K 5% MF 1/20W 201
T29_D2R_C_P<0> T29_D2R_C_N<0>

T29_A_BIAS_R2DP1
T29_A_BIAS_R2DN1
GND_VOID=TRUE (C9380/C9381)
C9380 0.47UF
C9381 0.47UF

T29_D2R_N<1> T29_D2R_P<1>
OVERSIZE_PAD=0.875 mm^2 (Both L's)
L9382 1.0NH+/-0.1NH 0201-1
L9383 1.0NH+/-0.1NH 0201-1
T29_R2D_C_N<1> T29_R2D_C_P<1>
T29_R2D_C_F_N<1> T29_R2D_C_F_P<1>
C9382 0.47UF (C9383.2)
C9383 0.47UF (C9383.2)
GND_VOID=TRUE

R9382 1.5K 5% MF 1/20W 201 T29_R2D_P<1>
R9383 1.5K 5% MF 1/20W 201 T29_R2D_N<1>

T29 Path Biasing

D9360 BAR90-02LRH TSLP-2-7 GND_VOID=TRUE (D9360.2)
D9382 BAR90-02LRH TSLP-2-7
D9383 BAR90-02LRH TSLP-2-7
D9361 BAR90-02LRH TSLP-2-7
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)

T29: TX_1
T29DPA_ML_C_P<2> T29DPA_ML_C_N<2>
GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)
R9384 1.5K 5% MF 1/20W 201
R9385 1.5K 5% MF 1/20W 201
T29_D2R_C_P<1> T29_D2R_C_N<1>

Both R's must connect to C in star topology.

DP A Super-Driver

PP3V3_S0

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

C9310 2.2UF 20% 6.3V CERM 402-LF
C9311 0.1UF 10% 16V X5R-CERM 0201
C9312 0.1UF 10% 16V X5R-CERM 0201

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL

DP_EXTA_ML_P<0>	IN_D0P	OUT_D0P	DP_SDRVA_ML_C_P<0>
DP_EXTA_ML_N<0>	IN_D0N	OUT_D0N	DP_SDRVA_ML_C_N<0>
DP_EXTA_ML_P<1>	IN_D1P	OUT_D1P	DP_SDRVA_ML_C_P<1>
DP_EXTA_ML_N<1>	IN_D1N	OUT_D1N	DP_SDRVA_ML_C_N<1>
DP_EXTA_ML_P<2>	IN_D2P	OUT_D2P	DP_SDRVA_ML_C_P<2>
DP_EXTA_ML_N<2>	IN_D2N	OUT_D2N	DP_SDRVA_ML_C_N<2>
DP_EXTA_ML_P<3>	IN_D3P	OUT_D3P	DP_SDRVA_ML_C_P<3>
DP_EXTA_ML_N<3>	IN_D3N	OUT_D3N	DP_SDRVA_ML_C_N<3>
DP_EXTA_DDC_CLK	IN_SCL	AC_AUXP	DP_SDRVA_AUXCH_C_P
DP_EXTA_DDC_DATA	IN_SDA	AC_AUXN	DP_SDRVA_AUXCH_C_N
DP_EXTA_AUXCH_P	IN_AUXP	OUT_AUXP_SCL	(DP_SDRVA_AUXCH_P)
DP_EXTA_AUXCH_N	IN_AUXN	OUT_AUXN_SDA	(DP_SDRVA_AUXCH_N)
DP_EXTA_HPD	IN_HPD	(IPD) OUT_HPD	(DP_SDRVA_HPD)
DPSDRVA_I2C_CTL_EN	I2C_CTL_EN (IPU)	CA_DET	DP_A_CA_DET
DPSDRVA_I2C_ADDR0	I2C_ADDR0 (IPD)	CEXT	DPSDRVA_CEXT
DPSDRVA_I2C_ADDR1	I2C_ADDR1 (IPD)		
I2C_DPSDRVA_SCL	SCL_CTL		
I2C_DPSDRVA_SDA	SDA_CTL		
DPSDRVA_REXT	REXT		
DP_AUXCH_ISOL	AUXDDC_OFF (IPD)		
DP_A_PWRDWN_R	PD (IPD)		

PLACE_NEAR=U9310.11:2 mm
C9319 2.2UF 20% 6.3V CERM 402-LF

NO STUFF R9311 1K 5% 1/16W MF-LF 402
R9310 1K 5% 1/16W MF-LF 402
R9312 1K 5% 1/16W MF-LF 402

SDRV_PD R9318 0 5% 1/20W MF 201
R9319 4.22K 1% 1/16W MF-LF 402

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

R9354 30 5% MF 1/20W 201 DP_SDRVA_ML_R_P<0>
R9355 30 5% MF 1/20W 201 DP_SDRVA_ML_R_N<0>
R9350 30 5% MF 1/20W 201 DP_SDRVA_ML_R_P<2>
R9351 30 5% MF 1/20W 201 DP_SDRVA_ML_R_N<2>

C9364 0.22UF 20% 6.3V X5R 201 DP_SDRVA_ML_P<0>
C9365 0.22UF 20% 6.3V X5R 201 DP_SDRVA_ML_N<0>
C9360 0.22UF 20% 6.3V X5R 201 DP_SDRVA_ML_P<2>
C9361 0.22UF 20% 6.3V X5R 201 DP_SDRVA_ML_N<2>

R9352 270 5% 1/20W MF 201
R9353 270 5% 1/20W MF 201
PP3V3_S0

C9359 0.1UF 10% 16V X5R 402
CRITICAL U9359 74LVC1G04DBVCK SC70
DP_A_PWRDWN DP_A_BIAS

IC supports input high while Vcc = 0V.

C9363 0.1UF
C9362 0.1UF
C9367 0.1UF
C9366 0.1UF
C9369 0.1UF
C9368 0.1UF
10% 16V X5R-CERM 0201

AUXCH Snoop Port, used by PS8301 during training.

I2C Addr: 0x26/0x27 (Wr/Rd)

DP Path Biasing

DP_A_BIAS0 VOLTAGE=3.3V
R9361 1.5K 5% MF 1/20W 201
R9360 1.5K 5% MF 1/20W 201
DP_A_BIAS2 VOLTAGE=3.3V
R9365 1.5K 5% MF 1/20W 201
R9364 1.5K 5% MF 1/20W 201

R9362 51 5% 1/20W MF 201
R9363 51 5% 1/20W MF 201
Both R's: PLACE_NEAR=C9361.1:2mm
C9358 0.1uF 10% 16V X5R 402

DP/T29 A Low-Speed MUX

PP3V3_SW_DPAPWR
Must be 3.3V DP A port power

C9390 0.1UF 10% 16V CERM 402
C9391 0.1UF 10% 16V CERM 402
R9399 100K 5% 1/20W MF 201

OMIT_TABLE
U9390 CBTL04DP081 HVQFN

DP_SDRVA_ML_N<3>	31	DIN1_0+	DOUT_0+ 1 T29DPA_ML_N<3>
DP_SDRVA_ML_P<3>	30	DIN1_0-	DOUT_0- 2 T29DPA_ML_P<3>
DP_SDRVA_ML_N<1>	27	DIN1_1+	T29: Unused
DP_SDRVA_ML_P<1>	26	DIN1_1-	
DP_SDRVA_AUXCH_P	19	AUX1+	CRITICAL
DP_SDRVA_AUXCH_N	18	AUX1-	
DP_SDRVA_HPD	17	HPD_1	DOUT_1+ 4 T29DPA_ML_N<1>
CKPLUS_WAIVE=NdifPr_badTerm			DOUT_1- 5 T29DPA_ML_P<1>
T29_A_RSVD_N	25	DIN2_0+	T29: LSX_A_R2P/P2R (P/N)
T29_A_RSVD_P	24	DIN2_0-	
(T29_A_LSX_P2R)	23	DIN2_1+	AUX+ 6 DP_A_EXT_AUXCH_P
(T29_A_LSX_R2P)	22	DIN2_1-	AUX- 7 DP_A_EXT_AUXCH_N
T29_D2R1_BIASP	15	AUX2+	T29: RX_1 Bias Sink
T29_D2R1_BIASN	14	AUX2-	HPD_IN 8 DP_A_EXT_HPD
NC	13	HPD_2	
DP_A_PWRDWN	10	GPU_SEL	LO=Port A
T29_A_BIAS	32	AUX_SEL	HI=Port B
	11	NC	

THMPAD GND
SIGNAL_MODEL=T29DP_MUX

R9398 100K 5% 1/20W MF 201

R9396 1K 5% 1/20W MF 201
R9397 1K 5% 1/20W MF 201

CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

Port A MCU

PP3V3_SW_DPAPWR
Must be 3.3V DP A port power

C9330 0.1UF 20% 10V CERM 402
C9331 0.1UF 20% 10V CERM 402

U9330 LPC1112A HVQFN25 CRITICAL OMIT_TABLE

DP_A_CA_DET	1	RESET#/PIO0_0	R/PIO1_0/AD1 16 T29DPA_CONFIG1_RC
	2	PIO0_1/CLKOUT	R/PIO1_1/AD2 17 T29DPA_CONFIG2_RC
T29_LSEO<0>	7	PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3 18 T29_A_HV_EN_R
I2C_T29_SCL	8	PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4 19 T29_A_UC_ADDR
I2C_T29_SDA	9	PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP 20 DP_A_EXT_HPD
T29DPA_HPD	10	PIO0_6/SCK	PIO1_6/RXD 23 T29_A_LSX_P2R
T29_A_BIAS_R	11	PIO0_7/CTS#	PIO1_7/TXD 24 T29_A_LSX_R2P
T29_LSOE<0>	12	PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0 6 T29_LSEO<1>
T29_LSOE<1>	13	PIO0_9/MOSI/CT16B0_MAT1	
T29_MCU_INT_L	14	SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)	
	15	R/PIO0_11/AD0 (OD)	XTALIN 4
		VSS 3, THRM PAD 21, VDD 5	

R9338 10K 5% 1/16W MF-LF 402
R9334 10K 5% 1/16W MF-LF 402
R9339 1M 5% 1/16W MF-LF 402
R9335 1K 5% 1/16W MF-LF 402
R9336 10K 5% 1/16W MF-LF 402

P2R = Plug to Receptacle
R2P = Receptacle to Plug

R9392 51 5% 1/20W MF 201
R9393 51 5% 1/20W MF 201

=T29_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#

=T29_WAKE_L
OMIT R9330 0 5% 1/16W MF-LF 402
SWCLK
SWDIO
T29_A_UC_ADDR

R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

SYNC_MASTER=T29	SYNC_DATE=10/16/2010
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Port A HV Power Switch

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance unknown

PP3V3_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

PP15V_T29
20V Max

R9416 470K 5% 1/16W MF-LF 402

C9410 0.1UF 10% 50V X7R 603-1

U9410 TPS2590 QFN
VIN, VOUT, EN* (IPU-Weak!), FLT*, RTRY*, ILIM, CT, IFLT, GND, THRM PAD

C9411 0.1UF 10% 50V X7R 603-1

PPHV_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

D9410 STPS2L30AF SM

DPAPWRSW_HVEN_L_R
TP_DPAPWRSW_FLT_L
DPAPWRSW_ILIM
DPAPWRSW_IFLT
DPAPWRSW_CT

C9412 0.47UF 10% 16V X5R 402 <CT>

R9410 100K 1% 1/16W MF-LF 402 <RFLT>

R9411 200K 1% 1/16W MF-LF 402 <RLIM>

IFLT = 200k / RFLT = 885mA
ILIM = 201k / RLIM = 935mA
TFLT = CCT * 38900
TSD = CCT * 100000

Q9415 SSM3K15FV SOD-VESM-HF

T29_A_HV_EN

Q9419 DMB53D0UV SOT-563

DPAPWR_BLDR_B
DPAPWR_BLDR_E

Bleeder Resistor
2.5V / 249 ohm = 10mA
R9419 249 1% 1/16W MF-LF 402 P = ~27mW
MIN_LINE_WIDTH=0.20 MM
MIN_NECK_WIDTH=0.20 MM

Note: Bleeder active when DPAPWRSW_HV_DET is HIGH and T29_A_HV_EN is LOW.

3.3V/HV Power MUX

B1100 chosen for high Vf for 2.9V mode.

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 65mOhm @ 2.5V Vgs
Id(max): 3.7A @ 70C

D9425 DFLS1100 POWERDI-123 CRITICAL

Q9425 SI8409DB BGA CRITICAL

3.3V/HV MUXed

3.3V Always

R9427 100K 1% 1/16W MF-LF 402

R9428 21.5K 1% 1/16W MF-LF 402

R9425 4.7K 5% 1/16W MF-LF 402

Blocking FET, off when Source >3.4V or HV_EN high.

R9426 1K 5% 1/16W MF-LF 402

R9430 4.7K 5% 1/16W MF-LF 402

DPAPWRSW_VREF
DPAPWRSW_P3V3_ON_L
DPAPWRSW_HV_DET_R_L

U9426 ZXRE060A SOT353 CRITICAL

R9429 4.7K 5% 1/16W MF-LF 402

C9424 0.47UF 10% 10V X5R 402

DPAPWRSW_ON_L_C

C9426 0.1UF 20% 10V CERM 402

NO STUFF
C9429 0.1UF 20% 10V CERM 402

R9424 22 5% 1/16W MF-LF 402

Q9426 MMDT3946XG SOT363

DPAPWRSW_HV_DET_L

DPAPWRSW_NPN_E

R9418 1K 5% 1/16W MF 402

DPAPWRSW_HV_DET

ZXRE060A REF range: 0.595-0.605V (0.600V nominal)
Circuit threshold range: 3.363-3.439V (3.395V nominal)

Port A 3.3V Power Switch

DP_PWR must be S4 to support wake from T29 devices.

U9480 TPS2051B SOT23 CRITICAL

PP3V3_S5

T29_A_HV_EN

SMC_S4_WAKESRC_EN

C9486 10UF 20% 6.3V X5R 603
C9485 0.1UF 20% 10V CERM 402
C9481 0.1UF 20% 10V CERM 402
C9480 22UF 20% 6.3V X5R-CERM-1 603
C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM

T29_A_BIAS

U9435 ZXRE060A SOT353 CRITICAL

C9435 0.1UF 20% 10V CERM 402

C9436 1UF 10% 10V X5R 402

DPAPWRSW_P3V3_ON

Q9430 SSM6N37FEAPE SOT563

DPAPWRSW_ON

T29_A_HV_EN

R9437 82 5% 1/16W MF-LF 402

R9435 100K 1% 1/16W MF-LF 402

DPAPWR_FB_DIV

R9436 24.9K 1% 1/16W MF-LF 402

R9433 220 5% 1/16W MF-LF 402

R9432 10K 5% 1/16W MF-LF 402

DisplayPort/T29 A Connector

L9400 FERR-120-OHM-3A 0603

PP3V3RHV_SW_DPAPWR_UF
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

PP3V3RHV_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

Circuit threshold range: 2.877-2.941V (2.903V nominal)

C9400 0.01UF 10% 50V X7R 402

C9490 0.1uF 10% 16V X5R 402

T29_A_BIAS_R

R9491 51 5% 1/20W MF 201

T29_A_BIAS
VOLTAGE=3.3V

T29_D2R_C_P<0>
T29_D2R_C_N<0>

R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

T29 Dir DP Dir

R9403 12 5% 1/20W MF 201 GND_DPACONN_8

R9404 12 5% 1/20W MF 201 GND_DPACONN_14

T29DPA_ML_P<3>
T29DPA_ML_N<3>

T29: Unused

T29_A_BIAS_D2RN1
T29_A_BIAS_D2RP1

R9498 2.2K 5% 1/20W MF 201

R9499 2.2K 5% 1/20W MF 201

T29_D2R_C_P<1>
T29_D2R_C_N<1>

D9498 BAR90-02LRH TSLP-2-7
D9499 BAR90-02LRH TSLP-2-7

CRITICAL
GND_VOID=TRUE
SIGNAL_MODEL=T29PIN
(Both L's)

DP_A_EXT_AUXCH_P
DP_A_EXT_AUXCH_N

L9498 650NH-5%-0.430MA-0.052OHM 0603 CRITICAL
L9499 650NH-5%-0.430MA-0.052OHM 0603 CRITICAL
SIGNAL_MODEL=EMPTY

T29DPA_D2R1_AUXCH_P
T29DPA_D2R1_AUXCH_N

R9402 12 5% 1/20W MF 201

T29DPA_HPD_R

DPCONN_20_RC

R9401 12 5% 1/20W MF 201

C9498 30PF 5% 50V CERM 402
C9499 30PF 5% 50V CERM 402
C9402 0.01UF 10% 50V X7R 402
C9401 0.01UF 10% 50V X7R 402

T29DPA_HPD
T29DPA_CONFIG1_RC
T29DPA_CONFIG2_RC

R9452 1M 5% 1/16W MF-LF 402
R9451 1M 5% 1/16W MF-LF 402

C9494 330PF 10% 50V CERM 402
C9495 330PF 10% 50V CERM 402

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

R9441 100K 5% 1/16W MF-LF 402

For J9400 T29 SMT pads (3, 5, 12 & 19):
GND_VOID=TRUE

CRITICAL
J9400 DSPLYPRT-M97-1 F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS
2	HOT_PLUG_DETECT	1 GND
4	CONFIG1	3 ML_LANE0P
6	CONFIG2	5 ML_LANE0N
8	GND	7 GND
10	ML_LANE3P	9 ML_LANE1P
12	ML_LANE3N	11 ML_LANE1N
14	GND	13 GND
16	AUX_CHP	15 ML_LANE2P
18	AUX_CHN	17 ML_LANE2N
20	DP_PWR	19 RETURN
SHIELD PINS		22 21

GND_DPACONN_1
GND_DPACONN_7
GND_DPACONN_13
GND_DPACONN_19

R9405 12 5% 1/20W MF 201
R9406 12 5% 1/20W MF 201
R9407 12 5% 1/20W MF 201
R9408 12 5% 1/20W MF 201

DP Dir T29 Dir

T29DPA_ML_P<0>
T29DPA_ML_N<0>

T29: TX_0

T29DPA_ML_P<1>
T29DPA_ML_N<1>

T29: LSX_R2P/P2R (P/N)

T29DPA_ML_P<2>
T29DPA_ML_N<2>

T29: TX_1

GND_VOID=TRUE (Both C's)

C9470 0.47UF 20% 4V CERM-X5R-1 201
C9471 0.47UF 20% 4V CERM-X5R-1 201
C9472 0.47UF 20% 4V CERM-X5R-1 201
C9473 0.47UF 20% 4V CERM-X5R-1 201

R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201

L9408 FERR-120-OHM-3A 0603

470k R's for ESD protection on AC-coupled signals.

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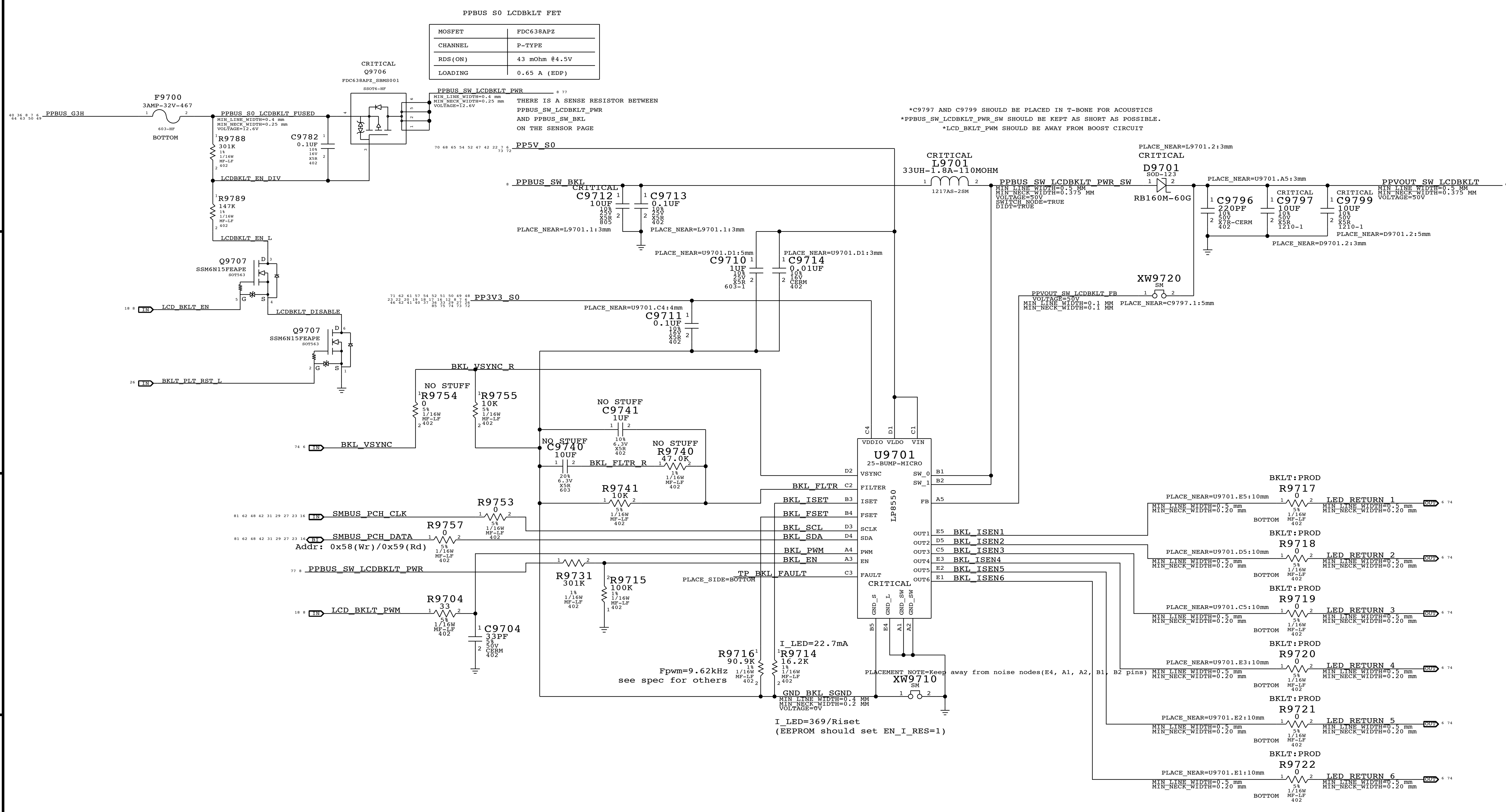

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=VEMURI K90I SYNC DATE=06/25/2010

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LCD Backlight Driver

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	7

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 45
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 30
	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 26
	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_VCCIO_SEL	12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_R_L	CPU_50S	CPU_ITP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 70
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 68
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 68
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
CPU_SVIDALERT_L	CPU_50S	CPU_COMP	CPU_VIDALERT_L	12 68
CPU_SVIDSCLK	CPU_50S	CPU_COMP	CPU_VIDSCLK	12 68
CPU_SVIDSOUT	CPU_50S	CPU_COMP	CPU_VIDSOUT	12 68
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	

CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>

SYNC MASTER=ANNE K90I SYNC DATE=06/08/2010

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CPU Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP,BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL10	N	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL10	N	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3,ISL4,ISL9	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3,ISL4,ISL9	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines
per Huron River SFF DG rev1.0 (#438297).
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQ to DQS matching per byte lane should be within 0.127mm.
DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from procesor ball to SODIMM pad is 88.9mm.
SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	11 27
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	11 27
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	11 28
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	11 28
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	11 28
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	11 28
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	11 27 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	11 27 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	11 27 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	11 28
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	11 28
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	11 28
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	11 28
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	11 28 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	11 28
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	11 28
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	11 28 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	11 28 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	11 28

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_P<3..0>	8
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_N<3..0>	8
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	8 17 75 81
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	8 17 75 81
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_P	18 74
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_N	18 74
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_P<2..0>	6 18 74
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_N<2..0>	6 18 74
	LVDS_90D	LVDS	NC_LVDS_IG_A_DATAP<3>	8 18
	LVDS_90D	LVDS	NC_LVDS_IG_A_DATAN<3>	8 18
T21	LVDS_90D	LVDS	LVDS_IG_B_DATA_P<3..0>	8
T21	LVDS_90D	LVDS	LVDS_IG_B_DATA_N<3..0>	8
T21	LVDS_90D	LVDS	TP_LVDS_IG_B_CLKP	6 8 18
T21	LVDS_90D	LVDS	TP_LVDS_IG_B_CLKN	6 8 18
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	16 42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_N	16 42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA_HDD_R2D_P	6 42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA_HDD_R2D_N	6 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	16 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_N	16 42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA_HDD_D2R_C_P	6 42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA_HDD_D2R_C_N	6 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	16 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_N	16 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P	6 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_N	6 42
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	16 42
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_N	16 42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA_HDD_R2D_RC_P	42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA_HDD_R2D_RC_N	42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA_HDD_D2R_RC_P	42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA_HDD_D2R_RC_N	42
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	18 24
	USB_85D	USB	USB_HUB1_UP_N	18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	18 24
	USB_85D	USB	USB_HUB2_UP_N	18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P	24 43
USB_EXTA	USB_85D	USB	USB_EXTA_N	24 43
USB_EXTB	USB_85D	USB	USB_EXTB_P	24 43
	USB_85D	USB	USB_EXTB_N	24 43
USB_EXTC	USB_85D	USB	USB_EXTC_P	8 24
	USB_85D	USB	USB_EXTC_N	8 24
USB_EXTD	USB_85D	USB	USB_T29A_P	8 24
T21	USB_85D	USB	USB_T29A_N	8 24
	USB_85D	USB	T29_A_RSVD_P	8 75
	USB_85D	USB	T29_A_RSVD_N	8 75
USB_CAMERA	USB_85D	USB	USB_CAMERA_P	18 32
	USB_85D	USB	USB_CAMERA_N	18 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	6 32
	USB_85D	USB	USB_CAMERA_CONN_N	6 32
USB_BT	USB_85D	USB	USB_BT_P	6 24 32
USB_BT	USB_85D	USB	USB_BT_N	6 24 32
USB_TPAD	USB_85D	USB	USB_TPAD_P	24 53
	USB_85D	USB	USB_TPAD_N	24 53
USB_IR	USB_85D	USB	USB_IR_P	24 44
	USB_85D	USB	USB_IR_N	24 44
USB_SDCARD	USB_85D	USB	USB_SDCARD_P	
	USB_85D	USB	USB_SDCARD_N	
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P	
	USB_85D	USB	USB_BRCRYPT_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16 25
	CLK_PCIE_90D	CLK_PCIE	NC_FSB_CLK133M_PCH_P	8
	CLK_PCIE_90D	CLK_PCIE	NC_FSB_CLK133M_PCH_N	8
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16 25
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16 25
LPC_CLK33M	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 26
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

DisplayPort Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?

PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 45 47
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 45 47
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 26 47
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	10 26
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	26 45
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 26 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 23 27 29 31 42 48 62 77
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 23 27 29 31 42 48 62 77
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 48
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 48
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 48
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 57
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 57
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	16 57
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 57
	HDA_50S	HDA	AUD_SDI_R	57
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 57
	HDA_50S	HDA	HDA_SDOUT_R	16
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 47
	SPI_55S	SPI	SPI_CLK	47
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 47
	SPI_55S	SPI	SPI_MOSI	47
SPI_MISO	SPI_55S	SPI	SPI_MISO	16 47
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 47
	SPI_55S	SPI	SPI_CS0_L	47
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	37
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	37
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	16 37
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	16 37
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	16 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	16 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	37
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 32
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 32
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 32
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 32
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	16 32
	PCIE_85D	PCIE	PCIE_AP_D2R_N	16 32
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	16 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	16 39
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	16 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	16 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P	6 32
	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N	6 32
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P	32
	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N	32
	CLK_PCIE_90D	CLK_PCIE	NC_PEG_CLK100MP	8 16
	CLK_PCIE_90D	CLK_PCIE	NC_PEG_CLK100MN	8 16
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 37
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 37
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 32
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 39
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARDP	8 16
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARDN	8 16
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6
VSS	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 81
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 81
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6
VSS	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	8 75
DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	8 75
	DP_85D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	75
	DP_85D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	75
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	8 17 75 80
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	8 17 75 80
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_P	75
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_N	75
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 34
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 34
	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0>	34
	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0>	34
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0>	8 34
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0>	8 34
	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	34
	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	34
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 34
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 34

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 26
SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	16 26
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	16
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	26 37
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29	26 34
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R	34

SYNC MASTER=K91_MLB SYNC DATE=05/15/2010

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	8MIL	?

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	
	ENET_50S	ENET_3X	ENET_RESET_L	33 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	37 38
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	37 38
CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>	33 37
CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_CMD	33 37
CR_CLK	ENET_50S	ENET_CR_DATA	ENET_CR_CLK	33 37
CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>	33
CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_CMD	33
CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK	33
CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK_L	33

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	6 39 41
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN	39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP	6 39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN	6 39 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	39 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	39 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	39 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	39 41

Port 2 Not Used

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29/DP Net Properties

	ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
		NET_TYPE		
F2	T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0> 75
F3	T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0> 75
F4	T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1> 75
F5	T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1> 75
F6		T29DP_80D	T29DP	T29_R2D_C_F_P<1..0> 75
F7		T29DP_80D	T29DP	T29_R2D_C_F_N<1..0> 75
F8	T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_P<0> 75 76
F9	T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_N<0> 75 76
F10	T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_P<1> 75 76
F11	T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_N<1> 75 76
F12		T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P 76
F13		T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N 76
F14		T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0> 75
F15		T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0> 75
F16		T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0> 75
F17		T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0> 75
F18	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2> 75 83
F19	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2> 75 83
F20	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2> 75
F21	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2> 75
F22	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P 75
F23	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N 75
F24		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P 75
F25		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N 75
F26		T29DP_80D	T29DP	T29DPA_ML_P<3..0> 75 76
F27		T29DP_80D	T29DP	T29DPA_ML_N<3..0> 75 76
F28		T29DP_80D	T29DP	T29DPA_ML_C_P<3..0> 75 76
F29		T29DP_80D	T29DP	T29DPA_ML_C_N<3..0> 75 76
F30		T29DP_80D	T29DP	DP_A_EXT_AUXCH_P 75 76
F31		T29DP_80D	T29DP	DP_A_EXT_AUXCH_N 75 76
F32	T29_R2D2	T29DP_80D	T29DP	T29_R2D_P<2>
F33	T29_R2D2	T29DP_80D	T29DP	T29_R2D_N<2>
F34	T29_R2D3	T29DP_80D	T29DP	T29_R2D_P<3>
F35	T29_R2D3	T29DP_80D	T29DP	T29_R2D_N<3>
F36		T29DP_80D	T29DP	T29_R2D_C_F_P<3..2>
F37		T29DP_80D	T29DP	T29_R2D_C_F_N<3..2>
F38	T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_P<2>
F39	T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_N<2>
F40	T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_P<3>
F41	T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_N<3>
F42		T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P
F43		T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N
F44		T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>
F45		T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>
F46		T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>
F47		T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>
F48	DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2> 83
F49	DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2> 83
F50	DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>
F51	DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>
F52	DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P
F53	DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N
F54		T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P
F55		T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N
F56		T29DP_80D	T29DP	T29DPB_ML_P<3..0>
F57		T29DP_80D	T29DP	T29DPB_ML_N<3..0>
F58		T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>
F59		T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>
F60		T29DP_80D	T29DP	DP_B_EXT_AUXCH_P
F61		T29DP_80D	T29DP	DP_B_EXT_AUXCH_N

Only used on dual-port hosts.

T29 IC Net Properties

	ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
		NET_TYPE		
E62		DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0> 8 34
E61		DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0> 8 34
E63	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0> 34
E64	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0> 34
E65		DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P 8 17 34
E66		DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N 8 17 34
E67	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P 34
E68	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N 34
E69		DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0> 8 34
E70		DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0> 8 34
E71	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0> 34
E72	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0> 34
E74		DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P 8 17 34
E73		DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N 8 17 34
E75	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P 34
E76	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N 34
E77		DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>
E78		DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>
E79		DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P
E80		DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N
E81		T29_I2C_55S	T29_I2C	I2C_T29_SCL 34 48 75
E82		T29_I2C_55S	T29_I2C	I2C_T29_SDA 34 48 75
E83	T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK 34
E84	T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI 34
E85	T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO 34
E86	T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L 34
E87		T29DP_80D	T29DP	T29_R2D_C_P<3..0> 8 34 75
E88		T29DP_80D	T29DP	T29_R2D_C_N<3..0> 8 34 75
E89		T29DP_100D	T29DP	T29_D2R_P<3..0> 8 34 75
E90		T29DP_100D	T29DP	T29_D2R_N<3..0> 8 34 75

Only used on hosts supporting T29 video-in

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	6 32 45 48 54 55
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	6 32 45 48 54 55
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	45 48 51
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	45 48 51
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	6 32 45 48 51
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	6 32 45 48 51
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	6 45 48 63 64
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	6 45 48 63 64
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	45 48
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	45 48

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	64
	1TO1_DIFFPAIR		CHGR_CSI_N	64
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	64
	1TO1_DIFFPAIR		CHGR_CSO_N	64

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIE_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K90i Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	38
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	38
	SATA_90D	SATA	SATA_ODD_D2R_UP_P	6 42
	SATA_90D	SATA	SATA_ODD_D2R_UP_N	6 42
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_P	42
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_N	42
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_P	42
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_N	42
E293	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_P	42
E291	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_N	42
E292	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_P	42
E290	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_N	42
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	51
J287 SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 51
J288	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P	34 51
	THERM_1TO1_55S	THERM	T29_THERMD_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29THMSNS_D2_P	51
	THERM_1TO1_55S	THERM	T29THMSNS_D2_N	51
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	49 70
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	49 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	49 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P	49 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	49 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	49
J249 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	65
J250	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	65
J252 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_P	68 69
J251	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_N	68 69
J253 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	
J254	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	
J256 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	
J255	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	
J281 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	
J282	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	
J283 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
J284	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
J285 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	
J286	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_N	
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_P	
J292 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_N	
J293	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_P	
P29	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_N	6 74
P29	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_P	6 74

K90i Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 32
	1TO1_DIFFPAIR		CHGR_CSI_R_P	64
	1TO1_DIFFPAIR		CHGR_CSI_R_N	64
	1TO1_DIFFPAIR		CHGR_CSO_R_P	50 64
	1TO1_DIFFPAIR		CHGR_CSO_R_N	50 64
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	43
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	43
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	43
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	43
	USB_85D	USB	CONN_USB2_BT_P	
	USB_85D	USB	CONN_USB2_BT_N	
	USB_85D	USB	USB_LT2_P	43
	USB_85D	USB	USB_LT2_N	43
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P	
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N	
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_N_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT	6 60 61
E299 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_N	60
E300 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_P	60
E302 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_N	60
E303 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_P	60
E304 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_N	60
E305 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_P	60
E306 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_R	57 60
E307 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_R	57 60
E308 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_N_R	57 60
E309 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_P_R	57 60
E310 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_L	57 60
E311 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_L	57 60
E312 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_P	60
E313 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_N	60
E314 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	60
E315 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	60
E316 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_P	60
E317 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_N	60
	USB_85D	USB	USB_TPAD_R_P	53
	USB_85D	USB	USB_TPAD_R_N	53
	SB_POWER		PP3V3_S5	4 7 8 12 15 30 32 33 34 36 37 40 41 45 46 56 66 72 73 74 76 48 49 50
	SB_POWER		PP3V3_S0	4 7 8 12 16 17 18 19 20 22 23 26 27 29 33 36 37 40 41 52 54
	SB_POWER		PP1V5_S3R80	6 7 10 12 15 30 72 73 57 61 62 71 73 74 77
	GND		GND	

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K90i Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
40_OHM_SE	ISL10	N	0.126 MM	0.126 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	ISL3,ISL4,ISL9	Y	0.126 MM	0.126 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.190 MM	0.1 MM			
37_OHM_SE	ISL10	N	0.145 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	ISL3,ISL4,ISL9	Y	0.145 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.235 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	ISL10	N	0.140MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.1 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.111 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM

NOTE: These are Intel recommended impedances for PEG, unused on K90i.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
48_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

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