1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEMATIC,Folsten_MBP17

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
B		738810	Production Release	6/19/09	6/19/09

06/15/09

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

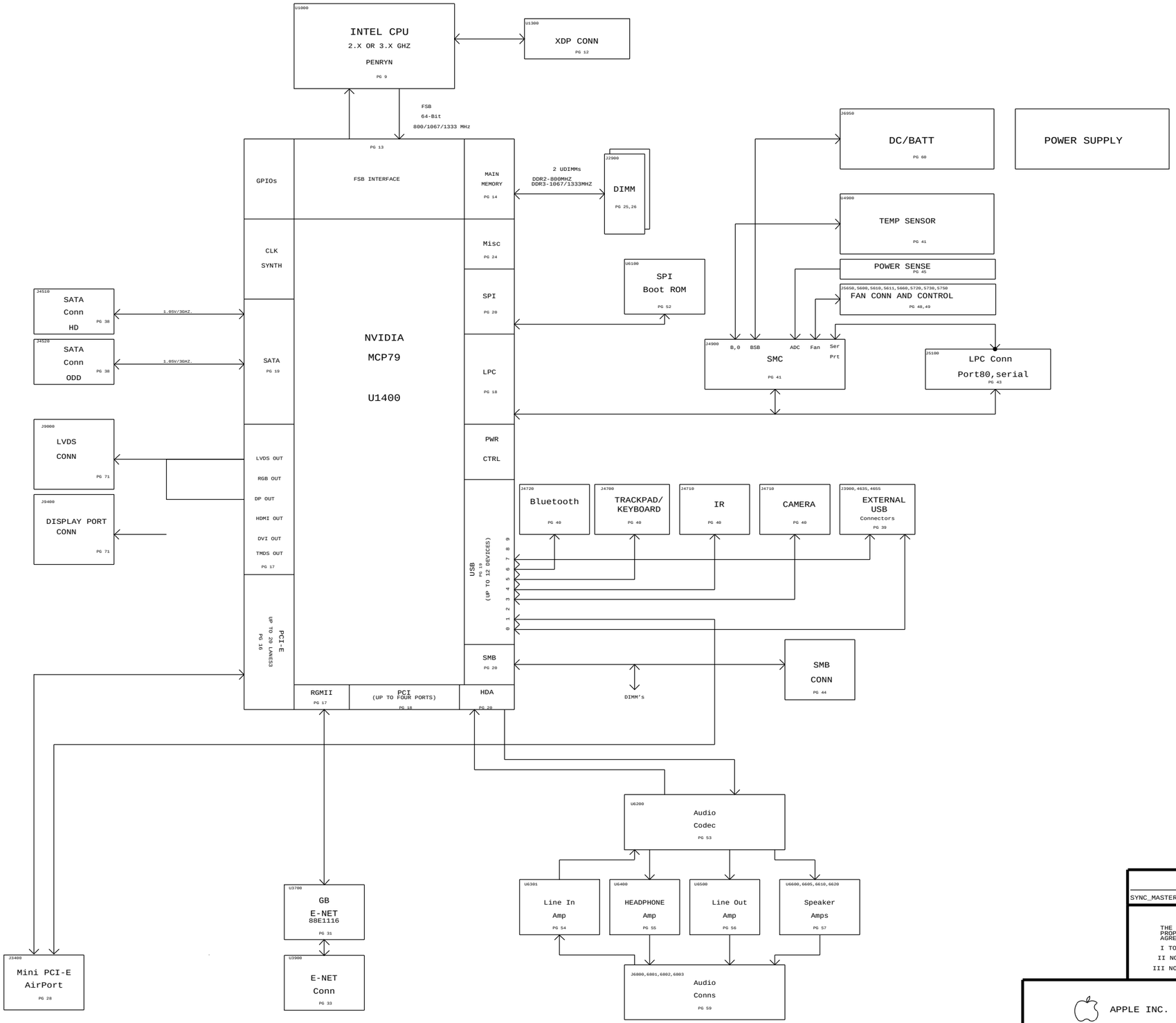
SIZE D

APPLE INC.

TITLE: SCHEM,Folsten,MBP17

DRAWING NUMBER 051-8071 REV. B

SHT 1 OF 98



System Block Diagram

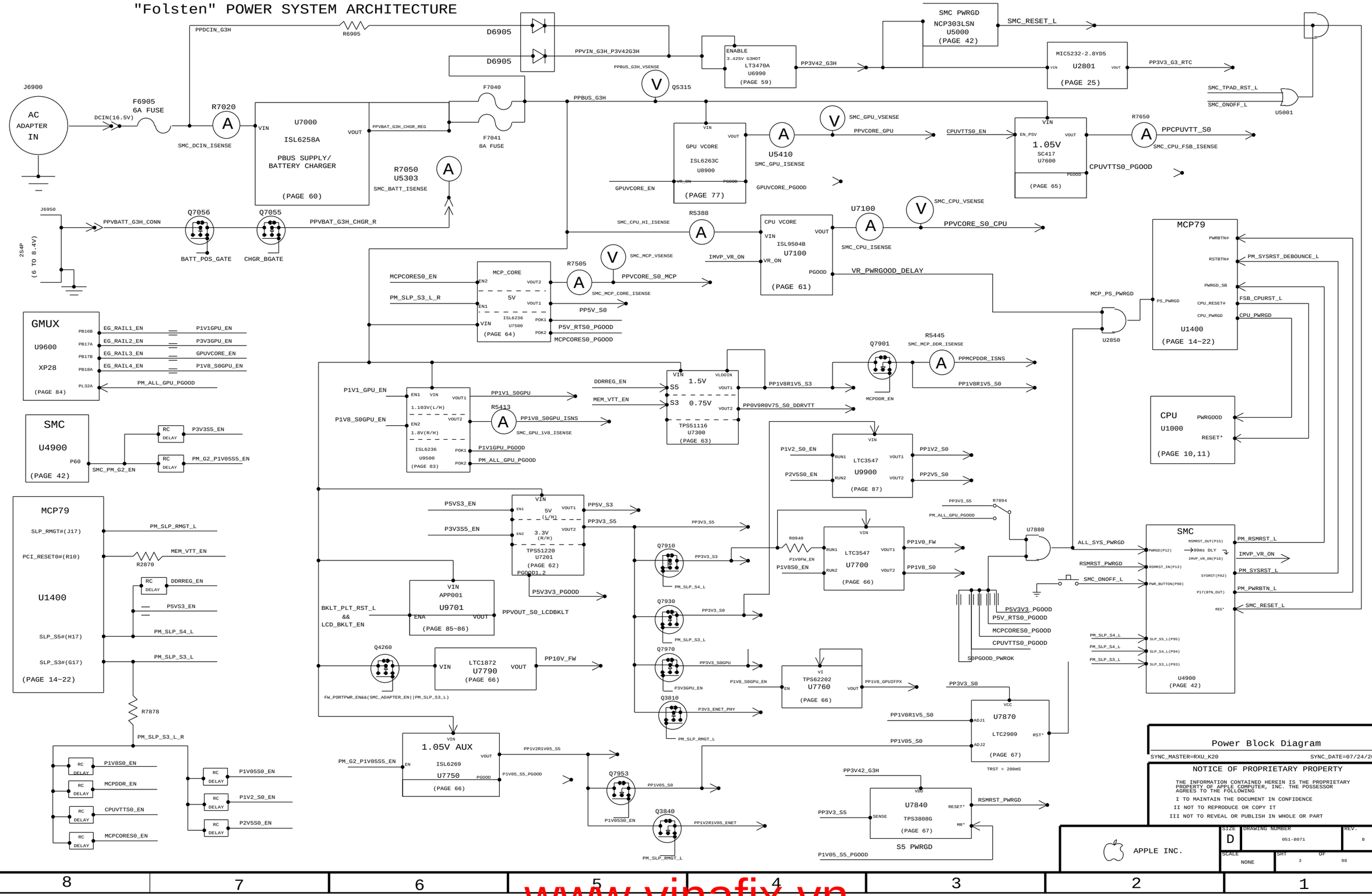
SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 2 OF 98	

"Folsten" POWER SYSTEM ARCHITECTURE



PVT:

03/24/09
csa.5: Project copied from K20 mlb_pvt.
Changed CPU APNs for 2.8 and 3.06GHz CPUs.
Changed BOM and EEE codes for K20A.
csa.45: Connected =PP1V5_EXP_S0 to J4501.13 for SATA redriver on flex.
03/25/09
csa.9: Added PBUS VS 5V voltage selection resistors for keyboard backlight driver.
03/27/09
csa.90: Added 1000pF cap to the backlight power pin for EMI baseline noise.
03/30/09
csa.5: Changed the bom option to KBDLED_5V per radar# 6723272.
03/31/09
csa.1: Changed rev to 1.0.0
04/09/09
csa.70: No stuff C7099 per radar# 6772695.
04/29/09
Production Release Fab to rev A
csa.5: Changed K20A EFI ROM APN 341S2507 (BOM change only)
05/05/09
Added 128S0264 (SANYO) as alternate to 128S0257 (KEMET ELEC) per Radar# 6656624.
06/15/09
Added 107S0136 (DALE/VISHAY) as alternate to 107S0132 (CYNTEC) per Radar# 6971400.
For U7871 P/N 353S2718 is made primary. P/N 353S2310 is added back as alternate.
For U6100 Locked Bootrom P/N 341S2506 replaces existing Unlock Bootrom P/N 341S2507.

Revision History

SYNC_MASTER=NA SYNC_DATE=NA

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT	OF
NONE	4	98

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0172	PCBA,BEST,2.8,512SAM_VRAM,K20A	K20A_COMMON,EEE_9EH,CPU_2_80GHZ,FB_512_SAMSUNG
639-0173	PCBA,BEST,3.06,512SAM_VRAM,K20A	K20A_COMMON,EEE_9EK,CPU_3_06GHZ,FB_512_SAMSUNG
639-0174	PCBA,BEST,2.8,512HYN_VRAM,K20A	K20A_COMMON,EEE_9EL,CPU_2_80GHZ,FB_512_HYNIX
639-0175	PCBA,BEST,3.06,512HYN_VRAM,K20A	K20A_COMMON,EEE_9EM,CPU_3_06GHZ,FB_512_HYNIX

Folsten BOM GROUPS

BOM GROUP	BOM OPTIONS
K20A_COMMON	ALTERNATE,COMMON,K20A_COMMON1,K20A_COMMON2,K20A_DEBUG,K20A_PROGPARTS
K20A_COMMON1	ONEWIRE_PU,ISL6258,MEMRESET_HW,MEMRESET_MCP,MCP_B03,MCP_PROD,MCPSEQ_SMC,BMON_PROD,MCP_CS1_NO,FW_LVG_NEW,PROD_DIGSMS,TPDT_DEBOUNCE,KBDLED_5V
K20A_COMMON2	BOOT_MODE_USER,GPUVID_1P00V,MUXGFX,DPMUX_EN_S0,DP_ESD,EG_PWRSEQ_GMUX,DP_CA_DET_EG_PLD,BKLT_PLL_NOT,GMUX_1V8
K20A_DEBUG	SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K20A_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_1024_SAMSUNG	VRAM8,VRAM_1024_SAMSUNG
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM4,VRAM_512_HYNIX

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung
152S0684	152S0368		ALL	Maglayers alt to Dale/Vishay
104S0023	104S0018		ALL	Cyntec alt to sense resistor
104S0024	104S0017		ALL	Panasonic alt to FW resistor
341S2367	341S2366		ALL	Macronix alt to SST
152S0876	152S0782		ALL	Maglayer alt to Delta
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
514-0612	514-0607		ALL	FOXLINK ALT TO FOXCONN XCVR
514-0613	514-0608		ALL	FOXLINK ALT TO FOXCONN RCVR
152S0684	152S0421		ALL	MAG LAYERS ALT TO VISHAY
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
152S0915	152S0796		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
128S0264	128S0257		ALL	SANYO ALT TO KEMET ELEC.
107S0136	107S0132		ALL	DALE/VISHAY ALT TO CYNTEC.
353S2310	353S2718		ALL	INTERSIL.COMMON TO K24/K19

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9EH]	CRITICAL	EEE_9EH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9EK]	CRITICAL	EEE_9EK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9EL]	CRITICAL	EEE_9EL
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9EM]	CRITICAL	EEE_9EM

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0737	1	IC,ASSP,GPU,NV G96-GS,VLOWLKG,BGA969,LF	U8000	CRITICAL	
338S0694	1	IC,RTL8251CA-VB-GR,GIGE TRANSCEIVER,48P LQFP	U3700	CRITICAL	
338S0654	1	IC,FW643-E,1394B PHY/DHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0710	1	IC,MCP79XT-B3,35X35MM,BGA1437	U1400	CRITICAL	MCP_B03
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2355	1	IC,SMC,DEVELOPMENT,K20	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2506	1	IC,LOCKED EFI ROM,K20A	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
341S2383	1	IC,PSOC +W/USB,56PIN,MLF,M98	U5701	CRITICAL	TPAD_PROG
337S3744	1	IC,PDC,SLGKH,PMQ,3.06,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_3_06GHZ
337S3682	1	IC,PDC,SLGEM,PMQ,2.80,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_80GHZ
333S0481	4	IC,SGRAM,GDDR3,32MX32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0481	8	IC,SGRAM,GDDR3,32MX32,800MHZ,136 FBGA	U8400,U8450,U8500,U8510,U8520,U8530,U8540,U8550	CRITICAL	VRAM_1024_SAMSUNG
333S0506	4	IC,SDRAM,GDDR3,32MX32,900MHZ,TIVA,HF	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX

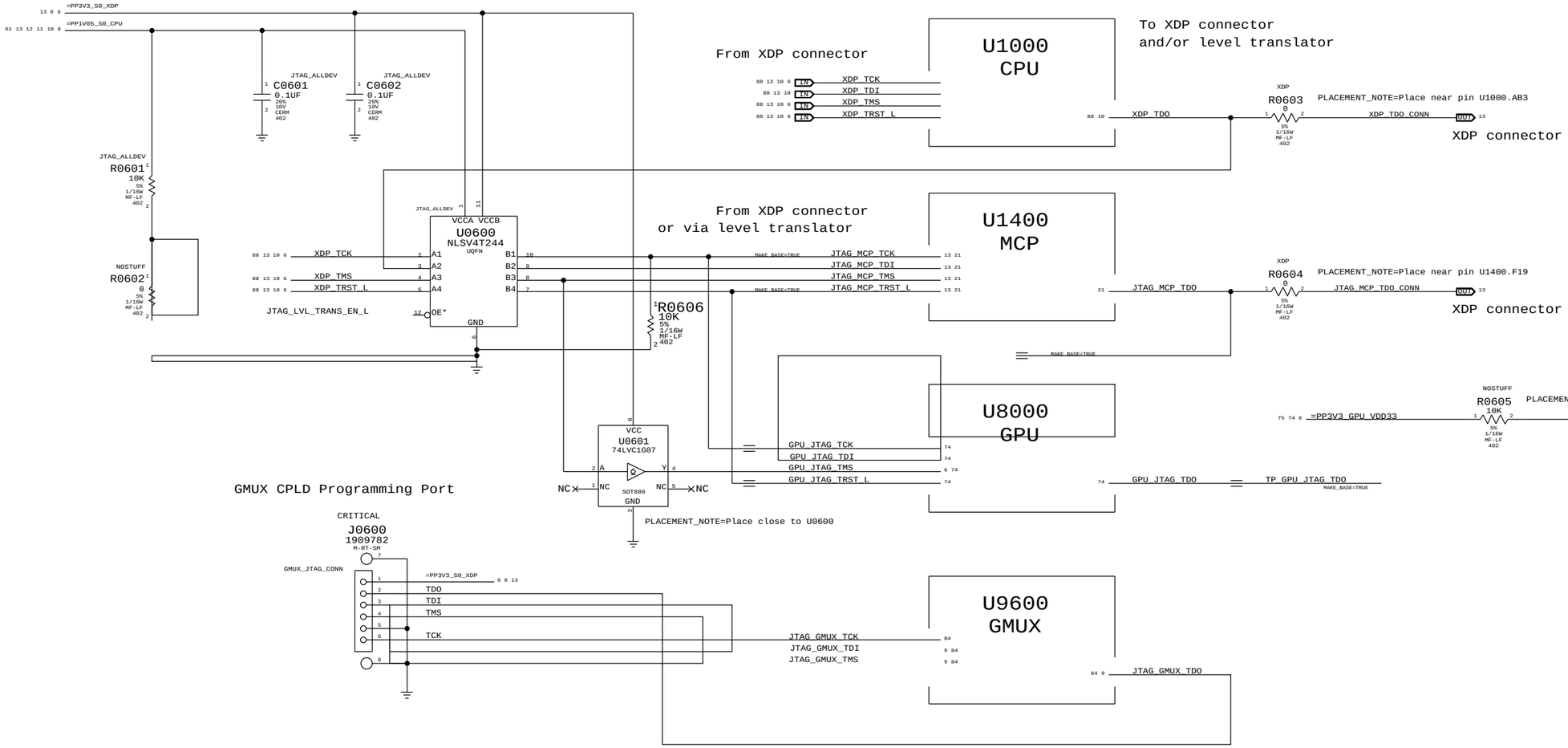
BOM Configuration

SYNC_MASTER=K20A_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 5 OF 98	

1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)



JTAG Scan Chain

SYNC_MASTER=BEN_K20 SYNC_DATE=07/11/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 6 OF 98	

Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	8 48	3 TPs per Fan
TRUE	FAN_LT_PWM	48	
TRUE	FAN_LT_TACH	48	

J5660 (RIGHT FAN CONN)

TRUE	FAN_RT_PWM	48	
TRUE	FAN_RT_TACH	48	5 TPs per Fan
TRUE	GND		

J6780 (MIC CONN)

J557	TRUE	BI_MIC_LO	57 58
J558	TRUE	BI_MIC_SHIELD	57 58
J559	TRUE	BI_MIC_HI	57 58

J6781 (LEFT SPEAKER)

J986	TRUE	SPKRAMP_L1_OUT_P	56 57 96
J987	TRUE	SPKRAMP_L1_OUT_N	56 57 96
J988	TRUE	SPKRAMP_L2_OUT_P	56 57 96
J989	TRUE	SPKRAMP_L2_OUT_N	56 57 96

J6782 (RIGHT & SUB SPEAKER)

J990	TRUE	SPKRAMP_LFE_OUT_P	56 57 96
J991	TRUE	SPKRAMP_LFE_OUT_N	56 57 96
J992	TRUE	SPKRAMP_R1_OUT_P	56 57 96
J993	TRUE	SPKRAMP_R1_OUT_N	56 57 96
J994	TRUE	SPKRAMP_R2_OUT_P	56 57 96
J995	TRUE	SPKRAMP_R2_OUT_N	56 57 96

J9000 (LVDS CONN)

J120	TRUE	BKL_SYNC	78 85
J995	TRUE	PP3V3_SW_LCD	78
J996	TRUE	=PP3V3_S0_DDC_LCD	8 75 78
J997	TRUE	PPVOUT_S0_LCDBKLT	78 85
J998	TRUE	LVDS_DDC_CLK	78 81
J999	TRUE	LVDS_DDC_DATA	78 81
J100	TRUE	LVDS_CONN_A_DATA_P<0>	78 81 95
J100	TRUE	LVDS_CONN_A_DATA_N<0>	78 81 95
J100	TRUE	LVDS_CONN_A_DATA_P<1>	78 81 95
J100	TRUE	LVDS_CONN_A_DATA_N<1>	78 81 95
J100	TRUE	LVDS_CONN_A_DATA_P<2>	78 81 95
J100	TRUE	LVDS_CONN_A_DATA_N<2>	78 81 95
J100	TRUE	LVDS_CONN_A_CLK_F_P	78 95
J100	TRUE	LVDS_CONN_A_CLK_F_N	78 95
J100	TRUE	LVDS_CONN_B_DATA_P<0>	78 81 95
J100	TRUE	LVDS_CONN_B_DATA_N<0>	78 81 95
J101	TRUE	LVDS_CONN_B_DATA_P<1>	78 81 95
J101	TRUE	LVDS_CONN_B_DATA_N<1>	78 81 95
J101	TRUE	LVDS_CONN_B_DATA_P<2>	78 81 95
J101	TRUE	LVDS_CONN_B_DATA_N<2>	78 81 95
J101	TRUE	LVDS_CONN_B_CLK_F_P	78 95
J101	TRUE	LVDS_CONN_B_CLK_F_N	78 95
J101	TRUE	LED_RETURN_1	78 85
J101	TRUE	LED_RETURN_2	78 85
J101	TRUE	LED_RETURN_3	78 85
J101	TRUE	LED_RETURN_4	78 85
J101	TRUE	LED_RETURN_5	78 85
J101	TRUE	LED_RETURN_6	78 85
	TRUE	GND	

2 TP needed

J4500 (SATA ODD CONN)

J102	TRUE	PP5V_SW_ODD	38
J102	TRUE	SMC_ODD_DETECT	38 41
J102	TRUE	SATA_ODD_D2R_C_P	38 90
J102	TRUE	SATA_ODD_D2R_C_N	38 90
J102	TRUE	SATA_ODD_R2D_P	38 90
J102	TRUE	SATA_ODD_R2D_N	38 90
	TRUE	GND	

4 TPs

3 TPs

5 TPs

J4501 (SATA HDD CONN)

J103	TRUE	PP5V_S0_HDD_FLT	38
J103	TRUE	SATA_HDD_R2D_P	38 90
J103	TRUE	SATA_HDD_R2D_N	38 90
J103	TRUE	SATA_HDD_D2R_C_N	38 90
J103	TRUE	SATA_HDD_D2R_C_P	38 90
	TRUE	GND	

J5815 (KBD BACKLIGHT CONN)

J114	TRUE	KBDLED_ANODE	50
J114	TRUE	SMC_KDBLED_PRESENT_L	50
	TRUE	GND	

FUNC_TEST

TRUE GND

TRUE GND

6 TPs

USB PORTS

J105	TRUE	PP5V_S3_RTUSB_A_F	39
J105	TRUE	USB2_LT1_N	39 96
J105	TRUE	USB2_LT1_P	39 96
	TRUE	GND	
J105	TRUE	PP5V_S3_RTUSB_B_F	39
J105	TRUE	USB_LT2_N	39 96
J105	TRUE	USB_LT2_P	39 96
	TRUE	GND	
J105	TRUE	PP5V_S3_RTUSB_C_F	98
J105	TRUE	USB_LT3_N	96 98
J105	TRUE	USB_LT3_P	96 98
	TRUE	GND	

J3401 (AIRPORT/BT/CAMERA CONN)

J105	TRUE	PCIE_MINI_D2R_P	17 30 90
J105	TRUE	PCIE_MINI_D2R_N	17 30 90
J105	TRUE	PCIE_MINI_R2D_P	30 90
J105	TRUE	PCIE_MINI_R2D_N	30 90
J105	TRUE	PCIE_CLK100M_MINI_CONN_P	30 96
J105	TRUE	PCIE_CLK100M_MINI_CONN_N	30 96
J105	TRUE	MINI_CLKREQ_O_L	30
J105	TRUE	PCIE_WAKE_L	7 17 30 31
J105	TRUE	MINI_RESET_CONN_L	30
J106	TRUE	PP5V_WLAN	30
J106	TRUE	PP5V_S3_BTCAMERA_F	30
J106	TRUE	SMBUS_SMC_A_S3_SDA	7 44 94
J106	TRUE	SMBUS_SMC_A_S3_SCL	7 44 94
J106	TRUE	USB_CAMERA_CONN_P	30 96
J106	TRUE	USB_CAMERA_CONN_N	30 96
J106	TRUE	CONN_USB2_BT_P	30 96
J106	TRUE	CONN_USB2_BT_N	30 96

J3500 (EXPRESS CARD CONN)

J106	TRUE	PP1V5_S0_EXCARD_SWITCH	31
J106	TRUE	PCIE_WAKE_L	7 17 30 31
J106	TRUE	SMBUS_MCP_0_CLK	13 21 44 91
J106	TRUE	SMBUS_MCP_0_DATA	13 21 44 91
J107	TRUE	PP3V3_S0_EXCARD_SWITCH	31
J107	TRUE	PP3V3_S3_EXCARD_SWITCH	31
J107	TRUE	USB2_EXCARD_CONN_N	31 96
J107	TRUE	USB2_EXCARD_CONN_P	31 96
J107	TRUE	EXCARD_CPUSB_L	31
J107	TRUE	EXCARD_CLKREQ_CONN_L	31
J107	TRUE	EXCARD_CPPE_L	31
J107	TRUE	PLT_RESET_SWITCH_L	31
J107	TRUE	PCIE_EXCARD_D2R_P	17 31 90
J108	TRUE	PCIE_EXCARD_D2R_N	17 31 90
J108	TRUE	PCIE_EXCARD_R2D_P	31 90
J108	TRUE	PCIE_EXCARD_R2D_N	31 90
J108	TRUE	PCIE_CLK100M_EXCARD_CONN_P	31 96
J108	TRUE	PCIE_CLK100M_EXCARD_CONN_N	31 96

J5800 (IPD FLEX CONN)

J108	TRUE	PP3V3_S3_LDO	50
J108	TRUE	PP18V5_S3	7 50
J108	TRUE	TPAD_GND_F	50
J127	TRUE	Z2_CS_L	49 50
J108	TRUE	Z2_DEBUG3	49 50
J108	TRUE	Z2_MISO	49 50
J109	TRUE	Z2_BOOST_EN	50
J109	TRUE	Z2_BOOT_CFG1	49 50
J109	TRUE	Z2_CLKIN	49 50
J109	TRUE	Z2_KEY_ACT_L	49 50
J109	TRUE	Z2_RESET	49 50
J109	TRUE	PSOC_F_CS_L	49 50
J109	TRUE	PICKB_L	49 50
J109	TRUE	PSOC_MISO	49 50
J109	TRUE	PSOC_MOSI	49 50
J109	TRUE	PSOC_SCLK	49 50
J110	TRUE	SMBUS_SMC_A_S3_SCL	7 44 94
J110	TRUE	SMBUS_SMC_A_S3_SDA	7 44 94

J6900 (DC POWER CONN)

J113	TRUE	ADAPTER_SENSE	59
J113	TRUE	PP18V5_DCIN_FUSE	59
	TRUE	GND	

J6950 (MAIN BATT CONN)

J113	TRUE	PPVBAT_G3H_CONN_F	59
J113	TRUE	SMBUS_SMC_BSA_SCL	7 44 94
J113	TRUE	SMBUS_SMC_BSA_SDA	7 44 94
J113	TRUE	SMC_BS_ALRT_L	41 42 59
	TRUE	GND	

J6995 (BAT LED CONN)

J114	TRUE	PP3V42_G3H	7 8 42
J114	TRUE	SMBUS_SMC_BSA_SDA	7 44 94
J114	TRUE	SMBUS_SMC_BSA_SCL	7 44 94
J114	TRUE	SMC_BIL_BUTTON_DB_L	42 59
	TRUE	GND	

J5713 (KEY BOARD CONN)

J110	TRUE	PP3V3_S3	7 8
J110	TRUE	PP3V42_G3H	7 8 42
J110	TRUE	WS_KBD1	49
J110	TRUE	WS_KBD2	49
J110	TRUE	WS_KBD3	49
J110	TRUE	WS_KBD4	49
J110	TRUE	WS_KBD5	49
J110	TRUE	WS_KBD6	49
J111	TRUE	WS_KBD7	49
J111	TRUE	WS_KBD8	49
J111	TRUE	WS_KBD9	49
J111	TRUE	WS_KBD10	49
J111	TRUE	WS_KBD11	49
J111	TRUE	WS_KBD12	49
J111	TRUE	WS_KBD13	49
J111	TRUE	WS_KBD14	49
J111	TRUE	WS_KBD15_CAP	49
J111	TRUE	WS_KBD16_NUM	49
J111	TRUE	WS_KBD17	49
J112	TRUE	WS_KBD18	49
J112	TRUE	WS_KBD19	49
J112	TRUE	WS_KBD20	49
J112	TRUE	WS_KBD21	49
J112	TRUE	WS_KBD22	49
J112	TRUE	WS_KBD23	49
J112	TRUE	WS_KBD_ONOFF_L	49
J113	TRUE	WS_LEFT_SHIFT_KBD	49
J113	TRUE	WS_LEFT_OPTION_KBD	49
J113	TRUE	WS_CONTROL_KBD	49

J4800 (FRONT CABLE CONN)

J114	TRUE	PP3V42_G3H_LIDSWITCH_R	40
J114	TRUE	PP5V_S3_IR_R	40
J114	TRUE	SMC_LID_R	40
J114	TRUE	IR_RX_OUT	40
J114	TRUE	SYS_LED_ANODE	40 42
	TRUE	GND	

J5502 (SENSOR CONN)

J115	TRUE	MCPTHMSNS_D_P	47 96
J115	TRUE	MCPTHMSNS_D_N	47 96

POWER RAILS

FUNC_TEST

L640	TRUE	PM_SLP_S3_L	21 33 36 41 67 82 84
L602	TRUE	PPBUS_G3H	8 45
L603	TRUE	PPBUS_CPU_IMVP_ISNS	8
L604	TRUE	PP3V42_G3H	7 8 42
L605	TRUE	PP5V_S3	8
L606	TRUE	PP5V_S0	8
L607	TRUE	PPVCORE_S0_CPU	8
L608	TRUE	PPVCORE_S0_MCP	7 8
L609	TRUE	PP3V3_S5	8 96
L610	TRUE	PP3V3_S3	7 8
L611	TRUE	PP3V3_S0	8 9 96
L612	TRUE	PP2V5_S0	8
L613	TRUE	PP1V2_S0	8
L614	TRUE	PP1V8_S0	8
L615	TRUE	PP1V8R1V5_S3	8
L616	TRUE	PP1V8R1V5_S0	8
L617	TRUE	PPMCPDDR_ISNS	7 8
L618	TRUE	PP1V05_S0	8
L619	TRUE	PP1V2R1V05_S5	8
L620	TRUE	PPCPUVTT_S0	8
L621	TRUE	PP0V9R0V75_S0_DDRVTT	8
L622	TRUE	PP1V2R1V05_ENET	8
L623	TRUE	PP3V3_ENET_PHY	8
L624	TRUE	PPVP_FW	8
L625	TRUE	PP1V0_FW	8
L626	TRUE	PP3V3_S0GPU	8
L627	TRUE	PP1V1_S0GPU	8
L628	TRUE	PP1V8_S0GPU_ISNS	8
L629	TRUE	PPVCORE_GPU	8
L630	TRUE	PP1V8_S0GPU_ISNS_R	8
L631	TRUE	PP3V3_S5_AVREF_SMC	41 42
L632	TRUE	PP18V5_S3	7 50
L633	TRUE	PPDCIN_G3H	8
L634	TRUE	PPVCORE_S0_MCP	7 8
L635	TRUE	PPMCPDDR_ISNS	7 8
L636	TRUE	PPVTTDDR_S3	8
L637	TRUE	PP1V8_GPUIFPX	8

FUNC_TEST

U720	TRUE	SYS_LED_ANODE_R	40
U720	TRUE	LPC_CLK33M_LPCPLUS	25 43 91
U720	TRUE	LPC_AD<0..3>	19 41 43 84 91
U720	TRUE	SPI_ALT_MOSI	43
U720	TRUE	SPI_ALT_MISO	43
U720	TRUE	LPC_FRAME_L	19 41 43 84 91
U720	TRUE	PM_CLKRUN_L	19 41 43
U720	TRUE	SMC_TMS	41 42 43
U720	TRUE	DEBUG_RESET_L	25 43
U720	TRUE	SMC_TDO	41 42 43
U720	TRUE	SMC_TRST_L	41 43
U721	TRUE	SMC_MD1	41 43
U721	TRUE	SMC_TX_L	39 41 42 43
U720	TRUE	SPIROM_USE_MLB	43
U720	TRUE	SPI_ALT_CLK	43
U720	TRUE	SPI_ALT_CS_L	43
U720	TRUE	LPC_SERIRQ	19 41 43
U720	TRUE	LPC_PWRDWN_L	19 41 43
U720	TRUE	SMC_TDI	41 42 43
U720	TRUE	SMC_TCK	41 42 43
U720	TRUE	SMC_RESET_L	41 42 43
U721	TRUE	SMC_NMI	41 43
U721	TRUE	SMC_RX_L	39 41 42 43
U720	TRUE	LPCPLUS_GPIO	18 43
U765	TRUE	ISSP_SCLK_P1_1	49
U765	TRUE	ISSP_SDATA_P1_0	49
	TRUE	SMC_ONOFF_L	41 42 49
U720	TRUE	PM_SYSRST_L	25 41
U630	TRUE	BKL_FB	
U630	TRUE	BKL_GD	
U630	TRUE	BKL_SW	
U630	TRUE	BKLT_EN	85
U630	TRUE	BKL_SCL	
U630	TRUE	BKL_SDA	
U630	TRUE	LCD_BKLT_PWM	84 85

ICT Test Points

CPU FSB NO_TESTs

NO_TEST

	TRUE	FSB_A_L<31..3>	10 14 88
	TRUE	FSB_ADS_L	10 14 88
	TRUE	FSB_ADSTB_L<1..0>	10 14 88
	TRUE	FSB_D_L<63..0>	10 14 88
	TRUE	FSB_DBSY_L	10 14 88
	TRUE	FSB_DINV_L<3..0>	10 14 88
	TRUE	FSB_DRDY_L	10 14 88
	TRUE	FSB_DSTB_L_N<3..0>	10 14 88
	TRUE	FSB_DSTB_L_P<3..0>	10 14 88
	TRUE	FSB_HIT_L	10 14 88
	TRUE	FSB_HITM_L	10 14 88
	TRUE	FSB_LOCK_L	10 14 88
	TRUE	FSB_REQ_L<4..0>	10 14 88

FB NO_TESTs

NO_TEST

U680	TRUE	FB_A_DQ<63..0>	71 72 79 95
U681	TRUE	FB_B_DQ<63..0>	71 73 80 95
U682	TRUE	FB_B_BA<1>	71 73 80 95
U683	TRUE	FB_B_CAS_L	71 73 80 95
U684	TRUE	FB_B_CS0_L	71 73 95
U685	TRUE	FB_B_MA<11>	71 73 80 95

LVDS NO_TESTs

NO_TEST

U120	TRUE	LVDS_A_DATA_N<0>	81 84 95
U120	TRUE	LVDS_A_DATA_P<0>	81 84 95
U120	TRUE	LVDS_B_CLK_P	81 84 95
U120	TRUE	LVDS_B_DATA_N<0>	81 84 95
U120	TRUE	LVDS_B_DATA_P<0>	81 84 95
U120	TRUE	LVDS_EG_A_DATA_N<2>	76 84 95

NC NO_TESTs

NO_TEST

19	TP_PCI_AD<31..8>	TRUE	NC_PCI_AD<31..8>	
19	TP_PCI_C_BE_L<3..0>	TRUE	NC_PCI_C_BE_L<3..0>	
19	TP_PCI_CLK0	TRUE	NC_PCI_CLK0	
19	TP_PCI_CLK1	TRUE	NC_PCI_CLK1	
19	TP_PCI_DEVSEL_L	TRUE	NC_PCI_DEVSEL_L	
19	TP_PCI_FRAME_L	TRUE	NC_PCI_FRAME_L	
19	TP_PCI_GNT0_L	TRUE	NC_PCI_GNT0_L	
19	TP_PCI_GNT1_L	TRUE	NC_PCI_GNT1_L	
19	TP_PCI_INTW_L	TRUE	NC_PCI_INTW_L	
19	TP_PCI_INTX_L	TRUE	NC_PCI_INTX_L	
19	TP_PCI_INTY_L	TRUE	NC_PCI_INTY_L	
19	TP_PCI_INTZ_L	TRUE	NC_PCI_INTZ_L	
19	TP_PCI_IRDY_L	TRUE	NC_PCI_IRDY_L	
19	TP_PCI_PAR	TRUE	NC_PCI_PAR	
19	TP_PCI_PERR_L	TRUE	NC_PCI_PERR_L	
19	TP_PCI_RESET1_L	TRUE	NC_PCI_RESET1_L	
19	TP_PCI_SERR_L	TRUE	NC_PCI_SERR_L	
19	TP_PCI_STOP_L	TRUE	NC_PCI_STOP_L	
19	TP_PCI_TRDY_L	TRUE	NC_PCI_TRDY_L	
17	TP_PCIE_CLK100M_PE4P	TRUE	NC_PCIE_CLK100M_PE4P	
17	TP_PCIE_CLK100M_PE5N	TRUE	NC_PCIE_CLK100M_PE5N	
17	TP_PCIE_CLK100M_PE5P	TRUE	NC_PCIE_CLK100M_PE5P	
17	TP_PCIE_CLK100M_PE6N	TRUE	NC_PCIE_CLK100M_PE6N	
17	TP_PCIE_CLK100M_PE6P	TRUE	NC_PCIE_CLK100M_PE6P	
17	TP_PCIE_PE4_D2RN	TRUE	NC_PCIE_PE4_D2RN	
17	TP_PCIE_PE4_D2RP	TRUE	NC_PCIE_PE4_D2RP	
17	TP_PE4_CLKREQ_L	TRUE	NC_PE4_CLKREQ_L	
69	TP_PEX_CLKREQ_L	TRUE	NC_PEX_CLKREQ_L	
49	TP_PSOC_P1_3	TRUE	NC_PSOC_P1_3	
20	TP_SATA_C_D2RN	TRUE	NC_SATA_C_D2RN	
20	TP_SATA_C_D2RP	TRUE	NC_SATA_C_D2RP	
20	TP_SATA_C_R2D_CN	TRUE	NC_SATA_C_R2D_CN	
20	TP_SATA_C_R2D_CP	TRUE	NC_SATA_C_R2D_CP	
20	TP_SATA_D_D2RN	TRUE	NC_SATA_D_D2RN	
20	TP_SATA_D_D2RP	TRUE	NC_SATA_D_D2RP	
20	TP_SATA_D_R2D_CN	TRUE	NC_SATA_D_R2D_CN	
20	TP_SATA_D_R2D_CP	TRUE	NC_SATA_D_R2D_CP	
20	TP_SATA_E_D2RN	TRUE	NC_SATA_E_D2RN	
20	TP_SATA_E_D2RP	TRUE	NC_SATA_E_D2RP	
20	TP_SATA_E_R2D_CN	TRUE	NC_SATA_E_R2D_CN	
20	TP_SATA_E_R2D_CP	TRUE	NC_SATA_E_R2D_CP	
20	TP_SATA_F_D2RN	TRUE	NC_SATA_F_D2RN	
20	TP_SATA_F_D2RP	TRUE	NC_SATA_F_D2RP	
20	TP_SATA_F_R2D_CN	TRUE	NC_SATA_F_R2D_CN	
20	TP_SATA_F_R2D_CP	TRUE	NC_SATA_F_R2D_CP	
21	TP_SB_A20GATE	TRUE	NC_SB_A20GATE	
42	TP_SMC_P41	TRUE	NC_SMC_P41	
20	TP_USB_10P	TRUE	NC_USB_10P	
20	TP_USB_11N	TRUE	NC_USB_11N	
20	TP_USB_11P	TRUE	NC_USB_11P	
9	TP_USB_EXTDN	TRUE	NC_USB_EXTDN	
9	TP_USB_EXTDP	TRUE	NC_USB_EXTDP	
9	TP_USB_MININ	TRUE	NC_USB_MININ	
9	TP_USB_MINIP	TRUE	NC_USB_MINIP	
13	TP_XDP_OBSDATA_B2	TRUE	NC_XDP_OBSDATA_B2	
13	TP_XDP_OBSDATA_B3	TRUE	NC_XDP_OBSDATA_B3	

NC NO_TESTs

NO_TEST

U720	NC_SMC_FAN_3_TACH	42		
U761	NC_SMC_FAN_3_CTL	42		
U762	NC_SMC_FAN_2_TACH	42		
U763	NC_SMC_FAN_2_CTL	42		
U764	NC_FW2_TPBP	37		
U765	NC_FW2_TPBN	37		
U767	NC_FW2_TPBIAS	37		
U766	NC_FW2_TPAP	37		
U768	NC_FW2_TPAN	37		
U688	NC_FW0_TPBP	37		
U770	NC_FW0_TPBN	37		
U772	NC_FW0_TPAP	37		
U771	NC_ESTARLDO_EN	42		
U774	NC_ALS_GAIN	42		

NC NO_TESTs

NO_TEST

9	TP_CPU_PECI_MCP	TRUE	NC_CPU_PECI_MCP	
10	TP_CPU_TEST3	TRUE	NC_CPU_TEST3	
18	TP_ENET_INTR_L	TRUE	NC_ENET_INTR_L	
18	TP_ENET_PWRDWN_L	TRUE	NC_ENET_PWRDWN_L	
35	TP_FW643_AVREG	TRUE	NC_FW643_AVREG	
35	TP_FW643_TDI	TRUE	NC_FW643_TDI	
9	TP_MEM_A_A<15>	TRUE	NC_MEM_A_A<15>	
16	TP_MEM_A_CKE<2>	TRUE	NC_MEM_A_CKE<2>	
16	TP_MEM_A_CKE<3>	TRUE	NC_MEM_A_CKE<3>	
15	TP_MEM_A_CLK2N	TRUE	NC_MEM_A_CLK2N	
15	TP_MEM_A_CLK2P	TRUE	NC_MEM_A_CLK2P	
16	TP_MEM_A_CLK3N	TRUE	NC_MEM_A_CLK3N	
16	TP_MEM_A_CLK3P	TRUE	NC_MEM_A_CLK3P	
16	TP_MEM_A_CLK4N	TRUE	NC_MEM_A_CLK4N	
16	TP_MEM_A_CLK4P	TRUE	NC_MEM_A_CLK4P	
16	TP_MEM_A_CLK5N	TRUE	NC_MEM_A_CLK5N	
16	TP_MEM_A_CLK5P	TRUE	NC_MEM_A_CLK5P	
16	TP_MEM_A_CS_L<2>	TRUE	NC_MEM_A_CS_L<2>	
16	TP_MEM_A_CS_L<3>	TRUE	NC_MEM_A_CS_L<3>	
16	TP_MEM_A_ODT<2>	TRUE	NC_MEM_A_ODT<2>	
16	TP_MEM_A_ODT<3>	TRUE	NC_MEM_A_ODT<3>	
9	TP_MEM_B_A<15>	TRUE	NC_MEM_B_A<15>	
16	TP_MEM_B_CKE<2>	TRUE	NC_MEM_B_CKE<2>	
15	TP_MEM_B_CLK2P	TRUE	NC_MEM_B_CLK2P	
16	TP_MEM_B_CLK3N	TRUE	NC_MEM_B_CLK3N	
16	TP_MEM_B_CLK3P	TRUE	NC_MEM_B_CLK3P	
16	TP_MEM_B_CLK4N	TRUE	NC_MEM_B_CLK4N	
16	TP_MEM_B_CLK4P	TRUE	NC_MEM_B_CLK4P	
16	TP_MEM_B_CLK5N	TRUE	NC_MEM_B_CLK5N	
16	TP_MEM_B_CLK5P	TRUE	NC_MEM_B_CLK5P	
16	TP_MEM_B_CS_L<2>	TRUE	NC_MEM_B_CS_L<2>	
16	TP_MEM_B_CS_L<3>	TRUE	NC_MEM_B_CS_L<3>	
16	TP_MEM_B_ODT<2>	TRUE	NC_MEM_B_ODT<2>	
16	TP_MEM_B_ODT<3>	TRUE	NC_MEM_B_ODT<3>	
21	TP_MLB_RAM_SIZE	TRUE	NC_MLB_RAM_SIZE	
21	TP_MLB_RAM_VENDOR	TRUE	NC_MLB_RAM_VENDOR	
74	TP_GPU_BUFRST_L	TRUE	NC_GPU_BUFRST_L	
75	TP_GPU_GSTATE<0>	TRUE	NC_GPU_GSTATE<0>	
75	TP_GPU_GSTATE<1>	TRUE	NC_GPU_GSTATE<1>	
75	TP_GPU_MIOA_D<9..0>	TRUE	NC_GPU_MIOA_D<9..0>	
75	TP_GPU_MIOA_DE	TRUE	NC_GPU_MIOA_DE	
74	TP_GPU_PGOOD_OUT_L	TRUE	NC_GPU_PGOOD_OUT_L	
75	TP_GPU_VCORE_VID3	TRUE	NC_GPU_VCORE_VID3	
19	TP_LPC_DRQ0_L	TRUE	NC_LPC_DRQ0_L	
75	TP_LVDS_EG_B_CLK_N	TRUE	NC_LVDS_EG_B_CLK_N	
75	TP_LVDS_EG_B_CLK_P	TRUE	NC_LVDS_EG_B_CLK_P	
75	TP_LVDS_EG_BKL_PWM	TRUE	NC_LVDS_EG_BKL_PWM	
9	TP_LVDS_IG_B_CLKN	TRUE	NC_LVDS_IG_B_CLKN	
9	TP_LVDS_IG_B_CLKP	TRUE	NC_LVDS_IG_B_CLKP	
9	TP_LVDS_IG_BKL_PWM	TRUE	NC_LVDS_IG_BKL_PWM	
21	TP_MCP_BUF_SIO_CLK	TRUE	NC_MCP_BUF_SIO_CLK	
17	TP_MCP_GPIO_18	TRUE	NC_MCP_GPIO_18	
21	TP_MCP_KBDRSTIN_L	TRUE	NC_MCP_KBDRSTIN_L	
20	TP_MCP_SATALED_L	TRUE	NC_MCP_SATALED_L	

Functional / ICT Test

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 7 OF 98	

"G3Hot" (Always-Present) Rails

60 =PPBUS_G3H

PPBUS_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=6V
MAKE_BASE=TRUE

- =PPVIN_S5_P5VP3V3 — 62
- =PPVIN_S0_CPUVTTS0 — 65
- =PPBUS_S0_LCDBKLT — 86
- =PPVIN_GPU_GPUVCORE — 77
- =PPVIN_S5_CPU_IMVP_ISNS_R — 45
- =PPVIN_S0_P5VRTS0_MCPCORE — 64
- =PPVIN_S3_DDRREG — 63
- =PPVIN_S0GPU_P1V8P1V1 — 83
- =PPVBAT_G3H_P3V42G3H — 59
- =PPVIN_S0_P1V05S5 — 66
- =PPVIN_PBUS_KBDLED — 9
- =PPVIN_S5_FWPWRSW — 36
- =PPVIN_S5_BKL

45 =PPVIN_S5_CPU_IMVP_ISNS

PPBUS_CPU_IMVP_ISNS — 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=6V
MAKE_BASE=TRUE

- =PPVIN_S5_CPU_IMVP — 61

59 =PP18V5_DCIN_CONN

PPDCIN_G3H — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

- =PPDCIN_S5_CHGR — 60

59 =PP3V42_G3H_REG

PP3V42_G3H — 7 42
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE

- =PP3V42_G3H_SMCUSBMUX — 39
- =PP3V42_G3H_SMBUS_SMC_BSA — 44
- =PP3V42_G3H_LIDSWITCH — 40
- =PP3V3_S5_SMC — 41 42 51
- =PP3V3_S5_LPCPLUS — 43
- =PPVIN_S5_SMCVREF — 42
- =PP3V42_G3H_PWRCTL — 67
- =PP3V42_G3H_CHGR — 60
- =PP3V3_S5_RTC_D — 25
- =PP3V42_G3H_BATT — 59
- =PP3V42_G3H_TPAD — 49
- =PP3V42_G3H_BMON_ISNS — 45
- =PP3V42_G3H_CPUCOREISNS — 45

5V Rails

62 =PP5V_S3_REG

PP5V_S3 — 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE

- =PP5V_S3_SYSLED — 42
- =PP5V_S3_BTCAMERA — 30
- =PP5V_S3_WLAN — 30
- =PP5V_S3_IR — 40
- =PP5V_S3_DDRREG — 63
- =PP5V_S3_GPUVCORE — 77
- =PP5V_S3_RTUSB — 39 98
- =PP5V_S3_TPAD — 50
- =PP5V_S3_P1V05S0FET — 68
- =PP5V_S3_MCPDDRFET — 68
- =PP5V_S3_VTTCLAMP — 68
- =PP5V_S3_AUDIO_PWR — 9

64 =PP5V_S0_REG

PP5V_S0 — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
MAKE_BASE=TRUE

- =PP5V_S0_FAN_LT — 7 48
- =PP5V_S0_FAN_RT — 48
- =PP5V_S0_CPU_IMVP — 61
- =PP5V_S0_CPUVTTS0 — 65
- =PP5V_S0GPU_P1V1P1V8_GPU — 83
- =PP5V_S0_LPCPLUS — 43
- =PP5V_S0_ODD — 38
- =PP5V_S0_HDD — 38
- =PPVIN_PP5V_KBDLED — 9

Chipset "VCore" Rails

61 =PPVCORE_S0_CPU_REG

PPVCORE_S0_CPU — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE

- =PPVCORE_S0_CPU — 11 12 45

64 =PPMCPCORE_S0_REG

PPVCORE_S0_MCP — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

- =PPVCORE_S0_MCP — 22 23 45

3.3V-2.5V Rails

62 =PP3V3_S5_REG

PP3V3_S5 — 7 96
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_S5_ROM — 43 52
- =PP3V3_S5_MEMRESET — 29
- =PP3V3_S3_P3V3S3FET — 68
- =PP3V3_S0_LCD — 78
- =PP3V3_S0_P3V3S0FET — 68
- =PP3V3_GPU_P3V3GPUFET — 68
- =PP3V3_S5_PWRCTL — 67
- =PP3V3_S5_P1V05FET — 68
- =PP3V3_S5_MCP — 22 23
- =PP3V3_S5_MCP_GPIO — 18 20
- =PP3V3_FW_LATEVG_ACTIVE — 36
- =PP3V3_S5_MCPPWRGD — 25
- =PP3V3_FW_LATEVG — 37
- =PP3V3_S5_P1V05ENETFET — 33
- =PP3V3_S5_P3V3ENETFET — 33
- =PP3V3_S5_DP_PORT_PWR — 82

68 =PP3V3_S3_FET

PP3V3_S3 — 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_S3_GMUX — 84
- =PP3V3_S3_BT — 30
- =PP3V3_S3_P1V8S0 — 66
- =PP3V3_S3_SMBUS_SMC_A_S3 — 44
- =PP3V3_S3_SMS — 8 51
- =PP3V3_S3_TPAD — 49
- =PP3V3_S3_SMS — 8 51
- =PP3V3_S3_WLAN — 30
- =PP3V3_S3_MCP_GPIO — 21
- =PP3V3_S3_VREFMRGN — 26
- =PP3V3_S3_SMBUS_SMC_MGMT — 44
- =PP3V3_S3_EXCARD — 31
- =PP3V3_S3_P1V5EXPS0 — 66

68 =PP3V3_S0_FET

PP3V3_S0 — 7 9 96
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_S0_LPCPLUS — 43
- =PP3V3_S0_SMC — 42
- =PP3V3_S0_SMBUS_SMC_B_S0 — 44
- =PP3V3_S0_MCPDDRISNS — 46
- =PP3V3_S0_GPU1V8ISNS — 46
- =PP3V3_S0_CPUTHMSNS — 47
- =PP3V3_S0_GPUTHMSNS — 47
- =PP3V3_S0_FAN_LT — 48
- =PP3V3_S0_FAN_RT — 48
- =PP3V3_S0_IMVP — 61
- =PP3V3_S0_PWRCTL — 67
- =PP3V3_S0_DDC_LCD — 7 75 78
- =PP3V3_S0_XDP — 6 8 13
- =PP3V3_S0_MCPCOREISNS — 46
- =PP3V3_S0_XDP — 6 8 13
- =PPSPD_S0_MEM_A — 27
- =PPSPD_S0_MEM_B — 28
- =PP3V3_S0_SMBUS_MCP_0 — 44
- =PP3V3_S0_GMUX — 84
- =PP3V3_S0_DPMUX — 81
- =PP3V3_S0_DPCONN — 82
- =PP3V3_S0_P1V2P2V5 — 87
- =PP3V3_S0_MCP_GPIO — 18 19 21
- =PP3V3_S0_HDCPROM — 24
- =PP3V3R1V5_S0_MCP_HDA — 21 23
- =PP3V3_S0_MCP_PLL_UF — 23
- =PP3V3_S0_MCP_VPLL_UF — 24
- =PP3V3_S0_MCP_DAC_UF — 24
- =PP3V3_S0_MCP — 21 22 23
- =PP3V3_S0_AUDIO — 53 57 58
- =PP3V3_S0_ODD — 38
- =PP3V3_S0_VMON — 67
- =PP3V3_S0_SMBUS_MCP_1 — 44
- =PP3V3_S0_REMTHMSNS — 47
- =PP3V3_S0_EXCARD — 31
- =PP3V3_S0_LVDSDDCMUX — 81
- =PP3V3_S0_BATTCHARGERTMPSNSR — 47
- =PP3V3_GPU_SMBUS_SMC_0_S0 — 44
- =PP3V3_S0_TPAD — 50
- =PP3V3_S0_MCP_PLL_VLDO — 66
- =PP3V3_FW_FWPHY — 35 37
- =PP3V3_FW_P1V0FW — 66

87 =PP2V5_S0_REG

PP2V5_S0 — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=2.5V
MAKE_BASE=TRUE

- =PP2V5_S0_GMUX — 84

87 =PP1V2_S0_REG

PP1V2_S0 — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

- =PP1V2_S0_GMUX — 84

1.8V/DDR 1.5V Rails

66 =PP1V8_S0_REG

PP1V8_S0 — 7
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

500 mA max supply

- 190 mA =PP3V3R1V8_S0_MCP_IFP_VDD — 18 24
- =PP1V8_S0_MCP_PLL_VLDO — 66

63 =PPDDR_S3_REG

PP1V8R1V5_S3 — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

- =PP1V8R1V5_S0_MCP_FET — 68
- =PPVIN_S0_DDRREG_LDO — 63
- =PP1V5_S3_MEM_A — 27
- =PP1V5_S3_MEM_B — 28
- =PP1V5_S3_MEMRESET — 29

68 =PP1V8R1V5_S0_FET

PP1V8R1V5_S0 — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

- 4771 mA =PPMCPDDR_ISNS_R — 46
- 130 mA =PP1V5_S0_CPU — 11 12
- 500 mA =PP1V5_S0_VMON — 67

66 38 =PP1V5_EXP_S0

PP1V5_EXP_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

- =PP1V5_S0_EXCARD — 31

23 16 =PP1V8R1V5_S0_MCP_MEM

PPMCPDDR_ISNS — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

- =PP1V5_S0_MEM_A — 27
- =PP1V5_S0_MEM_B — 28
- =PPMCPDDR_ISNS — 46

68 66 =PP1V05_S0_FET

PP1V05_S0 — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

1034 mA

- =PP1V05_S0_MCP_AVDD_UF — 23
- =PP1V05_S0_MCP_PEX_DVDD — 8 23
- =PP1V05_S0_MCP_SATA_DVDD — 8 23
- =PP1V05_S0_MCP_HDMI_VDD — 18 24
- =PP1V05_S0_VMON — 67
- =PP1V05_S0_MCP_PLL_PEX_UF — 23

PP1V05_S0_MCP_PLL_UF (MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V) — =PP1V05_S0_MCP_PLL_UF — 23 66

23 8 =PP1V05_S0_MCP_PEX_DVDD — =PP1V05_S0_MCP_PEX_DVDD0 — 17; =PP1V05_S0_MCP_PEX_DVDD1 — 17

23 PP1V05_S0_MCP_PEX_AVDD (MAKE_BASE=TRUE) — =PP1V05_S0_MCP_PEX_AVDD0 — 17; =PP1V05_S0_MCP_PEX_AVDD1 — 17

23 8 =PP1V05_S0_MCP_SATA_DVDD — =PP1V05_S0_MCP_SATA_DVDD0 — 20

23 PP1V05_S0_MCP_SATA_AVDD (MAKE_BASE=TRUE) — =PP1V05_S0_MCP_SATA_AVDD0 — 20

66 =PP1V05_S5_MCP

PP1V2R1V05_S5 — 7 (1.1V for A01)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

241 mA max load

- 105 mA/241 mA =PP1V05_S5_MCP_VDD_AUXC — 22 23
- 139 mA/ 0 mA =PP1V05_S0_ENET_P1V05ENETFET — 33
- =PP1V05_S5_P1V05S0FET — 68

65 =PPCPUVTT_S0_REG

PPCPUVTT_S0 — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

5300 mA

- 4500 mA =PP1V05_S0_CPU — 6 10 11 12 13 61
- =PP1V05_S0_SMC_LS — 42
- 1182 mA =PP1V05_S0_MCP_FSB — 9 14 22 23

63 26 =PPVTT_S3_DDR_BUF

PPVTTDDR_S3 — 7
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

63 =PPVTT_S0_DDR_LDO

PP0V9R0V75_S0_DDRVTT — 7
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

- =PP0V75_S0_MEM_VTT_A — 27
- =PP0V75_S0_MEM_VTT_B — 28
- =PPVTT_S0_VTTCLAMP — 68

OR 0.75V

ENET Rails

33 =PP1V05_ENET_FET

PP1V2R1V05_ENET — 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

- =PP1V05_ENET_MCP_PLL_MAC — 23
- =PP1V05_ENET_MCP_RMGT — 18 23
- =PP1V05_ENET_PHY — 32

33 =PP3V3_ENET_FET

PP3V3_ENET_PHY — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_ENET_MCP_RMGT — 18 23
- =PP3V3_ENET_PHY — 32

"FW" (FireWire) Rails

36 =PPVOUT_FW_FWPWRSW

PPBUS_FW_FWBOOST
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=6V
MAKE_BASE=TRUE

- =PPVIN_PFWBOOST — 66

66 =PFWBOOST_REG

PP10V_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=10V
MAKE_BASE=TRUE

- =PPBOOST_FW_FWPWRSW_F — 36

36 =PPBOOST_S5_FW_FET

PPVP_FW — 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=10V
MAKE_BASE=TRUE

- =PPVP_FW_PORT1 — 37
- =PPVP_FW_PHY_CPS_FET — 37

66 =PP1V0_FW_REG

PP1V0_FW — 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
MAKE_BASE=TRUE

- =PP1V0_FW_FWPHY — 35

"GPU" Rails

68 =PP3V3_S0GPU_FET

PP3V3_S0GPU — 7
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_GPU_VDD33 — 6 74 75
- =PP3V3_GPU_MIO — 74 75
- =PP3V3_GPU_LVDS_DDC — 81
- =PP3V3_GPU_PWRCTL — 67
- =PP3V3_GPU_VCORELOGIC — 77
- =PP3V3_GPU_P1V8S0 — 66

83 =PP1V1_S0GPU_REG

PP1V1_S0GPU — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.1V
MAKE_BASE=TRUE

- =PP1V1_GPU_PEX_IOVDDQ — 69
- =PP1V1_GPU_PEX_IOVDD — 69
- =PP1V1_GPU_PEX_PLLXVDD — 69
- =PP1V1_GPU_PLLVDD — 74
- =PP1V1_GPU_H_PLLVDD — 74
- =PP1V1_GPU_VID_PLLVDD — 74
- =PP1V1_GPU_FBPLLAVDD — 71
- =PP1V1_GPU_IFPCD_IOVDD — 76

66 =PP1V8_GPUIFPX_REG

PP1V8_GPUIFPX — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

- =PP1V8_GPU_IFPX — 76

46 =PP1V8_S0GPU_ISNS

PP1V8_S0GPU_ISNS — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

- =PP1V8_GPU_FB_VDD — 72 73 79 80
- =PP1V8_GPU_FB_VDDQ — 9 72 73 79 80
- =PP1V8_GPU_FBVDDQ — 70
- =PP1V8_GPU_FBIO — 71

77 45 =PPVCORE_GPU_REG

PPVCORE_GPU — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

- =PPVCORE_GPU — 70

83 =PP1V8_GPU_REG

PP1V8_S0GPU_ISNS_R — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE

- =PP1V8_S0GPU_ISNS_R — 46

Power Aliases

SYNC_MASTER=RXU_K20 SYNC_DATE=05/07/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 8 OF 98	

Thermal Module Holes

ZT0982 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0983 STDOFF-4.50D.98H-1.1-3.48-TH
Left CPU TM Hole
Right CPU TM Hole
ZT0984 STDOFF-4.50D.98H-1.1-3.48-TH
Top GPU Right TM Hole
ZT0980 STDOFF-4.50D.98H-1.1-3.48-TH
Bottom Left GPU TM Hole
ZT0981 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0985 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0986 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0930 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0987 STDOFF-4.50D.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 — GND_BATT_CHGND
ZT0945 3R2P5 — GND_CHASSIS_USB
ZT0932 3R2P5 — GND_CHASSIS_RIGHTHS
ZT0960 3R2P5 — GND_CHASSIS_SATA
ZT0971 3R2P5 — GND_CHASSIS_TPAD
ZT0965 3R2P5 — GND_CHASSIS_CLUTCH
ZT0940 3R2P5 — GND_CHASSIS_LVDS
ZT0970 3R2P5 — GND_CHASSIS_DIMM

Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa

=PP1V05_S0_MCP_FSB
R0950 220 5% 1/16W MF-LF 402 — NO STUFF
R0960 62 5% 1/16W MF-LF 402 — NO STUFF
R0970 200 5% 1/16W MF-LF 402 — NO STUFF
R0980 150 1% 1/16W MF-LF 402 — NO STUFF
R0990 150 1% 1/16W MF-LF 402
CPU_DPRSTP_L
FSB_BREQ0_L
FSB_CPURST_L
CPU_INTR
CPU_NMI

Bosses for Flex Protector Bracket

ZT0931 STDOFF-4.0OD3.0H-SM
ZT0934 STDOFF-4.0OD3.0H-SM
ZT0957 4.0OD1.65H-M1.6X0.35
ZT0958 4.0OD1.65H-M1.6X0.35
ZT0988 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0989 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0991 STDOFF-4.50D.98H-1.1-3.48-TH

R0900 10 1% 1/16W MF-LF 402 — GPU_FB_A_VREF_DIV — =PP1V8_GPU_FB_VREF_A
R0901 10 1% 1/16W MF-LF 402 — GPU_FB_B_VREF_DIV — =PP1V8_GPU_FB_VREF_B
=PP1V8_GPU_FB_VDDQ

KBDLED_PBUS
R0998 0 5% 1/10W MF-LF 603 — =PPVIN_PBUS_KBDLED — PP5VR8V4_KBDLED — =PPVIN_S0_KBDLED
KBDLED_5V
R0999 0 5% 1/10W MF-LF 603 — =PPVIN_PP5V_KBDLED
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V

SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0901 2.0DIA-TALL-EMI-MLB-M97-M98
SH0920 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0923 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0924 2.0DIA-TALL-EMI-MLB-M97-M98
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98
SH0917 2.0DIA-TALL-EMI-MLB-M97-M98
SH0918 2.0DIA-TALL-EMI-MLB-M97-M98
SH0919 2.0DIA-TALL-EMI-MLB-M97-M98
SH0930 2.0DIA-TALL-EMI-MLB-M97-M98
SH0921 2.0DIA-TALL-EMI-MLB-M97-M98
SH0931 2.0DIA-TALL-EMI-MLB-M97-M98
SH0922 2.0DIA-TALL-EMI-MLB-M97-M98
SH0932 2.0DIA-TALL-EMI-MLB-M97-M98
SH0934 2.0DIA-TALL-EMI-MLB-M97-M98
SH0933 2.0DIA-TALL-EMI-MLB-M97-M98
SH0935 2.0DIA-TALL-EMI-MLB-M97-M98
(all SM)

CPU signals

TP_IMVP6_CLKEN_L — VR_PWRGD_CLKEN_L
CPU_VID<0..6> — IMVP6_VID<0..6>
CPU_BSEL<0..2> — =MCP_BSEL<0..2>
MEM_VTT_EN — =DDRVTT_EN
TP_SPI_CS1_R_L_USE_MLB — =SPI_CS1_R_L_USE_MLB

GPU signals

PEG_D2R_P<0..15> — =PEG_D2R_P<0..15>
PEG_D2R_N<0..15> — =PEG_D2R_N<0..15>
PEG_R2D_C_P<0..15> — =PEG_R2D_C_P<0..15>
PEG_R2D_C_N<0..15> — =PEG_R2D_C_N<0..15>

LCD_BKLT_EN — LVDS_BKL_ON
DP_IG_ML_P<3> — =MCP_HDMI_TXC_P
DP_IG_ML_N<3> — =MCP_HDMI_TXC_N
DP_IG_ML_P<2..0> — =MCP_HDMI_TXD_P<0..2>
DP_IG_ML_N<2..0> — =MCP_HDMI_TXD_N<0..2>
DP_IG_DDC_CLK — =MCP_HDMI_DDC_CLK
DP_IG_DDC_DATA — =MCP_HDMI_DDC_DATA
DP_IG_HPD — =MCP_HDMI_HPD

GMUX ALIASES

PM_ALL_GPU_PGOOD — ALL_EG_PGOOD
TP_LVDS_MUX_SEL_EG — LVDS_MUX_SEL_EG
EG_RESET_L — GPU_RESET_L
JTAG_GMUX_TDI — GMUX_JTAG_TDI
JTAG_GMUX_TMS — GMUX_JTAG_TMS
JTAG_GMUX_TDO — GMUX_JTAG_TDO
GMUX_INT — =DVI_HPD_GMUX_INT
LVDS_IG_BKL_ON — IG_BKLT_EN
LVDS_IG_PANEL_PWR — IG_LCD_PWR_EN

=PP1V05_S0_MCP_SATA_DVDD1
=PP1V05_S0_MCP_SATA_AVDD1

=P1V5_EXP_S0_EN — PP3V3_S0

MCP_MII_PD
R0930 47K 5% 1/16W MF-LF 402
=MCP_MII_RXER
=MCP_MII_CRS
=MCP_MII_COL

Digital Ground

GND MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

TP_USB_EXTDP — USB_EXTD_P
TP_USB_EXTDN — USB_EXTD_N
TP_USB_MINIP — USB_MINI_P
TP_USB_MININ — USB_MINI_N
TP_MEM_A_A<15> — MEM_A_A<15>
TP_MEM_B_A<15> — MEM_B_A<15>
TP_CPU_PECI_MCP — CPU_PECI_MCP
TP_LVDS_IG_B_CLKP — LVDS_IG_B_CLK_P
TP_LVDS_IG_B_CLKN — LVDS_IG_B_CLK_N
TP_LVDS_IG_BKL_PWM — LVDS_IG_BKL_PWM

NC_LVDS_IG_A_DATAP<3> — LVDS_IG_A_DATA_P<3>
NC_LVDS_IG_A_DATAN<3> — LVDS_IG_A_DATA_N<3>
NC_LVDS_IG_B_DATAP<3> — LVDS_IG_B_DATA_P<3>
NC_LVDS_IG_B_DATAN<3> — LVDS_IG_B_DATA_N<3>
(NO_TEST=TRUE)

AUDIO ALIASES

HDA_BITCLK — HDA_BIT_CLK
=PP5V_S3_AUDIO_PWR
XW0900 PP5V_S3_AUDIO — MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V
XW0901 PP5V_S3_AUDIO_AMP — MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V
R0902 10K 5% 1/16W MF-LF 402 — AUD_IPHS_SWITCH_EN

R0903 0 1/16W MF-LF 402 — MCP_SPKR — SMC_MCP_SAFE_MODE

ETHERNET ALIASES

=P3V3ENET_EN — PM_SLP_RMGT_L
=P1V05ENET_EN
=PP3V3_ENET_PHY_VDDREG — TP_PP3V3_ENET_PHY_VDDREG
=RTL8211_REGOUT — NC_RTL8211_REGOUT
=RTL8211_ENSWREG

MCP79 PCIe PRSNT# Straps

R0925 0 5% 1/16W MF-LF 402 — PCIE_FW_PRSNT_L (OUT)
R0927 0 5% 1/16W MF-LF 402 — NO STUFF — PEG_PRSNT_L (OUT)
R0926 0 5% 1/16W MF-LF 402 — EG_CLKREQ_OUT_L (IN)

Signal Aliases

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 9 OF 98	

OMIT

U1000
PENRYN
FCBGA
1 OF 4

ADDR GROUP0
A3* A4* A5* A6* A7* A8* A9* A10* A11* A12* A13* A14* A15* A16* ADSTB0*
FSB_A_L<3> FSB_A_L<4> FSB_A_L<5> FSB_A_L<6> FSB_A_L<7> FSB_A_L<8> FSB_A_L<9> FSB_A_L<10> FSB_A_L<11> FSB_A_L<12> FSB_A_L<13> FSB_A_L<14> FSB_A_L<15> FSB_A_L<16> FSB_ADSTB_L<0>

REQ0* REQ1* REQ2* REQ3* REQ4*
FSB_REQ_L<0> FSB_REQ_L<1> FSB_REQ_L<2> FSB_REQ_L<3> FSB_REQ_L<4>

ADDR GROUP1
A17* A18* A19* A20* A21* A22* A23* A24* A25* A26* A27* A28* A29* A30* A31* A32* A33* A34* A35* ADSTB1*
FSB_A_L<17> FSB_A_L<18> FSB_A_L<19> FSB_A_L<20> FSB_A_L<21> FSB_A_L<22> FSB_A_L<23> FSB_A_L<24> FSB_A_L<25> FSB_A_L<26> FSB_A_L<27> FSB_A_L<28> FSB_A_L<29> FSB_A_L<30> FSB_A_L<31> FSB_A_L<32> FSB_A_L<33> FSB_A_L<34> FSB_A_L<35> FSB_ADSTB_L<1>

ICH
A20M* FERR* IGNNE* STPCLK* LINT0 LINT1 SMI*
CPU_A20M_L CPU_FERR_L CPU_IGNNE_L CPU_STPCLK_L CPU_INTR CPU_NMI CPU_SMI_L

RESERVED
RSVD0 RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8
TP_CPU_RSVD0 TP_CPU_RSVD1 TP_CPU_RSVD2 TP_CPU_RSVD3 TP_CPU_RSVD4 TP_CPU_RSVD5 TP_CPU_RSVD6 TP_CPU_RSVD7 TP_CPU_RSVD8

CONTROL
ADS* BNR* BPRI* DEFER* DRDY* DBSY* BR0* IERR* INIT* LOCK* RESET* RS0* RS1* RS2* TRDY* HIT* HITM*
FSB_ADS_L FSB_BNR_L FSB_BPRI_L FSB_DEFER_L FSB_DRDY_L FSB_DBSY_L FSB_BREQ0_L CPU_IERR_L CPU_INIT_L FSB_LOCK_L FSB_CPURST_L FSB_RS_L<0> FSB_RS_L<1> FSB_RS_L<2> FSB_TRDY_L FSB_HIT_L FSB_HITM_L

XDP/ITP SIGNALS
BPM0* BPM1* BPM2* BPM3* PRDY* PREQ* TCK TDI TDO TMS TRST* DBR*
XDP_BPM_L<0> XDP_BPM_L<1> XDP_BPM_L<2> XDP_BPM_L<3> XDP_BPM_L<4> XDP_BPM_L<5> XDP_TCK XDP_TDI XDP_TDO XDP_TMS XDP_TRST_L XDP_DBRESET_L

THERMAL
PROCHOT* THERMDA THERMDC THERMTRIP*
CPU_PROCHOT_L CPU_THERMD_P CPU_THERMD_N PM_THRMTRIP_L

H CLK
BCLK0 BCLK1
FSB_CLK_CPU_P FSB_CLK_CPU_N

=PP1V05_S0_CPU
R1002 54.9 1% 1/16W MF-LF 402

PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY

=PP1V05_S0_CPU
R1003 54.9 1% 1/16W MF-LF 402

R1004 68 5% 1/16W MF-LF 402

PM_THRMTRIP# SHOULD CONNECT TO ICH AND GMCH WITHOUT T (NO STUB)

=PP1V05_S0_CPU
R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402

0.5" MAX LENGTH FOR CPU_GTLREF

NOSTUFF C1000 0.1uF 10% 16V X5R 402

PLACE C1000 CLOSE TO CPU_TEST4 PIN. MAKE SURE CPU_TEST4 IS REFERENCED TO GND

R1020 54.9 1% 1/16W MF-LF 402
R1021 54.9 1% 1/16W MF-LF 402
R1022 54.9 1% 1/16W MF-LF 402
R1023 649 1% 1/16W MF-LF 402
R1024 54.9 1% 1/16W MF-LF 402
=PP1V05_S0_CPU

PLACEMENT_NOTE=Place R1024 near ITP connector (if present)

OMIT

U1000
PENRYN
FCBGA
2 OF 4

DATA GRP 0
D0* D1* D2* D3* D4* D5* D6* D7* D8* D9* D10* D11* D12* D13* D14* D15* DSTBN0* DSTBP0* DINV0*
FSB_D_L<0> FSB_D_L<1> FSB_D_L<2> FSB_D_L<3> FSB_D_L<4> FSB_D_L<5> FSB_D_L<6> FSB_D_L<7> FSB_D_L<8> FSB_D_L<9> FSB_D_L<10> FSB_D_L<11> FSB_D_L<12> FSB_D_L<13> FSB_D_L<14> FSB_D_L<15> FSB_DSTB_L_N<0> FSB_DSTB_L_P<0> FSB_DINV_L<0>

DATA GRP 1
D16* D17* D18* D19* D20* D21* D22* D23* D24* D25* D26* D27* D28* D29* D30* D31* DSTBN1* DSTBP1* DINV1*
FSB_D_L<16> FSB_D_L<17> FSB_D_L<18> FSB_D_L<19> FSB_D_L<20> FSB_D_L<21> FSB_D_L<22> FSB_D_L<23> FSB_D_L<24> FSB_D_L<25> FSB_D_L<26> FSB_D_L<27> FSB_D_L<28> FSB_D_L<29> FSB_D_L<30> FSB_D_L<31> FSB_DSTB_L_N<1> FSB_DSTB_L_P<1> FSB_DINV_L<1>

DATA GRP 2
D32* D33* D34* D35* D36* D37* D38* D39* D40* D41* D42* D43* D44* D45* D46* D47* DSTBN2* DSTBP2* DINV2*
FSB_D_L<32> FSB_D_L<33> FSB_D_L<34> FSB_D_L<35> FSB_D_L<36> FSB_D_L<37> FSB_D_L<38> FSB_D_L<39> FSB_D_L<40> FSB_D_L<41> FSB_D_L<42> FSB_D_L<43> FSB_D_L<44> FSB_D_L<45> FSB_D_L<46> FSB_D_L<47> FSB_DSTB_L_N<2> FSB_DSTB_L_P<2> FSB_DINV_L<2>

DATA GRP 3
D48* D49* D50* D51* D52* D53* D54* D55* D56* D57* D58* D59* D60* D61* D62* D63* DSTBN3* DSTBP3* DINV3*
FSB_D_L<48> FSB_D_L<49> FSB_D_L<50> FSB_D_L<51> FSB_D_L<52> FSB_D_L<53> FSB_D_L<54> FSB_D_L<55> FSB_D_L<56> FSB_D_L<57> FSB_D_L<58> FSB_D_L<59> FSB_D_L<60> FSB_D_L<61> FSB_D_L<62> FSB_D_L<63> FSB_DSTB_L_N<3> FSB_DSTB_L_P<3> FSB_DINV_L<3>

MISC
GTLREF TEST1 TEST2 TEST3 TEST4 TEST5 TEST6 TEST7 BSEL0 BSEL1 BSEL2
CPU_GTLREF CPU_TEST1 CPU_TEST2 TP_CPU_TEST3 CPU_TEST4 TP_CPU_TEST5 TP_CPU_TEST6 TP_CPU_TEST7 CPU_BSEL<0> CPU_BSEL<1> CPU_BSEL<2>

COMP0 COMP1 COMP2 COMP3
CPU_COMP<0> CPU_COMP<1> CPU_COMP<2> CPU_COMP<3>

DPRSTP* DPSLP* DPWR* PWRGOOD* SLP* PSI*
CPU_DPRSTP_L CPU_DPSLP_L FSB_DPWR_L CPU_PWRGD FSB_CPUSLP_L CPU_PSI_L

R1016 27.4 1% 1/16W MF-LF 402
R1017 54.9 1% 1/16W MF-LF 402
R1018 27.4 1% 1/16W MF-LF 402
R1019 54.9 1% 1/16W MF-LF 402

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".

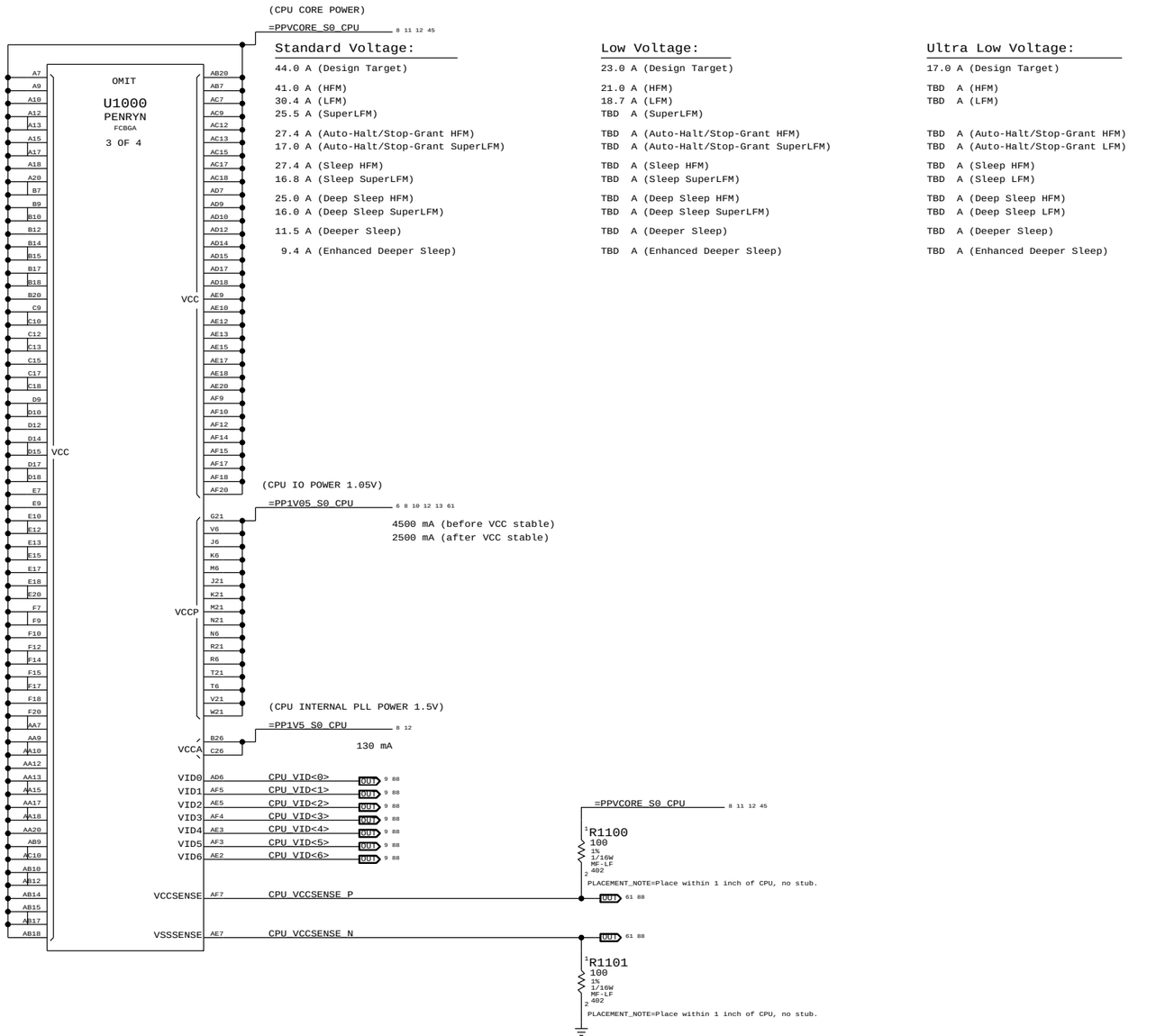
NOSTUFF R1030 0 5% 1/16W MF-LF 402
NOSTUFF R1012 1K 5% 1/16W MF-LF 402
NOSTUFF R1007 1K 5% 1/16W MF-LF 402

CPU FSB

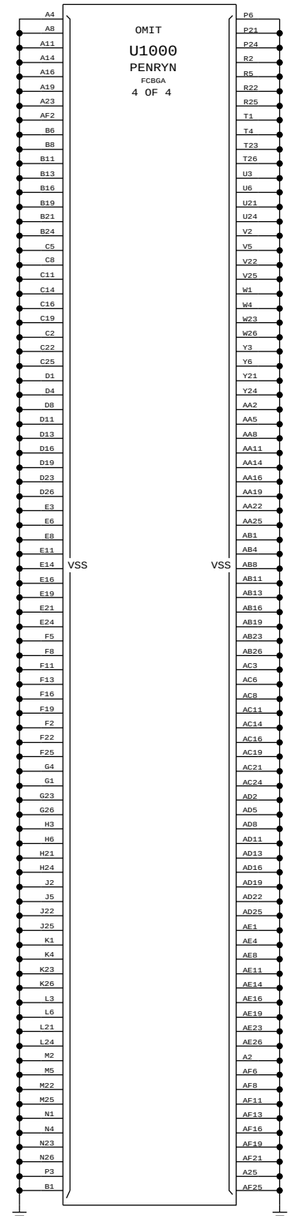
SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 10 OF 98	



Standard Voltage:	Low Voltage:	Ultra Low Voltage:
44.0 A (Design Target)	23.0 A (Design Target)	17.0 A (Design Target)
41.0 A (HFM)	21.0 A (HFM)	TBD A (HFM)
30.4 A (LFM)	18.7 A (LFM)	TBD A (LFM)
25.5 A (SuperLFM)	TBD A (SuperLFM)	
27.4 A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant LFM)
27.4 A (Sleep HFM)	TBD A (Sleep HFM)	TBD A (Sleep HFM)
16.8 A (Sleep SuperLFM)	TBD A (Sleep SuperLFM)	TBD A (Sleep LFM)
25.0 A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)	TBD A (Deep Sleep SuperLFM)	TBD A (Deep Sleep LFM)
11.5 A (Deeper Sleep)	TBD A (Deeper Sleep)	TBD A (Deeper Sleep)
9.4 A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)



Current numbers from Merom for Santa Rosa EMTS, doc #22221.

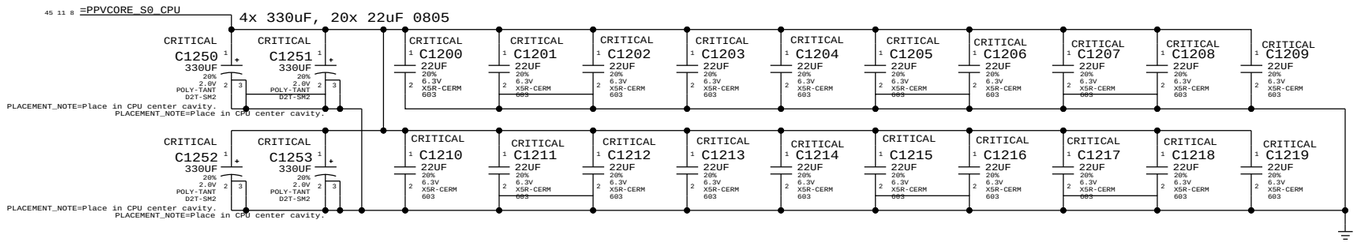
CPU Power & Ground

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

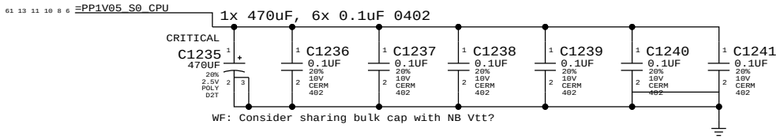
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 11 OF 98	

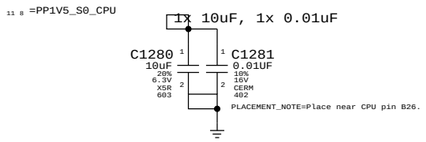
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

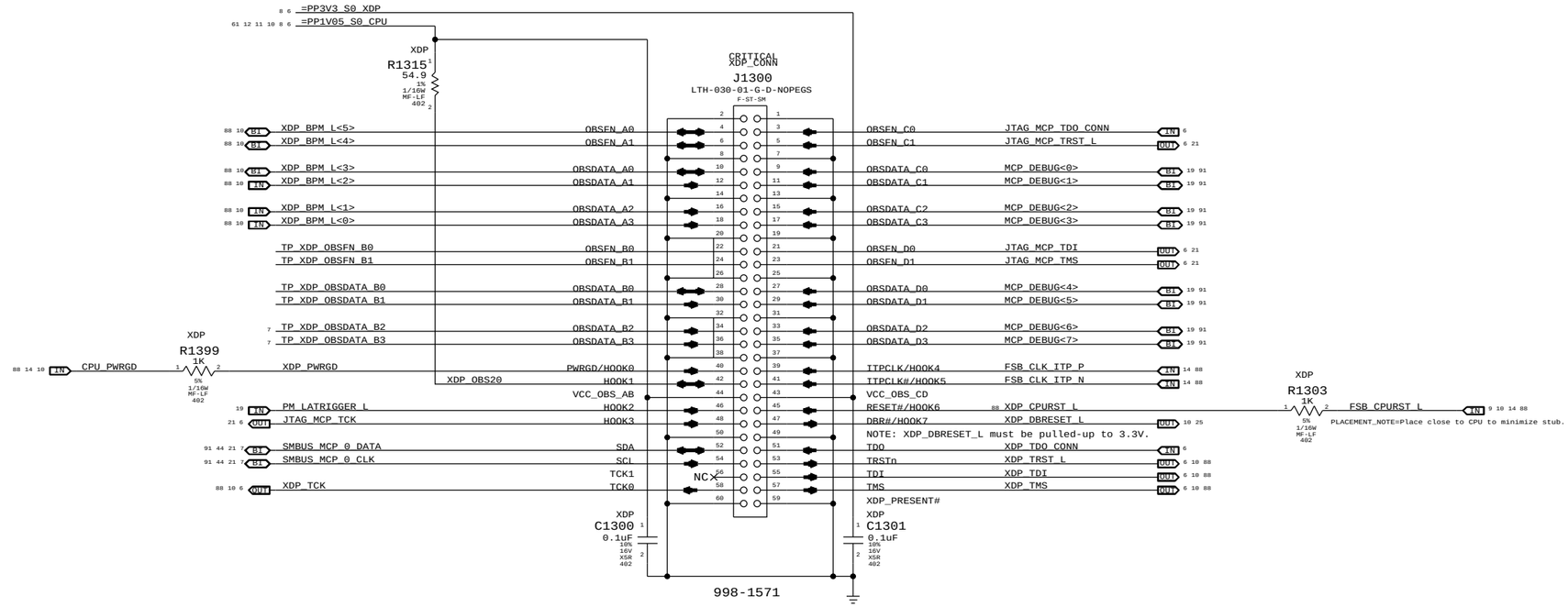
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 12 OF 98	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port(MiniXDP)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 13 OF 98	

OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#	
FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#	
FSB_DINV_L<0>	V41	CPU_DBI0#	
FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#	
FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#	
FSB_DINV_L<1>	V35	CPU_DBI1#	
FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#	
FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#	
FSB_DINV_L<2>	N35	CPU_DBI2#	
FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#	
FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#	
FSB_DINV_L<3>	J41	CPU_DBI3#	
FSB_A_L<3>	AC34	CPU_A3#	
FSB_A_L<4>	AE38	CPU_A4#	
FSB_A_L<5>	AE34	CPU_A5#	
FSB_A_L<6>	AC37	CPU_A6#	
FSB_A_L<7>	AE37	CPU_A7#	
FSB_A_L<8>	AE35	CPU_A8#	
FSB_A_L<9>	AB35	CPU_A9#	
FSB_A_L<10>	AF35	CPU_A10#	
FSB_A_L<11>	AG35	CPU_A11#	
FSB_A_L<12>	AG39	CPU_A12#	
FSB_A_L<13>	AE33	CPU_A13#	
FSB_A_L<14>	AG37	CPU_A14#	
FSB_A_L<15>	AG38	CPU_A15#	
FSB_A_L<16>	AG34	CPU_A16#	
FSB_A_L<17>	AN38	CPU_A17#	
FSB_A_L<18>	AL39	CPU_A18#	
FSB_A_L<19>	AG33	CPU_A19#	
FSB_A_L<20>	AL33	CPU_A20#	
FSB_A_L<21>	AJ33	CPU_A21#	
FSB_A_L<22>	AN36	CPU_A22#	
FSB_A_L<23>	AJ35	CPU_A23#	
FSB_A_L<24>	AJ37	CPU_A24#	
FSB_A_L<25>	AJ36	CPU_A25#	
FSB_A_L<26>	AJ38	CPU_A26#	
FSB_A_L<27>	AL37	CPU_A27#	
FSB_A_L<28>	AL34	CPU_A28#	
FSB_A_L<29>	AN37	CPU_A29#	
FSB_A_L<30>	AJ34	CPU_A30#	
FSB_A_L<31>	AL38	CPU_A31#	
FSB_A_L<32>	AL35	CPU_A32#	
FSB_A_L<33>	AN34	CPU_A33#	
FSB_A_L<34>	AR39	CPU_A34#	
FSB_A_L<35>	AN35	CPU_A35#	
FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#	
FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#	
FSB_REQ_L<0>	AC38	CPU_REQ0#	
FSB_REQ_L<1>	AA33	CPU_REQ1#	
FSB_REQ_L<2>	AC39	CPU_REQ2#	
FSB_REQ_L<3>	AC33	CPU_REQ3#	
FSB_REQ_L<4>	AC35	CPU_REQ4#	
FSB_ADS_L	AD42	CPU_ADS#	
FSB_BNR_L	AD43	CPU_BNR#	
FSB_BREQ0_L	AE40	CPU_BR0#	
FSB_BREQ1_L	AL32	CPU_BR1#	
FSB_DBSY_L	AD39	CPU_DBSY#	
FSB_DRDY_L	AD41	CPU_DRDY#	
FSB_HIT_L	AB42	CPU_HIT#	
FSB_HITM_L	AD40	CPU_HITM#	
FSB_LOCK_L	AC43	CPU_LOCK#	
FSB_TRDY_L	AE41	CPU_TRDY#	
CPU_PECI_MCP	E41	CPU_PECI	
CPU_PROCHOT_L	AJ41	CPU_PROCHOT#	
	AG43	CPU_THERMTRIP#	
	AH40	CPU_FERR#	
(MCP_BSEL<2>)	F42	CPU_BSEL2	
(MCP_BSEL<1>)	D42	CPU_BSEL1	
(MCP_BSEL<0>)	F41	CPU_BSEL0	
FSB_RS_L<0>	AC41	CPU_RS0#	
FSB_RS_L<1>	AB41	CPU_RS1#	
FSB_RS_L<2>	AC42	CPU_RS2#	
PP1V05_S0_MCP_PLL_FSB	AG27	+V_DLL_DLCELL_AVDD	206 mA
	AH27	+V_PLL_MCLK	20 mA
	AG28	+V_PLL_FSB	29 mA
	AH28	+V_PLL_CPU	15 mA
MCP_BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD	
MCP_BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND	
MCP_CPU_COMP_VCC	AM43	CPU_COMP_VCC	
MCP_CPU_COMP_GND	AM42	CPU_COMP_GND	

CPU_D0#	Y43	FSB_D_L<0>	
CPU_D1#	W42	FSB_D_L<1>	
CPU_D2#	Y40	FSB_D_L<2>	
CPU_D3#	W41	FSB_D_L<3>	
CPU_D4#	Y39	FSB_D_L<4>	
CPU_D5#	V42	FSB_D_L<5>	
CPU_D6#	Y41	FSB_D_L<6>	
CPU_D7#	Y42	FSB_D_L<7>	
CPU_D8#	P42	FSB_D_L<8>	
CPU_D9#	U41	FSB_D_L<9>	
CPU_D10#	R42	FSB_D_L<10>	
CPU_D11#	T39	FSB_D_L<11>	
CPU_D12#	T42	FSB_D_L<12>	
CPU_D13#	T41	FSB_D_L<13>	
CPU_D14#	R41	FSB_D_L<14>	
CPU_D15#	T43	FSB_D_L<15>	
CPU_D16#	W35	FSB_D_L<16>	
CPU_D17#	AA37	FSB_D_L<17>	
CPU_D18#	W33	FSB_D_L<18>	
CPU_D19#	W34	FSB_D_L<19>	
CPU_D20#	AA36	FSB_D_L<20>	
CPU_D21#	AA34	FSB_D_L<21>	
CPU_D22#	AA38	FSB_D_L<22>	
CPU_D23#	AA35	FSB_D_L<23>	
CPU_D24#	U38	FSB_D_L<24>	
CPU_D25#	U36	FSB_D_L<25>	
CPU_D26#	U35	FSB_D_L<26>	
CPU_D27#	U33	FSB_D_L<27>	
CPU_D28#	U34	FSB_D_L<28>	
CPU_D29#	W38	FSB_D_L<29>	
CPU_D30#	R33	FSB_D_L<30>	
CPU_D31#	U37	FSB_D_L<31>	
CPU_D32#	N34	FSB_D_L<32>	
CPU_D33#	N33	FSB_D_L<33>	
CPU_D34#	R34	FSB_D_L<34>	
CPU_D35#	R35	FSB_D_L<35>	
CPU_D36#	P35	FSB_D_L<36>	
CPU_D37#	R39	FSB_D_L<37>	
CPU_D38#	R37	FSB_D_L<38>	
CPU_D39#	R38	FSB_D_L<39>	
CPU_D40#	L37	FSB_D_L<40>	
CPU_D41#	L39	FSB_D_L<41>	
CPU_D42#	L38	FSB_D_L<42>	
CPU_D43#	N36	FSB_D_L<43>	
CPU_D44#	N38	FSB_D_L<44>	
CPU_D45#	J39	FSB_D_L<45>	
CPU_D46#	J38	FSB_D_L<46>	
CPU_D47#	J37	FSB_D_L<47>	
CPU_D48#	L42	FSB_D_L<48>	
CPU_D49#	M42	FSB_D_L<49>	
CPU_D50#	P41	FSB_D_L<50>	
CPU_D51#	N41	FSB_D_L<51>	
CPU_D52#	N40	FSB_D_L<52>	
CPU_D53#	M40	FSB_D_L<53>	
CPU_D54#	H40	FSB_D_L<54>	
CPU_D55#	K42	FSB_D_L<55>	
CPU_D56#	H41	FSB_D_L<56>	
CPU_D57#	L41	FSB_D_L<57>	
CPU_D58#	H43	FSB_D_L<58>	
CPU_D59#	H42	FSB_D_L<59>	
CPU_D60#	K41	FSB_D_L<60>	
CPU_D61#	J40	FSB_D_L<61>	
CPU_D62#	H39	FSB_D_L<62>	
CPU_D63#	M43	FSB_D_L<63>	
CPU_BPRI#	AA41	FSB_BPRI_L	
CPU_DEFER#	AA40	FSB_DEFER_L	
BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P	
BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N	
BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P	
BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N	
BCLK_OUT_NB_P	AL41	FSB_CLK_MCP_P	
BCLK_OUT_NB_N	AK42	FSB_CLK_MCP_N	
BCLK_IN_N	AK41		
BCLK_IN_P	AJ40		
CPU_A20M#	AF41	CPU_A20M_L	
CPU_IGNNE#	AH39	CPU_IGNNE_L	
CPU_INIT#	AH42	CPU_INIT_L	
CPU_INTR	AF42	CPU_INTR	
CPU_NMI	AG41	CPU_NMI	
CPU_SMI#	AH41	CPU_SMI_L	
CPU_PWRGD	AH43	CPU_PWRGD	
CPU_RESET#	H38	FSB_CPURST_L	
CPU_SLP#	AM33	FSB_CPUSLP_L	
CPU_DPSLP#	AN33	CPU_DPSLP_L	
CPU_DPWR#	AM32	FSB_DPWR_L	
CPU_STPCLK#	AG42	CPU_STPCLK_L	
CPU_DPRSTP#	AN32	CPU_DPRSTP_L	

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/16W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

PM_THRMTRIP_L
CPU_FERR_L

NO STUFF
R1420 1K 5% 1/16W MF-LF 402
R1421 1K 5% 1/16W MF-LF 402
R1422 1K 5% 1/16W MF-LF 402

=MCP_BSEL<2>
=MCP_BSEL<1>
=MCP_BSEL<0>

R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

=PP1V05_S0_MCP_FSB
NO STUFF
R1440 150 5% 1/16W MF-LF 402

MCP CPU Interface

SYNC_MASTER=T18_MLB
SYNC_DATE=06/06/2008

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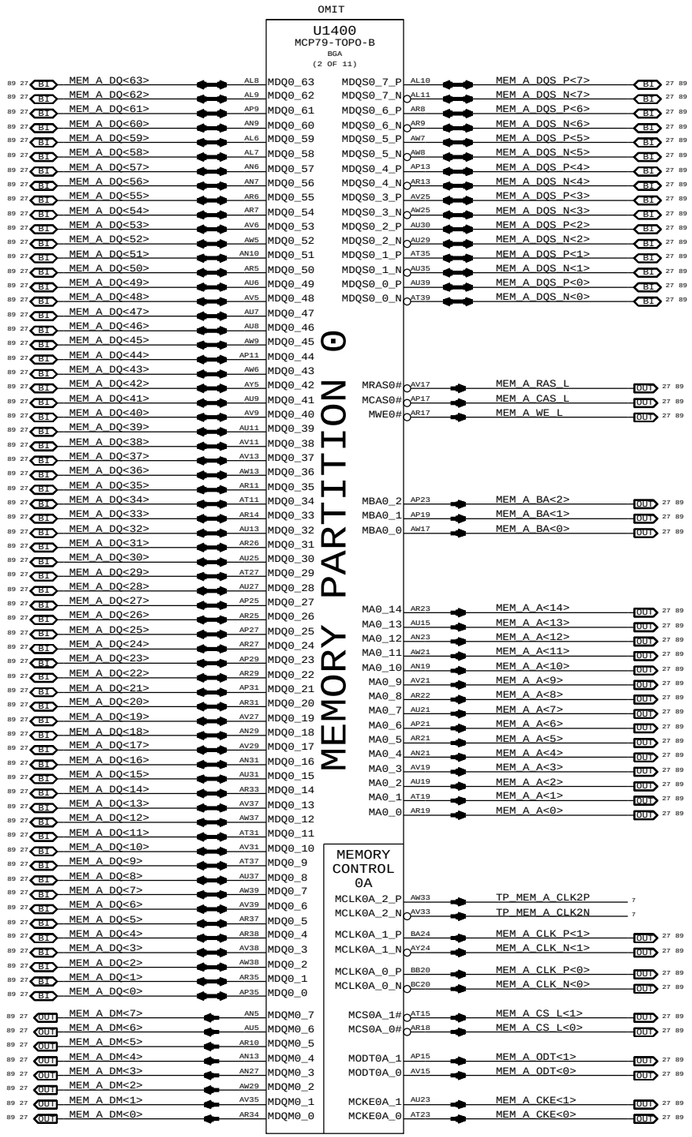
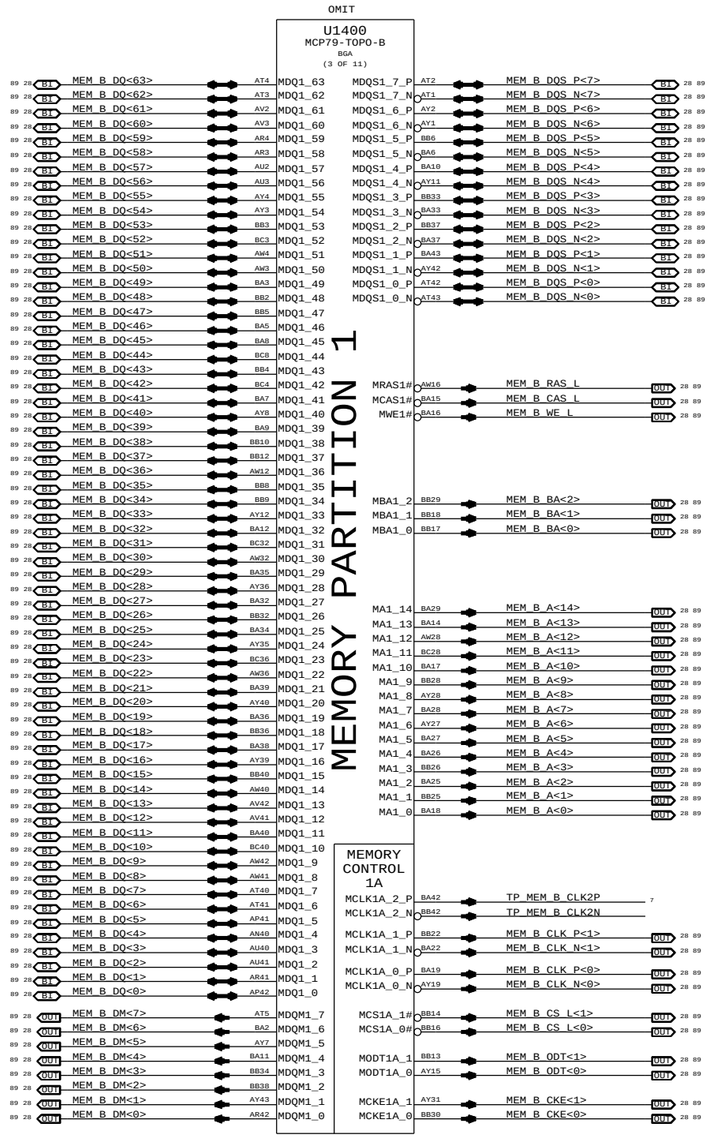
SCALE: NONE	SHT 14 OF 98	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).





MCP Memory Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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SCALE: NONE	SHT 15 OF 98	

OMIT

U1400
MCP79-TOPO-B
BGA
(4 OF 11)

MEMORY CONTROL 0B

7 TP_MEM_A_CLK5P	AU33	MCLK0B_2_P	
7 TP_MEM_A_CLK5N	AU32	MCLK0B_2_N	
7 TP_MEM_A_CLK4P	BB24	MCLK0B_1_P	
7 TP_MEM_A_CLK4N	BC22	MCLK0B_1_N	
7 TP_MEM_A_CLK3P	BA21	MCLK0B_0_P	
7 TP_MEM_A_CLK3N	BB21	MCLK0B_0_N	
7 TP_MEM_A_CS_L<2>	AU17	MCS0B_0#	
7 TP_MEM_A_CS_L<3>	AR17	MCS0B_1#	
7 TP_MEM_A_ODT<2>	AN17	MODT0B_0	
7 TP_MEM_A_ODT<3>	AN15	MODT0B_1	
7 TP_MEM_A_CKE<2>	AV23	MCKE0B_0	
7 TP_MEM_A_CKE<3>	AN25	MCKE0B_1	

MEMORY CONTROL 1B

MCLK1B_2_P	BA41	TP_MEM_B_CLK5P	7
MCLK1B_2_N	BB41	TP_MEM_B_CLK5N	7
MCLK1B_1_P	AY23	TP_MEM_B_CLK4P	7
MCLK1B_1_N	BA23	TP_MEM_B_CLK4N	7
MCLK1B_0_P	BA20	TP_MEM_B_CLK3P	7
MCLK1B_0_N	AY20	TP_MEM_B_CLK3N	7
MCS1B_0#	BC16	TP_MEM_B_CS_L<2>	7
MCS1B_1#	BA13	TP_MEM_B_CS_L<3>	7
MODT1B_0	AY16	TP_MEM_B_ODT<2>	7
MODT1B_1	BC13	TP_MEM_B_ODT<3>	7
MCKE1B_0	BA30	TP_MEM_B_CKE<2>	7
MCKE1B_1	BA31	TP_MEM_B_CKE<3>	

23 16 8 =PP1V8R1V5_S0_MCP_MEM

R1610 1
40.2
1%
1/16W
MF-LF
402
2

R1611 1
40.2
1%
1/16W
MF-LF
402
2

23 PP1V05_S0_MCP_PLL_CORE
87 mA (A01)

17 mA	T27	+V_PLL_XREF_XS
12 mA	U28	+V_PLL_DP
19 mA	U27	+V_PLL_CORE
39 mA	T28	+V_VPLL

89 MCP_MEM_COMP_VDD AN41 MEM_COMP_VDD
89 MCP_MEM_COMP_GND AM41 MEM_COMP_GND

MRESET0# AY32 MCP_MEM_RESET_L OUT 29
TP or NC for DDR2.

=PP1V8R1V5_S0_MCP_MEM 8 16 23
4771 mA (A01, DDR3)

AA22	GND1	+VDD_MEM1	AM17
AP12	GND2	+VDD_MEM2	AM19
G30	GND3	+VDD_MEM3	AM21
P10	GND4	+VDD_MEM4	AM23
T10	GND5	+VDD_MEM5	AM25
T6	GND6	+VDD_MEM6	AM27
V10	GND7	+VDD_MEM7	AM29
V34	GND8	+VDD_MEM8	AN16
W5	GND9	+VDD_MEM9	BC29
AA39	GND10	+VDD_MEM10	AN20
AB22	GND11	+VDD_MEM11	AN24
AB7	GND12	+VDD_MEM12	AT17
AD22	GND13	+VDD_MEM13	AP16
AE20	GND14	+VDD_MEM14	AN22
AF24	GND15	+VDD_MEM15	AP20
AG24	GND16	+VDD_MEM16	AP24
AH35	GND17	+VDD_MEM17	AV16
AK7	GND18	+VDD_MEM18	AR16
AM28	GND19	+VDD_MEM19	AR20
AT25	GND20	+VDD_MEM20	AR24
AP30	GND21	+VDD_MEM21	AW15
AR36	GND22	+VDD_MEM22	AP22
AU10	GND23	+VDD_MEM23	AP18
F28	GND24	+VDD_MEM24	AU16
BC21	GND25	+VDD_MEM25	AN18
AY9	GND26	+VDD_MEM26	AU24
BC9	GND27	+VDD_MEM27	AT21
D34	GND28	+VDD_MEM28	AY29
F24	GND29	+VDD_MEM29	AV24
G32	GND30	+VDD_MEM30	AU20
H31	GND31	+VDD_MEM31	AU22
K7	GND32	+VDD_MEM32	AW27
M38	GND33	+VDD_MEM33	BC17
M5	GND34	+VDD_MEM34	AV20
M6	GND35	+VDD_MEM35	AY17
M7	GND36	+VDD_MEM36	AY18
M9	GND37	+VDD_MEM37	AM15
N39	GND38	+VDD_MEM38	AU18
N8	GND39	+VDD_MEM39	AY25
P33	GND40	+VDD_MEM40	AY26
P34	GND41	+VDD_MEM41	AW19
P37	GND42	+VDD_MEM42	AW24
P4	GND43	+VDD_MEM43	BC25
P40	GND44	+VDD_MEM44	AL30
P7	GND45	+VDD_MEM45	AM31
R36	GND46		
R40	GND47	GND55	T33
R43	GND48	GND56	T34
R5	GND49	GND57	T35
T18	GND50	GND58	T37
T20	GND51	GND59	T38
AK11	GND52	GND60	T7
T24	GND53	GND61	T9
T26	GND54	GND62	U18
		GND63	U20
		GND64	U22

MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 16 OF 98	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

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U1400
MCP79-TOPO-B
BGA
(5 OF 11)

PCI EXPRESS

=PEG_D2R_P<0>	F7	PE0_RX0_P		PE0_TX0_P	C5	=PEG_R2D_C_P<0>	
=PEG_D2R_N<0>	E7	PE0_RX0_N		PE0_TX0_N	D4	=PEG_R2D_C_N<0>	
=PEG_D2R_P<1>	D7	PE0_RX1_P		PE0_TX1_P	C4	=PEG_R2D_C_P<1>	
=PEG_D2R_N<1>	C7	PE0_RX1_N		PE0_TX1_N	B4	=PEG_R2D_C_N<1>	
=PEG_D2R_P<2>	E6	PE0_RX2_P		PE0_TX2_P	A4	=PEG_R2D_C_P<2>	
=PEG_D2R_N<2>	E6	PE0_RX2_N		PE0_TX2_N	A3	=PEG_R2D_C_N<2>	
=PEG_D2R_P<3>	E5	PE0_RX3_P		PE0_TX3_P	B3	=PEG_R2D_C_P<3>	
=PEG_D2R_N<3>	F5	PE0_RX3_N		PE0_TX3_N	B2	=PEG_R2D_C_N<3>	
=PEG_D2R_P<4>	E4	PE0_RX4_P		PE0_TX4_P	C1	=PEG_R2D_C_P<4>	
=PEG_D2R_N<4>	E3	PE0_RX4_N		PE0_TX4_N	D1	=PEG_R2D_C_N<4>	
=PEG_D2R_P<5>	C3	PE0_RX5_P		PE0_TX5_P	D2	=PEG_R2D_C_P<5>	
=PEG_D2R_N<5>	D3	PE0_RX5_N		PE0_TX5_N	E1	=PEG_R2D_C_N<5>	
=PEG_D2R_P<6>	G5	PE0_RX6_P		PE0_TX6_P	E2	=PEG_R2D_C_P<6>	
=PEG_D2R_N<6>	H5	PE0_RX6_N		PE0_TX6_N	F2	=PEG_R2D_C_N<6>	
=PEG_D2R_P<7>	J7	PE0_RX7_P		PE0_TX7_P	F3	=PEG_R2D_C_P<7>	
=PEG_D2R_N<7>	J6	PE0_RX7_N		PE0_TX7_N	F4	=PEG_R2D_C_N<7>	
=PEG_D2R_P<8>	J5	PE0_RX8_P		PE0_TX8_P	G3	=PEG_R2D_C_P<8>	
=PEG_D2R_N<8>	J4	PE0_RX8_N		PE0_TX8_N	H4	=PEG_R2D_C_N<8>	
=PEG_D2R_P<9>	L11	PE0_RX9_P		PE0_TX9_P	H3	=PEG_R2D_C_P<9>	
=PEG_D2R_N<9>	L10	PE0_RX9_N		PE0_TX9_N	H2	=PEG_R2D_C_N<9>	
=PEG_D2R_P<10>	L9	PE0_RX10_P		PE0_TX10_P	H1	=PEG_R2D_C_P<10>	
=PEG_D2R_N<10>	L8	PE0_RX10_N		PE0_TX10_N	J1	=PEG_R2D_C_N<10>	
=PEG_D2R_P<11>	L7	PE0_RX11_P		PE0_TX11_P	J2	=PEG_R2D_C_P<11>	
=PEG_D2R_N<11>	L6	PE0_RX11_N		PE0_TX11_N	J3	=PEG_R2D_C_N<11>	
=PEG_D2R_P<12>	N11	PE0_RX12_P		PE0_TX12_P	K2	=PEG_R2D_C_P<12>	
=PEG_D2R_N<12>	N10	PE0_RX12_N		PE0_TX12_N	K3	=PEG_R2D_C_N<12>	
=PEG_D2R_P<13>	N9	PE0_RX13_P		PE0_TX13_P	L4	=PEG_R2D_C_P<13>	
=PEG_D2R_N<13>	P9	PE0_RX13_N		PE0_TX13_N	L3	=PEG_R2D_C_N<13>	
=PEG_D2R_P<14>	N7	PE0_RX14_P		PE0_TX14_P	M4	=PEG_R2D_C_P<14>	
=PEG_D2R_N<14>	N6	PE0_RX14_N		PE0_TX14_N	M3	=PEG_R2D_C_N<14>	
=PEG_D2R_P<15>	N5	PE0_RX15_P		PE0_TX15_P	M2	=PEG_R2D_C_P<15>	
=PEG_D2R_N<15>	N4	PE0_RX15_N		PE0_TX15_N	M1	=PEG_R2D_C_N<15>	

			PE0_REFCLK_P	E11	PEG_CLK100M_P	69 90
			PE0_REFCLK_N	D11	PEG_CLK100M_N	69 90
PEG_PRSNT_L	C9	PE0_PRSNT_16# Int PU				
MINI_CLKREQ_L	D5	PEB_CLKREQ#/GPIO_49 Int PU	PE1_REFCLK_P	G11	PCIE_CLK100M_MINI_P	30 90
PCIE_MINI_PRSNT_L	D9	PEB_PRSNT# Int PU	PE1_REFCLK_N	F11	PCIE_CLK100M_MINI_N	30 90
FW_CLKREQ_L	E8	PEC_CLKREQ#/GPIO_50 Int PU	PE2_REFCLK_P	J11	PCIE_CLK100M_FW_P	35 90
PCIE_FW_PRSNT_L	C10	PEC_PRSNT# Int PU	PE2_REFCLK_N	J10	PCIE_CLK100M_FW_N	35 90
EXCARD_CLKREQ_L	M15	PED_CLKREQ#/GPIO_51 Int PU	PE3_REFCLK_P	G13	PCIE_CLK100M_EXCARD_P	31 90
PCIE_EXCARD_PRSNT_L	B10	PED_PRSNT# Int PU	PE3_REFCLK_N	F13	PCIE_CLK100M_EXCARD_N	31 90
TP_PE4_CLKREQ_L	L16	PEE_CLKREQ#/GPIO_16 Int PU	PE4_REFCLK_P	J13	TP_PCIE_CLK100M_PE4P	7
TP_PE4_PRSNT_L	L18	PEE_PRSNT#/GPIO_46 Int PU	PE4_REFCLK_N	H13	TP_PCIE_CLK100M_PE4N	
AUD_IP_PERIPHERAL_DET	M16	PEF_CLKREQ#/GPIO_17 Int PU	PE5_REFCLK_P	L14	TP_PCIE_CLK100M_PE5P	7
GMUX_JTAG_TCK_L	M18	PEF_PRSNT#/GPIO_47 Int PU	PE5_REFCLK_N	K14	TP_PCIE_CLK100M_PE5N	7
TP_MCP_GPIO_18	M17	PEG_CLKREQ#/GPIO_18 Int PU	PE6_REFCLK_P	N14	TP_PCIE_CLK100M_PE6P	7
GMUX_JTAG_TDO	M19	PEG_PRSNT#/GPIO_48 Int PU	PE6_REFCLK_N	M14	TP_PCIE_CLK100M_PE6N	7
PCIE_WAKE_L	F17	PE_WAKE# Int PU (S5)	PEX_RST0#	K11	PCIE_RESET_L	25
PCIE_MINI_D2R_P	K9	PE1_RX0_P	PE1_TX0_P	D8	PCIE_MINI_R2D_C_P	30 90
PCIE_MINI_D2R_N	J9	PE1_RX0_N	PE1_TX0_N	C8	PCIE_MINI_R2D_C_N	30 90
PCIE_FW_D2R_P	H9	PE1_RX1_P	PE1_TX1_P	B8	PCIE_FW_R2D_C_P	35 90
PCIE_FW_D2R_N	G9	PE1_RX1_N	PE1_TX1_N	A8	PCIE_FW_R2D_C_N	35 90
PCIE_EXCARD_D2R_P	F9	PE1_RX2_P	PE1_TX2_P	A7	PCIE_EXCARD_R2D_C_P	31 90
PCIE_EXCARD_D2R_N	E9	PE1_RX2_N	PE1_TX2_N	B7	PCIE_EXCARD_R2D_C_N	31 90
TP_PCIE_PE4_D2RP	H7	PE1_RX3_P	PE1_TX3_P	B6	TP_PCIE_PE4_R2D_CP	
TP_PCIE_PE4_D2RN	G7	PE1_RX3_N	PE1_TX3_N	C6	TP_PCIE_PE4_R2D_CN	

=PP1V05_S0_MCP_PEX_DVDD0
57 mA (A01, DVDD0 & 1)
Minimum 1.025V for Gen2 support

+DVDD0_PEX1	T17
+DVDD0_PEX2	W19
+DVDD0_PEX3	U17
+DVDD0_PEX4	V19
+DVDD0_PEX5	W16
+DVDD0_PEX6	W17
+DVDD0_PEX7	W18
+DVDD0_PEX8	U16

=PP1V05_S0_MCP_PEX_DVDD1

+DVDD1_PEX1	T19
+DVDD1_PEX2	U19

PP1V05_S0_MCP_PLL_PEX
84 mA (A01)

+V_PLL_PEX T16

MCP_PEX_CLK_COMP
NO STUFF
R1710
2.37K
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 12.7mm of U1400

PEX_CLK_COMP A11

=PP1V05_S0_MCP_PEX_AVDD0
206 mA (A01, AVDD0 & 1)
Minimum 1.025V for Gen2 support

+AVDD0_PEX1	Y12
+AVDD0_PEX2	AA12
+AVDD0_PEX3	AB12
+AVDD0_PEX4	M12
+AVDD0_PEX5	P12
+AVDD0_PEX6	R12
+AVDD0_PEX7	N12
+AVDD0_PEX8	T12
+AVDD0_PEX9	U12
+AVDD0_PEX10	AC12
+AVDD0_PEX11	AD12
+AVDD0_PEX12	V12
+AVDD0_PEX13	W12

=PP1V05_S0_MCP_PEX_AVDD1

+AVDD1_PEX1	M13
+AVDD1_PEX2	N13
+AVDD1_PEX3	P13

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

MCP PCIe Interfaces

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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SCALE: NONE	SHT 17 OF 98	

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MCP79-TOPO-B
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LAN

DACS

FLAT PANEL

RGB ONLY

=PP3V3_ENET_MCP_RMGT — 83 mA (A01)
=PP1V05_ENET_MCP_RMGT — 131 mA (A01)

ENET_RXD<0>	C23	RGMII_RXD0	
ENET_RXD<1>	B23	RGMII_RXD1	
ENET_RXD<2>	E24	RGMII_RXD2	
ENET_RXD<3>	A24	RGMII_RXD3	
ENET_CLK125M_RXCLK	A23	RGMII_RXC/MII_RXCLK	
ENET_RX_CTRL	C22	RGMII_RXCTL/MII_RXDV	
=MCP_MII_RXER	F23	MII_RXER/GPIO_36	
=MCP_MII_COL	B26	MII_COL/GPIO_20/MSMB_DATA	
=MCP_MII_CRS	B22	MII_CRS/GPIO_21/MSMB_CLK	
TP_ENET_INTR_L	J22	RGMII_INTR/GPIO_35	
PP1V05_ENET_MCP_PLL_MAC (5 mA (A01))	T23	+V_DUAL_MACPLL	
MCP_MII_COMP_VDD	C27	MII_COMP_VDD	
MCP_MII_COMP_GND	B27	MII_COMP_GND	
TP_MCP_RGB_DAC_RSET	C39	RGB_DAC_RSET	
TP_MCP_RGB_DAC_VREF	B38	RGB_DAC_VREF	
MCP_TV_DAC_RSET	E36	TV_DAC_RSET	
MCP_TV_DAC_VREF	A35	TV_DAC_VREF	
MCP_CLK27M_XTALIN	C38	XTALIN_TV	
MCP_CLK27M_XTALOUT	D38	XTALOUT_TV	
LPCPLUS_GPIO	E16	GPIO_6/FERR*/IGPU_GPIO_6	
DP_IG_CA_DET	B15	GPIO_7/NFERR*/IGPU_GPIO_7	
LVDS_IG_BKL_PWM	G39	LCD_BKL_CTL/GPIO_57	(See below)
LVDS_IG_BKL_ON	E37	LCD_BKL_ON/GPIO_59	
LVDS_IG_PANEL_PWR	F40	LCD_PANEL_PWR/GPIO_58	
=MCP_HDMI_TXC_P	D35	HDMI_TXC_P/ML0_LANE3_P	
=MCP_HDMI_TXC_N	E35	HDMI_TXC_N/ML0_LANE3_N	
=MCP_HDMI_TXD_P<0>	G35	HDMI_TXD0_P/ML0_LANE2_P	
=MCP_HDMI_TXD_N<0>	F35	HDMI_TXD0_N/ML0_LANE2_N	
=MCP_HDMI_TXD_P<1>	F33	HDMI_TXD1_P/ML0_LANE1_P	
=MCP_HDMI_TXD_N<1>	G33	HDMI_TXD1_N/ML0_LANE1_N	
=MCP_HDMI_TXD_P<2>	J33	HDMI_TXD2_P/ML0_LANE0_P	
=MCP_HDMI_TXD_N<2>	H33	HDMI_TXD2_N/ML0_LANE0_N	
DP_IG_AUX_CH_P	D43	DP_AUX_CH0_P	
DP_IG_AUX_CH_N	C43	DP_AUX_CH0_N	
=DVI_HPD_GMUX_INT	C31	HPLUG_DET2/GPIO_22	(See below)
=MCP_HDMI_HPD	F31	HPLUG_DET3	
=PP3V3R1V8_S0_MCP_IFP_VDD (190 mA (A01, 1.8V))	M27	+VDD_IFPA	
	M26	+VDD_IFPB	
PP3V3_S0_MCP_VPLL (16 mA (A01))	M28	+V_PLL_IFPAB (8 mA)	
	M29	+V_PLL_HDMI (8 mA)	
=PP1V05_S0_MCP_HDMI_VDD (95 mA (A01))	T25	+VDD_HDMI	
MCP_HDMI_RSET	J31	HDMI_RSET	
MCP_HDMI_VPROBE	J30	HDMI_VPROBE	

+3.3V_DUAL_RMGT1	J24		
+3.3V_DUAL_RMGT2	K24		
+V_DUAL_RMGT1	U23		
+V_DUAL_RMGT2	V23		
MII_VREF	E28	MCP_MII_VREF	
RGMII_TXD0	B24	ENET_TXD<0>	
RGMII_TXD1	C24	ENET_TXD<1>	
RGMII_TXD2	C25	ENET_TXD<2>	
RGMII_TXD3	D25	ENET_TXD<3>	
RGMII_TXC/MII_TXCLK	D24	ENET_CLK125M_TXCLK	
RGMII_TXCTL/MII_TXEN	C26	ENET_TX_CTRL	
RGMII_MDC	D21	ENET_MDC	
RGMII_MDIO	C21	ENET_MDIO	
RGMII_PWRDWN/GPIO_37	G23	TP_ENET_PWRDWN_L	
BUF_25MHZ	E23	MCP_CLK25M_BUF0_R	
MII_RESET#	J23	ENET_RESET_L	
+V_RGB_DAC	J32	PP3V3_S0_MCP_DAC (103 mA)	206 mA (A01)
+V_TV_DAC	K32	(103 mA)	
DDC_CLK0	B31	MCP_DDC_CLK0	
DDC_DATA0	A31	MCP_DDC_DATA0	
RGB_DAC_RED	B39	TP_MCP_RGB_RED	
RGB_DAC_GREEN	A39	TP_MCP_RGB_GREEN	
RGB_DAC_BLUE	B40	TP_MCP_RGB_BLUE	
RGB_DAC_HSYNC	A40	TP_MCP_RGB_HSYNC	
RGB_DAC_VSYNC	A41	TP_MCP_RGB_VSYNC	
TV_DAC_RED	A36	CRT_IG_R_C_PR	
TV_DAC_GREEN	B36	CRT_IG_G_Y_Y	
TV_DAC_BLUE	C36	CRT_IG_B_COMP_PB	
TV_DAC_HSYNC/GPIO_44	D36	CRT_IG_HSYNC	
TV_DAC_VSYNC/GPIO_45	C37	CRT_IG_VSYNC	
IFPA_TXC_P	B35	LVDS_IG_A_CLK_P	
IFPA_TXC_N	C35	LVDS_IG_A_CLK_N	
IFPA_TXD0_P	B32	LVDS_IG_A_DATA_P<0>	
IFPA_TXD0_N	A32	LVDS_IG_A_DATA_N<0>	
IFPA_TXD1_P	D32	LVDS_IG_A_DATA_P<1>	
IFPA_TXD1_N	C32	LVDS_IG_A_DATA_N<1>	
IFPA_TXD2_P	D33	LVDS_IG_A_DATA_P<2>	
IFPA_TXD2_N	C33	LVDS_IG_A_DATA_N<2>	
IFPA_TXD3_P	B34	LVDS_IG_A_DATA_P<3>	
IFPA_TXD3_N	C34	LVDS_IG_A_DATA_N<3>	
IFPB_TXC_P	L31	LVDS_IG_B_CLK_P	
IFPB_TXC_N	K31	LVDS_IG_B_CLK_N	
IFPB_TXD4_P	J29	LVDS_IG_B_DATA_P<0>	
IFPB_TXD4_N	H29	LVDS_IG_B_DATA_N<0>	
IFPB_TXD5_P	L29	LVDS_IG_B_DATA_P<1>	
IFPB_TXD5_N	K29	LVDS_IG_B_DATA_N<1>	
IFPB_TXD6_P	L30	LVDS_IG_B_DATA_P<2>	
IFPB_TXD6_N	K30	LVDS_IG_B_DATA_N<2>	
IFPB_TXD7_P	N30	LVDS_IG_B_DATA_P<3>	
IFPB_TXD7_N	M30	LVDS_IG_B_DATA_N<3>	
DDC_CLK2/GPIO_23	C30	LVDS_IG_DDC_CLK	
DDC_DATA2/GPIO_24	B30	LVDS_IG_DDC_DATA	
DDC_CLK3	D31	=MCP_HDMI_DDC_CLK	
DDC_DATA3	E31	=MCP_HDMI_DDC_DATA	
IFPAB_RSET	E32	MCP_IFPAB_RSET	
IFPAB_VPROBE	G31	MCP_IFPAB_VPROBE	

R1850 10K 5% 1/16W MF-LF 402

R1810 49.9 1% 1/16W MF-LF 402
R1811 49.9 1% 1/16W MF-LF 402
R1820 47K 5% 1/16W MF-LF 402
R1860 100K 5% 1/16W MF-LF 402
R1861 100K 5% 1/16W MF-LF 402

=PP3V3_S0_MCP_GPIO

TV / Component
C / Pr
Y / Y
Comp / Pb

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

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MCP Ethernet & Graphics

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SIZE	DRAWING NUMBER	REV.
D	051-8071	8

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PCI

91 19	PCI_REQ0_L	T2	PCI_REQ0#		
91 19	PCI_REQ1_L	V9	PCI_REQ1#/FANRPM2		
19 OUT	CRTMUX_SEL_TV_L	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	PCI_GNT0#	R3
58 9 OUT	AUD_IPHS_SWITCH_EN	U9	PCI_REQ3#/GPIO_38/RS232_CTS#	PCI_GNT1#/FANCTL2	U10
19 IN	MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	PCI_GNT2#/GPIO_41/RS232_DTR#	R4
				PCI_GNT3#/GPIO_39/RS232_RTS#	U11
				PCI_GNT4#/GPIO_53/RS232_SOUT#	P3

TP_PCI_GNT0_L	7			MCP_RS232_SOUT_L	19 OUT
TP_PCI_GNT1_L	7				
GMUX_JTAG_TMS	OUT 9				
GMUX_JTAG_TDI	OUT 9				

91 13 B1	MCP_DEBUG<0>	AC3	PCI_AD0	PCI_CBE0#	AA3
91 13 B1	MCP_DEBUG<1>	AE10	PCI_AD1	PCI_CBE1#	AA6
91 13 B1	MCP_DEBUG<2>	AC4	PCI_AD2	PCI_CBE2#	AA11
91 13 B1	MCP_DEBUG<3>	AE11	PCI_AD3	PCI_CBE3#	W10
91 13 B1	MCP_DEBUG<4>	AB3	PCI_AD4		
91 13 B1	MCP_DEBUG<5>	AC6	PCI_AD5		
91 13 B1	MCP_DEBUG<6>	AB2	PCI_AD6		
91 13 B1	MCP_DEBUG<7>	AC7	PCI_AD7		
7	TP_PCI_AD<8>	AC8	PCI_AD8		
7	TP_PCI_AD<9>	AA2	PCI_AD9		
7	TP_PCI_AD<10>	AC9	PCI_AD10		
7	TP_PCI_AD<11>	AC10	PCI_AD11		
7	TP_PCI_AD<12>	AC11	PCI_AD12		
7	TP_PCI_AD<13>	AA1	PCI_AD13		
7	TP_PCI_AD<14>	AA5	PCI_AD14		
7	TP_PCI_AD<15>	Y5	PCI_AD15		
7	TP_PCI_AD<16>	W3	PCI_AD16		
7	TP_PCI_AD<17>	W6	PCI_AD17		
7	TP_PCI_AD<18>	W4	PCI_AD18		
7	TP_PCI_AD<19>	W7	PCI_AD19		
7	TP_PCI_AD<20>	V3	PCI_AD20		
7	TP_PCI_AD<21>	W8	PCI_AD21		
7	TP_PCI_AD<22>	V2	PCI_AD22		
7	TP_PCI_AD<23>	W9	PCI_AD23		
7	TP_PCI_AD<24>	U3	PCI_AD24		
7	TP_PCI_AD<25>	W11	PCI_AD25		
7	TP_PCI_AD<26>	U2	PCI_AD26		
7	TP_PCI_AD<27>	U5	PCI_AD27		
7	TP_PCI_AD<28>	U1	PCI_AD28		
7	TP_PCI_AD<29>	U6	PCI_AD29		
7	TP_PCI_AD<30>	T5	PCI_AD30		
7	TP_PCI_AD<31>	U7	PCI_AD31		

7	TP_PCI_INTW_L	P2	PCI_INTW#	PCI_FRAME#	AD4
7	TP_PCI_INTX_L	N3	PCI_INTX#	LPC_PWRDWN#/GPIO_54/EXT_NMI#	AE12
7	TP_PCI_INTY_L	N2	PCI_INTY#	LPC_RESET0#	AE5
7	TP_PCI_INTZ_L	N1	PCI_INTZ#		
7	TP_PCI_TRDY_L	Y3	PCI_TRDY#		
43 41 7 IN	PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42		
35 IN	FW_PME_L	AE2	LPC_DRQ1#/GPIO_19 Int PU		
7	TP_LPC_DRQ0_L	AE1	LPC_DRQ0# Int PU		
43 41 7 B1	LPC_SERIRQ	AE6	LPC_SERIRQ Int PU		

PCI_DEVSEL#	AA9		TP_PCI_DEVSEL_L	7	
PCI_FRAME#	Y4		TP_PCI_FRAME_L	7	
PCI_IRDY#	AA10		TP_PCI_IRDY_L	7	
PCI_PAR	Y1		TP_PCI_PAR	7	
PCI_PERR#/GPIO_43/RS232_DCD#	AB9		TP_PCI_PERR_L	7	
PCI_SERR#	AA7		TP_PCI_SERR_L	7	
PCI_STOP#	Y2		TP_PCI_STOP_L	7	
PCI_PME#/GPIO_30 Int PU (S5)	T1		PM_LATRIGGER_L	OUT 13	
PCI_RESET0#	R10		MEM_VTT_EN_R	OUT 25	
PCI_RESET1#	R11		TP_PCI_RESET1_L	7	
PCI_CLK0	R6		TP_PCI_CLK0	7	
PCI_CLK1	R7		TP_PCI_CLK1	7	
PCI_CLK2	R8	91	PCI_CLK33M_MCP_R		
PCI_CLKIN	R9	91	PCI_CLK33M_MCP		

R1910 22 5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

LPC

LPC_AD0	AD3		LPC_AD_R<0>	R1950 22 5% 1/16W MF-LF 402	LPC_AD<0> BI 7 41 43 84 91
LPC_AD1	AD2		LPC_AD_R<1>	R1951 22 5% 1/16W MF-LF 402	LPC_AD<1> BI 7 41 43 84 91
LPC_AD2	AD1		LPC_AD_R<2>	R1952 22 5% 1/16W MF-LF 402	LPC_AD<2> BI 7 41 43 84 91
LPC_AD3	AD5		LPC_AD_R<3>	R1953 22 5% 1/16W MF-LF 402	LPC_AD<3> BI 7 41 43 84 91
LPC_CLK0	AE9		LPC_CLK33M_SMC_R		OUT 25 91

LPC_FRAME#	AD4	43	LPC_FRAME_R_L	R1960 22 5% 1/16W MF-LF 402	LPC_FRAME_L OUT 7 41 43 84 91
LPC_PWRDWN#/GPIO_54/EXT_NMI#	AE12		LPC_PWRDWN_L		OUT 7 41 43
LPC_RESET0#	AE5		LPC_RESET_L		OUT 25 84 91

R1961 10K 5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

GND65	U24		GND98	Y26	
GND66	U26		GND99	Y27	
GND67	U39		GND100	AB18	
GND68	U4		GND101	H34	
GND69	U8		GND102	AB20	
GND70	V16		GND103	AB21	
GND71	V17		GND104	AB23	
GND72	V18		GND105	AB24	
GND73	V20		GND106	AB25	
GND74	V22		GND107	AB26	
GND75	V24		GND108	AB27	
GND76	V26		GND109	AB28	
GND77	V27		GND110	AB34	
GND78	V28		GND111	AB37	
GND79	V33		GND112	AB4	
GND80	V37		GND113	AB40	
GND81	V4		GND114	AC22	
GND82	V40		GND115	AC36	
GND83	V7		GND116	AC40	
GND84	W20		GND117	AB33	
GND85	W22		GND118	AC5	
GND86	W24		GND119	AD16	
GND87	W36		GND120	AD17	
GND88	W40		GND121	AD18	
GND89	W43		GND122	AD19	
GND90	Y16		GND123	AD20	
GND91	Y17		GND124	AD24	
GND92	Y18		GND125	AD25	
GND93	Y19		GND126	AD26	
GND94	Y20		GND127	AD27	
GND95	Y22		GND128	AD28	
GND96	Y24		GND129	AD33	
GND97	Y25		GND130	AD34	

21 18 8 =PP3V3_S0_MCP_GPIO

19	MCP_RS232_SOUT_L	R1989	8.2K	5% 1/16W MF-LF 402	
91 19	PCI_REQ0_L	R1990	8.2K	5% 1/16W MF-LF 402	
91 19	PCI_REQ1_L	R1991	8.2K	5% 1/16W MF-LF 402	
19	CRTMUX_SEL_TV_L	R1992	8.2K	5% 1/16W MF-LF 402	
19	MCP_RS232_SIN_L	R1994	8.2K	5% 1/16W MF-LF 402	

MCP PCI & LPC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE	SHT	OF
NONE	19	98

OMIT

U1400
MCP79-TOPO-B
BGA
(8 OF 11)

SATA

90 38 OUT	SATA_HDD_R2D_C_P	AJ7	SATA_A0_TX_P
90 38 OUT	SATA_HDD_R2D_C_N	AJ6	SATA_A0_TX_N
90 38 IN	SATA_HDD_D2R_N	AJ5	SATA_A0_RX_N
90 38 IN	SATA_HDD_D2R_P	AJ4	SATA_A0_RX_P
90 38 OUT	SATA_ODD_R2D_C_P	AJ11	SATA_A1_TX_P
90 38 OUT	SATA_ODD_R2D_C_N	AJ10	SATA_A1_TX_N
90 38 IN	SATA_ODD_D2R_N	AJ9	SATA_A1_RX_N
90 38 IN	SATA_ODD_D2R_P	AK9	SATA_A1_RX_P
7	TP_SATA_C_R2D_CP	AK2	SATA_B0_TX_P
7	TP_SATA_C_R2D_CN	AJ3	SATA_B0_TX_N
7	TP_SATA_C_D2RN	AJ2	SATA_B0_RX_N
7	TP_SATA_C_D2RP	AJ1	SATA_B0_RX_P
7	TP_SATA_D_R2D_CP	AM4	SATA_B1_TX_P
7	TP_SATA_D_R2D_CN	AL3	SATA_B1_TX_N
7	TP_SATA_D_D2RN	AL4	SATA_B1_RX_N
7	TP_SATA_D_D2RP	AK3	SATA_B1_RX_P
7	TP_SATA_E_R2D_CP	AN1	SATA_C0_TX_P
7	TP_SATA_E_R2D_CN	AM1	SATA_C0_TX_N
7	TP_SATA_E_D2RN	AM2	SATA_C0_RX_N
7	TP_SATA_E_D2RP	AM3	SATA_C0_RX_P
7	TP_SATA_F_R2D_CP	AP3	SATA_C1_TX_P
7	TP_SATA_F_R2D_CN	AP2	SATA_C1_TX_N
7	TP_SATA_F_D2RN	AN3	SATA_C1_RX_N
7	TP_SATA_F_D2RP	AN2	SATA_C1_RX_P
7	TP_MCP_SATALED_L	E12	SATA_LED#

23	PP1V05_S0_MCP_PLL_SATA	AE16	+V_PLL_SATA
	84 mA (A01)		
8	=PP1V05_S0_MCP_SATA_DVDD0		
	43 mA (A01, DVDD0 & 1)	AF19	+DVDD0_SATA1
		AG16	+DVDD0_SATA2
	Minimum 1.025V for Gen2 support	AG17	+DVDD0_SATA3
		AG19	+DVDD0_SATA4
9	=PP1V05_S0_MCP_SATA_DVDD1		
		AH17	+DVDD1_SATA1
		AH19	+DVDD1_SATA2
8	=PP1V05_S0_MCP_SATA_AVDD0		
	127 mA (A01, AVDD0 & 1)	AJ12	+AVDD0_SATA1
		AN11	+AVDD0_SATA2
	Minimum 1.025V for Gen2 support	AK12	+AVDD0_SATA3
		AK13	+AVDD0_SATA4
		AL12	+AVDD0_SATA5
		AM11	+AVDD0_SATA6
		AM12	+AVDD0_SATA7
		AN12	+AVDD0_SATA8
		AL13	+AVDD0_SATA9
9	=PP1V05_S0_MCP_SATA_AVDD1		
		AN14	+AVDD1_SATA1
		AL14	+AVDD1_SATA2
		AM13	+AVDD1_SATA3
		AM14	+AVDD1_SATA4
90	MCP_SATA_TERMP	AE3	SATA_TERMP

R2010
2.49K
1%
1/16W
MF-LF
402

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

USB

External A

USB0_P	C29	USB_EXTA_P	BI 39 91
USB0_N	D29	USB_EXTA_N	BI 39 91

AirPort (PCIe Mini-Card)

USB1_P	C28	USB_MINI_P	BI 9 91
USB1_N	D28	USB_MINI_N	BI 9 91

External D

USB2_P	A28	USB_EXTD_P	BI 9 91
USB2_N	B28	USB_EXTD_N	BI 9 91

Camera

USB3_P	F29	USB_CAMERA_P	BI 30 91
USB3_N	G29	USB_CAMERA_N	BI 30 91

IR

USB4_P	K27	USB_IR_P	BI 40 91
USB4_N	L27	USB_IR_N	BI 40 91

Geyser Trackpad/Keyboard

USB5_P	J26	USB_TPAD_P	BI 49 91
USB5_N	J27	USB_TPAD_N	BI 49 91

Bluetooth

USB6_P	F27	USB_BT_P	BI 30 91
USB6_N	G27	USB_BT_N	BI 30 91

External B

USB7_P	D27	USB_EXTB_P	BI 39 91
USB7_N	E27	USB_EXTB_N	BI 39 91

ExpressCard

USB8_P	K25	USB_EXCARD_P	BI 31 91
USB8_N	L25	USB_EXCARD_N	BI 31 91

External C

USB9_P	H25	USB_EXTC_P	BI 91 96 98
USB9_N	J25	USB_EXTC_N	BI 91 96 98

USB10_P	F25	TP_USB_10P	7
USB10_N	G25	TP_USB_10N	
USB11_P	K23	TP_USB_11P	7
USB11_N	L23	TP_USB_11N	7

USB_OC0#/GPIO_25	L21	USB_EXTA_OC_L	IN 39
USB_OC1#/GPIO_26	K21	USB_EXTB_OC_L	IN 39
USB_OC2#/GPIO_27/MGPIO	J21	USB_EXTC_OC_L	IN 98
USB_OC3#/GPIO_28/MGPIO	H21	EXCARD_OC_L	IN 31 42

+V_PLL_USB	L28	PP3V3_S0_MCP_PLL_USB	23
		19 mA (A01)	
USB_RBIAS_GND	A27	91 MCP_USB_RBIAS_GND	

R2060
806
1%
1/16W
MF-LF
402

GND131	AD35	
GND132	AD37	
GND133	AD38	
GND134	AE22	
GND135	AE24	
GND136	AE39	
GND137	AE4	
GND138	AD6	
GND139	AF16	
GND140	AF17	
GND141	AF18	
GND142	AF20	
GND143	AF22	
GND144	AF26	
GND145	AF27	
GND146	AF28	
GND147	AF33	
GND148	AF34	
GND149	AF37	
GND150	AF40	
GND151	AG18	
GND152	AG20	
GND153	AG22	
GND154	AG26	
GND155	AG36	
GND156	AG40	
GND157	AH18	
GND158	AH20	
GND159	AH22	
GND160	AH24	

=PP3V3_S5_MCP_GPIO 8 18

R2051
8.2K
5%
1/16W
MF-LF
402

R2053
8.2K
5%
1/16W
MF-LF
402

R2050
8.2K
5%
1/16W
MF-LF
402

R2052
8.2K
5%
1/16W
MF-LF
402

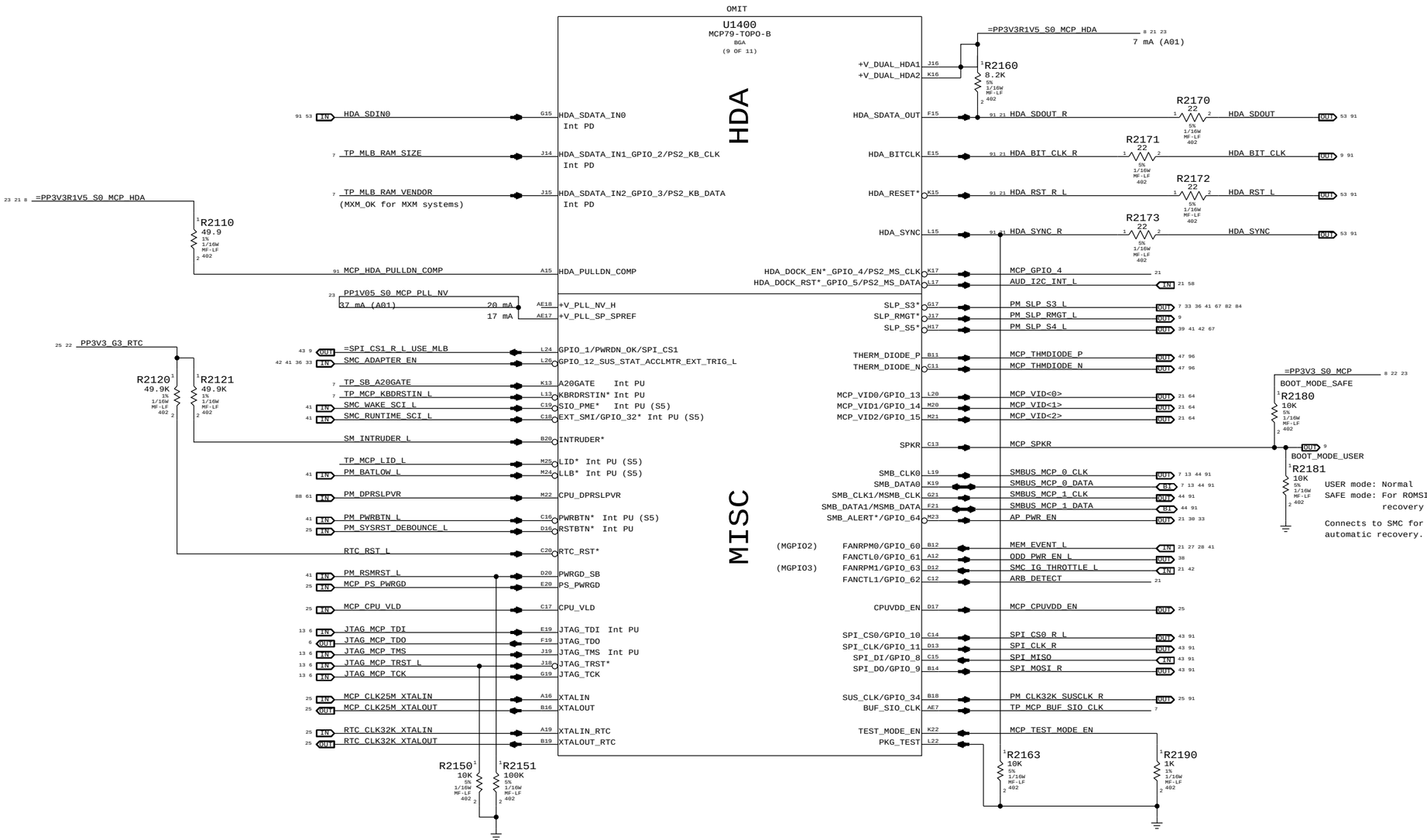
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

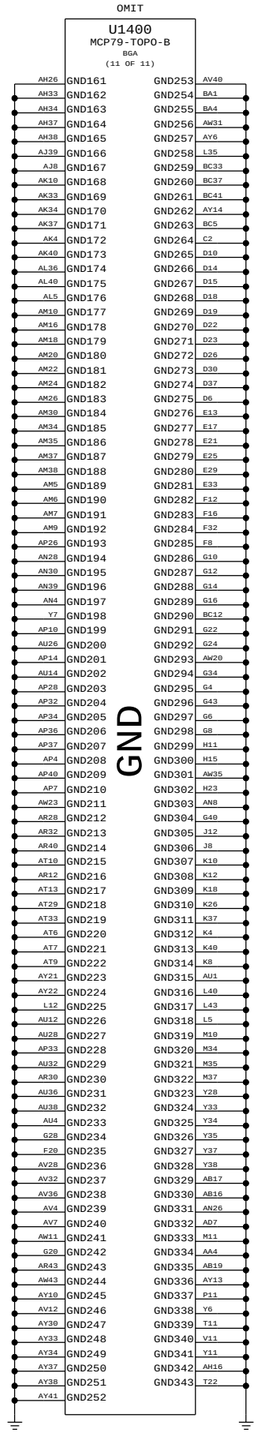
MCP SATA & USB

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

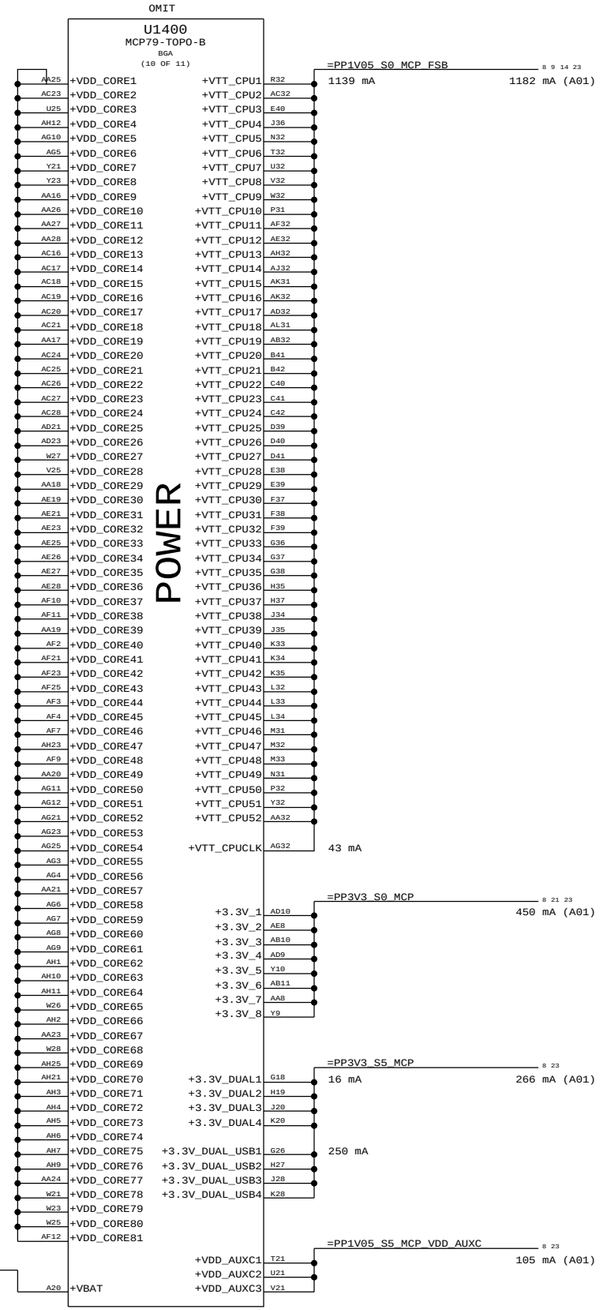
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 20 OF 98	





45 23 8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)



25 21 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

MCP Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT	OF
NONE	22	98

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Core Power

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)

45 22 8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

(No IG vs. EG data)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power

8 =PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)

C2515 4.7UF 20% 4V X5R 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power

8 =PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power

22 8 =PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)

C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power

18 8 =PP1V05_ENET_MCP_RMGT
131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

22 14 9 8 =PP1V05_S0_MCP_FSB
1182 mA (A01)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power

16 8 =PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

22 21 8 =PP3V3_S0_MCP
450 mA (A01)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

22 8 =PP3V3_S5_MCP
266 mA (A01)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

21 8 =PP3V3R1V5_S0_MCP_HDA
7 mA (A01)

C2562 2.2UF 20% 6.3V CERM 402-LF

8 =PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)

L2595 30-OHM-1.7A 0402
C2595 4.7UF 20% 4V X5R 402
C2596 2.2UF 20% 6.3V CERM 402-LF
PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
18
5 mA (A01)

L2555

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

8 =PP3V3_S0_MCP_PLL_UF
19 mA (A01)

L2555 30-OHM-1.7A 0402
PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
20
19 mA (A01)
C2555 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

23 18 8 =PP3V3_ENET_MCP_RMGT
83 mA (A01)

C2564 2.2UF 20% 6.3V CERM 402-LF

MCP79 Ethernet VRef

23 18 8 =PP3V3_ENET_MCP_RMGT
R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402
MCP_MII_VREF
MUX
18
C2591 0.1UF 20% 10V CERM 402

L2570

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

8 =PP1V05_S0_MCP_AVDD_UF
333 mA (A01)

L2570 30-OHM-5A 0603
C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF
PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
8
206 mA (A01)

L2575

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

L2575 30-OHM-5A 0603
C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF
PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
8
127 mA (A01)

L2582

8 =PP1V05_S0_MCP_PLL_PEX_UF

L2582 30-OHM-1.7A 0402
C2582 4.7UF 20% 4V X5R 402
C2583 2.2UF 20% 6.3V CERM 402-LF
PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
17
84 mA (A01)

R2580

66 8 =PP1V05_S0_MCP_PLL_UF
562 mA (A01)

R2580 0.2 1% 1/5W MF 402-HF
C2580 4.7UF 20% 4V X5R 402
C2581 2.2UF 10% 16V X5R 603
PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
14
270 mA (A01)

L2584

L2584 30-OHM-1.7A 0402
C2584 4.7UF 20% 4V X5R 402
C2585 2.2UF 20% 6.3V CERM 402-LF
PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
20
84 mA (A01)

L2586

L2586 30-OHM-1.7A 0402
C2586 4.7UF 20% 4V X5R 402
C2587 2.2UF 20% 6.3V CERM 402-LF
PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
16
87 mA (A01)

L2588

L2588 30-OHM-1.7A 0402
C2588 4.7UF 20% 4V X5R 402
C2589 2.2UF 20% 6.3V CERM 402-LF
C2590 0.1UF 20% 10V CERM 402
PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
21
37 mA (A01)

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE D | DRAWING NUMBER 051-8071 | REV. 8
SCALE NONE | SHT 23 OF 98

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

18 8 =PP3V3R1V8_S0_MCP_IFP_VDD
190 mA (A01, 1.8V)

C2610 2.2UF 20% 6.3V CERM 402-LF

18 8 =PP1V05_S0_MCP_HDMI_VDD
95 mA (A01)

C2615 4.7UF 20% 4V X5R 402
C2616 2.2UF 20% 6.3V CERM 402-LF

90 18 MCP_HDMI_RSET
90 18 MCP_HDMI_VPROBE

NO STUFF C2620 0.1UF 20% 10V CERM 402
R2620 1K 1% 1/16W MF-LF 402

90 18 MCP_IFPAB_RSET
90 18 MCP_IFPAB_VPROBE

NO STUFF C2630 0.1UF 20% 10V CERM 402
NO STUFF R2630 1K 1% 1/16W MF-LF 402

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???

8 =PP3V3_S0_MCP_VPLL_UF
16 mA (A01)

L2640 30-OHM-1.7A 0402

PP3V3_S0_MCP_VPLL 18
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
16 mA (A01)

C2640 4.7UF 20% 6.3V CERM 603
C2641 2.2UF 20% 6.3V CERM 402-LF

HDCP ROM

WF: Open question on which packge option(s) nVidia can support.

8 =PP3V3_S0_HDCPROM

NO STUFF C2690 0.1UF 20% 10V CERM 402
NO STUFF R2690 10K 5% 1/16W MF-LF 402

U2695 AT24C08 SOIC
A0 A1 A2 GND VCC SDA SCL WP

=I2C_HDCPROM_SDA
=I2C_HDCPROM_SCL
HDCPROM_WP

NO STUFF L2650 30-OHM-1.7A 0402

8 =PP3V3_S0_MCP_DAC_UF
206 mA (A01)

NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

PP3V3_S0_MCP_DAC 18
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
206 mA (A01)

NO STUFF C2650 2.2UF 20% 6.3V CERM 402-LF
R2651 0 5% 1/10W MF-LF 402

18 TP_MCP_RGB_RED — NC_MCP_RGB_RED
18 TP_MCP_RGB_GREEN — NC_MCP_RGB_GREEN
18 TP_MCP_RGB_BLUE — NC_MCP_RGB_BLUE
18 TP_MCP_RGB_HSYNC — NC_MCP_RGB_HSYNC
18 TP_MCP_RGB_VSYNC — NC_MCP_RGB_VSYNC
90 18 CRT_IG_R_C_PR — NC_CRT_IG_R_C_PR
90 18 CRT_IG_G_Y_Y — NC_CRT_IG_G_Y_Y
90 18 CRT_IG_B_COMP_PB — NC_CRT_IG_B_COMP_PB
90 18 CRT_IG_HSYNC — NC_CRT_IG_HSYNC
90 18 CRT_IG_VSYNC — NC_CRT_IG_VSYNC
18 TP_MCP_RGB_DAC_RSET — NC_MCP_RGB_DAC_RSET
18 TP_MCP_RGB_DAC_VREF — NC_MCP_RGB_DAC_VREF
90 18 MCP_TV_DAC_RSET — NC_MCP_TV_DAC_RSET
90 18 MCP_TV_DAC_VREF — NC_MCP_TV_DAC_VREF
18 MCP_CLK27M_XTALIN — NC_MCP_CLK27M_XTALIN
18 MCP_CLK27M_XTALOUT — NC_MCP_CLK27M_XTALOUT

(MAKE_BASE=TRUE, NO_TEST=TRUE)

Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

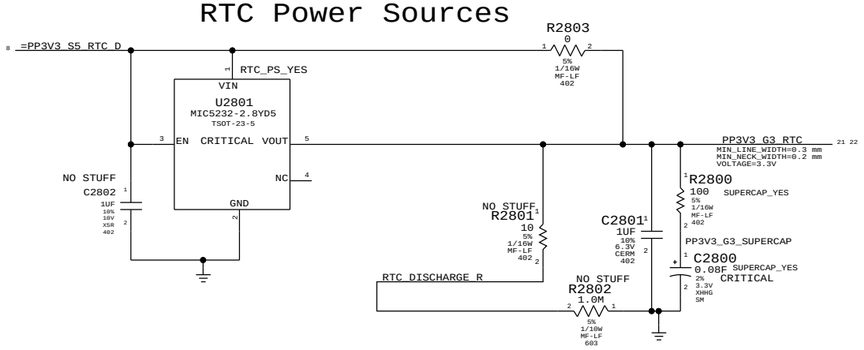
MCP Graphics Support

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

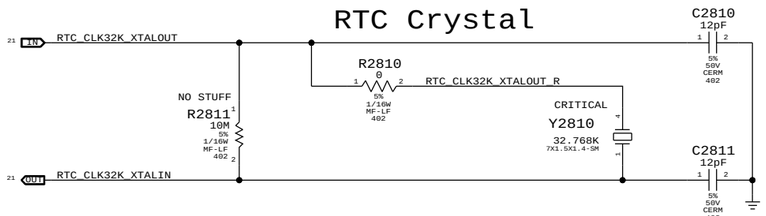
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 24 OF 98	

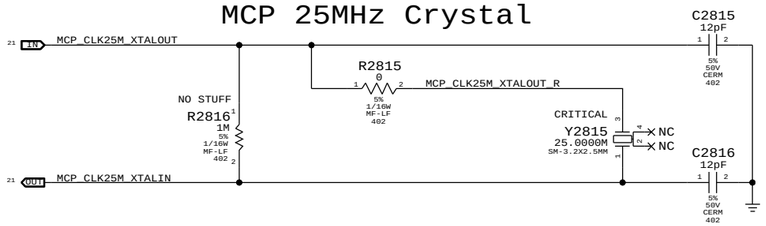
RTC Power Sources



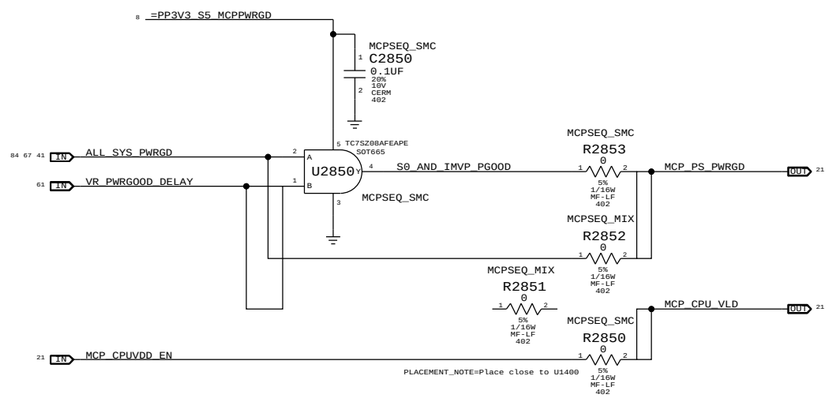
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

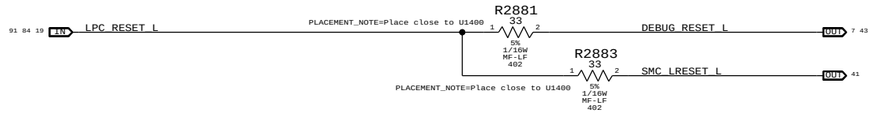
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

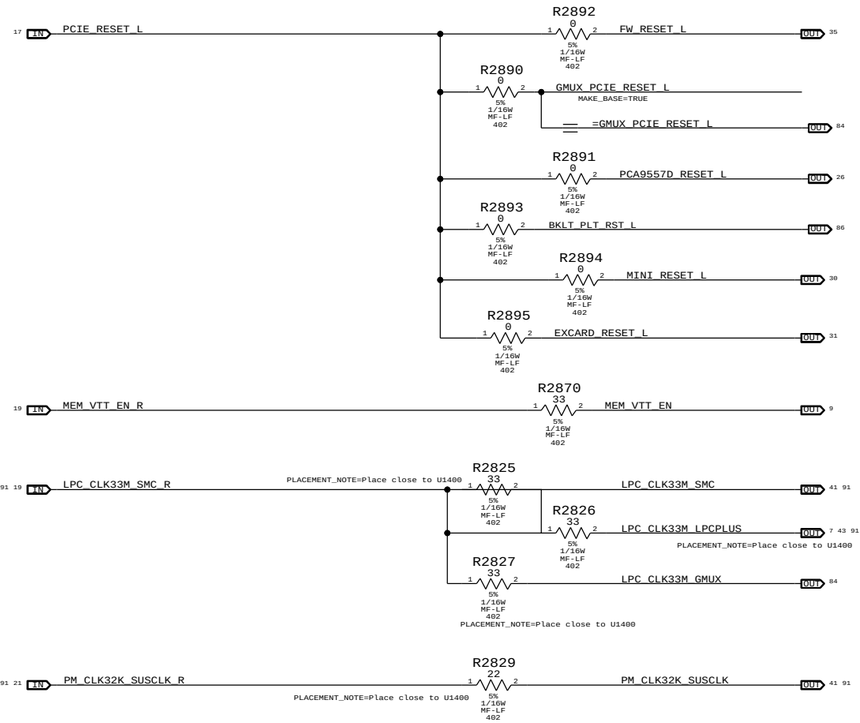
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Platform Reset Connections

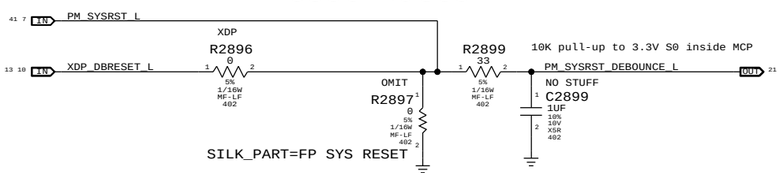
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



Reset Button



SB Misc		
SYNC_MASTER=M98_MLB		SYNC_DATE=05/01/2008

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-8071	B
	SCALE: NONE	SHT 25 OF 98	

Page Notes

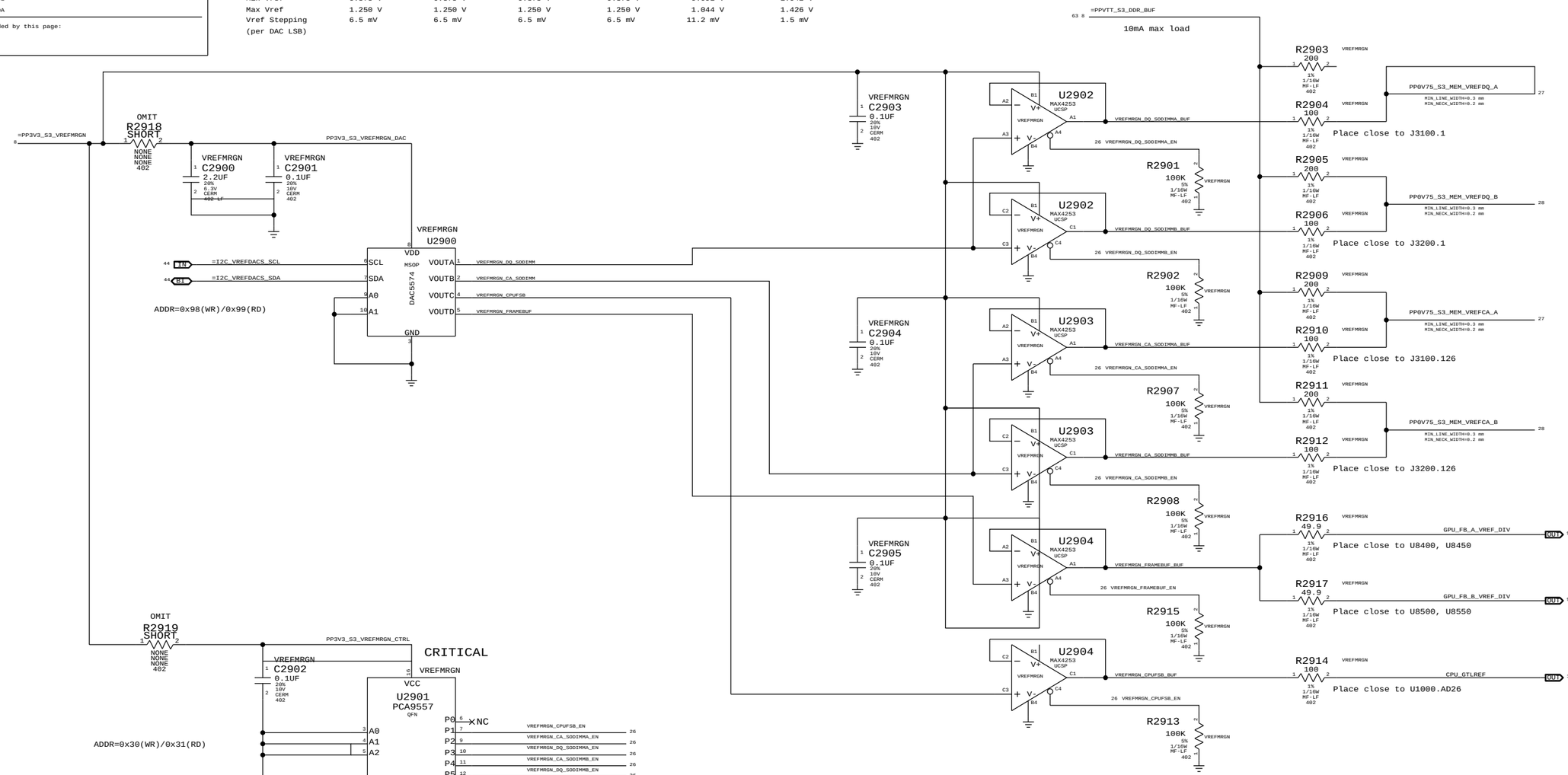
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel	MEM A VREF DQ A	MEM A VREF CA B	MEM B VREF DQ A	MEM B VREF CA B	CPU FSB VREF C	FRAME BUFFER VREF D
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55	0xFF
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining

SYNC_MASTER=BEN_K20 SYNC_DATE=10/15/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 26 OF 98	

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

8 =PP1V5_S0_MEM_A

8 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603

C3101 10UF 20% 6.3V X5R 603

C3110 C3111 C3112 C3113 C3114 C3115 C3116 C3117 C3118 C3119 C3120 C3121 C3122 C3123 0.1UF 20% 10V CERM 402

26 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF

C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-THB

DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)

KEY

73	CKE0		74	CKE1		MEM_A_CKE<1>	IN 15 89
75	VDD		76	VDD			
77	NC	×NC	78	A15		MEM_A_A<15>	IN 9
79	BA2		80	A14		MEM_A_A<14>	IN 15 89
81	VDD		82	VDD			
83	A12/BC*		84	A11		MEM_A_A<11>	IN 15 89
85	A9		86	A7		MEM_A_A<7>	IN 15 89
87	VDD		88	VDD			
89	A8		90	A6		MEM_A_A<6>	IN 15 89
91	A5		92	A4		MEM_A_A<4>	IN 15 89
93	VDD		94	VDD			
95	A3		96	A2		MEM_A_A<2>	IN 15 89
97	A1		98	A0		MEM_A_A<0>	IN 15 89
99	VDD		100	VDD			
101	CK0		102	CK1		MEM_A_CLK_P<1>	IN 15 89
103	CK0*		104	CK1*		MEM_A_CLK_N<1>	IN 15 89
105	VDD		106	VDD			
107	A10/AP		108	BA1		MEM_A_BA<1>	IN 15 89
109	BA0		110	RAS*		MEM_A_RAS_L	IN 15 89
111	VDD		112	VDD			
113	WE*		114	S0*		MEM_A_CS_L<0>	IN 15 89
115	CAS*		116	ODT0		MEM_A_ODT<0>	IN 15 89
117	VDD		118	VDD			
119	A13		120	ODT1		MEM_A_ODT<1>	IN 15 89
121	S1*		122	NC	×NC		
123	VDD		124	VDD			
125	TEST		126	VREFCA			
127	VSS		128	VSS			
129	DQ32		130	DQ36		MEM_A_DQ<36>	BI 15 89
131	DQ33		132	DQ37		MEM_A_DQ<37>	BI 15 89
133	VSS		134	VSS			
135	DQS4*		136	DM4		MEM_A_DM<4>	IN 15 89
137	DQS4		138	VSS			
139	VSS		140	DQ38		MEM_A_DQ<38>	BI 15 89
141	DQ34		142	DQ39		MEM_A_DQ<39>	BI 15 89
143	DQ35		144	VSS			
145	VSS		146	DQ44		MEM_A_DQ<47>	BI 15 89
147	DQ40		148	DQ45		MEM_A_DQ<40>	BI 15 89
149	DQ41		150	VSS			
151	VSS		152	DQS5*		MEM_A_DQS_N<5>	BI 15 89
153	DM5		154	DQS5		MEM_A_DQS_P<5>	BI 15 89
155	VSS		156	VSS			
157	DQ42		158	DQ46		MEM_A_DQ<46>	BI 15 89
159	DQ43		160	DQ47		MEM_A_DQ<43>	BI 15 89
161	VSS		162	VSS			
163	DQ48		164	DQ52		MEM_A_DQ<48>	BI 15 89
165	DQ49		166	DQ53		MEM_A_DQ<53>	BI 15 89
167	VSS		168	VSS			
169	DQS6*		170	DM6		MEM_A_DM<6>	IN 15 89
171	DQS6		172	VSS			
173	VSS		174	DQ54		MEM_A_DQ<50>	BI 15 89
175	DQ50		176	DQ55		MEM_A_DQ<49>	BI 15 89
177	DQ51		178	VSS			
179	VSS		180	DQ60		MEM_A_DQ<57>	BI 15 89
181	DQ56		182	DQ61		MEM_A_DQ<56>	BI 15 89
183	DQ57		184	VSS			
185	VSS		186	DQS7*		MEM_A_DQS_N<7>	BI 15 89
187	DM7		188	DQS7		MEM_A_DQS_P<7>	BI 15 89
189	VSS		190	VSS			
191	DQ58		192	DQ62		MEM_A_DQ<62>	BI 15 89
193	DQ59		194	DQ63		MEM_A_DQ<63>	BI 15 89
195	VSS		196	VSS			
197	SA0		198	EVENT*		MEM_EVENT_L	OUT 21 28 41
199	VDDSPD		200	SDA		=I2C_SODIMMA_SDA	BI 44
201	SA1		202	SCL		=I2C_SODIMMA_SCL	IN 44
203	VTT		204	VTT		=PP0V75_S0_MEM_VTT_A	8

516-0201

SPD ADDR=0xA0(WR)/0xA1(RD)

8 =PPSPD_S0_MEM_A

C3140 2.2UF 10% 6.3V CERM 402-LF

R3140 10K 5% 1/16W MF-LF 402

R3141 10K 5% 1/16W MF-LF 402

MEM_A_SA<0>

MEM_A_SA<1>

J3100 F-RT-THB

DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)

CRITICAL

KEY

1	VREFDQ		2	VSS			
3	VSS		4	DQ4		MEM_A_DQ<4>	BI 15 89
5	DQ0		6	DQ5		MEM_A_DQ<5>	BI 15 89
7	DQ1		8	VSS			
9	VSS		10	DQS0*		MEM_A_DQS_N<0>	BI 15 89
11	DM0		12	DQS0		MEM_A_DQS_P<0>	BI 15 89
13	VSS		14	VSS			
15	DQ2		16	DQ6		MEM_A_DQ<6>	BI 15 89
17	DQ3		18	DQ7		MEM_A_DQ<7>	BI 15 89
19	VSS		20	VSS			
21	DQ8		22	DQ12		MEM_A_DQ<8>	BI 15 89
23	DQ9		24	DQ13		MEM_A_DQ<12>	BI 15 89
25	VSS		26	VSS			
27	DQS1*		28	DM1		MEM_A_DM<1>	IN 15 89
29	DQS1		30	RESET*	L	MEM_RESET_L	IN 28 29
31	VSS		32	VSS			
33	DQ10		34	DQ14		MEM_A_DQ<15>	BI 15 89
35	DQ11		36	DQ15		MEM_A_DQ<10>	BI 15 89
37	VSS		38	VSS			
39	DQ16		40	DQ20		MEM_A_DQ<21>	BI 15 89
41	DQ17		42	DQ21		MEM_A_DQ<20>	BI 15 89
43	VSS		44	VSS			
45	DQS2*		46	DM2		MEM_A_DM<2>	IN 15 89
47	DQS2		48	VSS			
49	VSS		50	DQ22		MEM_A_DQ<17>	BI 15 89
51	DQ18		52	DQ23		MEM_A_DQ<22>	BI 15 89
53	DQ19		54	VSS			
55	VSS		56	DQ28		MEM_A_DQ<29>	BI 15 89
57	DQ24		58	DQ29		MEM_A_DQ<28>	BI 15 89
59	DQ25		60	VSS			
61	VSS		62	DQS3*		MEM_A_DQS_N<3>	BI 15 89
63	DM3		64	DQS3		MEM_A_DQS_P<3>	BI 15 89
65	VSS		66	VSS			
67	DQ26		68	DQ30		MEM_A_DQ<26>	BI 15 89
69	DQ27		70	DQ31		MEM_A_DQ<31>	BI 15 89
71	VSS		72	VSS			

516-0201

PP0V75_S3_MEM_VREFCA_A 26

C3135 2.2UF 20% 6.3V CERM 402-LF

C3136 0.1UF 20% 10V CERM 402

=PP0V75_S0_MEM_VTT_A 8

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=BEN_K20 SYNC_DATE=06/10/2009

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 27 OF 98	

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PP5PO_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

8 =PP1V5_S0_MEM_B
8 =PP1V5_S3_MEM_B

C3210 0.1UF 20% 10V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 0.1UF 20% 10V CERM 402
C3213 0.1UF 20% 10V CERM 402
C3214 0.1UF 20% 10V CERM 402
C3215 0.1UF 20% 10V CERM 402
C3216 0.1UF 20% 10V CERM 402
C3217 0.1UF 20% 10V CERM 402
C3218 0.1UF 20% 10V CERM 402
C3219 0.1UF 20% 10V CERM 402
C3220 0.1UF 20% 10V CERM 402
C3221 0.1UF 20% 10V CERM 402
C3222 0.1UF 20% 10V CERM 402
C3223 0.1UF 20% 10V CERM 402

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603

26 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 F-RT-BGA3 DDR3-SODIMM (2 OF 2)

73	CKE0		74	CKE1	MEM_B_CKE<1>
75	VDD		76	VDD	
77	NC		78	A15	MEM_B_A<15>
79	BA2	MEM_B_BA<2>	80	A14	MEM_B_A<14>
81	VDD		82	VDD	
83	A12/BC*	MEM_B_A<12>	84	A11	MEM_B_A<11>
85	A9	MEM_B_A<9>	86	A7	MEM_B_A<7>
87	VDD		88	VDD	
89	A8	MEM_B_A<8>	90	A6	MEM_B_A<6>
91	A5	MEM_B_A<5>	92	A4	MEM_B_A<4>
93	VDD		94	VDD	
95	A3	MEM_B_A<3>	96	A2	MEM_B_A<2>
97	A1	MEM_B_A<1>	98	A0	MEM_B_A<0>
99	VDD		100	VDD	
101	CK0	MEM_B_CLK_P<0>	102	CK1	MEM_B_CLK_P<1>
103	CK0*	MEM_B_CLK_N<0>	104	CK1*	MEM_B_CLK_N<1>
105	VDD		106	VDD	
107	A10/AP	MEM_B_A<10>	108	BA1	MEM_B_BA<1>
109	BA0	MEM_B_BA<0>	110	RAS*	MEM_B_RAS_L
111	VDD		112	VDD	
113	WE*	MEM_B_WE_L	114	S0*	MEM_B_CS_L<0>
115	CAS*	MEM_B_CAS_L	116	ODT0	MEM_B_ODT<0>
117	VDD		118	VDD	
119	A13	MEM_B_A<13>	120	ODT1	MEM_B_ODT<1>
121	S1*	MEM_B_CS_L<1>	122	NC	
123	VDD		124	VDD	
125	TEST		126	VREFCA	
127	VSS		128	VSS	
129	DQ32	MEM_B_DQ<32>	130	DQ36	MEM_B_DQ<33>
131	DQ33	MEM_B_DQ<37>	132	DQ37	MEM_B_DQ<36>
133	VSS		134	VSS	
135	DQS4*	MEM_B_DQS_N<4>	136	DM4	MEM_B_DM<4>
137	DQS4	MEM_B_DQS_P<4>	138	VSS	
139	VSS		140	DQ38	MEM_B_DQ<38>
141	DQ34	MEM_B_DQ<34>	142	DQ39	MEM_B_DQ<39>
143	DQ35	MEM_B_DQ<35>	144	VSS	
145	VSS		146	DQ44	MEM_B_DQ<44>
147	DQ40	MEM_B_DQ<41>	148	DQ45	MEM_B_DQ<45>
149	DQ41	MEM_B_DQ<40>	150	VSS	
151	VSS		152	DQS5*	MEM_B_DQS_N<5>
153	DM5	MEM_B_DM<5>	154	DQS5	MEM_B_DQS_P<5>
155	VSS		156	VSS	
157	DQ42	MEM_B_DQ<43>	158	DQ46	MEM_B_DQ<47>
159	DQ43	MEM_B_DQ<42>	160	DQ47	MEM_B_DQ<46>
161	VSS		162	VSS	
163	DQ48	MEM_B_DQ<55>	164	DQ52	MEM_B_DQ<48>
165	DQ49	MEM_B_DQ<49>	166	DQ53	MEM_B_DQ<54>
167	VSS		168	VSS	
169	DQS6*	MEM_B_DQS_N<6>	170	DM6	MEM_B_DM<6>
171	DQS6	MEM_B_DQS_P<6>	172	VSS	
173	VSS		174	DQ54	MEM_B_DQ<53>
175	DQ50	MEM_B_DQ<52>	176	DQ55	MEM_B_DQ<50>
177	DQ51	MEM_B_DQ<51>	178	VSS	
179	VSS		180	DQ60	MEM_B_DQ<60>
181	DQ56	MEM_B_DQ<56>	182	DQ61	MEM_B_DQ<61>
183	DQ57	MEM_B_DQ<57>	184	VSS	
185	VSS		186	DQS7*	MEM_B_DQS_N<7>
187	DM7	MEM_B_DM<7>	188	DQS7	MEM_B_DQS_P<7>
189	VSS		190	VSS	
191	DQ58	MEM_B_DQ<63>	192	DQ62	MEM_B_DQ<58>
193	DQ59	MEM_B_DQ<59>	194	DQ63	MEM_B_DQ<62>
195	VSS		196	VSS	
197	SA0	MEM_B_SA<0>	198	EVENT*	MEM_EVENT_L
199	VDDSPD		200	SDA	=I2C_SODIMMB_SDA
201	SA1	MEM_B_SA<1>	202	SCL	=I2C_SODIMMB_SCL
203	VTT		204	VTT	=PP0V75_S0_MEM_VTT_B
205	MTG PIN		206	MTG PIN	
207	MTG PIN		208	MTG PIN	
209	MTG PIN		210	MTG PIN	
211	MTG PIN		212	MTG PIN	

KEY
MTG PINS
516s0706
SPD ADDR=0xA2(WR)/0xA3(RD)

R3240 10K 5% 1/16W MF-LF 402
R3241 10K 5% 1/16W MF-LF 402
C3240 2.2UF 20% 6.3V CERM 402-LF
8 =PPSPD_S0_MEM_B

J3200 F-RT-BGA3 DDR3-SODIMM (1 OF 2) CRITICAL

1	VREFDQ		2	VSS	
3	VSS		4	DQ4	MEM_B_DQ<4>
5	DQ0	MEM_B_DQ<0>	6	DQ5	MEM_B_DQ<5>
7	DQ1	MEM_B_DQ<1>	8	VSS	
9	VSS		10	DQS0*	MEM_B_DQS_N<0>
11	DM0	MEM_B_DM<0>	12	DQS0	MEM_B_DQS_P<0>
13	VSS		14	VSS	
15	DQ2	MEM_B_DQ<2>	16	DQ6	MEM_B_DQ<6>
17	DQ3	MEM_B_DQ<3>	18	DQ7	MEM_B_DQ<7>
19	VSS		20	VSS	
21	DQ8	MEM_B_DQ<28>	22	DQ12	MEM_B_DQ<29>
23	DQ9	MEM_B_DQ<24>	24	DQ13	MEM_B_DQ<25>
25	VSS		26	VSS	
27	DQS1*	MEM_B_DQS_N<3>	28	DM1	MEM_B_DM<3>
29	DQS1	MEM_B_DQS_P<3>	30	RESET*	MEM_RESET_L
31	VSS		32	VSS	
33	DQ10	MEM_B_DQ<31>	34	DQ14	MEM_B_DQ<26>
35	DQ11	MEM_B_DQ<30>	36	DQ15	MEM_B_DQ<27>
37	VSS		38	VSS	
39	DQ16	MEM_B_DQ<9>	40	DQ20	MEM_B_DQ<13>
41	DQ17	MEM_B_DQ<8>	42	DQ21	MEM_B_DQ<12>
43	VSS		44	VSS	
45	DQS2*	MEM_B_DQS_N<1>	46	DM2	MEM_B_DM<1>
47	DQS2	MEM_B_DQS_P<1>	48	VSS	
49	VSS		50	DQ22	MEM_B_DQ<14>
51	DQ18	MEM_B_DQ<15>	52	DQ23	MEM_B_DQ<11>
53	DQ19	MEM_B_DQ<10>	54	VSS	
55	VSS		56	DQ28	MEM_B_DQ<20>
57	DQ24	MEM_B_DQ<21>	58	DQ29	MEM_B_DQ<16>
59	DQ25	MEM_B_DQ<17>	60	VSS	
61	VSS		62	DQS3*	MEM_B_DQS_N<2>
63	DM3	MEM_B_DM<2>	64	DQS3	MEM_B_DQS_P<2>
65	VSS		66	VSS	
67	DQ26	MEM_B_DQ<18>	68	DQ30	MEM_B_DQ<19>
69	DQ27	MEM_B_DQ<22>	70	VSS	MEM_B_DQ<23>
71	VSS		72	VSS	

KEY
516s0706

26 PP0V75_S3_MEM_VREFCA_B
C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

SYNC_MASTER=BEN_K20 SYNC_DATE=07/14/2009

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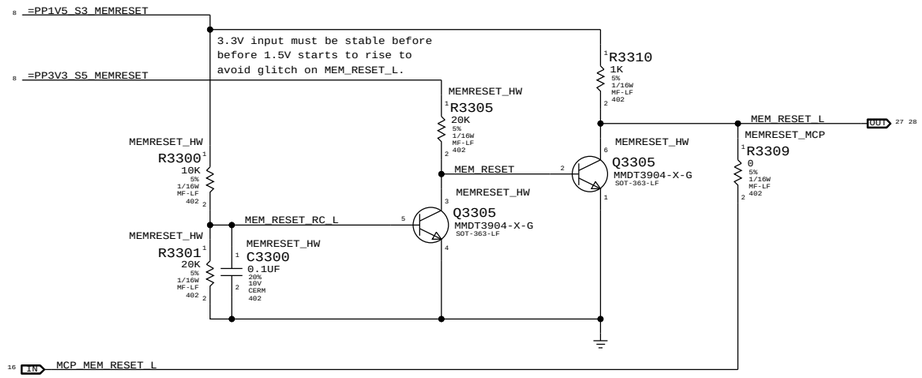
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 28 OF 98	

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



DDR3 Support			
SYNC_MASTER=M98_MLB		SYNC_DATE=04/01/2008	
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APPLE INC.	SIZE D	DRAWING NUMBER 051-8071	REV. 8
	SCALE NONE	SHT 29 OF 98	

AIRPORT

ALS CAMERA

BLUETOOTH

PCIE_MINI_PRSNT_L
Q3401 SSM6N15FEAPE SOT563
AP_PWR_EN
MINI_CLKREQ_L
Q3401 SSM6N15FEAPE SOT563

5V S3 WLAN FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM

PCIE_MINI_D2R_P
PCIE_MINI_D2R_N
PCIE_MINI_R2D_P
PCIE_MINI_R2D_N
PCIE_CLK100M_MINI_CONN_P
PCIE_CLK100M_MINI_CONN_N
MINI_CLKREQ_O_L
PCIE_WAKE_L
NC

C3431 0.1uF 10% 16V X5R 402
C3430 0.1uF 10% 16V X5R 402
PLACEMENT_NOTE=Place close to J3401.
1000 mA peak
750 mA nominal max
PCIE_MINI_R2D_C_P
PCIE_MINI_R2D_C_N
PP5V_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

L3401 90-OHM-100MA DLP11S
PCIE_CLK100M_MINI_P
PCIE_CLK100M_MINI_N

L3404 FERR-120-OHM-1.5A 0402-LF
C3422 0.1uF 20% 10V CERM 402
C3421 0.1uF 20% 10V CERM 402
C3420 10UF 20% 10V X5R 805
PP5V_WLAN_F
R3404 0 5% 1/10W MF-LF 603
PP5V_WLAN_R
PLACEMENT_NOTE=Place close to J3401.
PLACEMENT_NOTE=Place close to Q3450.

Q3450 FDC606P_G SOT-6
C3450 0.1UF 10% 16V X5R 402
C3451 0.033UF 10% 16V X5R 402
R3450 100K 5% 1/16W MF-LF 402
R3451 10K 5% 1/16W MF-LF 402
P5VWLAN_SS
=PP5V_S3_WLAN
PM_WLAN_EN_L

L3405 FERR-120-OHM-1.5A 0402-LF
C3452 0.1uF 20% 10V CERM 402
275 mA peak
206 mA nominal max
PP3V3_S3_BT_F
=PP5V_S3_BTCAMERA
PP5V_S3_BTCAMERA_F
I2C_ALS_SDA
I2C_ALS_SCL

L3406 FERR-120-OHM-1.5A 0402-LF
C3462 0.1uF 20% 10V CERM 402
=PP3V3_S3_BT

USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
L3402 90-OHM DLP0NS
USB_CAMERA_P
USB_CAMERA_N
PLACEMENT_NOTE=Place close to J3401.

CONN_USB2_BT_P
CONN_USB2_BT_N
L3403 90-OHM DLP0NS
USB_BT_P
USB_BT_N
PLACEMENT_NOTE=Place close to J3401.

=PP3V3_S3_WLAN
PP5V_WLAN_F
U3402 74LVC1G17DRL SOT-553
U3401 TC7SZ08AFEAPE SOT665
MINI_RESET_CONN_L
WLAN_SMIT_BUF
MINI_RESET_L
R3453 33K 5% 1/16W MF-LF 402
R3454 62K 5% 1/16W MF-LF 402
R3455 1 5% 1/10W MF-LF 402
C3453 1UF 10% 6.3V CERM 402
WLAN_SMIT_RC
WLAN_SMIT_RC_FET
Q3402 SSM3K15FV SOD-VESM-HF

Right Clutch Connector
SYNC_MASTER=M98_MLB
SYNC_DATE=05/01/2008
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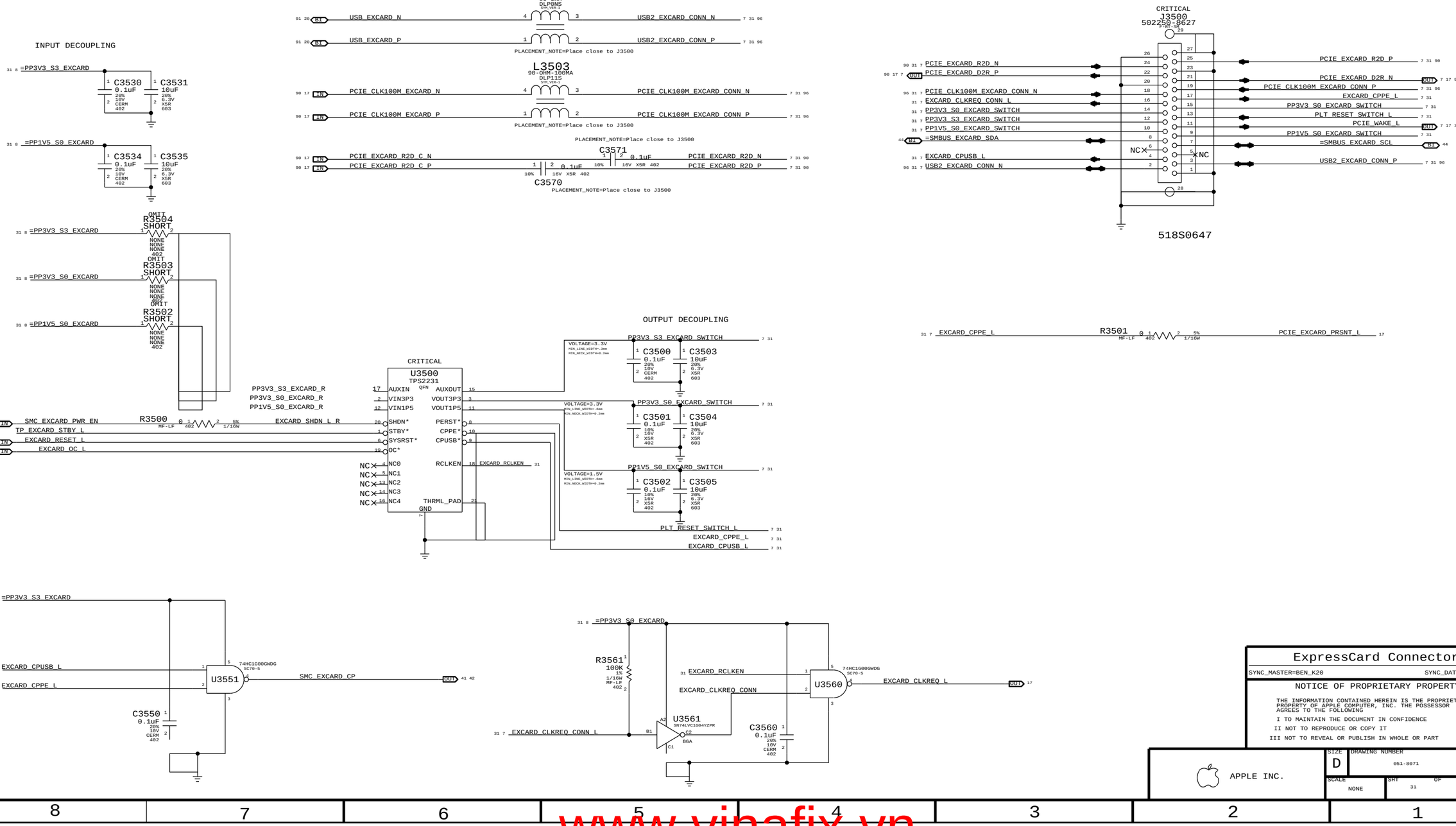
APPLE INC.
SIZE D
DRAWING NUMBER 051-8071
REV. 8
SCALE NONE
SHT 30 OF 98

EXPRESSCARD/34 FLEX CONNECTOR



ExpressCard Connector

SYNC_MASTER=BEN_K20 SYNC_DATE=10/15/2008

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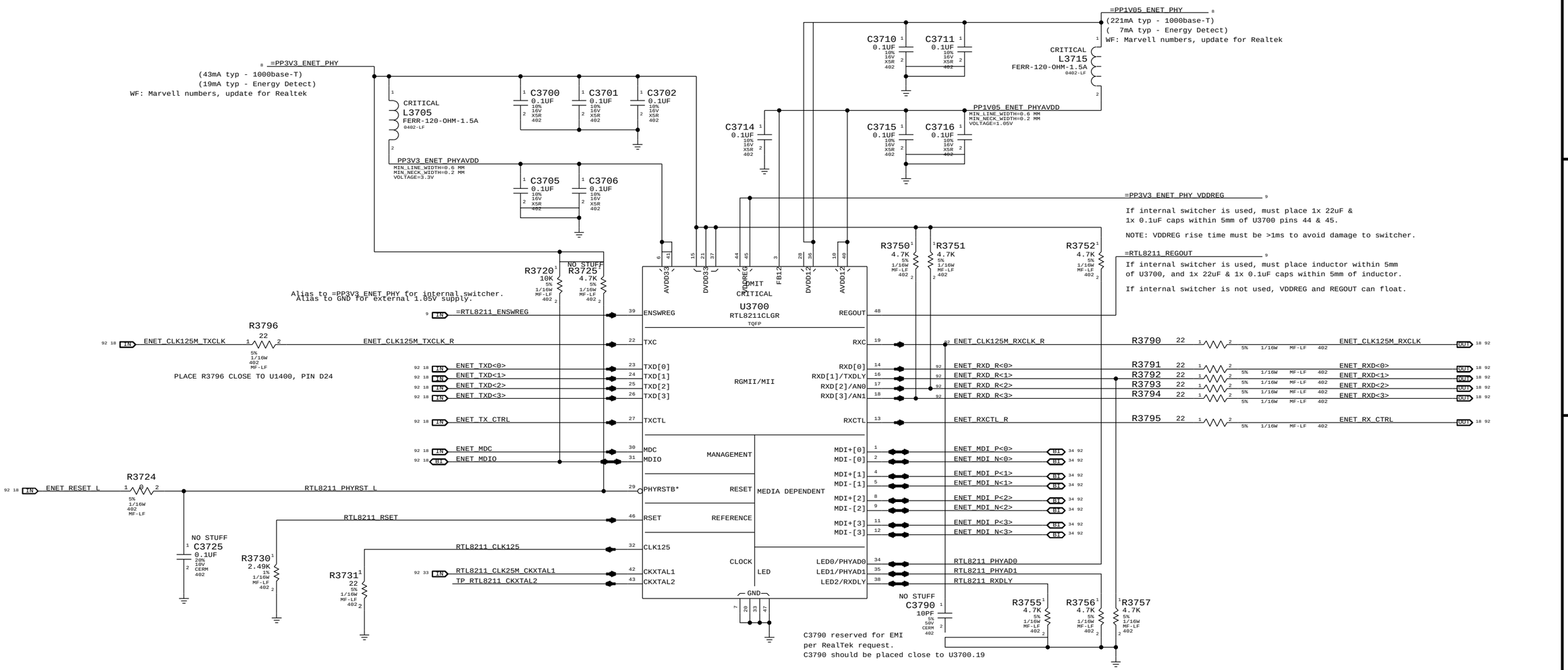
SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 31 OF 98	



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/22/2008

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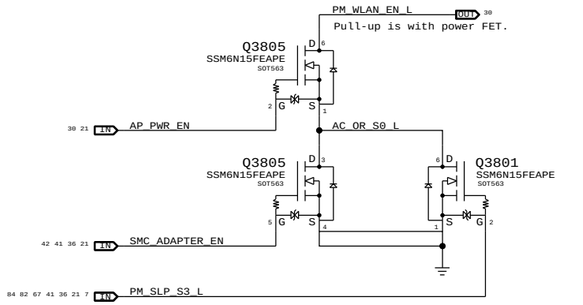
D	051-8071	B
SCALE: NONE	SHT 32 OF 98	

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

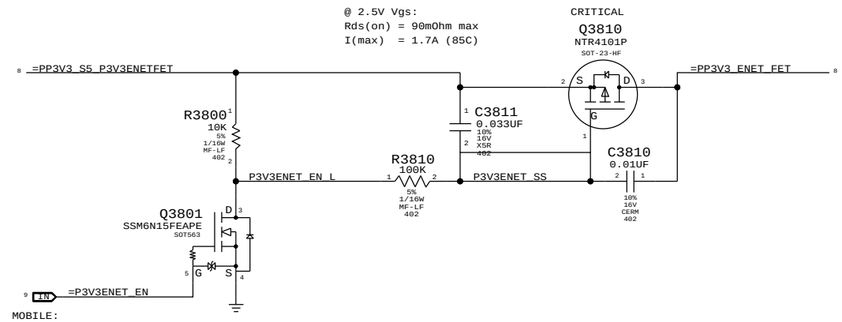
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

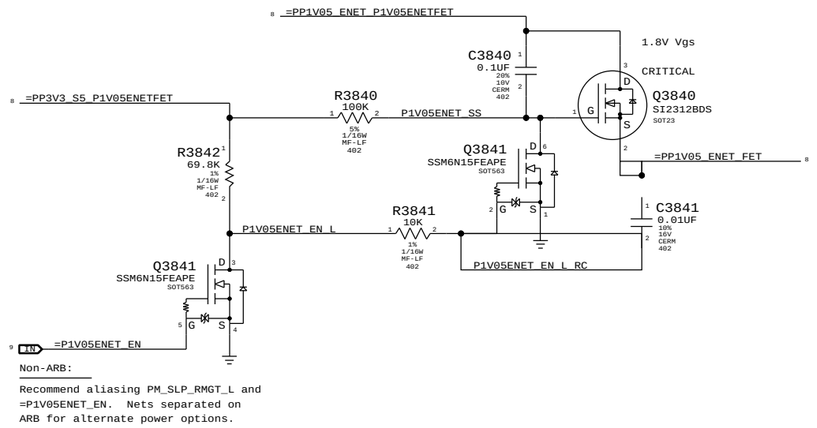
CRITICAL



MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

1.05V ENET FET



Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

PLACEMENT_NOTE=Place close to U1400

Ethernet & AirPort Support

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

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APPLE INC.

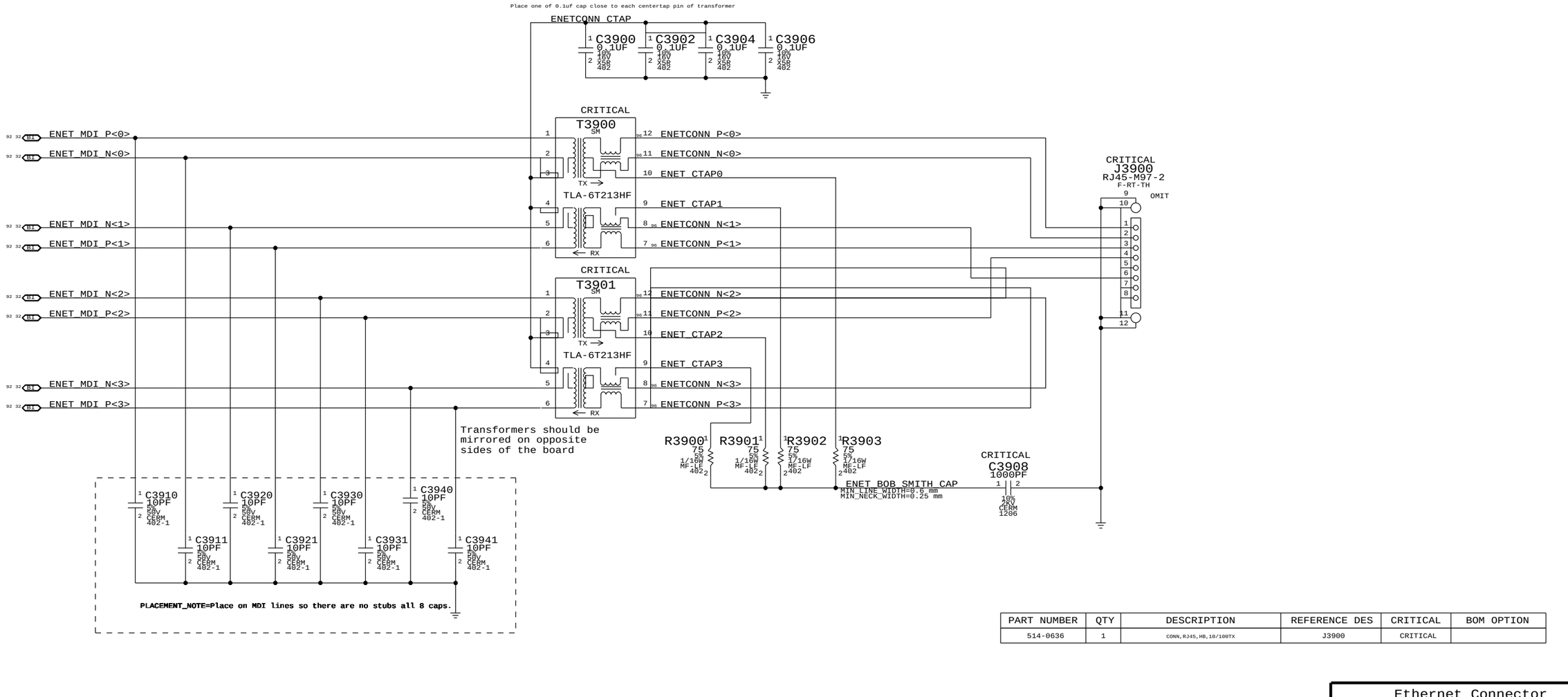
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 33 OF 98	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0636	1	CONN,RJ45,HB,10/100TX	J3900	CRITICAL	

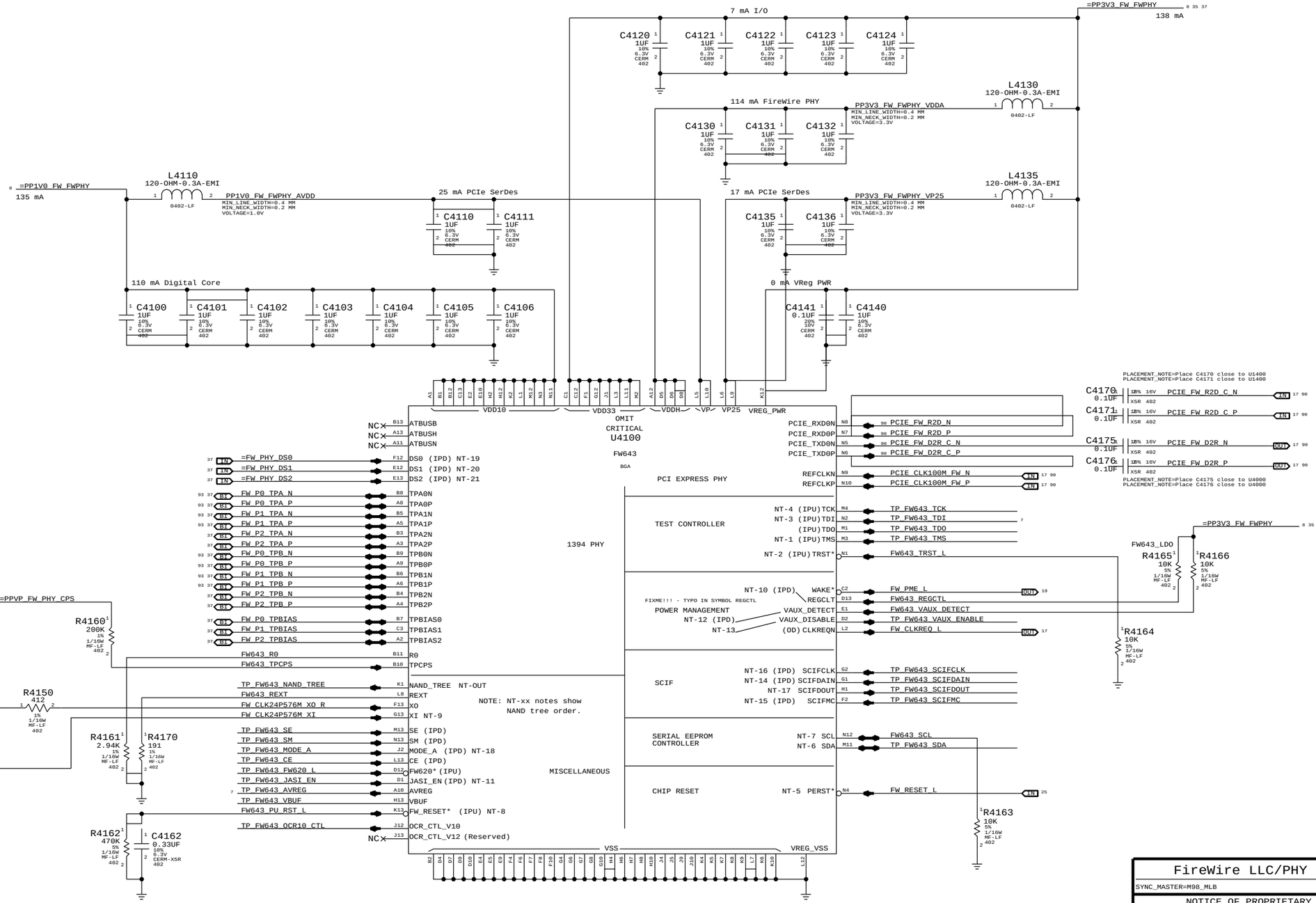
Ethernet Connector

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

APPLE INC.

SIZE D | DRAWING NUMBER 051-8071 | REV. 8

SCALE NONE | SHT 34 OF 98



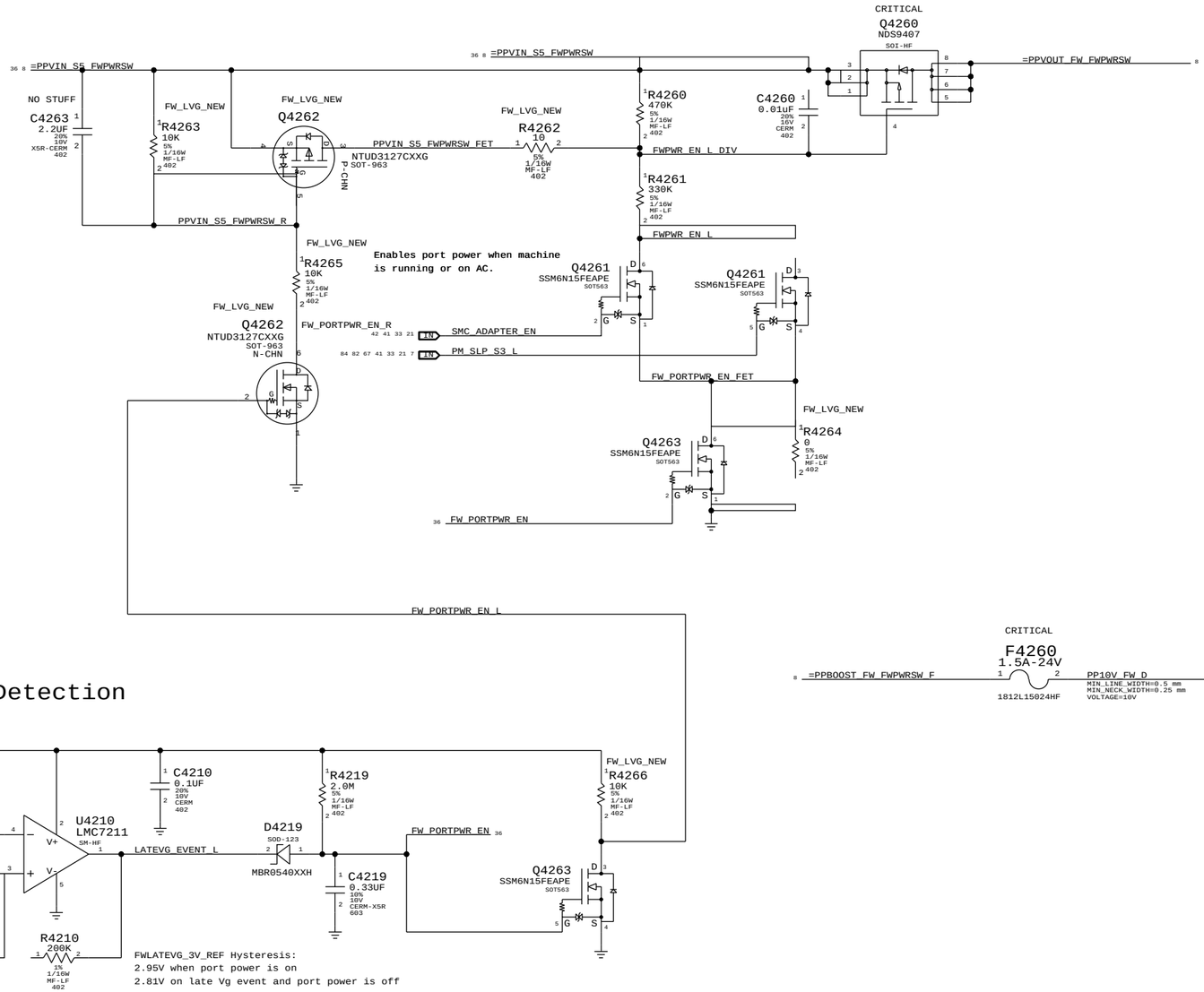
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection

FireWire Port Power

SYNC_MASTER=YWU_K20 SYNC_DATE=05/28/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT 36 OF 98	
NONE		

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

37 35 8 =PP3V3_FW_FWPHY

R4382 10K 1% 1/16W MF-LF 402

R4380 10K 1% 1/16W MF-LF 402

FWPHY_DS0 MAKE_BASE=TRUE — =FW_PHY_DS0 (35)

FWPHY_DS2 MAKE_BASE=TRUE — =FW_PHY_DS2 (35)

FWPHY_DS1 MAKE_BASE=TRUE — =FW_PHY_DS1 (35)

R4381 10K 1% 1/16W MF-LF 402

35	FW_P0_TPBIAS	NC_FW0_TPBIAS	MAKE_BASE=TRUE
35	FW_P2_TPBIAS	NC_FW2_TPBIAS	MAKE_BASE=TRUE (7)
93 35	FW_P0_TPA_N	NC_FW0_TPAN	MAKE_BASE=TRUE
93 35	FW_P0_TPA_P	NC_FW0_TPAP	MAKE_BASE=TRUE (7)
35	FW_P2_TPA_N	NC_FW2_TPAN	MAKE_BASE=TRUE (7)
35	FW_P2_TPA_P	NC_FW2_TPAP	MAKE_BASE=TRUE (7)
93 35	FW_P0_TPB_N	NC_FW0_TPBN	MAKE_BASE=TRUE
93 35	FW_P0_TPB_P	NC_FW0_TPBP	MAKE_BASE=TRUE (7)
35	FW_P2_TPB_N	NC_FW2_TPBN	MAKE_BASE=TRUE (7)
35	FW_P2_TPB_P	NC_FW2_TPBP	MAKE_BASE=TRUE (7)

Termination

Place close to FireWire PHY

35 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 6.3V CERM-X5R 402

SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402

R4361 56.2 1% 1/16W MF-LF 402

93 35	FW_P1_TPA_P	FW_PORT1_TPA_P MAKE_BASE=TRUE (37)
93 35	FW_P1_TPA_N	FW_PORT1_TPA_N MAKE_BASE=TRUE (37)
93 35	FW_P1_TPB_P	FW_PORT1_TPB_P MAKE_BASE=TRUE (37)
93 35	FW_P1_TPB_N	FW_PORT1_TPB_N MAKE_BASE=TRUE (37)

SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402

R4363 56.2 1% 1/16W MF-LF 402

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

8 =PPVP_FW_PHY_CPS_FET

Q4300 (SYM_VER_1) BSS8402DW

PPVP_FW_CPS MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=10V — MAKE_BASE=TRUE — =PPVP_FW_PHY_CPS (35)

R4311 470K 5% 1/16W MF-LF 402

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

Q4300 BSS8402DW SOT-363 (SYM-VER1)

37 35 8 =PP3V3_FW_FWPHY

"Snapback" & "Late VG" Protection

37 36 PP2V4_FW_LATEVG

DP4310 BAV99DW-X-G SOT-363

C4311 0.01uF 10% 50V X7R 402

C4310 0.01uF 10% 50V X7R 402

DP4311 BAV99DW-X-G SOT-363

C4312 0.01uF 10% 50V X7R 402

C4313 0.01uF 10% 50V X7R 402

37 FW_PORT1_TPB_N

37 FW_PORT1_TPB_P

37 FW_PORT1_TPA_N

37 FW_PORT1_TPA_P

C4319 0.1uF 10% 50V X7R 603-1

R4319 1M 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

Cable Power

8 =PPVP_FW_PORT1

CRITICAL L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

PORT 1

BILINGUAL

CRITICAL J4310 1394B-M97 F-RT-TH

1	TPB-	TPB(R)	TPB- / TPB<R>
9	TPB+	VP	TPB+ / VP
8			VP
7	NC	SC/NC	NC
6			VG
3	TPA-	VG	TPA- / TPA<R>
5			
4	TPA+	TPA(R)	TPA+
10			
11			
12	CHASSIS GND		
13			

OUTPUT

INPUT

(FW_PORT1_BREF)

(GND_FW_PORT1_VG)

FW_PORT1_AREF

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

514S0605

Late-VG Protection Power

8 =PP3V3_FW_LATEVG

R4390 332 1% 1/16W MF-LF 402

PP2V4_FW_LATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V (36 37)

CRITICAL D4390 MMBZ5227BLT1H SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

FireWire Ports

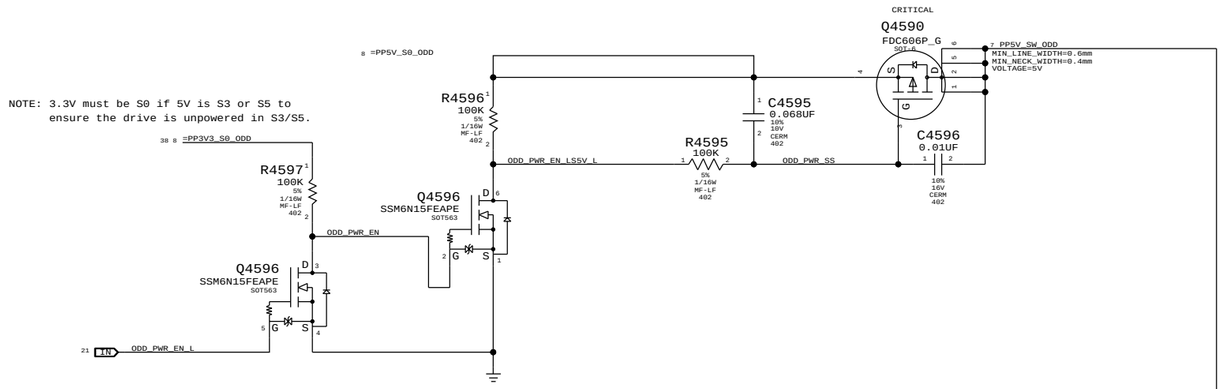
SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

APPLE INC.

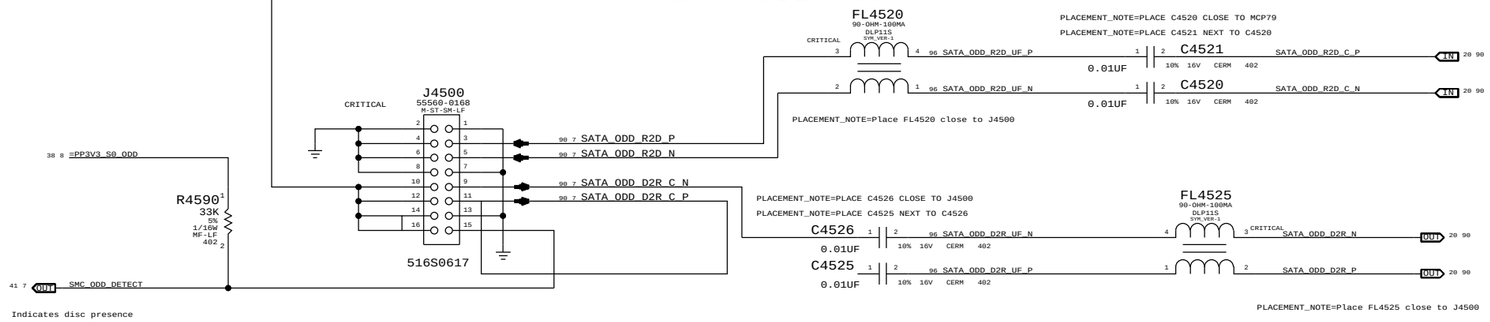
SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE: NONE — SHT 37 OF 98

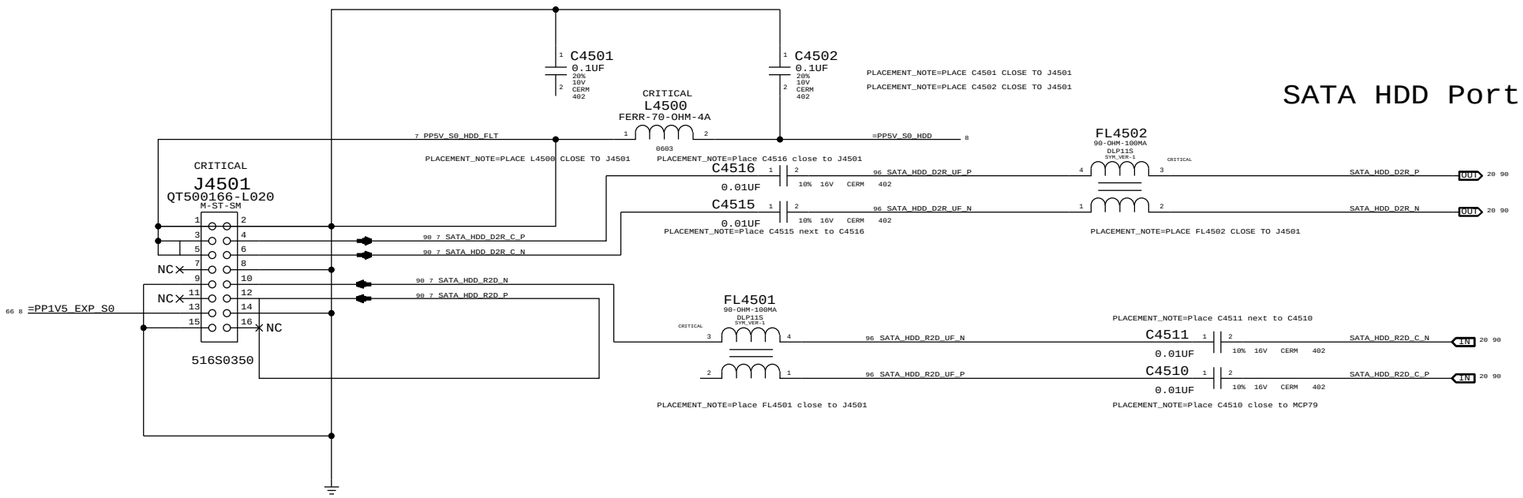
ODD Power Control



SATA ODD Port



SATA HDD Port



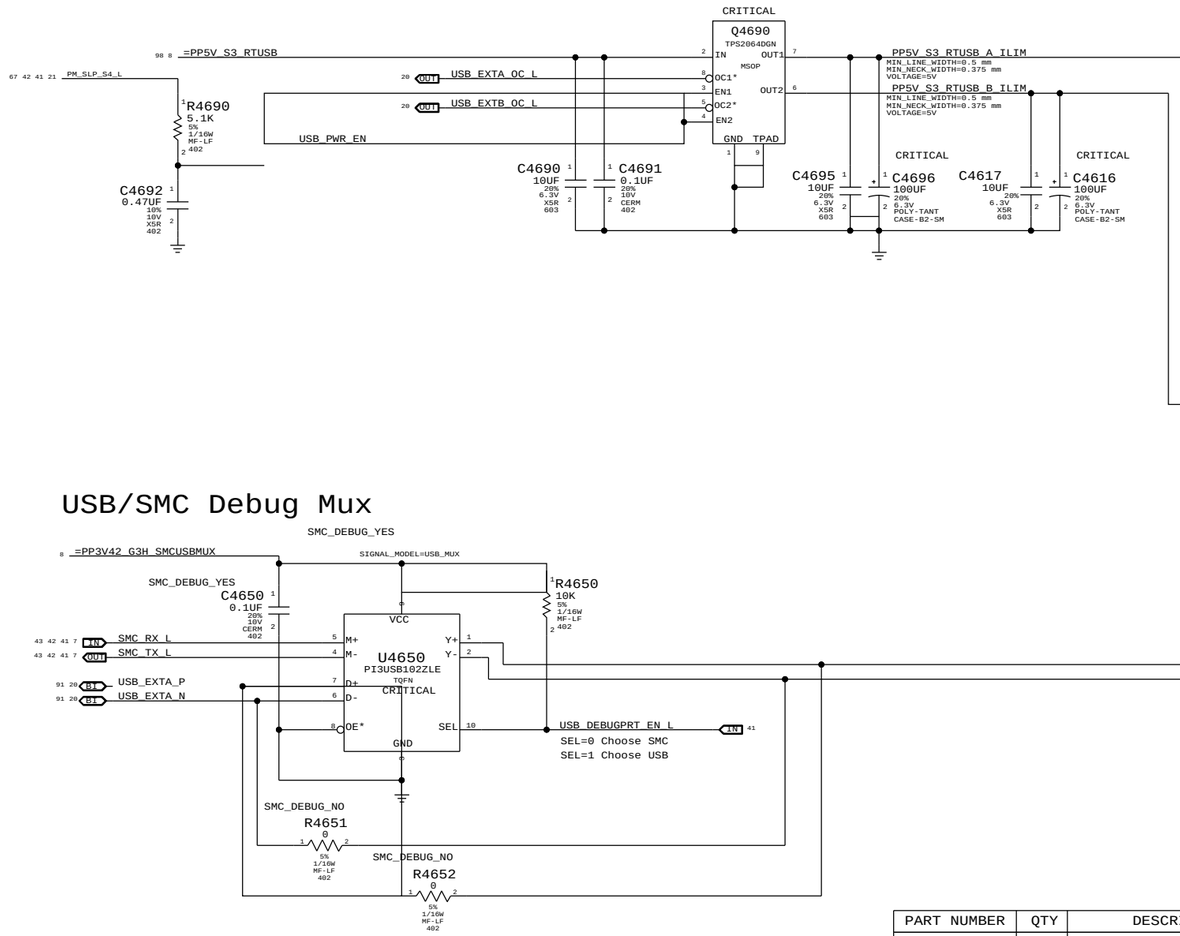
SATA Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

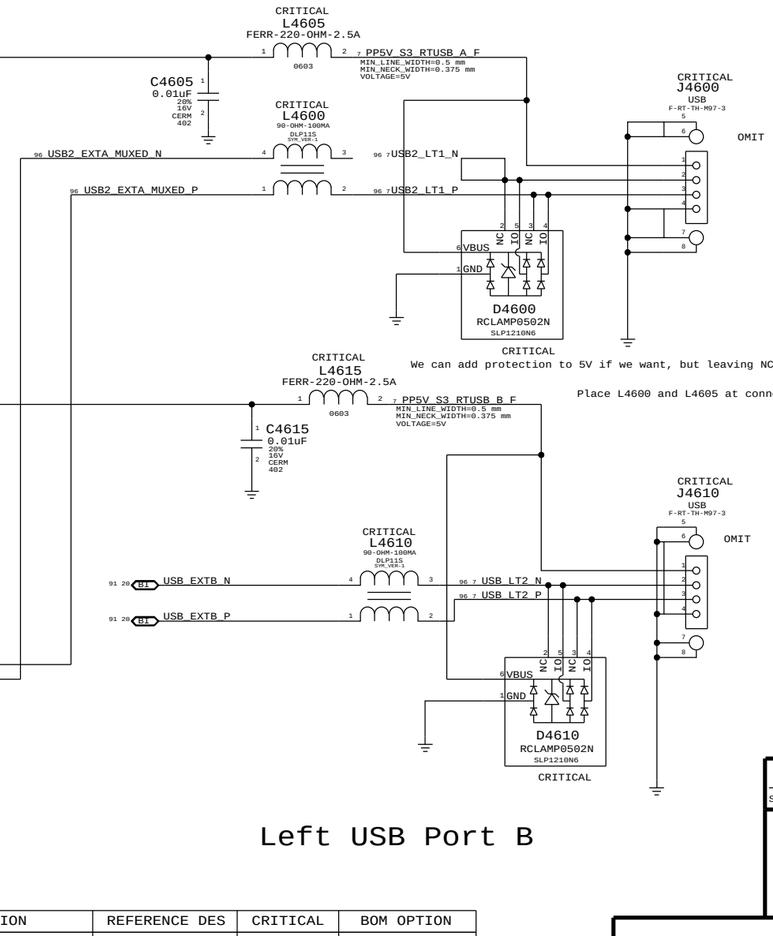
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 38 OF 98	

Port Power Switch



Left USB Port A



USB/SMC Debug Mux

Left USB Port B

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0638	2	CONN,RCPT,USB,HB,4P	J4600, J4610	CRITICAL	

External USB Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

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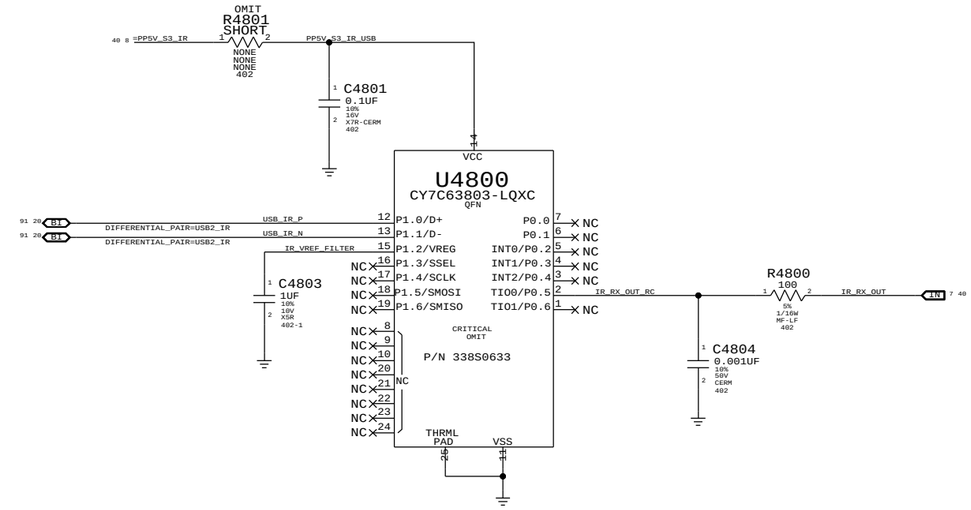
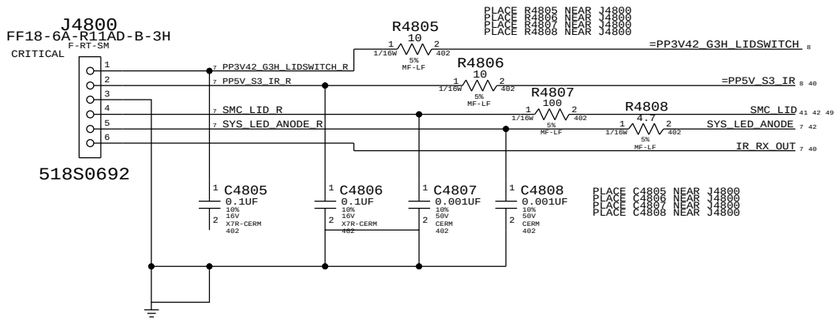
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 39 OF 98	





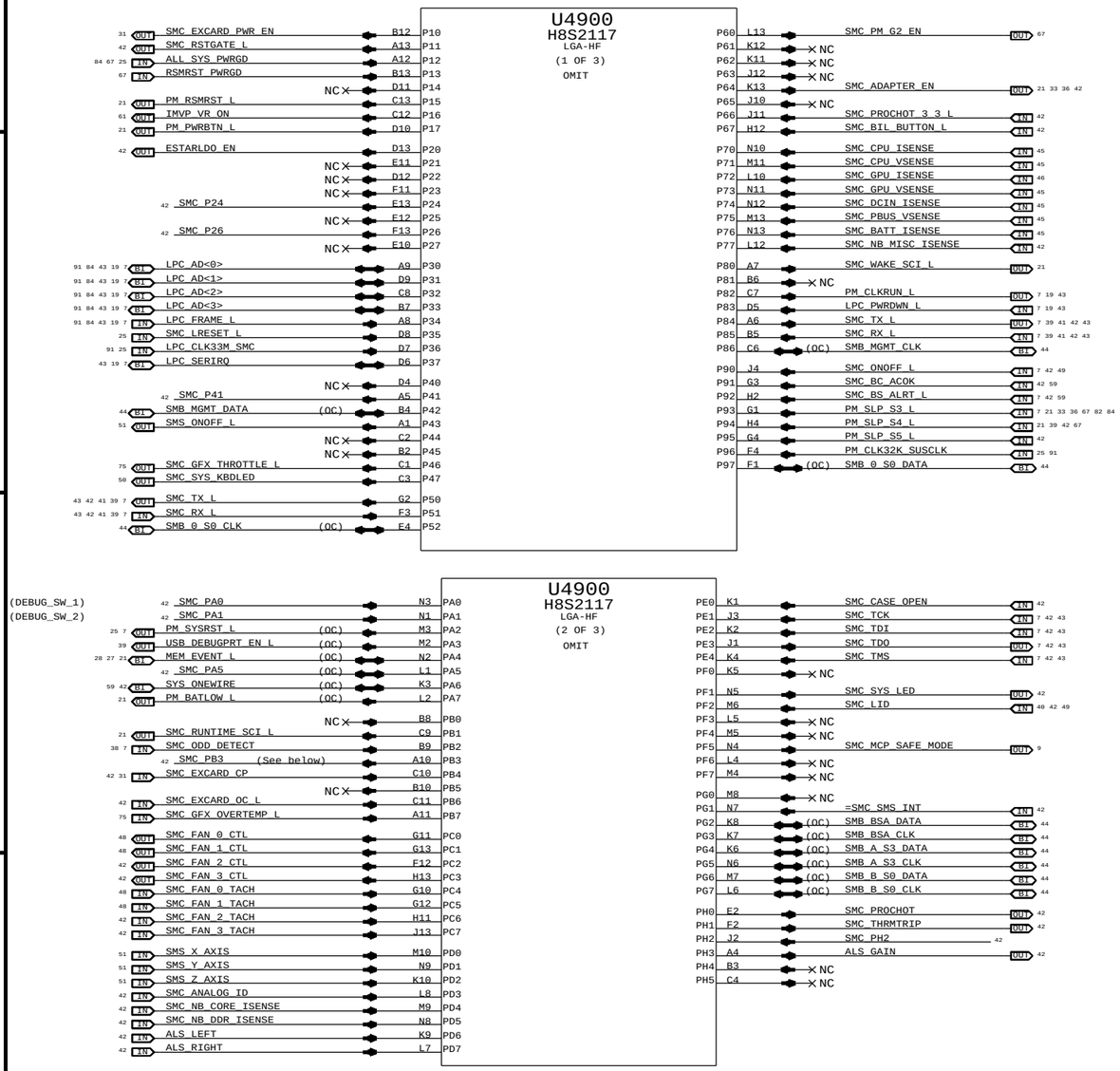
Front Flex Support

SYNC_MASTER=CHANG_K20 SYNC_DATE=07/18/2008

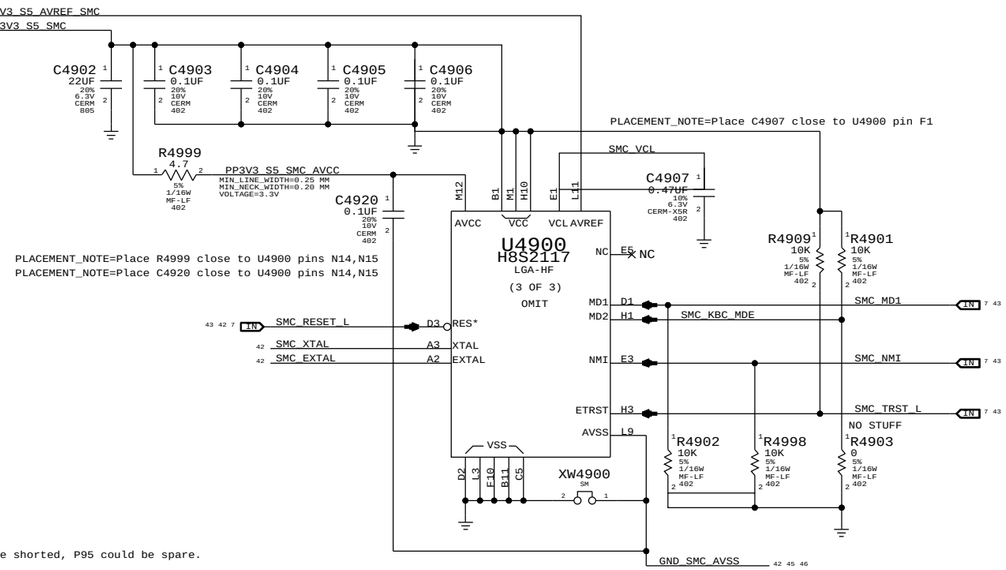
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT	OF
NONE	40	98

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: P94 and P95 are shorted, P95 could be spare.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SMC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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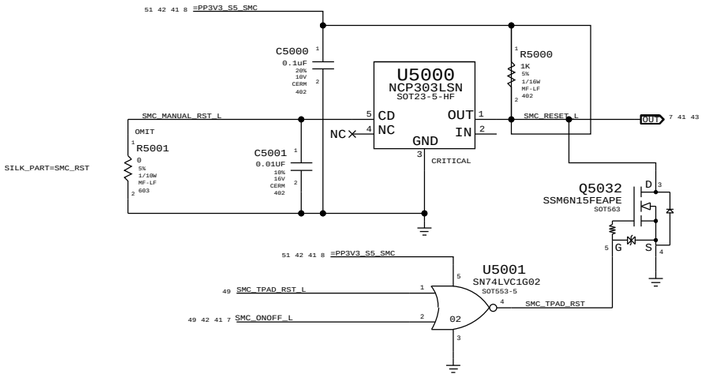
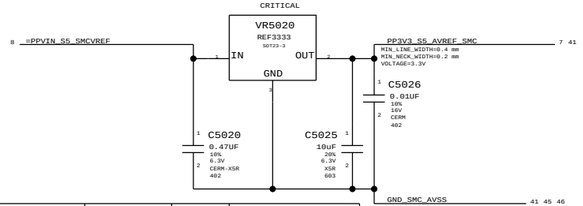
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE	SHT	OF
NONE	41	98

SMC Reset "Button" / Brownout Detect

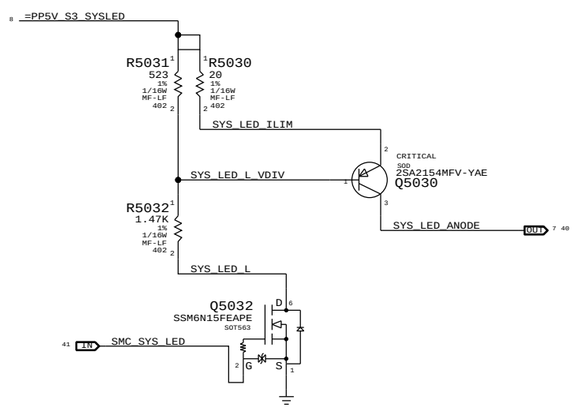


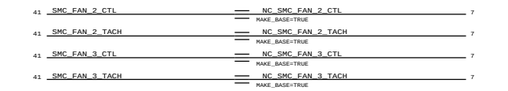
SMC AVREF Supply

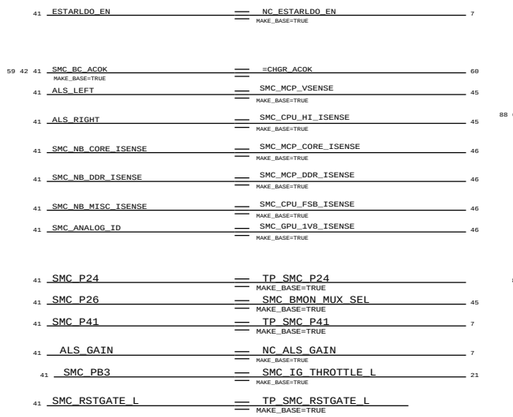


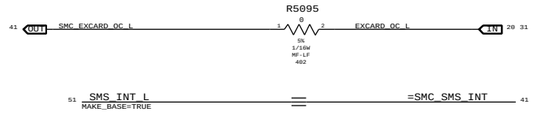
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

System (Sleep) LED Circuit

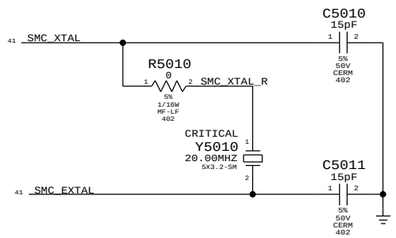




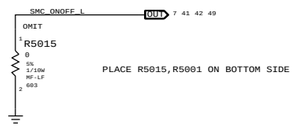




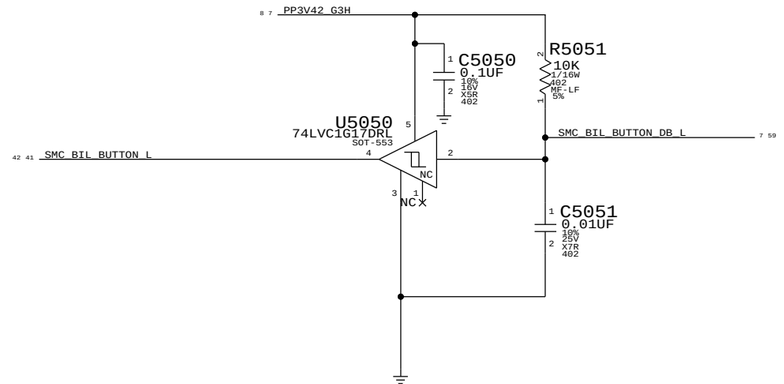
SMC Crystal Circuit



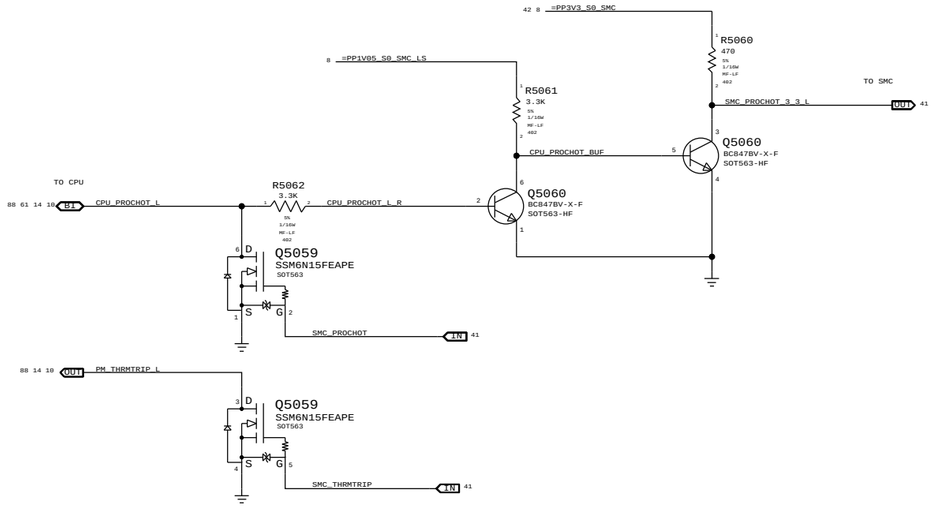
Debug Power "Button"

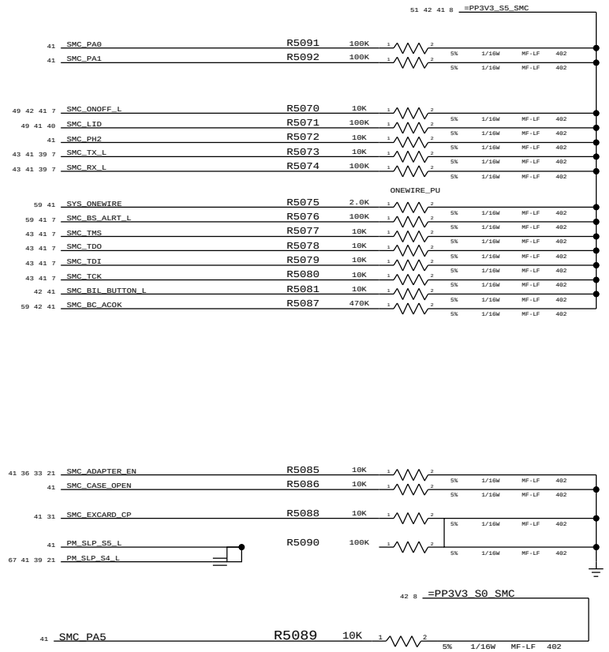


PLACE R5015,R5001 ON BOTTOM SIDE



SMC FSB to 3.3V Level Shifting





SMC Support

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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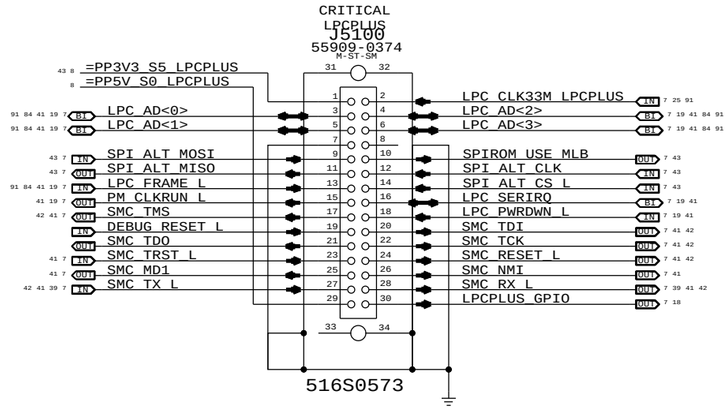
APPLE INC.

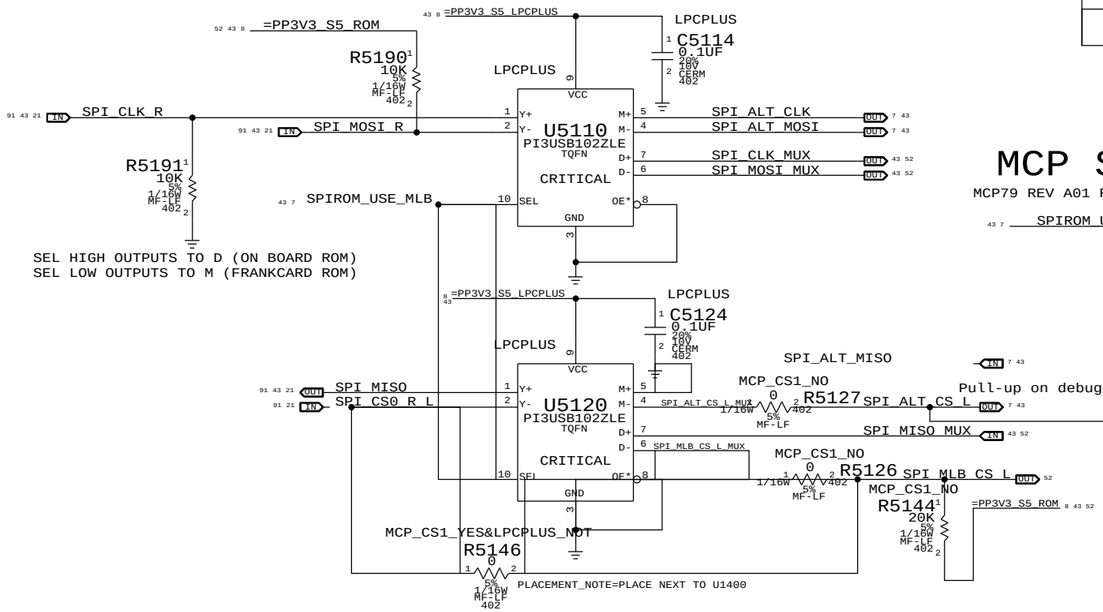
SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 42 OF 98	

LPC+SPI Connector



Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP

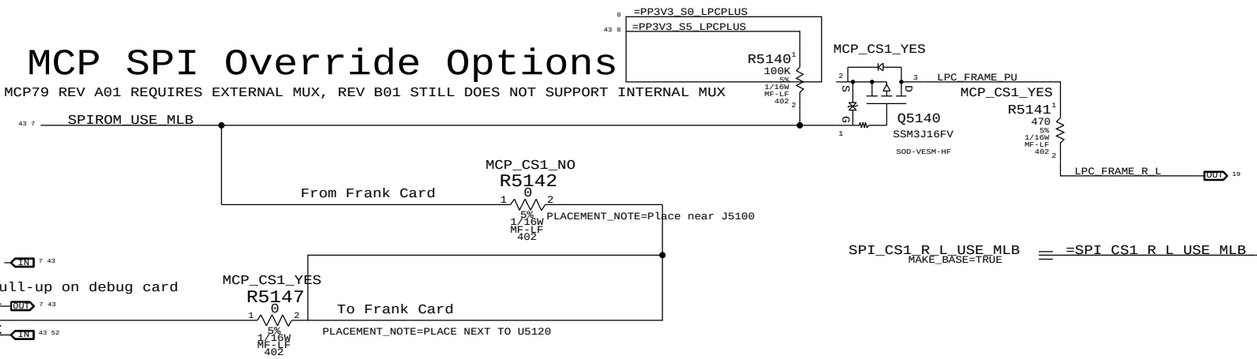


MCP79 Internal SPI MUX Support

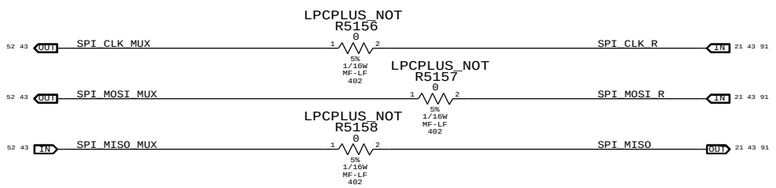
NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX



SPI MUX BYPASS



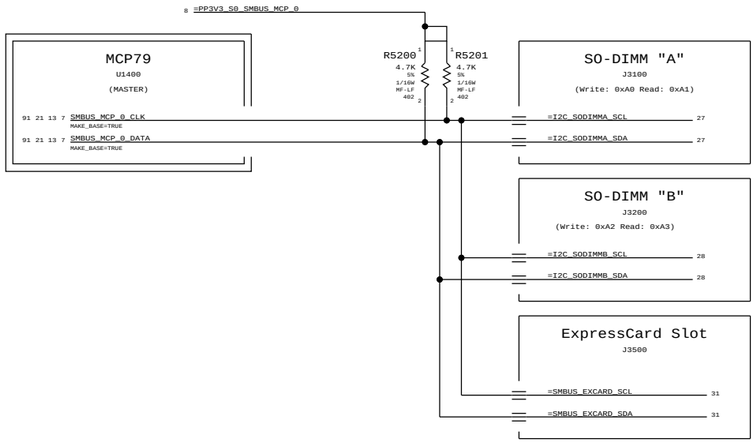
LPC+SPI Debug Connector

SYNC_MASTER=CHANG_K20 SYNC_DATE=05/28/2008

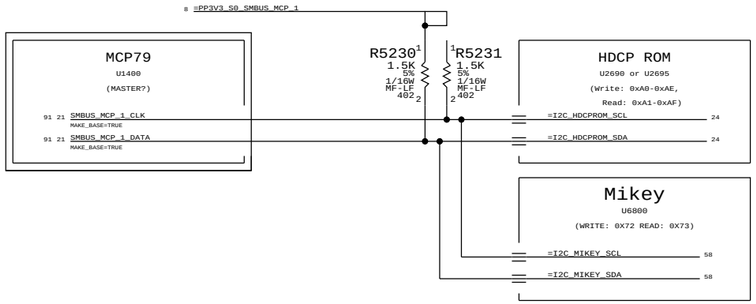
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 43 OF 98	

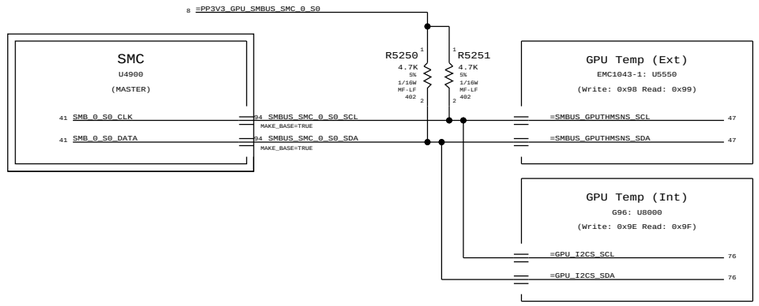
MCP79 SMBus "0" Connections



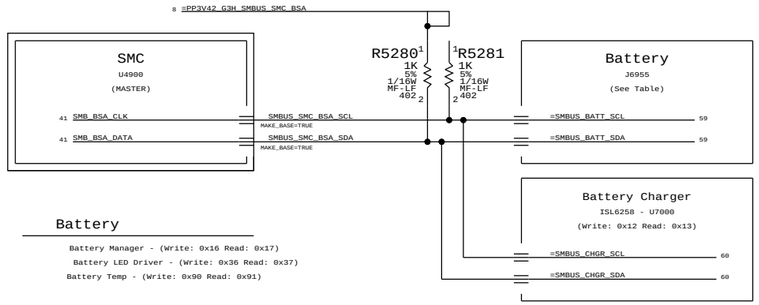
MCP79 SMBus "1" Connections



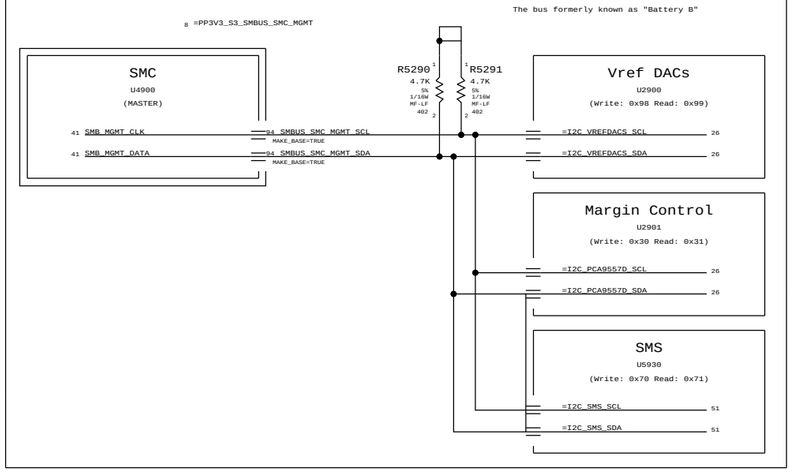
SMC "0" SMBus Connections



SMC "Battery A" SMBus Connections

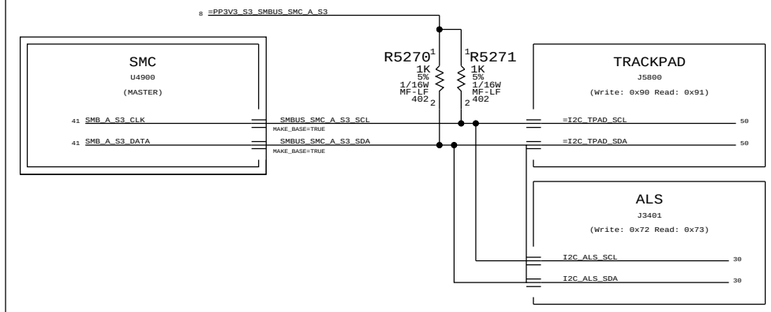


SMC "Management" SMBus Connections

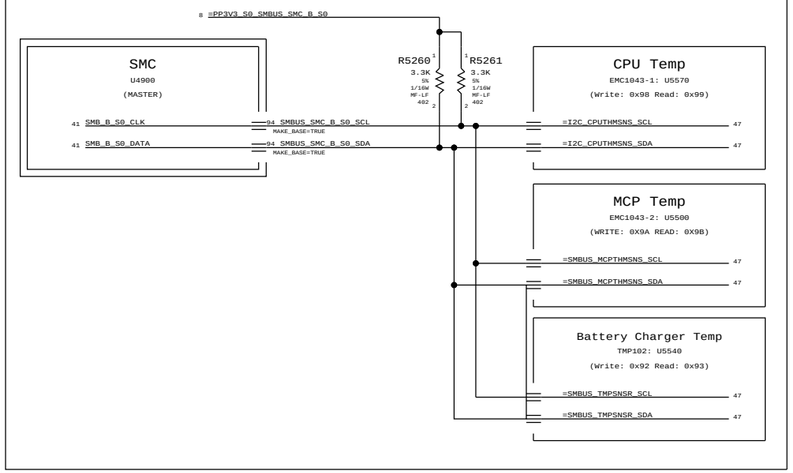


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "B" SMBus Connections



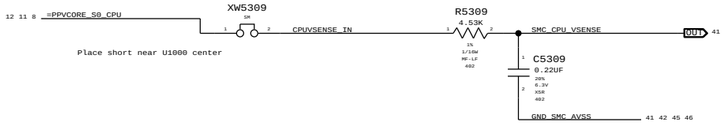
K20 SMBUS CONNECTIONS

SYNC_MASTER=BEN_K20 SYNC_DATE=07/22/2008

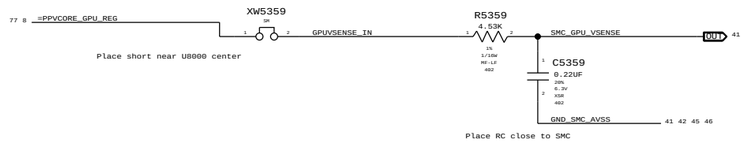
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 44 OF 98	

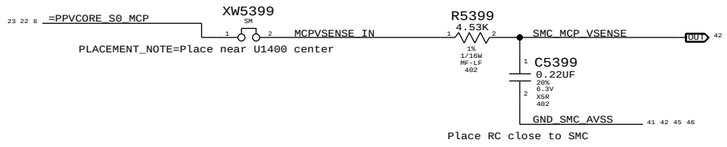
CPU Voltage Sense / Filter



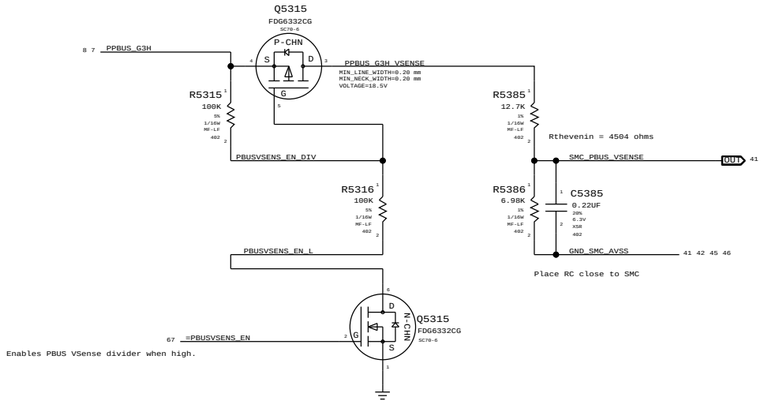
GPU Voltage Sense / Filter



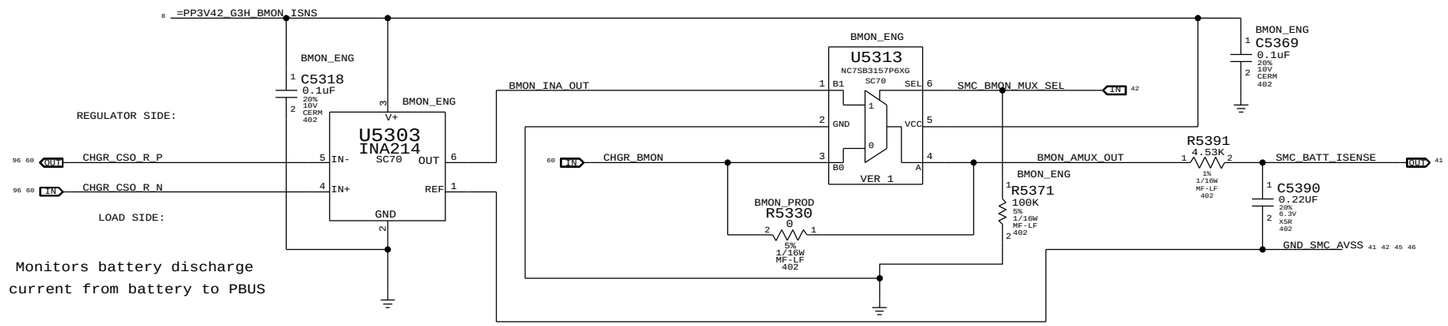
MCP Voltage Sense / Filter



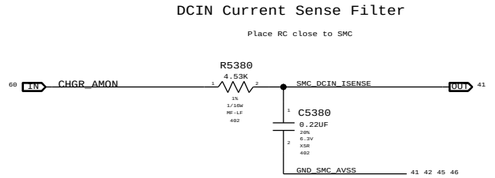
PBUS Voltage Sense & Filter



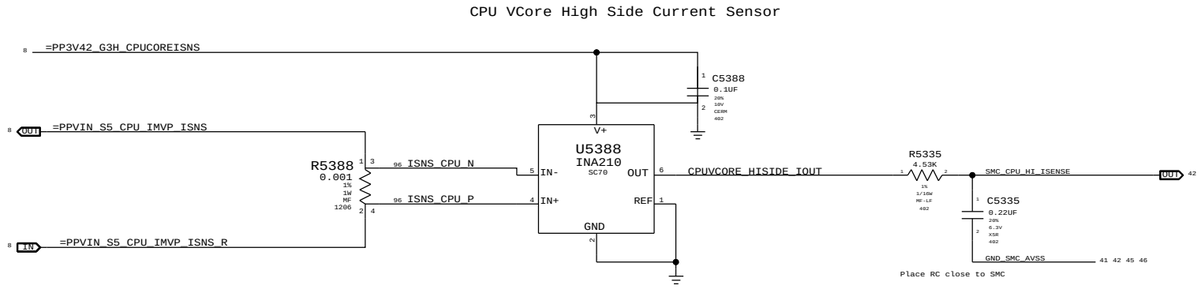
BMON Current Sense - Entire circuit must be near SMC (U4900)



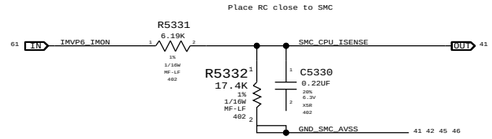
DCIN Current Sense Filter



CPU VCore High Side Current Sensor



CPU VCore Load Side Current Sense / Filter



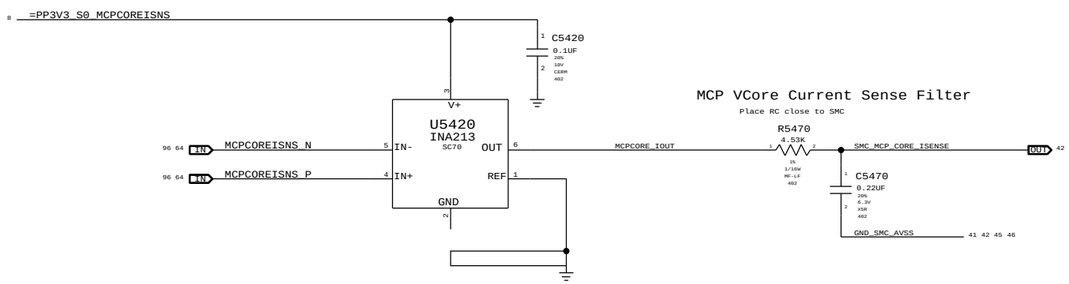
Current & Voltage Sensing

SYNC_MASTER=YWU_K20 SYNC_DATE=08/20/2008

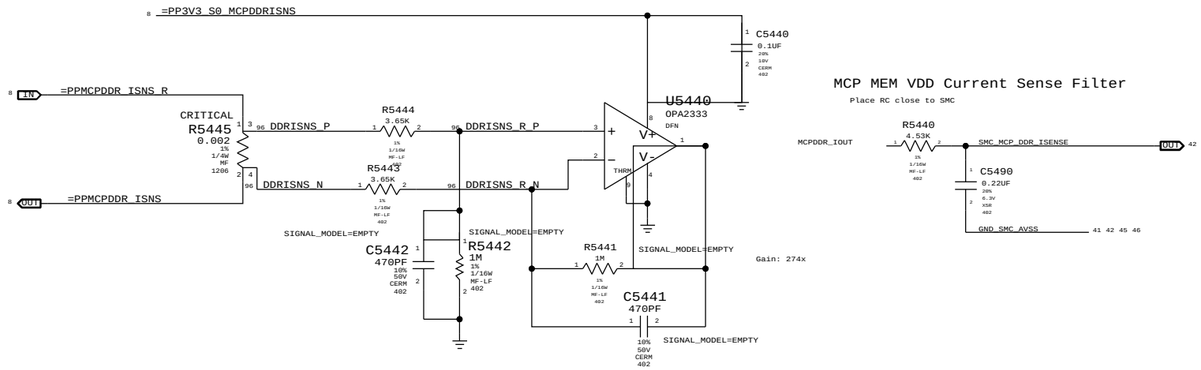
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT	OF
NONE	45	98

MCP VCore Current Sense



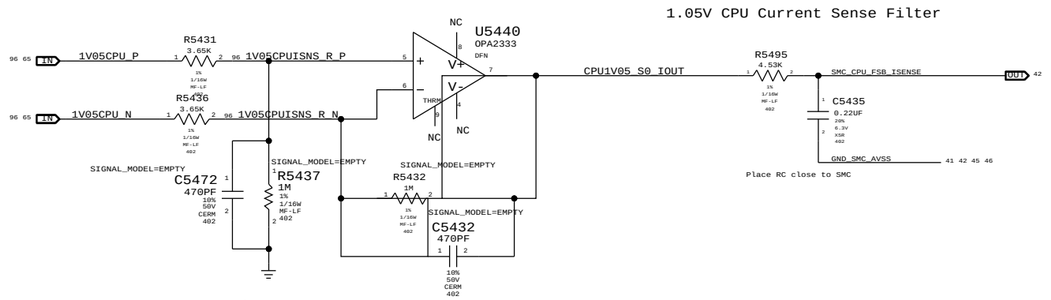
MCP MEM VDD Current Sense



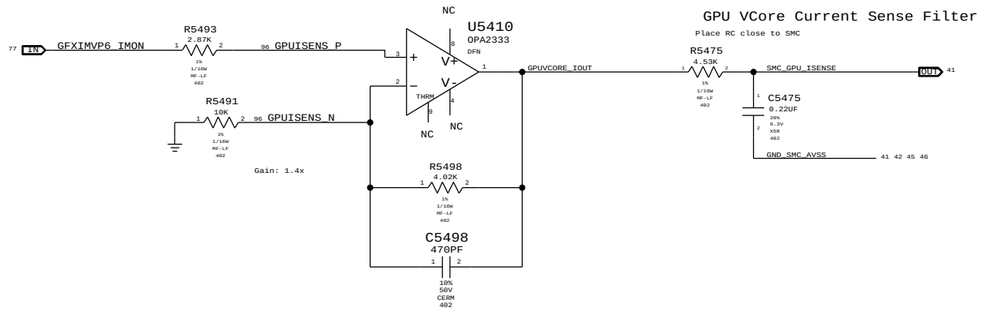
OPA2333s for proto are placeholders for OPA2330

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

CPU FSB 1.05V Current Sense

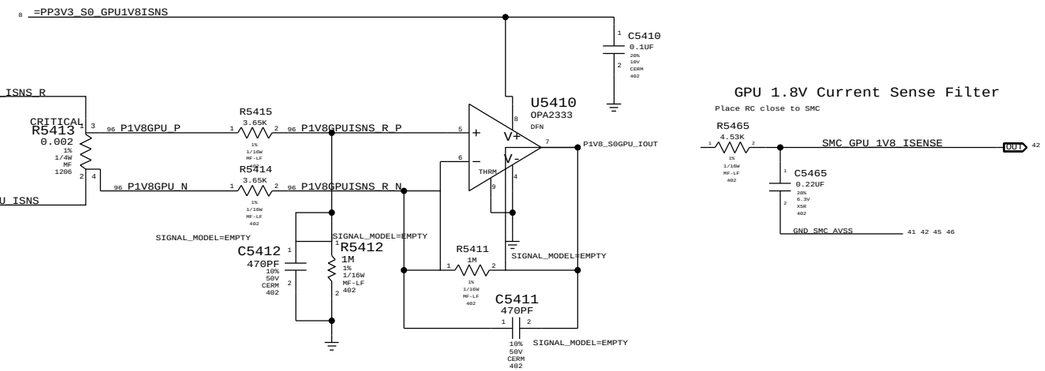


GPU VCore Current Sense



GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

GPU 1.8V Current Sense



Current Sensing

SYNC_MASTER=YWU_K20 SYNC_DATE=08/12/2008

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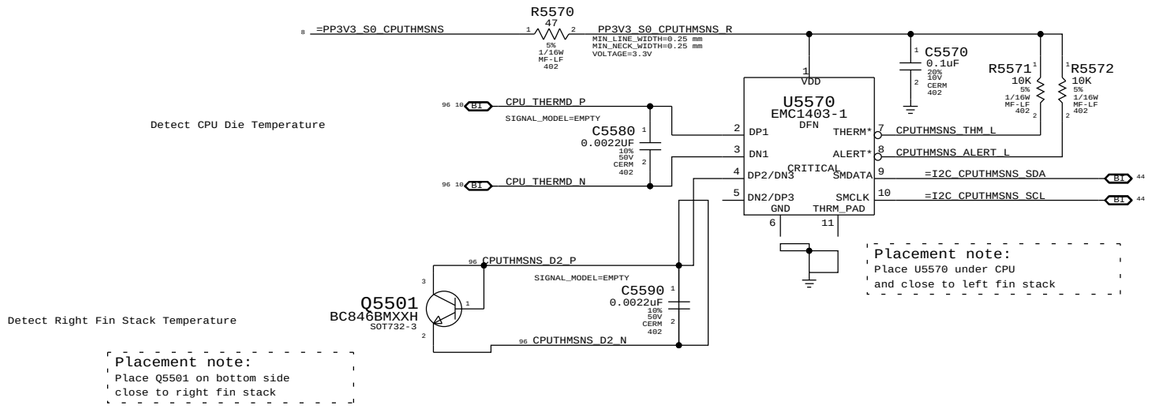
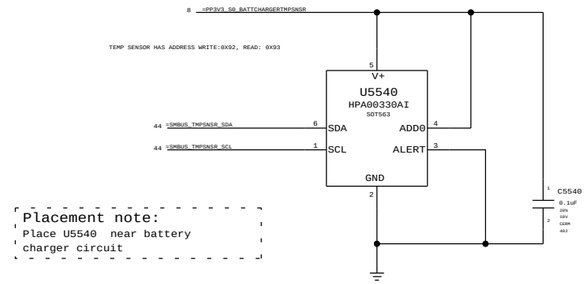
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT 46 OF 98	
NONE		

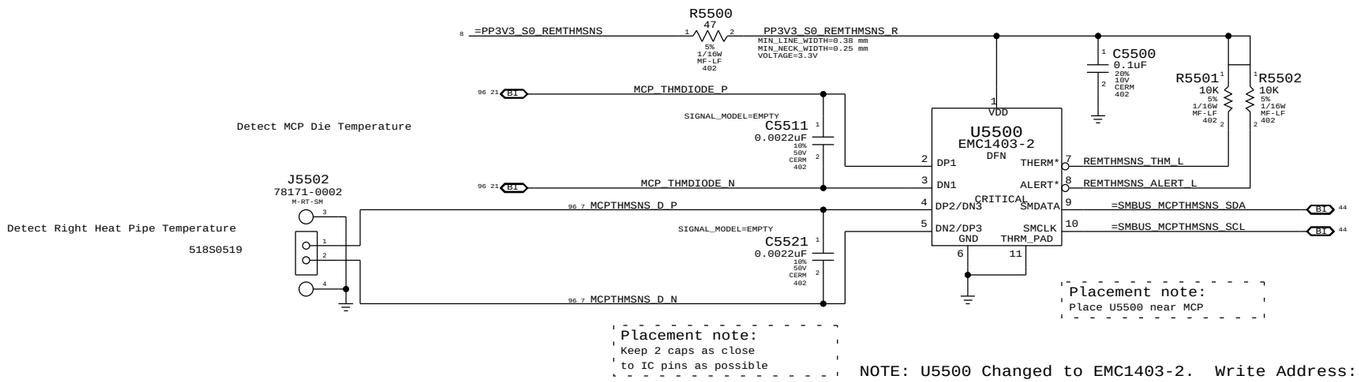
CPU Proximity/CPU Die/Right Fin Stack



Battery Charger Proximity



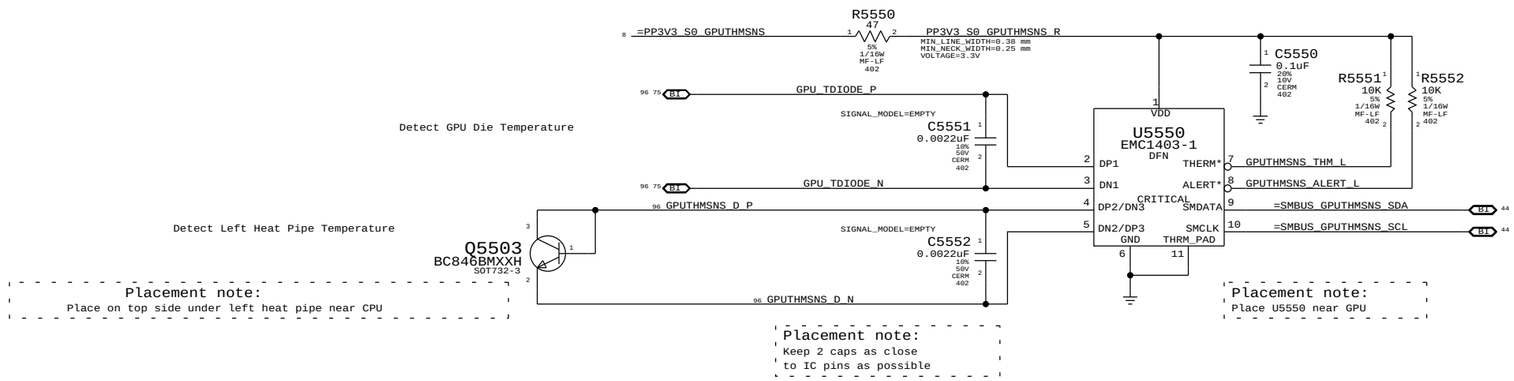
MCP Proximity/MCP Die/Right Heat Pipe



Note: EMC1403 can perform Beta
Compensation for External Diode 1 only

NOTE: U5500 Changed to EMC1403-2. Write Address: 0x9A

GPU Proximity/GPU Die/Left Heat Pipe



Thermal Sensors		
SYNC_MASTER=YWU_K20	SYNC_DATE=05/28/2008	
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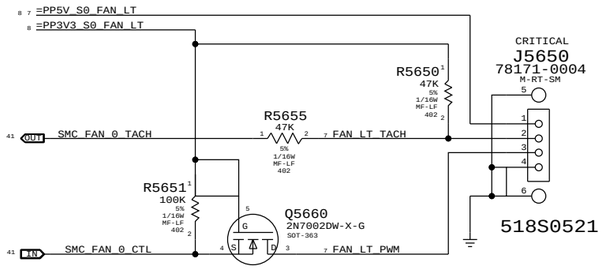
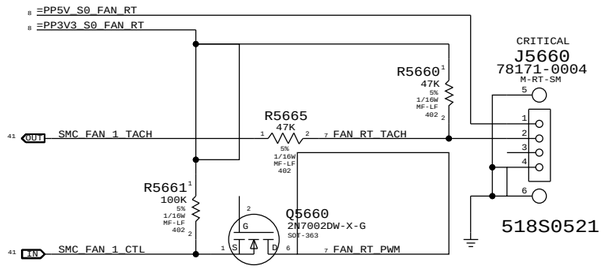
APPLE INC.	SIZE: D	DRAWING NUMBER: 051-8071
	REV: B	
	SCALE: NONE	SHT 47 OF 98

Left Fan



Right Fan



Fan Connectors

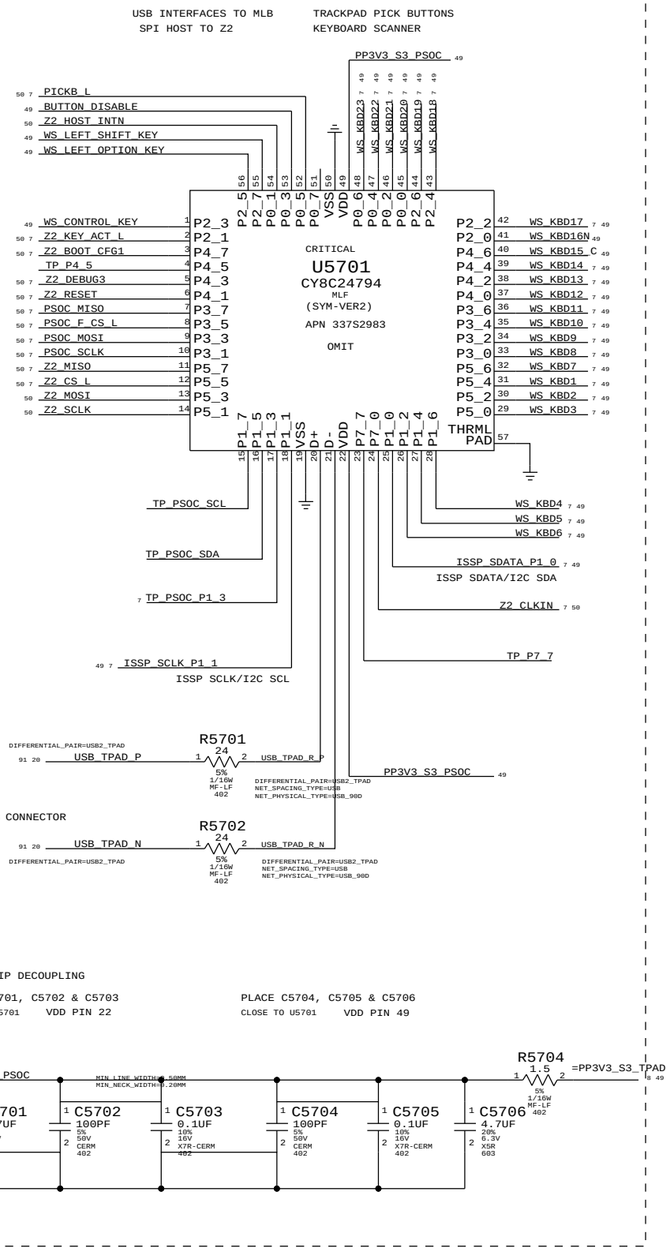
SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B

SCALE	SHT	OF
NONE	48	98

PSOC USB CONTROLLER



U5701 CHIP DECOUPLING

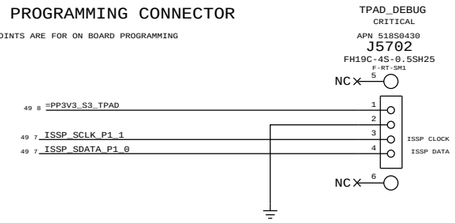
PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

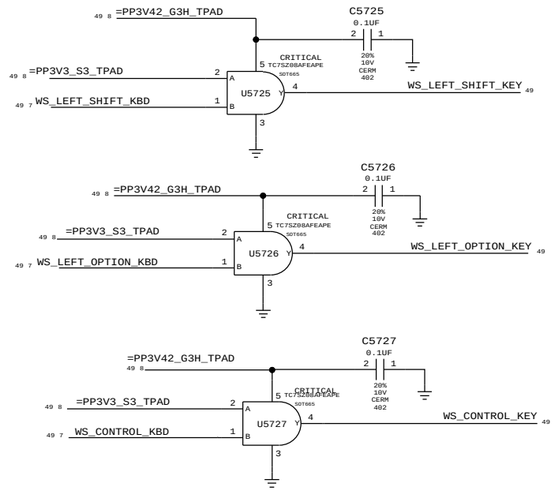
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC PROGRAMMING CONNECTOR

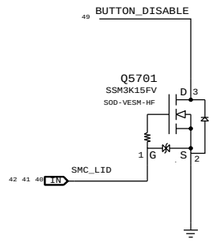
TEST POINTS ARE FOR ON BOARD PROGRAMMING



ISOLATION CIRCUIT



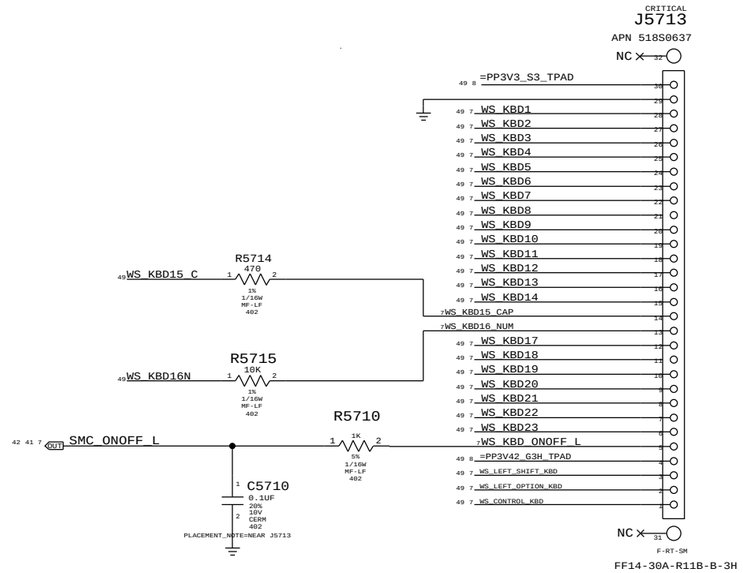
TPAD BUTTONS DISABLE



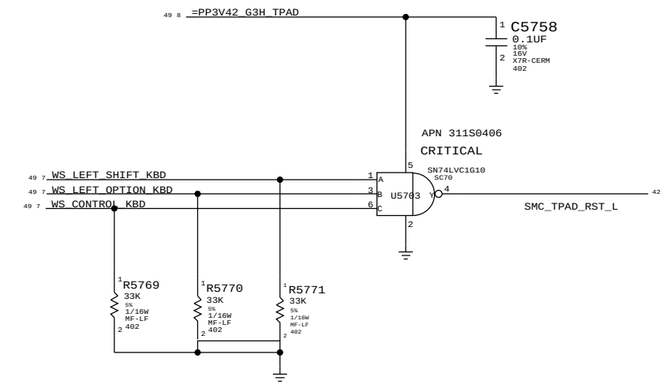
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC

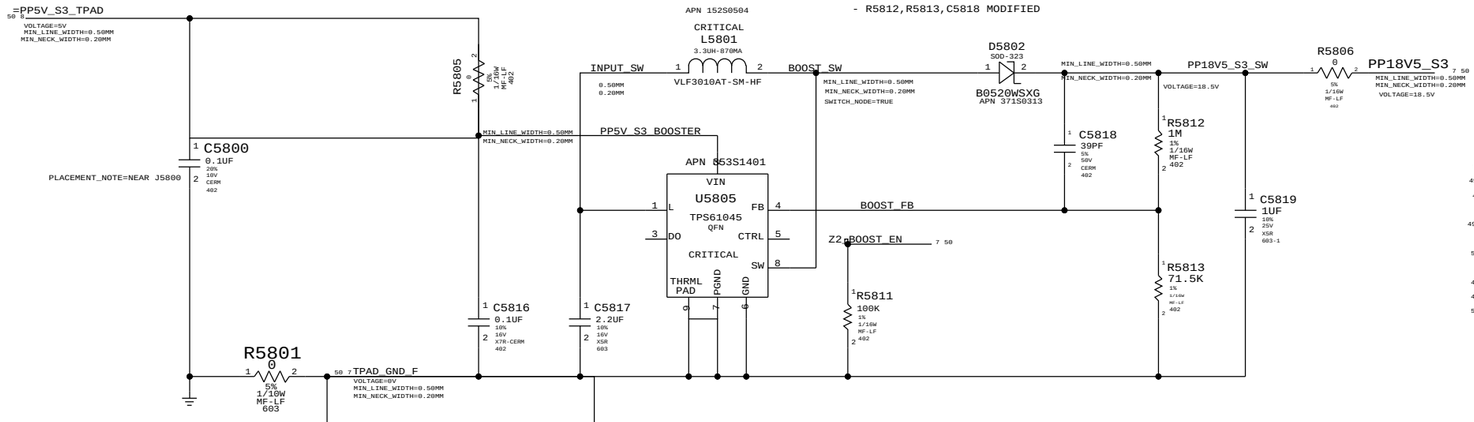


APPLE INC.

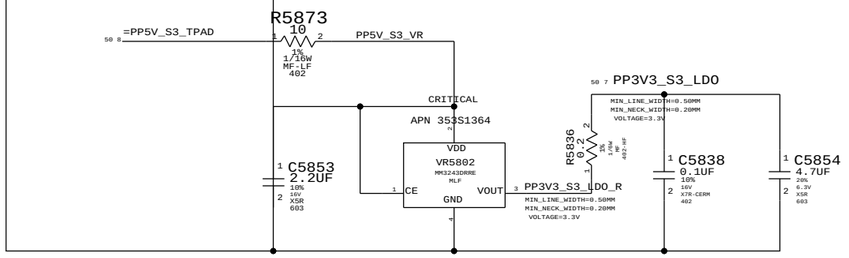
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE	SHT	OF
NONE	49	98

BOOSTER +18.5VDC FOR SENSORS

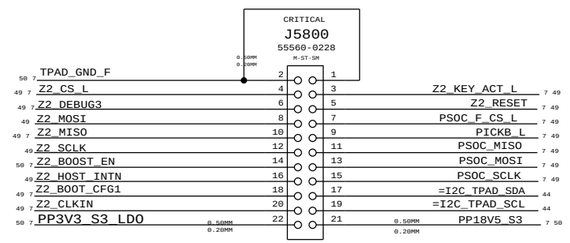
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



3V3 LDO FOR IPD



IPD FLEX CONNECTOR



Keyboard LED Driver

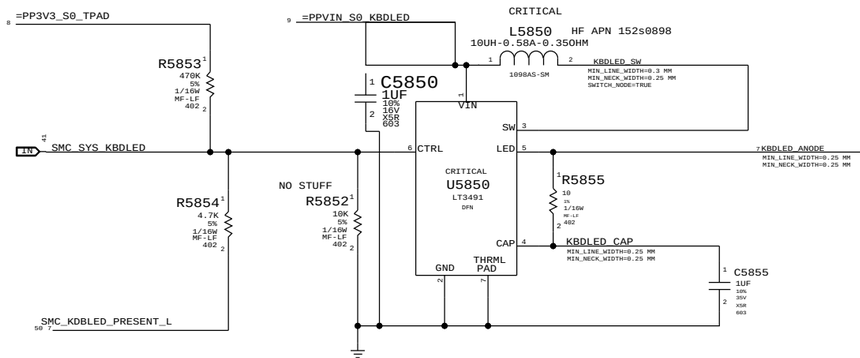
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

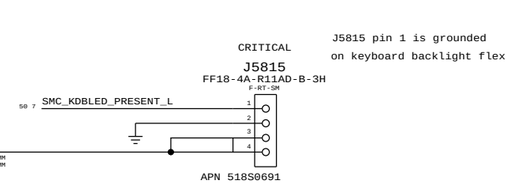
LOW = keyboard backlight present

HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT





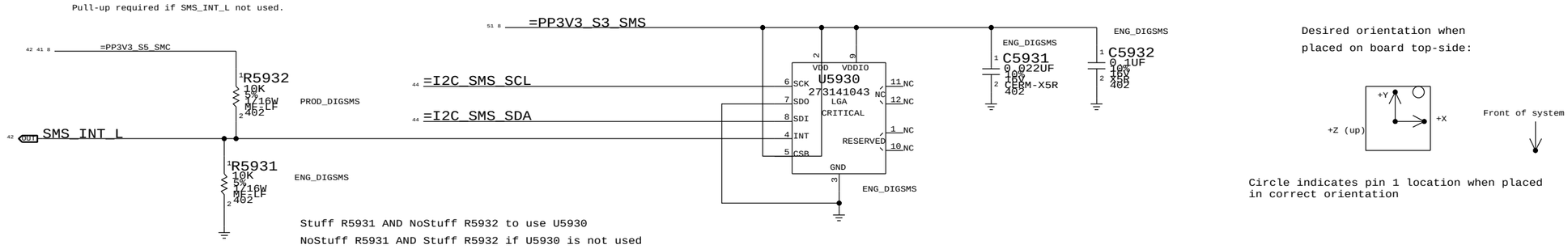
J5815 pin 1 is grounded on keyboard backlight flex

KBD BACKLIGHT CONNECTOR

WELLSPRING 2		
SYNC_MASTER=K20_MLB	SYNC_DATE=09/24/2008	

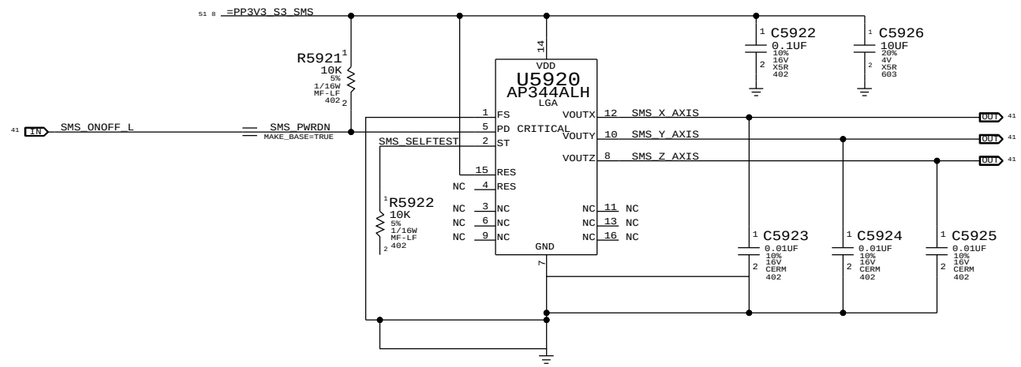
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-8071	B
	SCALE: NONE	SHT 50 OF 98	

Digital SMS



Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC

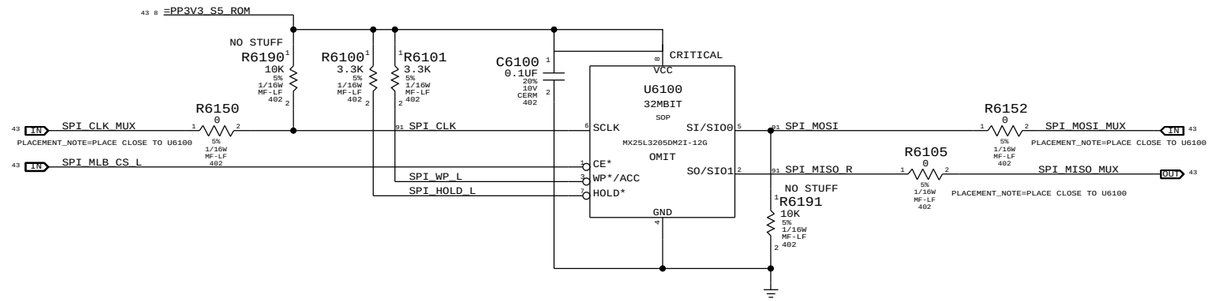


Sudden Motion Sensor (SMS)

SYNC_MASTER=YWU_K20 SYNC_DATE=06/17/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT 51 OF 98	
NONE		



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SPI ROM

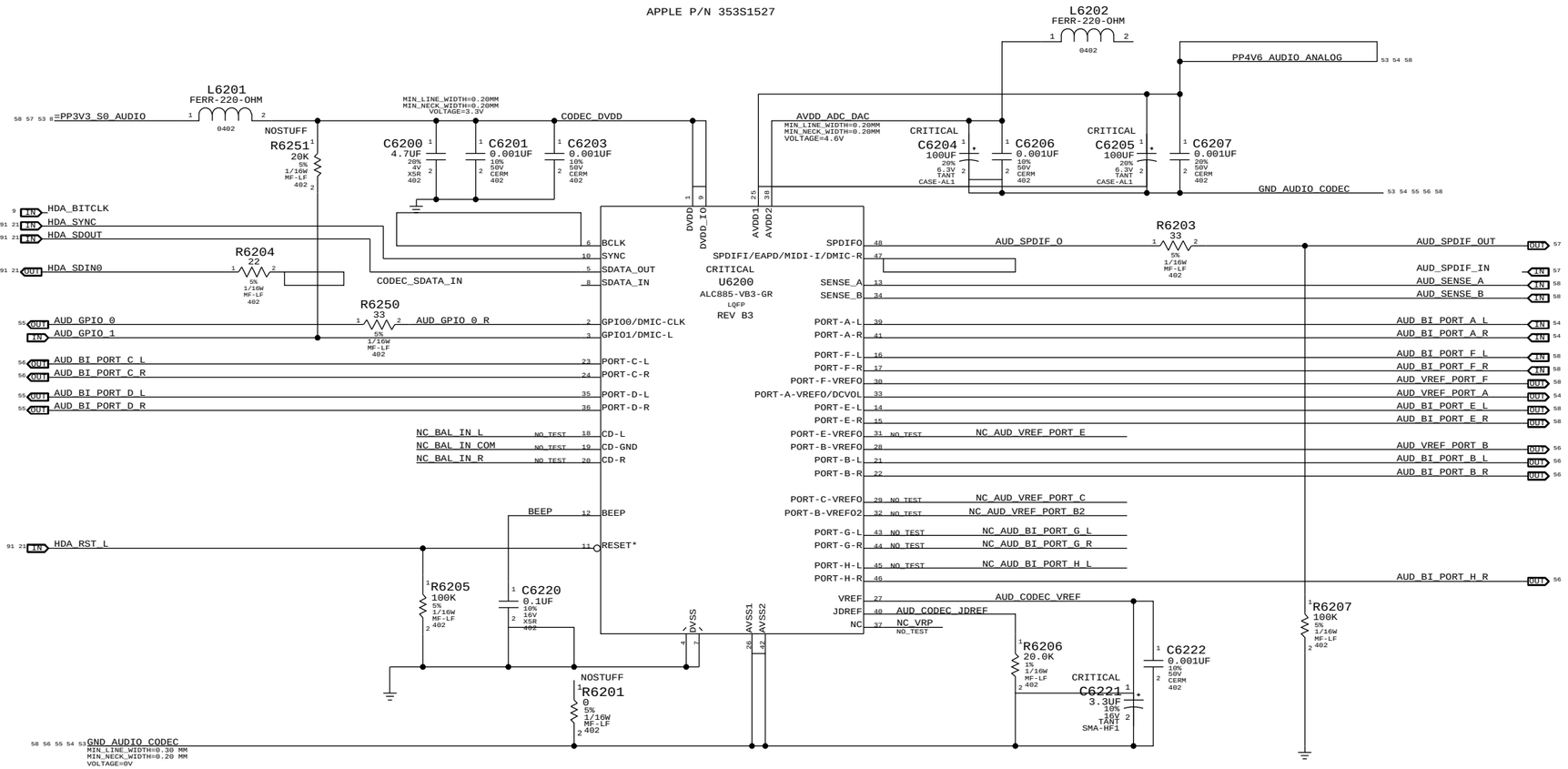
SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 52 OF 98	

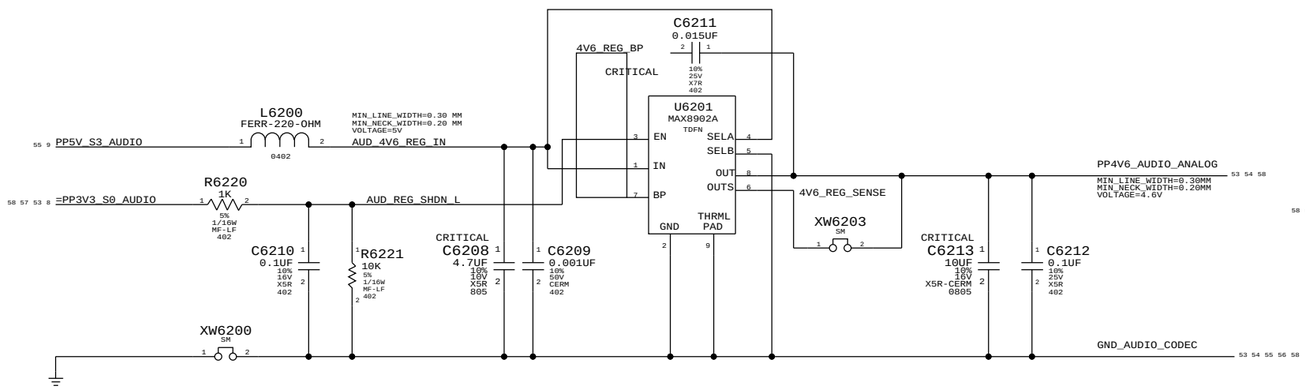
AUDIO CODEC

APPLE P/N 353S1527



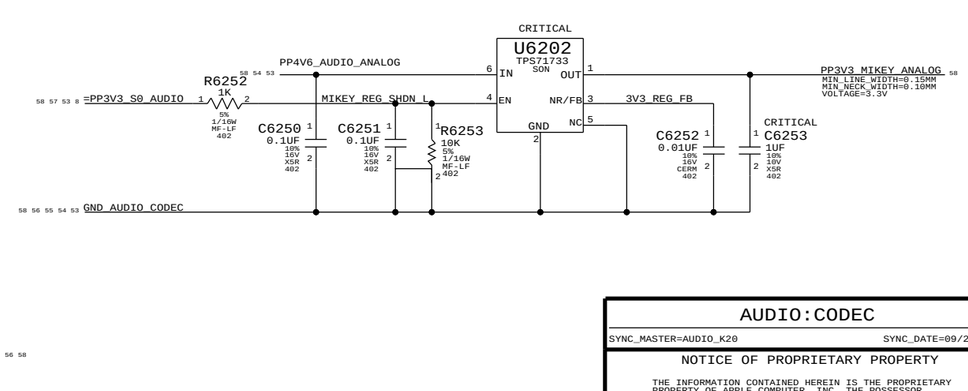
AUDIO 4.6 V REGULATOR

APPLE P/N 353S1897



MIKEY 3.3 V REGULATOR

APPLE P/N 353S1860



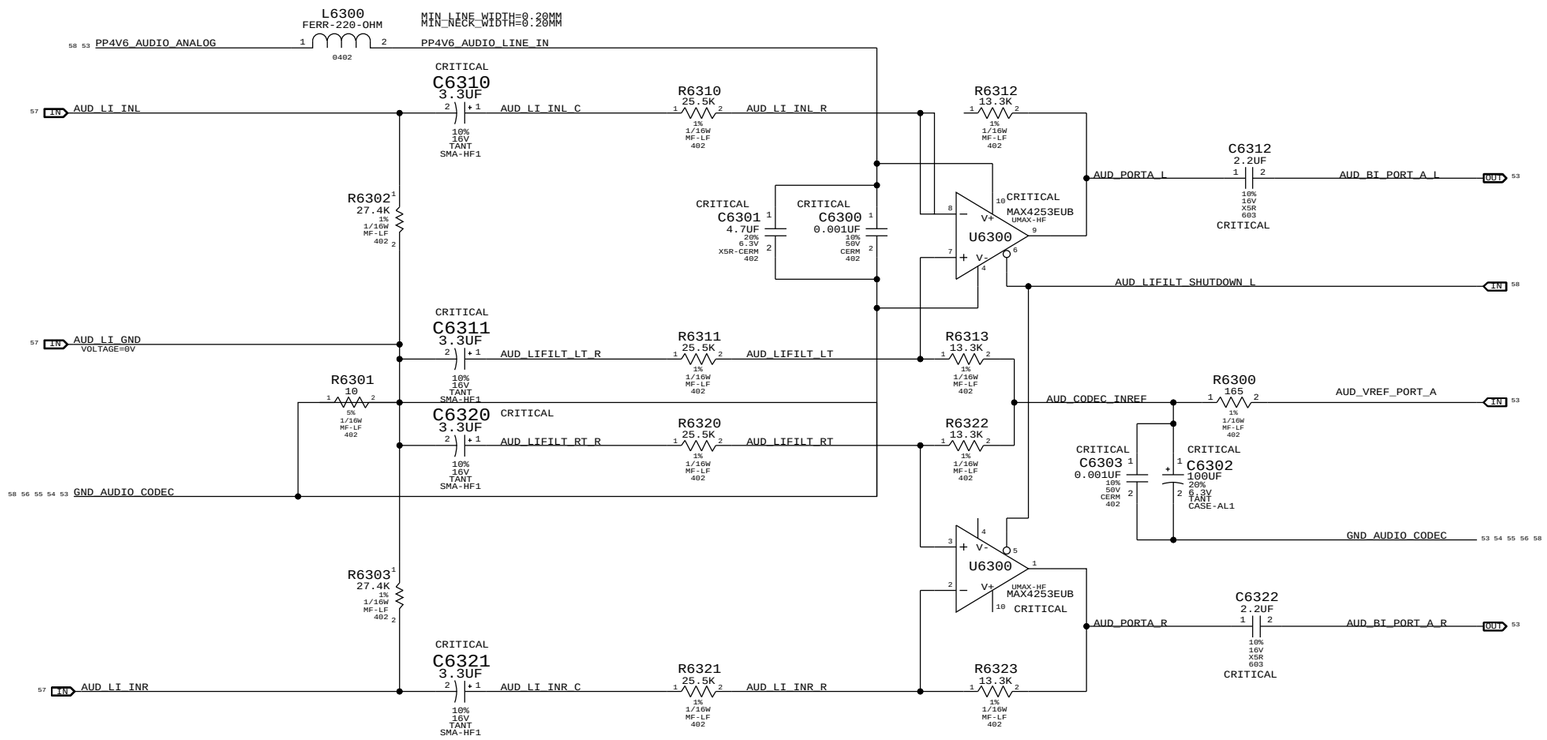
AUDIO:CODEC

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 53 OF 98	

Pseudo-Diff Line-In Filter
GAIN = -5.4 DB AV = 0.52
FC = 1.89 HZ



AUDIO: LINE IN

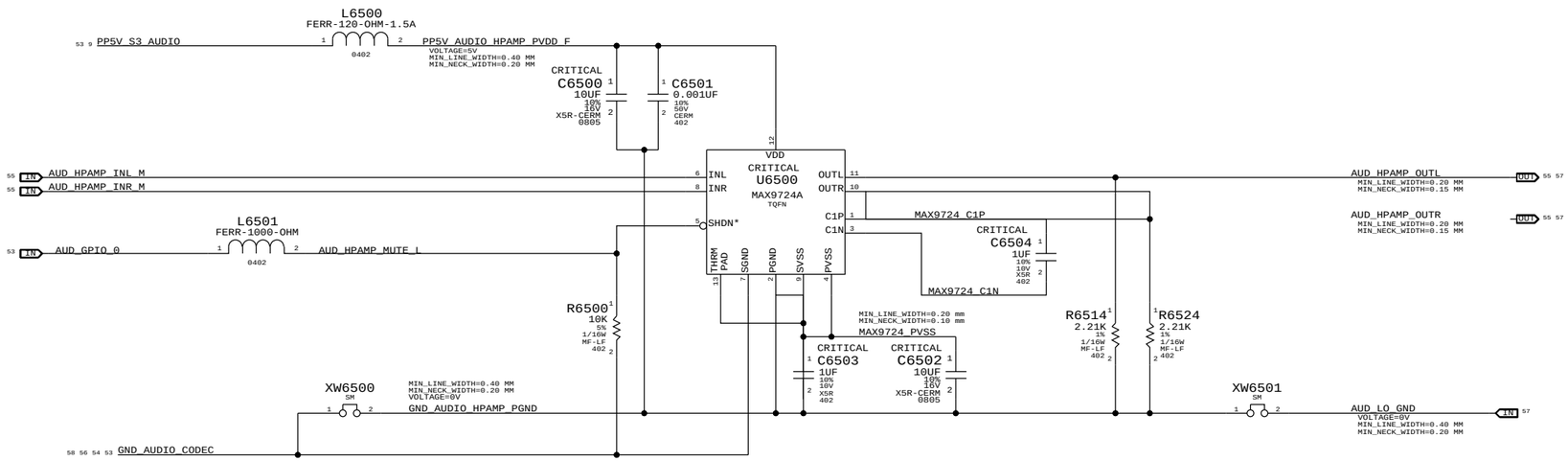
SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 54 OF 98	

Headphone Amplifier (MAX9724A)

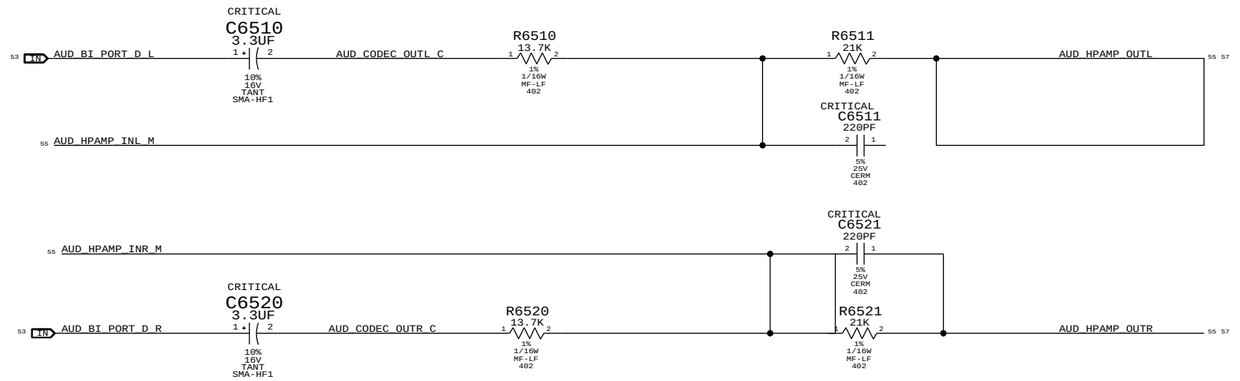
APN:353S1637



1st Order DAC Filter

HP:3.52 HZ LP:34 KHZ

VOLTAGE GAIN:1.53



AUDIO: HEADPHONE AMP	
SYNC_MASTER=AUDIO_K20	SYNC_DATE=09/29/2008

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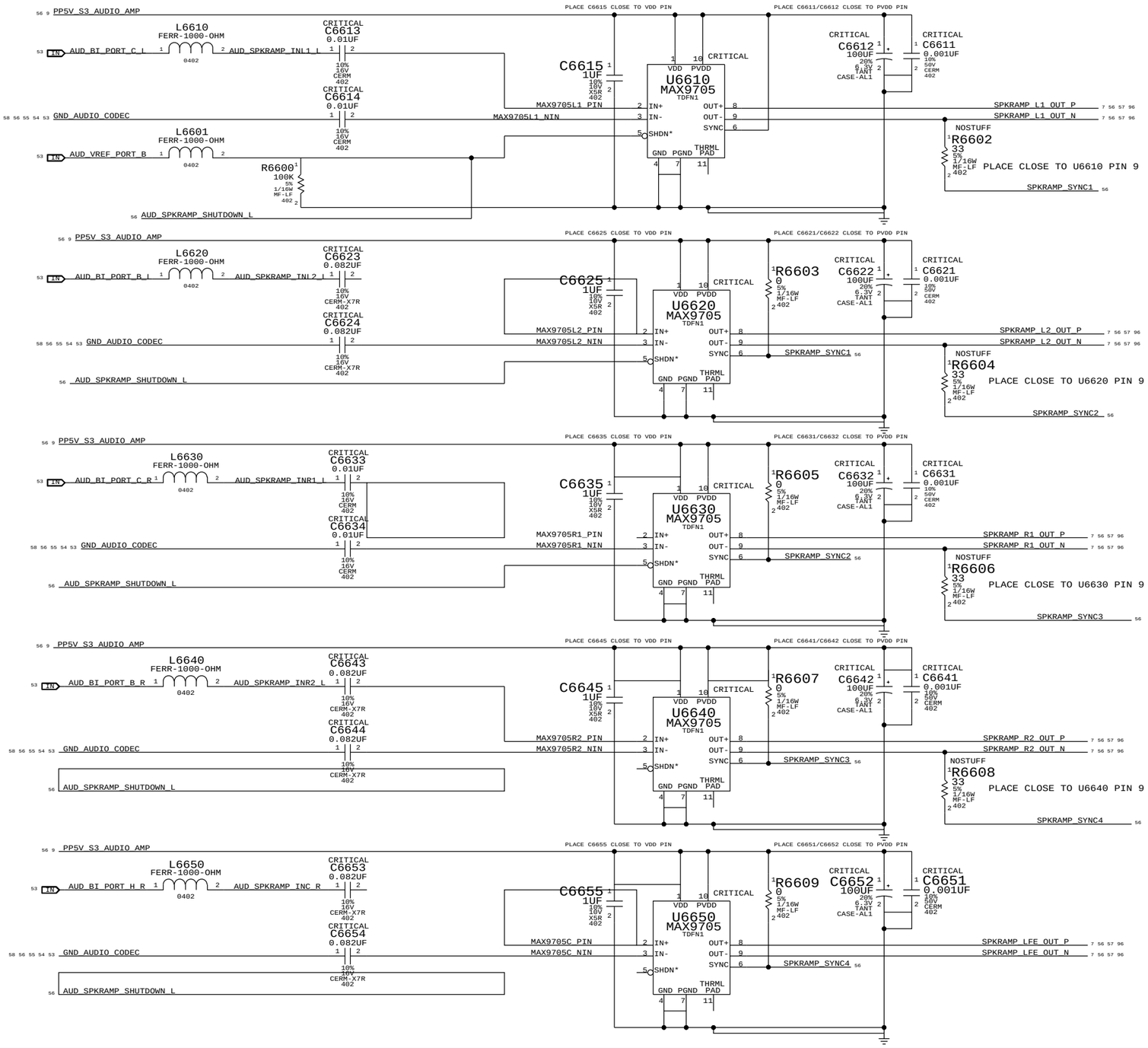
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 55 OF 98	

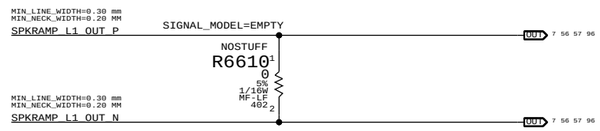
4X MONO SPEAKER AMPLIFIERS (MAX9705)

APN: 353S1595
GAIN = 12 DB

FC (SPEAKERS L1/R1) = ~796 HZ
FC (SPEAKERS L2/R2/LFE) = ~97 HZ



SPEAKER CHECKPOINTS



AUDIO:SPEAKER AMP

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

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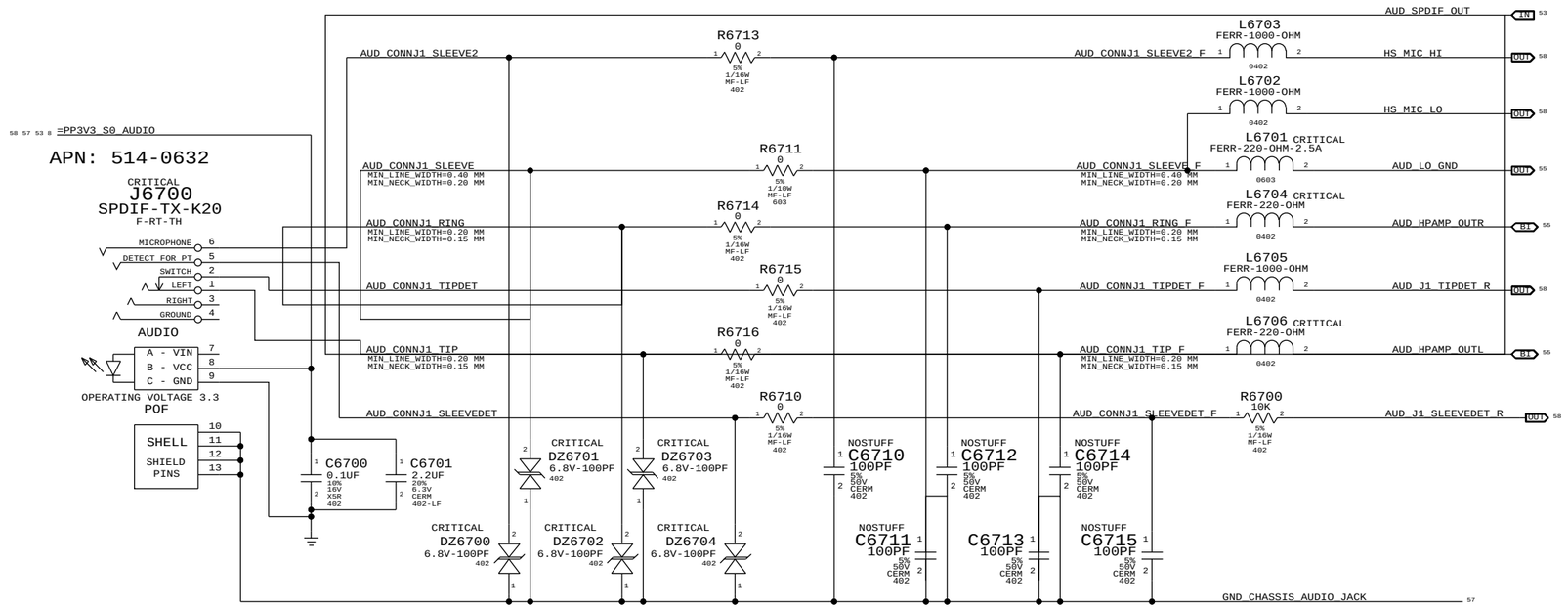
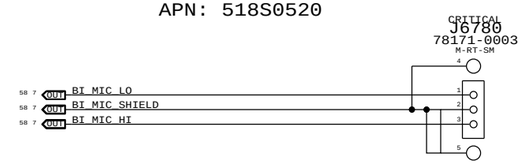
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 56 OF 98	

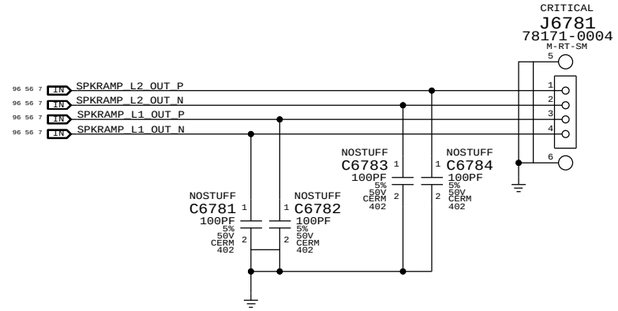
AUDIO JACK 1 LO/HP JACK, SPDIF TX



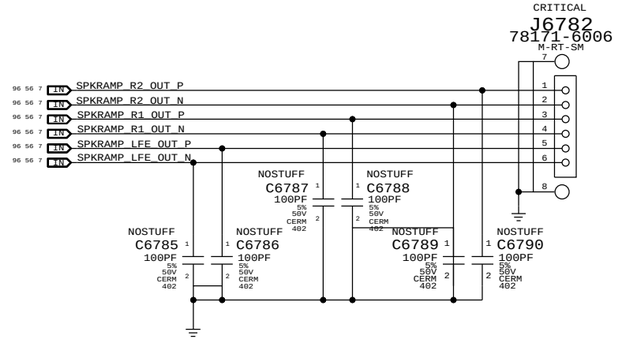
MIC CONNECTOR
APN: 518S0520



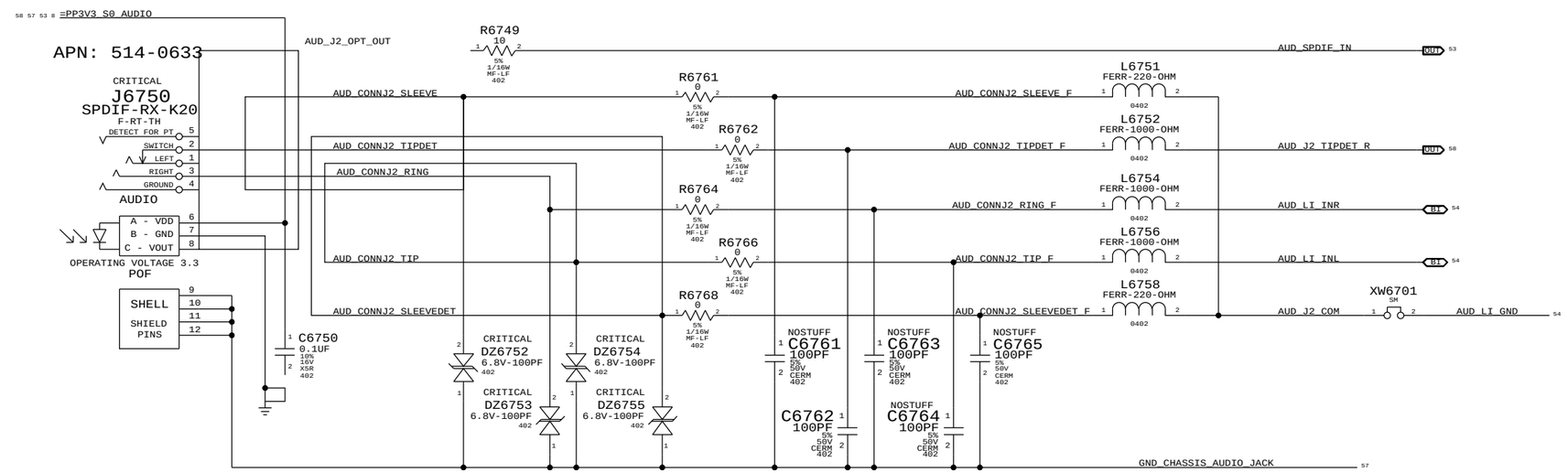
SPEAKER CONNECTORS
APN: 518S0521



APN: 518S0672



AUDIO JACK 2 LINE IN JACK, SPDIF RX



RETURN FOR HF NOISE

AUDIO: JACKS		
SYNC_MASTER=AUDIO_K20	SYNC_DATE=09/29/2008	
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APPLE INC.	SIZE: D	DRAWING NUMBER: 051-8071 REV: B
	SCALE: NONE	SHT: 57 OF 98

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	MIXER(OUTPUT)	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X0C (12)	0X02 (2)	0X0C (12)	0X14 (20,D)	GPIO_0	0X14 (20,D)
SPEAKERS L1/R1	0X0F (15)	0X05 (5)	0X0F (15)	0X1A (26,C)	VREF_B (100%)	N/A
SPEAKERS L2/R2	0X0D (13)	0X03 (3)	0X0D (13)	0X18 (24,B)	VREF_B (100%)	N/A
SPEAKER LFE	0X0E (14)	0X04 (4)	0X0E (14)	0X17 (23,H)	VREF_B (100%)	N/A
SPDIF OUT	N/A	0X06 (6)	N/A	0x1E (SPDIF OUT)	N/A	0X16 (22,G)

CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER(INPUT)	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X15 (21,A)	VREF_A (50%)	0X15 (21,A)
SPDIF IN	N/A	0X0A (10)	0x1F (SPDIF IN)	N/A	N/A
MIC	0X24 (36)	0X07 (7)	0X19 (25,F)	VREF_F (100%)	N/A
HEADSET MIC	0X24 (36)	0X07 (7)	0X1B (27,E)	MIKEY	MIKEY

PORT D DETECT (Line-out)

PORT G DETECT (SPDIF DELEGATE)

PORT A DETECT (Line-in)

LINE_IN AMP SHUTDOWN CONTROL

PORT F (BUILT-IN MIC)

TIPDET DEBOUNCE CIRCUIT

PLACE L6800/C6800 CLOSE TO Q6800/01/02

KEEP DET TRACE AS SHORT AS POSS

MIN_LINE_WIDTH=0.15MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3.3V

AUDIO: JACK TRANSLATORS

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

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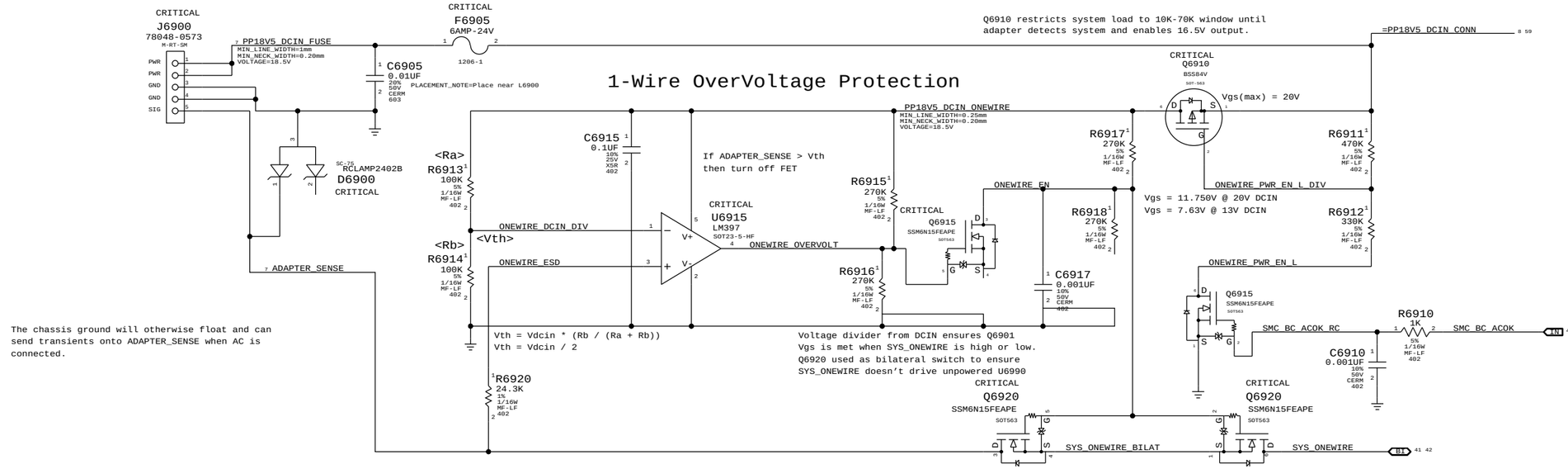
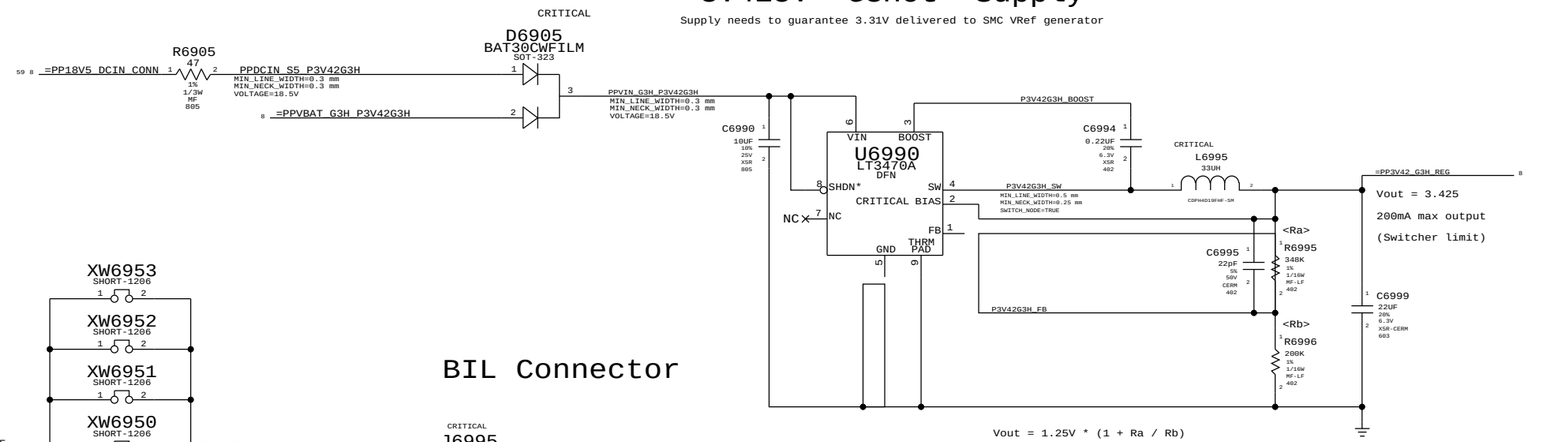
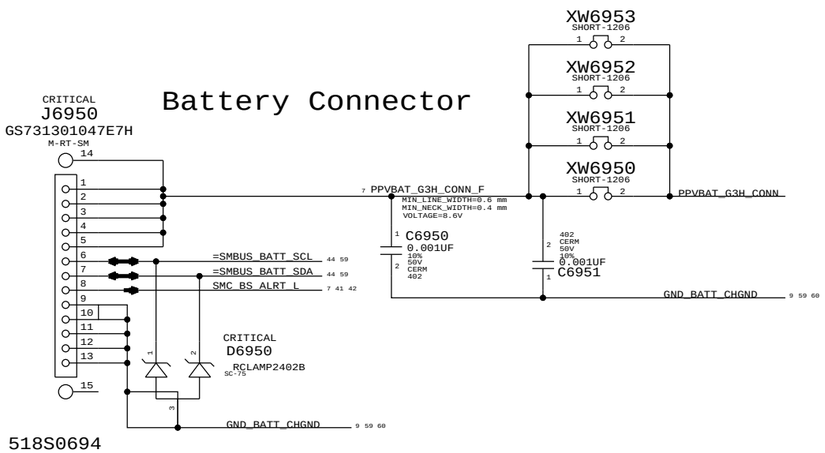
APPLE INC.

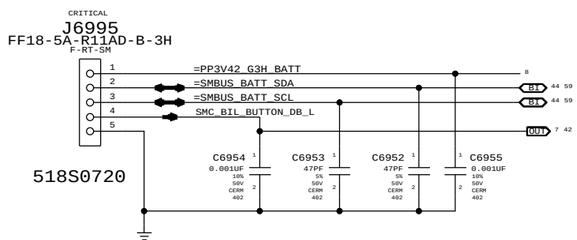
SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 58 OF 98	

MagSafe DC Power Jack









DC-In & Battery Connectors

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B

SCALE: NONE SHT 59 OF 98

FROM ADAPTER

=PPDCIN_S5_CHGR

Inrush Limiter

R7060 470K 1% 1/16W MF-LF 402

C7060 0.1UF 10% 25V X5R 402

CHGR_AGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

R7061 332K 1% 1/16W MF-LF 402

CRITICAL
Q7060
HAT1128R01
SO1

PPDCIN_S5_INRUSH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

Reverse-Current Protection

PPDCIN_S5_CHGR_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

CRITICAL
Q7065
HAT1128R01
SO1

R7065 100K 5% 1/16W MF-LF 402

CHGR_SGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

R7066 62K 5% 1/16W MF-LF 402

CHGR_SGATE
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.25 mm

U7070 TL331 SOT23-5
VCC
GND
SGATE_P0V1_VREF

C7070 0.1uF 10% 16V X5R 402

R7070 57.6K 1% 1/16W MF-LF 402

R7071 1.82K 1% 1/16W MF-LF 402

Q7074 SSM6N15FEAPE SOT563
AMON_CLAMP

=PP3V42_G3H_CHGR

R7074 1M 5% 1/16W MF-LF 402

CHGR_AMON

R7075 clamps CHGR_AMON when charger is not powered to counter TL331 bias current.

Q7074 SSM6N15FEAPE SOT563

PP5V1_CHGR_VDD

(CHGR_AGATE)

CRITICAL
D7005
BAT30CWFILM
SOT-323

(CHGR_DCIN)

R7021 10 5% 1/16W MF-LF 402

R7022 10 5% 1/16W MF-LF 402

C7020 0.047UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY

CHGR_CSI_R_P

CHGR_CSI_R_N

CRITICAL
R7020 0.02 0.5% 1W MF 0612

=PPBUS_G3H
TO SYSTEM

=PP3V42_G3H_CHGR

ACIN pin threshold is 3.2V, +/- 50mV

Divider sets ACIN threshold at 13.07V

Input impedance of ~40K meets sparkitecture requirements

C7002 1UF 10% 10V X5R 402

PP5V1_CHGR_VDD
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

30mA max load

R7001 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

C7001 1UF 10% 10V X5R 402

C7022 0.1UF 10% 25V X5R 402

C7021 0.1UF 10% 25V X5R 402

C7035 0.22UF 10% 16V CERM 402

GND_CHGR_AGND

PPDCIN_S5_FET_CHGR
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

CRITICAL
Q7030
RJK0305DPB
LFPAK-HF

152S0542

CRITICAL
Q7031
RJK0305DPB
LFPAK-HF

152S0542

CRITICAL
C7030 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL
C7031 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL
C7036 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL
C7037 22UF 20% 25V POLY-TANT CASE-D2-SM

C7032 1UF 10% 25V X5R 603-1

C7033 1UF 10% 25V X5R 603-1

C7034 0.001UF 10% 50V X7R 402

CRITICAL
L7030
2.2UH-20A-5.5M-OHM
SM

CRITICAL
L7031
2.2UH-20A-5.5M-OHM
SM

PPVBAT_G3H_CHGR_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

PPVBAT_G3H_CHGR_REG_L
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE

CRITICAL
F7040
8AMP-24V
1206

CRITICAL
F7041
8AMP-24V
1206

CRITICAL
C7043 33UF 20% 16V POLY-TANT CASED2E-SM

CRITICAL
C7040 33UF 20% 16V POLY-TANT CASED2E-SM

C7041 0.001UF 10% 50V X7R 402

R7010 30.1K 1% 1/16W MF-LF 402

R7011 9.31K 1% 1/16W MF-LF 402

R7015 56.2K 1% 1/16W MF-LF 402

CHGR_VCOMP_R

C7050 0.1uF 10% 16V X5R 402
SIGNAL_MODEL=EMPTY

C7015 0.001UF 10% 50V CERM 402

R7016 3.01K 1% 1/16W MF-LF 402

CHGR_VNEG_R

C7016 470PF 10% 50V CERM 402

U7000
ISL6258A
QFN

VHST	12	
SCL	11	=SMBUS_CHGR_SCL
SDA	10	=SMBUS_CHGR_SDA
VREF	4	NC
ACIN	3	CHGR_ACIN
ICOMP	5	CHGR_ICOMP
VCOMP	7	CHGR_VCOMP
VNEG	8	CHGR_VNEG
CSOP	18	CHGR_CSO_P
CSON	17	CHGR_CSO_N
AGATE	1	CHGR_AGATE
CSIP	28	CHGR_CSI_P
CSIN	27	CHGR_CSI_N
BGATE	16	CHGR_BGATE
DCIN	2	CHGR_DCIN
BOOT	25	CHGR_BOOT
UGATE	24	CHGR_UGATE
PHASE	23	CHGR_PHASE
LGATE	21	CHGR_LGATE
(OD) TRKL*	13	TP_CHGR_TRKL
20V/V AMON	9	CHGR_AMON
32V/V BMON	15	CHGR_BMON
(OD) ACOK	14	=CHGR_ACOK
THRM_PAD	29	
AGND	20	
PGND	22	

OMIT

XW7000 SM

Max Current = 8.5A (L7030 limit)
f = 400 kHz

R7051 10 5% 1/16W MF-LF 402

R7052 10 5% 1/16W MF-LF 402

CHGR_CSO_R_P

CHGR_CSO_R_N

(CHGR_CSO_P)
(CHGR_CSO_N)
(PPVBAT_G3H_CHGR_R)

CRITICAL
Q7035
RJK0305DPB
LFPAK-HF

NO STUFF
R7099 10 5% 1/10W MF-LF 603

CHGR_PHASE_RC

NO STUFF
C7099 0.001UF 10% 50V X7R 402

CRITICAL
Q7036
RJK0305DPB
LFPAK-HF

152S0542

CRITICAL
R7050 0.005 1% 1W MF 0612

PPVBAT_G3H_CHGR_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

C7055 1UF 10% 25V X5R 603-1

C7056 0.1UF 10% 16V X5R 402

C7057 0.01UF 10% 16V CERM 402

CRITICAL
HAT1127H
LFPAK-SM
Q7057

CRITICAL
HAT1127H
LFPAK-SM
Q7058

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

CRITICAL
HAT1127H
LFPAK-SM
Q7055

PPVBAT_G3H_FET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

CRITICAL
HAT1127H
LFPAK-SM
Q7056

PPVBAT_G3H_CONN
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

C7058 1UF 10% 16V X5R 402-1

BATT_POS_GATE

R7056 1M 5% MF-LF 402 1/16W

R7057 20K 5% MF-LF 402 1/16W

GND_BATT_CHGND

C7042 0.033UF 10% 16V X5R 402

C7000 1UF 10% 10V X5R 402

C7011 0.01UF 10% 16V CERM 402

C7005 0.1UF 10% 25V X5R 402

C7026 0.001UF 10% 50V CERM 402

GND_CHGR_AGND
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

M99 differences from last sync on 12/02/07 to T18 MLB:

1. L7030 changed from T18 MLB inductor to 152S0542.
2. Added Q7056, C7058,R7055,R7056..
3. U7000 Thermal Pad is now connected to GND, not through XW.
4. Q7060 and Q7065 changed to 376S0667.
5. Q7055 and Q7056 changed to 376S0666.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
353S1938	1	IC,ISL6258,BAT CHARGER,28P,4X4,QFN,L	U7000	CRITICAL	ISL6258	2S Battery Default
353S1832	1	IC,ISL6258A,BAT CHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6258A	3S Battery Default

PBus Supply & Battery Charger

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 60 OF 98	

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

Place R7131 Between L7100,L7101 and CPU

IMVP6 CPU VCore Regulator

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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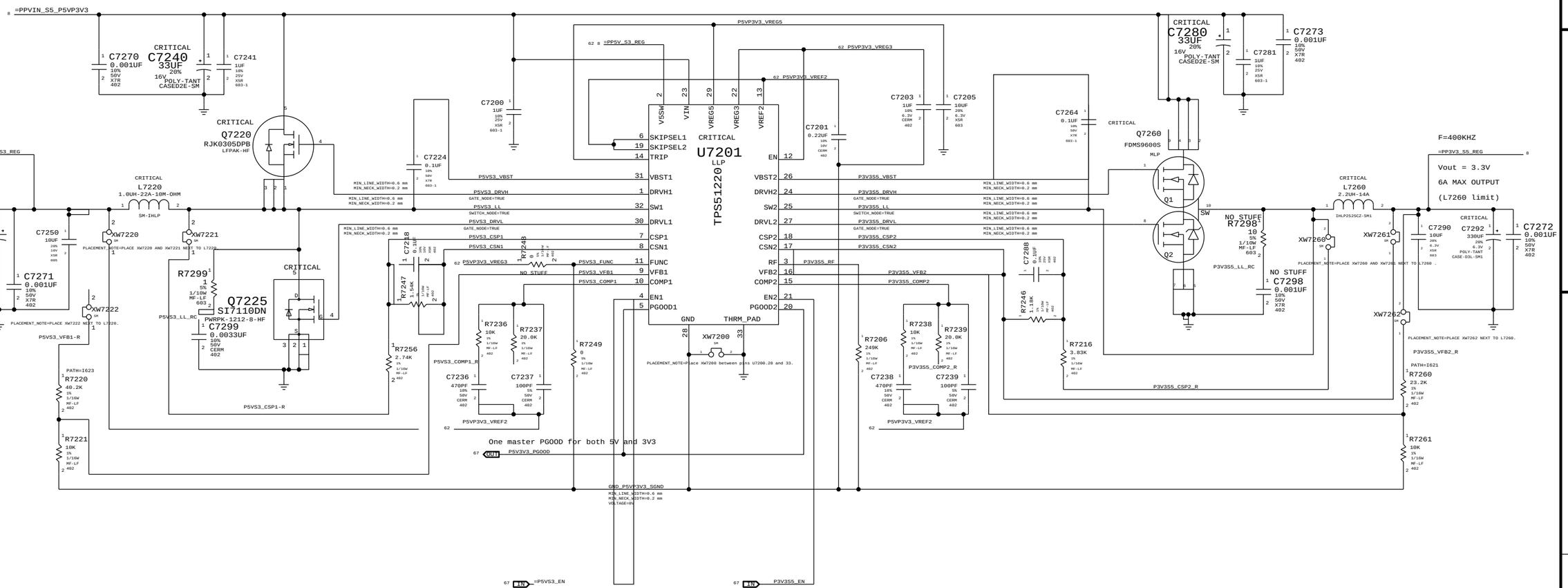
APPLE INC.

SIZE D | DRAWING NUMBER 051-8071 | REV. B

SCALE NONE | SHT 61 OF 98



5V / 3.3V Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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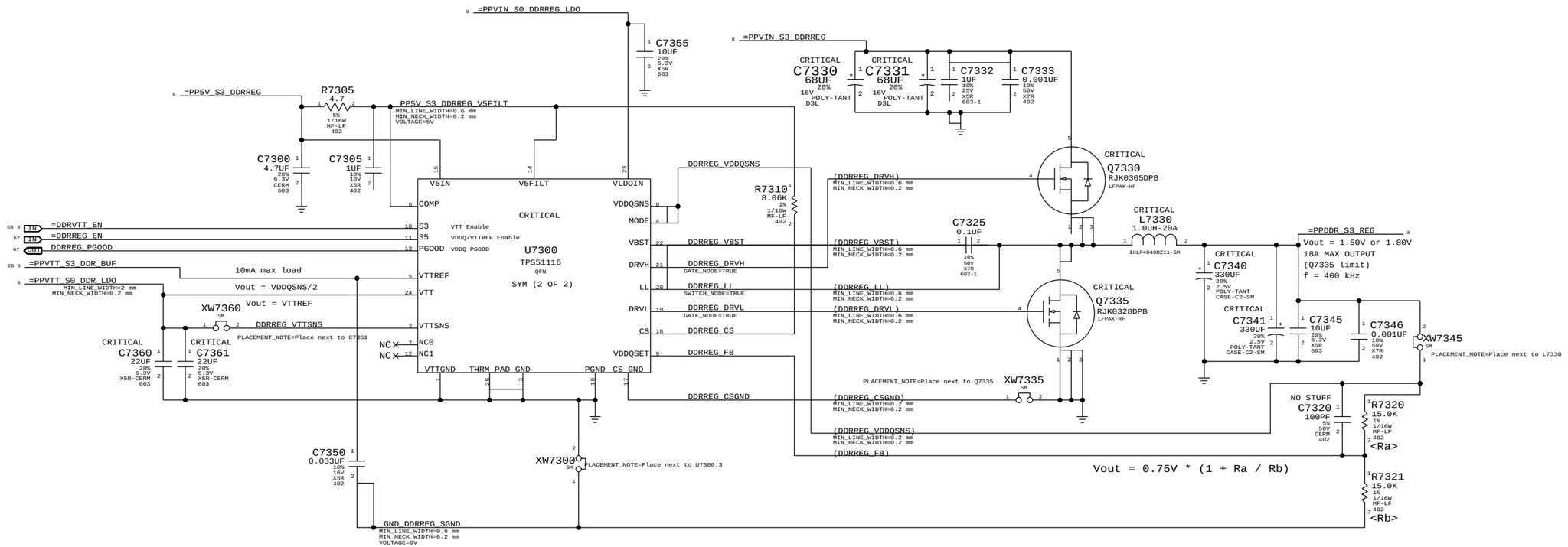
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 62 OF 98	



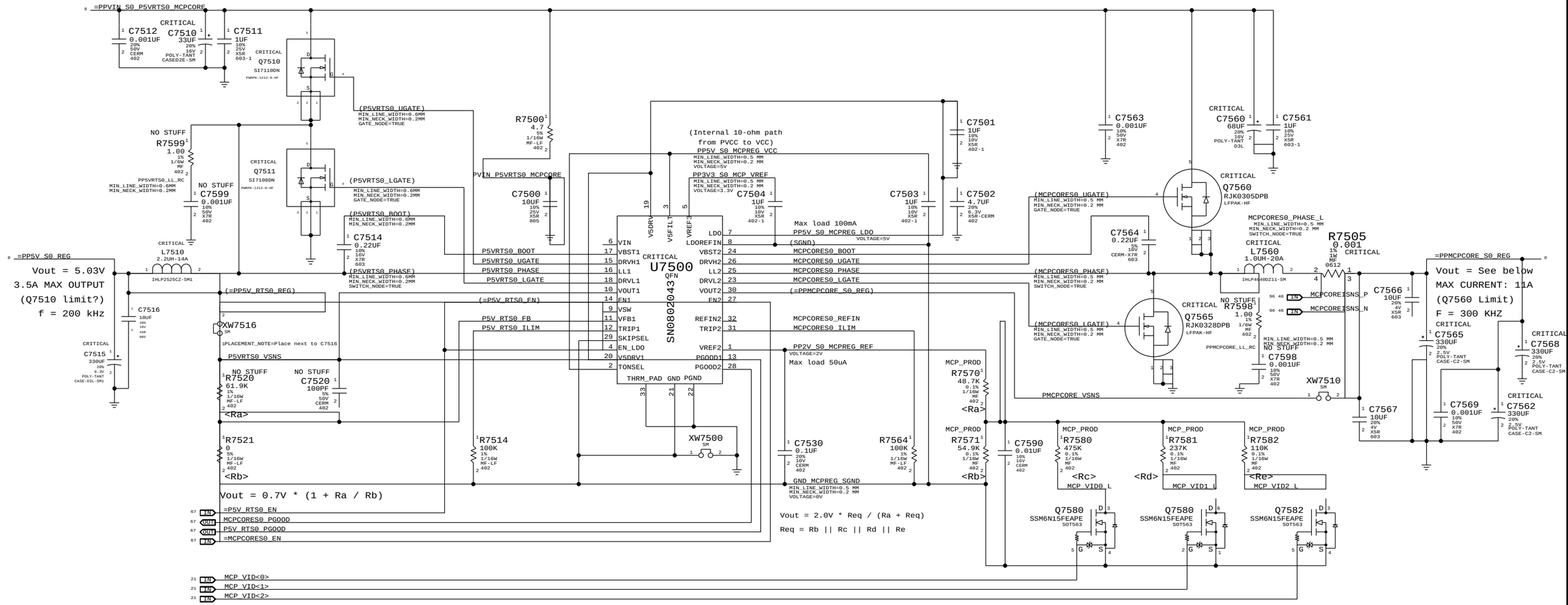
1.5V DDR3 Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 63 OF 98	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0382	1	RES,MTL FILM,1/16W,48.7K,1,0402,SMD,LF	R7570		MCP_A01
114S0400	1	RES,MTL FILM,1/16W,76.8K,1,0402,SMD,LF	R7571		MCP_A01
114S0482	1	RES,MTL FILM,1/16W,523K,1,0402,SMD,LF	R7580		MCP_A01
114S0453	1	RES,MTL FILM,1/16W,267K,1,0402,SMD,LF	R7581		MCP_A01
114S0422	1	RES,MTL FILM,1/16W,130K,1,0402,SMD,LF	R7582		MCP_A01
114S0373	1	RES,MTL FILM,1/16W,40.2K,1,0402,SMD,LF	R7570		MCP_A01Q
114S0404	1	RES,MTL FILM,1/16W,84.5K,1,0402,SMD,LF	R7571		MCP_A01Q
114S0458	1	RES,MTL FILM,1/16W,301K,1,0402,SMD,LF	R7580		MCP_A01Q
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R7581		MCP_A01Q
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7582		MCP_A01Q

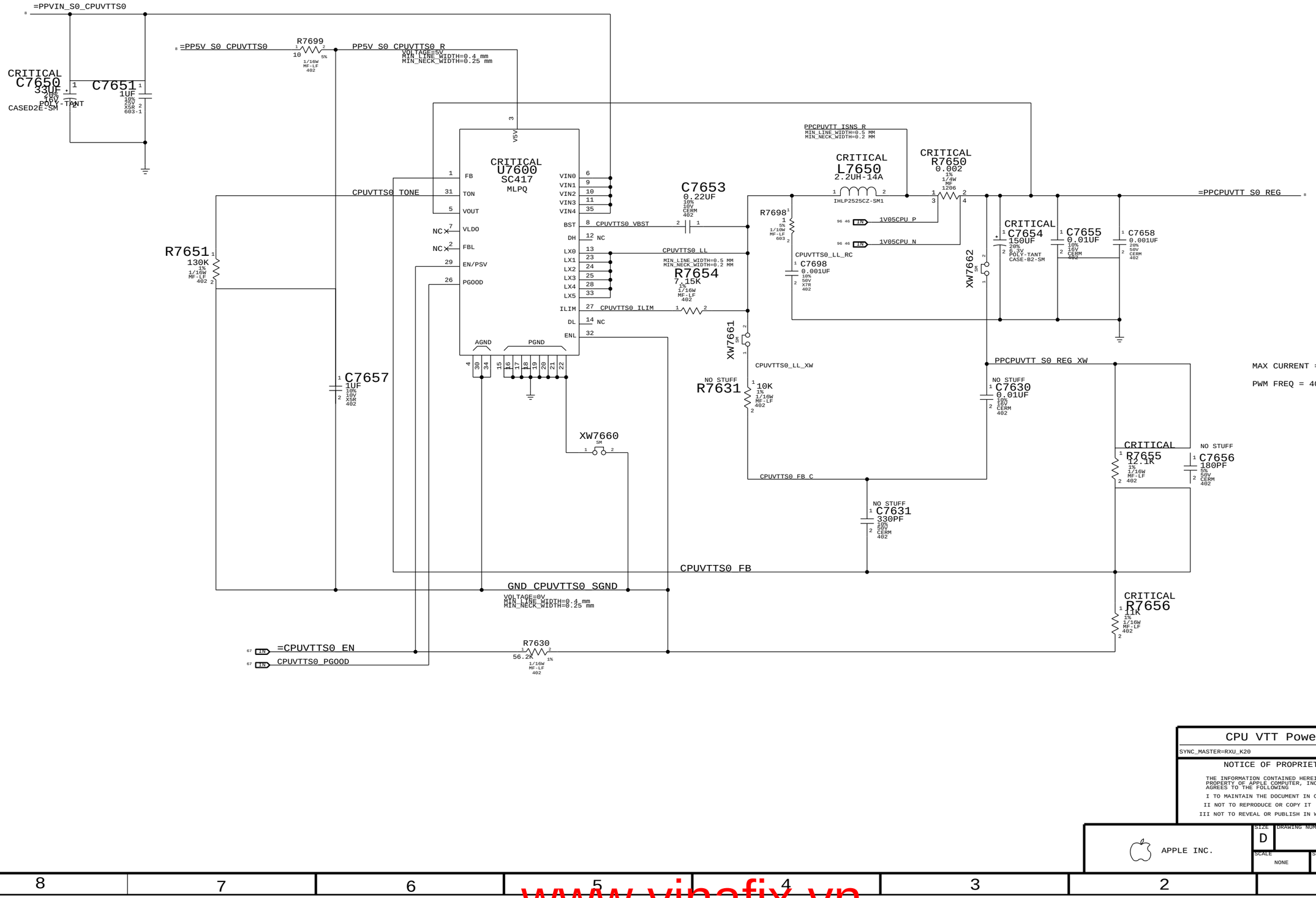
VID<2:0>	Rev A01 Voltage	Production Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

5V_S0 / MCP CORE REGULATOR

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 64 OF 98	

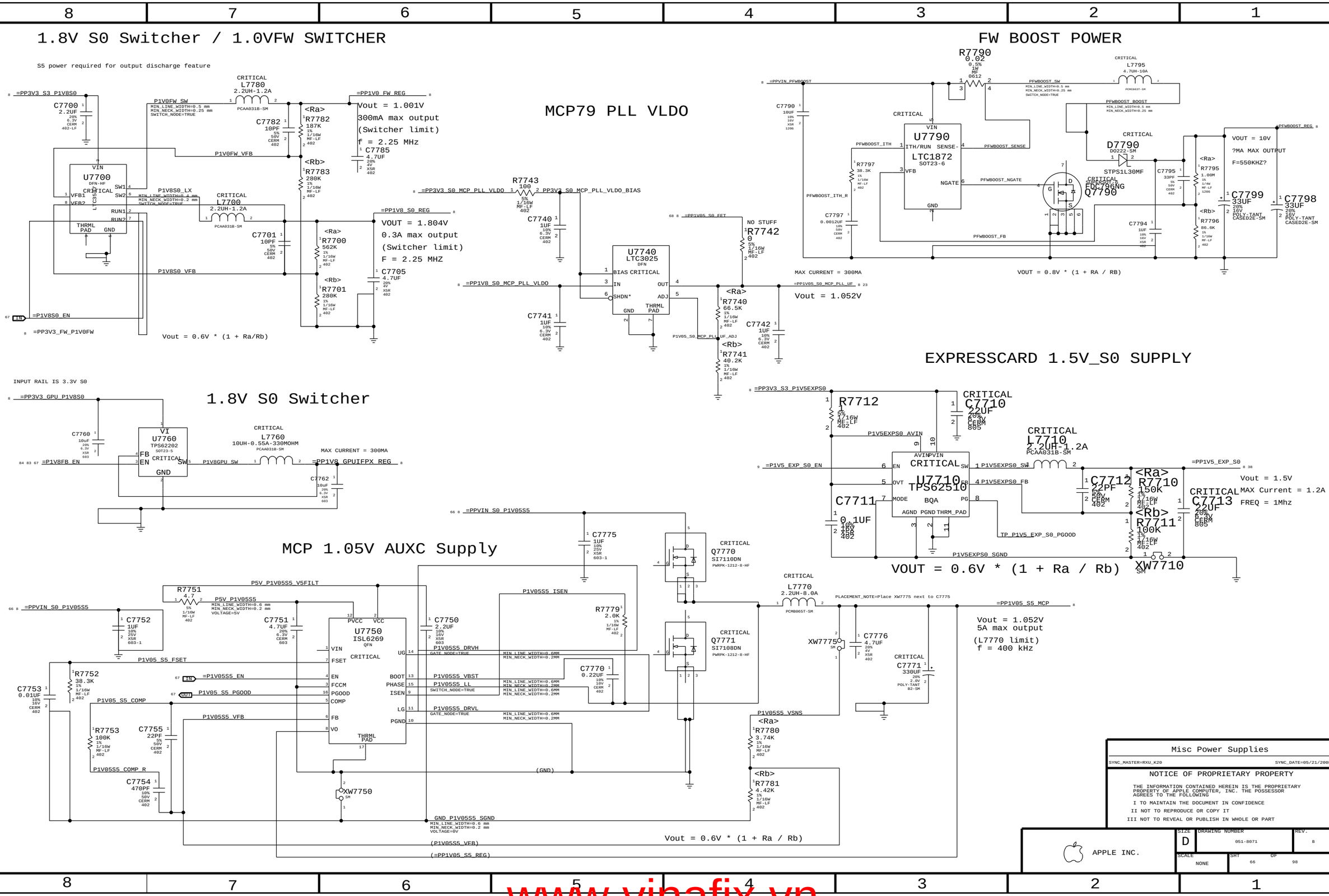


CPU VTT Power Supply

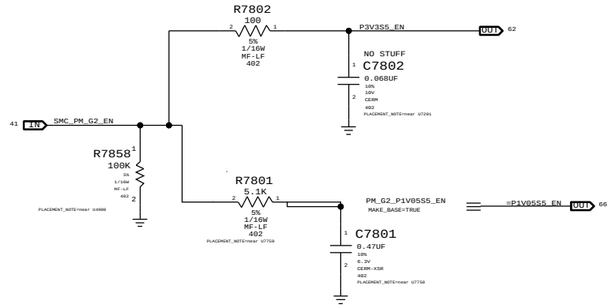
SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 65 OF 98	

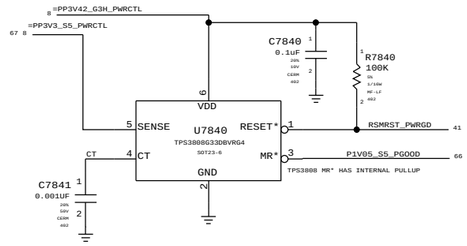


3.3V 1,05V S5 ENABLE

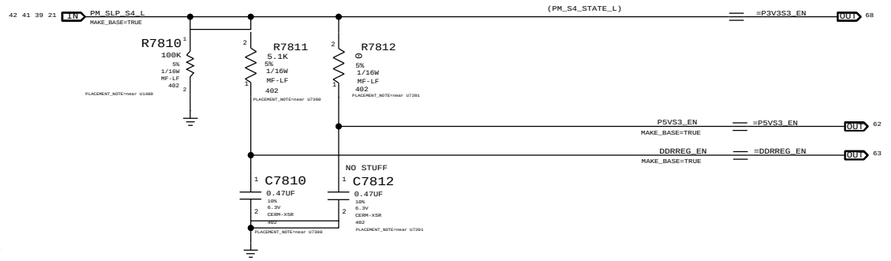


State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

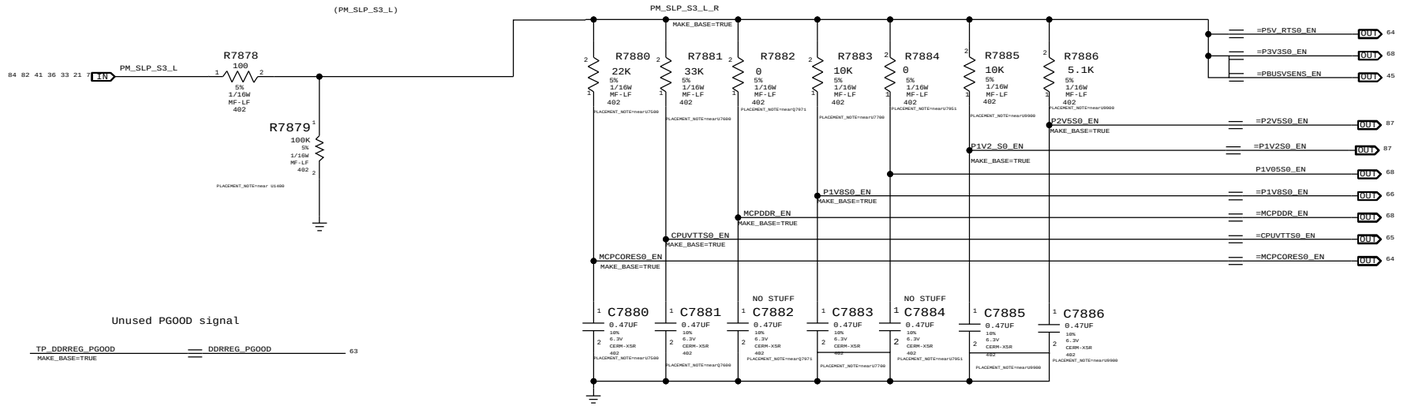
S5 rail PWRGD



3.3V,5V S3 ENABLE

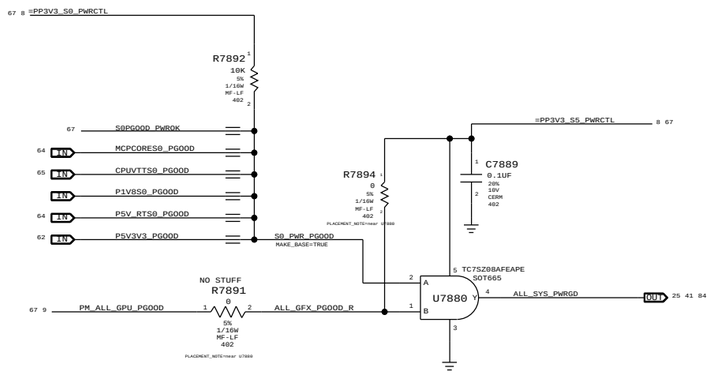


S0 ENABLE



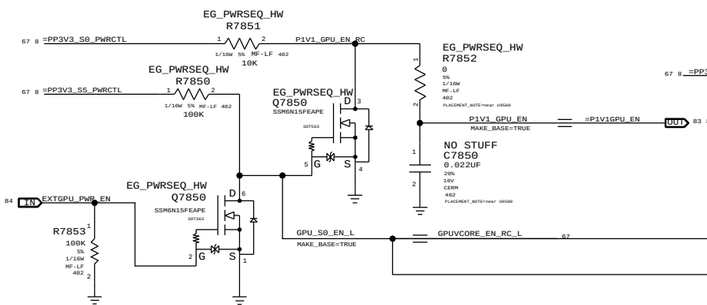
Other S0 RAILS

	PM_ALL_GFX_PGOOD
IG	high
EG	PM_ALL_GPU_PGOOD

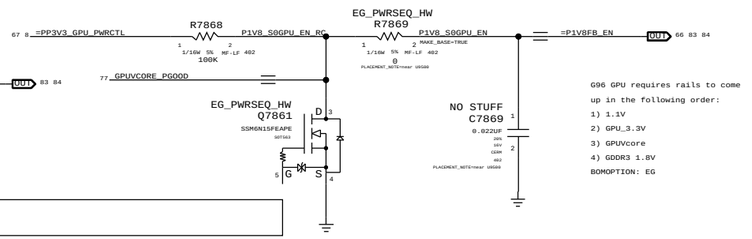


Unused PGOOD signal

1.1V GPU ENABLE

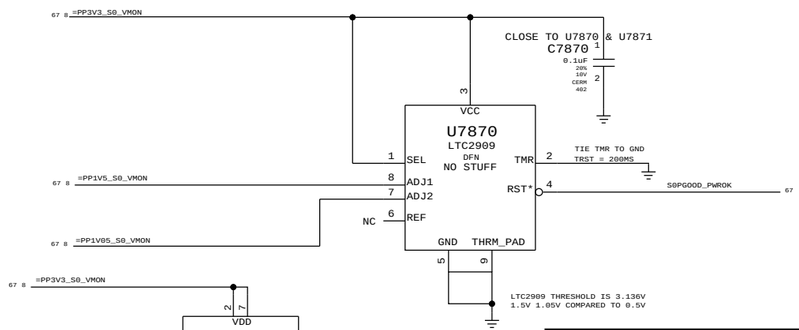


Graphic MEM ENABLE

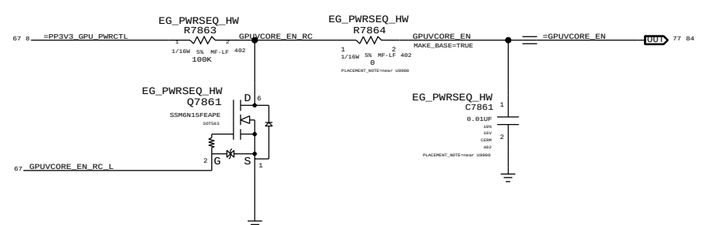


3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

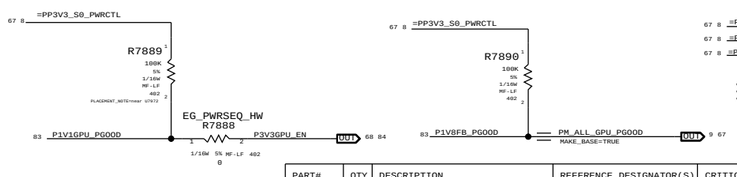
place XW0402 if needed to save trace space for pin 7,8



GPUVCORE ENABLE



EXT GPU PWRGD Pullup



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2718	1	IC, QUAD VOLTAGE MONITOR	U7871	CRITICAL	

U7871 IS TO REPLACE U7870

Power Control

SYNC_MASTER=YMA_K20 SYNC_DATE=09/09/2008

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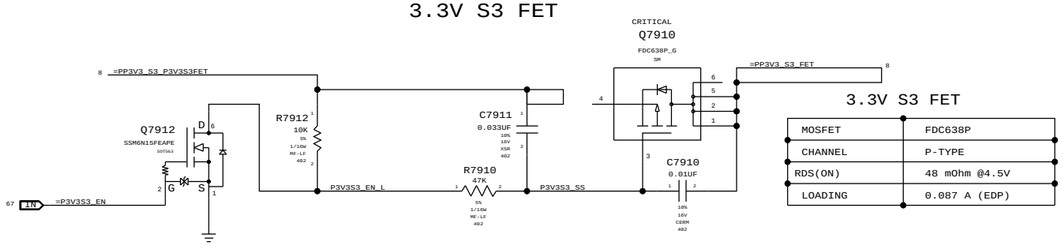
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE	SHT	OF
NONE	67	98

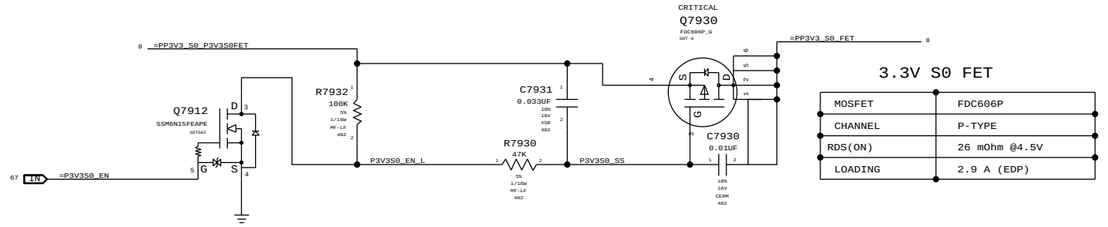
3.3V S3 FET



3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

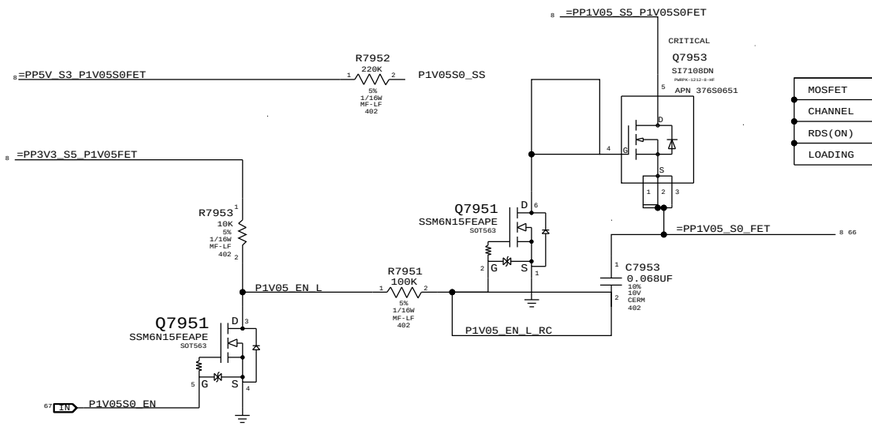
3.3V S0 FET



3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

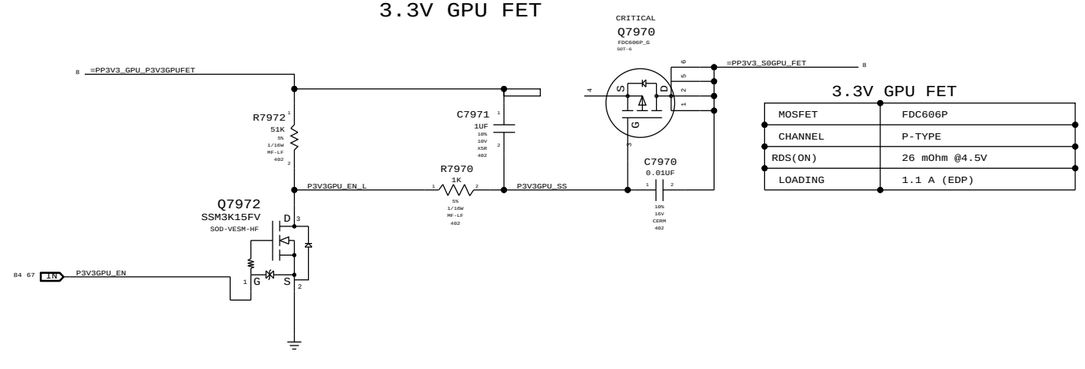
1.05V S0 FET



1.05V S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.1 A (EDP)

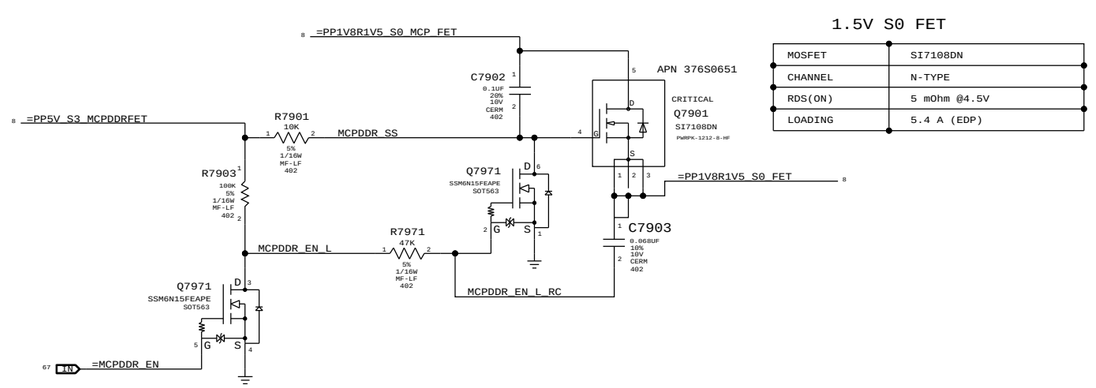
3.3V GPU FET



3.3V GPU FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)

1.5V S0 FET

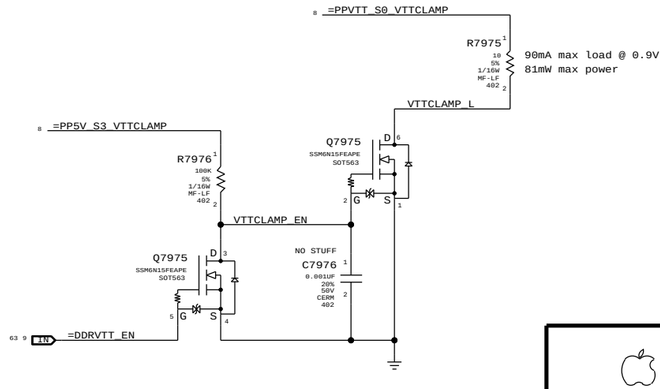


1.5V S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.4 A (EDP)

MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.



Power FETs

SYNC_MASTER=YMA_K20 SYNC_DATE=05/19/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 68 OF 98	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

8 =PP1V1_GPU_PEX_PLLXVDD
8 =PP1V1_GPU_PEX_IOVDDQ
8 =PP1V1_GPU_PEX_IOVDD

PEX 1.1V Current = 2A

250mA

C8002 1UF 10% 6.3V CERM 402
C8001 4.7UF 20% 6.3V CERM 603
C8000 22UF 20% 6.3V CERM-X5R 805
C8003 1UF 10% 6.3V CERM 402
C8004 0.1UF 20% 10V CERM 402
C8005 0.1UF 20% 10V CERM 402

1500mA

C8008 1UF 10% 6.3V CERM 402
C8007 4.7UF 20% 6.3V CERM 603
C8006 22UF 20% 6.3V CERM-X5R 805
C8009 1UF 10% 6.3V CERM 402
C8010 0.1UF 20% 10V CERM 402
C8011 0.1UF 20% 10V CERM 402

180mA

L8015 10NH-600MA 0603

PP1V1_GPU_PEX_PLLVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V

C8017 0.1UF 20% 10V CERM 402
C8016 4.7UF 20% 6.3V CERM 603
C8015 4.7UF 20% 6.3V CERM 603

NC_GPU_DFM
NO_TEST=TRUE

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PEX_IOVDD1	AK16
PEX_IOVDD2	AK17
PEX_IOVDD3	AK21
PEX_IOVDD4	AK24
PEX_IOVDD5	AK27
PEX_IOVDDQ1	AG11
PEX_IOVDDQ2	AG12
PEX_IOVDDQ3	AG13
PEX_IOVDDQ4	AG15
PEX_IOVDDQ5	AG16
PEX_IOVDDQ6	AG17
PEX_IOVDDQ7	AG18
PEX_IOVDDQ8	AG22
PEX_IOVDDQ9	AG23
PEX_IOVDDQ10	AG24
PEX_IOVDDQ11	AG25
PEX_IOVDDQ12	AG26
PEX_IOVDDQ13	AJ14
PEX_IOVDDQ14	AJ15
PEX_IOVDDQ15	AJ19
PEX_IOVDDQ16	AJ21
PEX_IOVDDQ17	AJ22
PEX_IOVDDQ18	AJ24
PEX_IOVDDQ19	AJ25
PEX_IOVDDQ20	AJ27
PEX_IOVDDQ21	AK18
PEX_IOVDDQ22	AK20
PEX_IOVDDQ23	AK23
PEX_IOVDDQ24	AK26
PEX_IOVDDQ25	AL16
PEX_PLLVDD	AG14
VDD_SENSE	AD20
GND_SENSE	AD19

NC: AG22, AG7, AF6, AG7, AG6, AG8, AE6, AE8, AG6, E25, D25, AK15, AL7, J7, E35, L7, J2

VDD_SENSE → GPU_VDD_SENSE 77
GND_SENSE → GPU_GND_SENSE 77

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PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AP17 PEX_RX0
PEG_R2D_C_N<0>	C8021 0.1uF	PEG_R2D_N<0>	AN17 PEX_RX0*
PEG_R2D_C_P<1>	C8022 0.1uF	PEG_R2D_P<1>	AN19 PEX_RX1
PEG_R2D_C_N<1>	C8023 0.1uF	PEG_R2D_N<1>	AP19 PEX_RX1*
PEG_R2D_C_P<2>	C8024 0.1uF	PEG_R2D_P<2>	AR19 PEX_RX2
PEG_R2D_C_N<2>	C8025 0.1uF	PEG_R2D_N<2>	AR20 PEX_RX2*
PEG_R2D_C_P<3>	C8026 0.1uF	PEG_R2D_P<3>	AP20 PEX_RX3
PEG_R2D_C_N<3>	C8027 0.1uF	PEG_R2D_N<3>	AN20 PEX_RX3*
PEG_R2D_C_P<4>	C8028 0.1uF	PEG_R2D_P<4>	AN22 PEX_RX4
PEG_R2D_C_N<4>	C8029 0.1uF	PEG_R2D_N<4>	AP22 PEX_RX4*
PEG_R2D_C_P<5>	C8030 0.1uF	PEG_R2D_P<5>	AR22 PEX_RX5
PEG_R2D_C_N<5>	C8031 0.1uF	PEG_R2D_N<5>	AR23 PEX_RX5*
PEG_R2D_C_P<6>	C8032 0.1uF	PEG_R2D_P<6>	AP23 PEX_RX6
PEG_R2D_C_N<6>	C8033 0.1uF	PEG_R2D_N<6>	AN23 PEX_RX6*
PEG_R2D_C_P<7>	C8034 0.1uF	PEG_R2D_P<7>	AN25 PEX_RX7
PEG_R2D_C_N<7>	C8035 0.1uF	PEG_R2D_N<7>	AP25 PEX_RX7*
PEG_R2D_C_P<8>	C8036 0.1uF	PEG_R2D_P<8>	AR25 PEX_RX8
PEG_R2D_C_N<8>	C8037 0.1uF	PEG_R2D_N<8>	AR26 PEX_RX8*
PEG_R2D_C_P<9>	C8038 0.1uF	PEG_R2D_P<9>	AP26 PEX_RX9
PEG_R2D_C_N<9>	C8039 0.1uF	PEG_R2D_N<9>	AN26 PEX_RX9*
PEG_R2D_C_P<10>	C8040 0.1uF	PEG_R2D_P<10>	AN28 PEX_RX10
PEG_R2D_C_N<10>	C8041 0.1uF	PEG_R2D_N<10>	AP28 PEX_RX10*
PEG_R2D_C_P<11>	C8042 0.1uF	PEG_R2D_P<11>	AR28 PEX_RX11
PEG_R2D_C_N<11>	C8043 0.1uF	PEG_R2D_N<11>	AR29 PEX_RX11*
PEG_R2D_C_P<12>	C8044 0.1uF	PEG_R2D_P<12>	AP29 PEX_RX12
PEG_R2D_C_N<12>	C8045 0.1uF	PEG_R2D_N<12>	AN29 PEX_RX12*
PEG_R2D_C_P<13>	C8046 0.1uF	PEG_R2D_P<13>	AN31 PEX_RX13
PEG_R2D_C_N<13>	C8047 0.1uF	PEG_R2D_N<13>	AP31 PEX_RX13*
PEG_R2D_C_P<14>	C8048 0.1uF	PEG_R2D_P<14>	AR31 PEX_RX14
PEG_R2D_C_N<14>	C8049 0.1uF	PEG_R2D_N<14>	AR32 PEX_RX14*
PEG_R2D_C_P<15>	C8050 0.1uF	PEG_R2D_P<15>	AR34 PEX_RX15
PEG_R2D_C_N<15>	C8051 0.1uF	PEG_R2D_N<15>	AP34 PEX_RX15*

All: 10% 16V X5R 402

PEG_CLK100M_P			AR16 PEX_REFCLK
PEG_CLK100M_N			AR17 PEX_REFCLK*
GPU_RESET_L	R8020 0 5% 1/16W MF-LF 402	GPU_RESET_R_L	AM16 PEX_RST*
TP_PEX_CLKREQ_L			AR13 PEX_CLKREQ*

PEX_TX0	AL17	PEG_D2R_C_P<0>	C8055 0.1uF
PEX_TX0*	AM17	PEG_D2R_C_N<0>	C8056 0.1uF
PEX_TX1	AM18	PEG_D2R_C_P<1>	C8057 0.1uF
PEX_TX1*	AM19	PEG_D2R_C_N<1>	C8058 0.1uF
PEX_TX2	AL19	PEG_D2R_C_P<2>	C8059 0.1uF
PEX_TX2*	AK19	PEG_D2R_C_N<2>	C8060 0.1uF
PEX_TX3	AL20	PEG_D2R_C_P<3>	C8061 0.1uF
PEX_TX3*	AM20	PEG_D2R_C_N<3>	C8062 0.1uF
PEX_TX4	AM21	PEG_D2R_C_P<4>	C8063 0.1uF
PEX_TX4*	AM22	PEG_D2R_C_N<4>	C8064 0.1uF
PEX_TX5	AL22	PEG_D2R_C_P<5>	C8065 0.1uF
PEX_TX5*	AK22	PEG_D2R_C_N<5>	C8066 0.1uF
PEX_TX6	AL23	PEG_D2R_C_P<6>	C8067 0.1uF
PEX_TX6*	AM23	PEG_D2R_C_N<6>	C8068 0.1uF
PEX_TX7	AM24	PEG_D2R_C_P<7>	C8069 0.1uF
PEX_TX7*	AM25	PEG_D2R_C_N<7>	C8070 0.1uF
PEX_TX8	AL25	PEG_D2R_C_P<8>	C8071 0.1uF
PEX_TX8*	AK25	PEG_D2R_C_N<8>	C8072 0.1uF
PEX_TX9	AL26	PEG_D2R_C_P<9>	C8073 0.1uF
PEX_TX9*	AM26	PEG_D2R_C_N<9>	C8074 0.1uF
PEX_TX10	AM27	PEG_D2R_C_P<10>	C8075 0.1uF
PEX_TX10*	AM28	PEG_D2R_C_N<10>	C8076 0.1uF
PEX_TX11	AL28	PEG_D2R_C_P<11>	C8077 0.1uF
PEX_TX11*	AK28	PEG_D2R_C_N<11>	C8078 0.1uF
PEX_TX12	AK29	PEG_D2R_C_P<12>	C8079 0.1uF
PEX_TX12*	AL29	PEG_D2R_C_N<12>	C8080 0.1uF
PEX_TX13	AM29	PEG_D2R_C_P<13>	C8081 0.1uF
PEX_TX13*	AM30	PEG_D2R_C_N<13>	C8082 0.1uF
PEX_TX14	AM31	PEG_D2R_C_P<14>	C8083 0.1uF
PEX_TX14*	AM32	PEG_D2R_C_N<14>	C8084 0.1uF
PEX_TX15	AN32	PEG_D2R_C_P<15>	C8085 0.1uF
PEX_TX15*	AP32	PEG_D2R_C_N<15>	C8086 0.1uF

All: 10% 16V X5R 402

PEX_TSTCLK_OUT	AJ17	PEX_TSTCLK_P
PEX_TSTCLK_OUT*	AJ18	PEX_TSTCLK_N
PEX_TERMP	AG21	PEX_TERMP_PD
PEX_RFU1	AG19	NC
PEX_RFU2	AG20	NC

R8060 200 1% 1/16W MF-LF 402
R8050 2.49K 1% 1/16W MF-LF 402

NV G96 PCI-E

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 69 OF 98	

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 4.7UF 20% 6.3V X5R-CERM 402
C8101 4.7UF 20% 6.3V X5R-CERM 402
C8102 4.7UF 20% 6.3V X5R-CERM 402
C8103 0.47UF 10% 6.3V CERM-X5R 402
C8104 0.47UF 10% 6.3V CERM-X5R 402
C8105 0.47UF 10% 6.3V CERM-X5R 402
C8106 0.47UF 10% 6.3V CERM-X5R 402
C8107 0.47UF 10% 6.3V CERM-X5R 402
C8108 0.47UF 10% 6.3V CERM-X5R 402
C8109 0.47UF 10% 6.3V CERM-X5R 402
C8110 0.47UF 10% 6.3V CERM-X5R 402
C8111 0.47UF 10% 6.3V CERM-X5R 402
C8112 0.47UF 10% 6.3V CERM-X5R 402
C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
C8115 0.1UF 20% 10V CERM 402
C8116 0.1UF 20% 10V CERM 402
C8117 0.1UF 20% 10V CERM 402
C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

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L11 L12 L13 L14 L15 L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 M12 M14 M16 M18 M20 M22 M24 P11 P13 P15 P17 P19 P21 P23 P25 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 T12 T14 T16 T18 T20 T22 T24 V11 V13 V15 V17
VDD
V19 V21 V23 V25 W11 W12 W13 W14 W15 W16 W17 W18 W19 AD24 W21 W22 W23 W24 W25 Y12 Y14 Y16 Y18 Y20 Y22 Y24 AB11 AB13 AB15 AB17 AB19 AB21 AB23 AB25 AC11 AC12 AC13 AC14 AC15 AC16 AC17 AC18 AC19 AC20 AC21 AC22 AC23 AC24 AC25 AD12 AD14 AD16 AD18 AD22 W20
VDD

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B3 B6 B9 B12 B15 B21 B24 B27 B30 B33 C2 C34 E6 E9 E12 E15 E18 E24 E27 E30 F2 F5 F31 F34 J2 J5 J31 J34 L9 M2 M5 M11 M13 M15 M17 M19 M21 M23 M25 M31 M34 N11 N12 N13 N14 N15 N16 N17 N18 N19 N20 N21 N22 N23 N24 N25 P12 P14 P16 P18 P20 P22 P24 R2 R5 R31 R34 T11 T13 T15 T17 T19 T21 T23 T25 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 V2 V5 V9 V12 V14 V16
GND
GND
V18 V20 V22 V24 V31 Y11 Y13 Y15 Y17 Y19 Y21 Y23 Y25 AA2 AA5 AA11 AA12 AA13 AA14 AA15 AA16 AA17 AA18 AA19 AA20 AA21 AA22 AA23 AA24 AA25 AA34 AB12 AB14 AB16 AB18 AB20 AB22 AB24 AC9 AD2 AD5 AD11 AD13 AD15 AD17 AD21 AD23 AD25 AD31 AD34 AE11 AE12 AE13 AE14 AE15 AE16 AE17 AE18 AE19 AE20 AE21 AE22 AE23 AE24 AE25 AG2 AG5 AG31 AG34 AK2 AK5 AP33 AK31 AK34 AL6 AL9 AL12 AL15 AL18 AL21 AL24 AL27 AL30 AN2 AN34 AP3 AP6 AP9 AP12 AP15 AP18 AP21 AP24 AP27 AP30

=PP1V8_GPU_FBVDDQ

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603
C8156 0.1UF 20% 10V CERM 402
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402
C8162 0.1UF 20% 10V CERM 402
C8163 0.1UF 20% 10V CERM 402
C8164 0.1UF 20% 10V CERM 402
C8165 0.1UF 20% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402
C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

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B18 J17 U27 AB27 AB29 AC27 AD27 AE27 AJ28 E21 G8 G9 G17 G18 G22 H29 J14 J15 J16
FBVDDQ
J20 J21 J22 J23 J24 J29 N27 P27 R27 T27 U29 V27 V29 V34 W27 Y27 AA27 AA29 AA31
FBVDDQ

NV G96 CORE/FB POWER

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

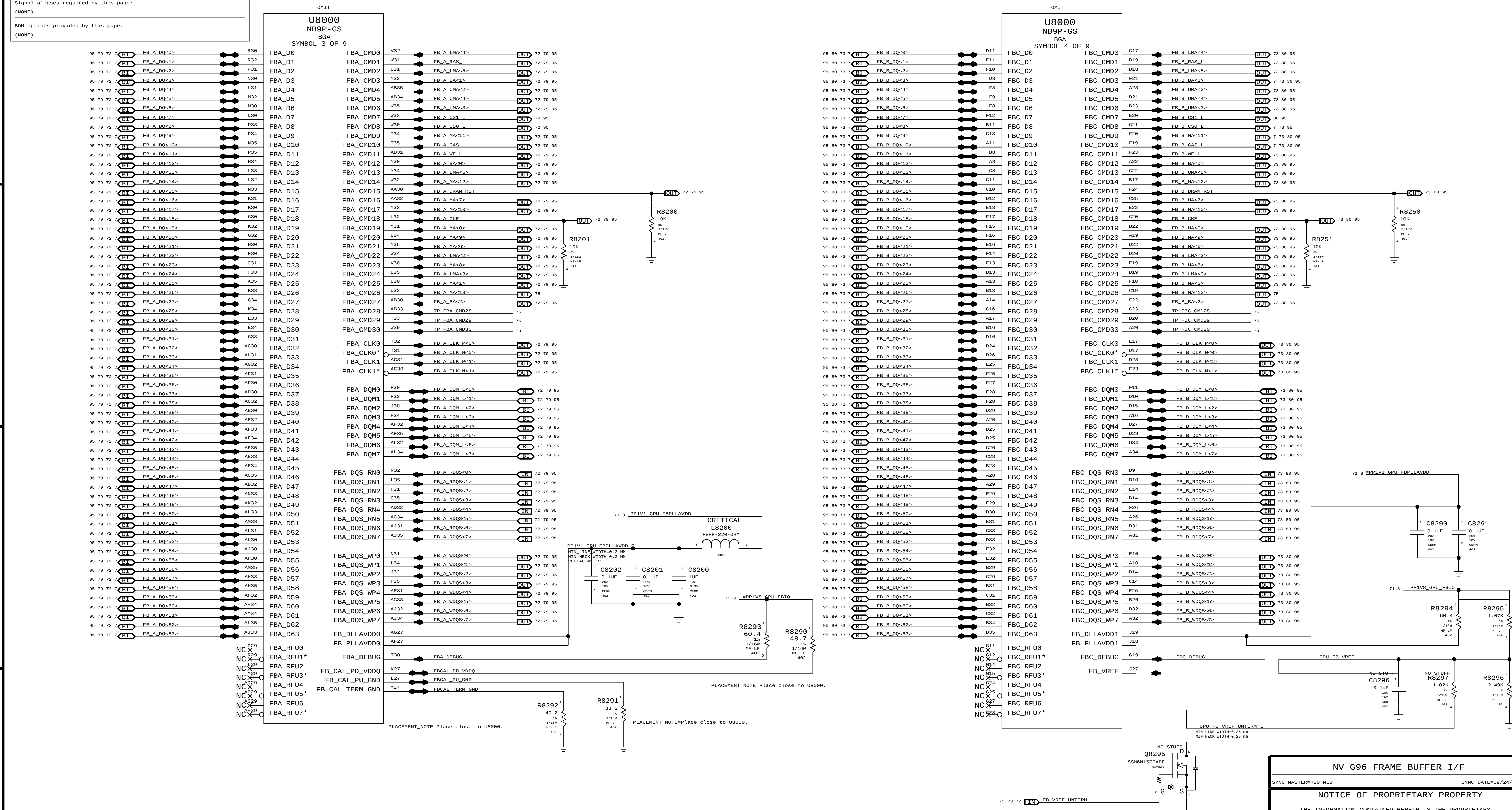
SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT	OF
NONE	70	98

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

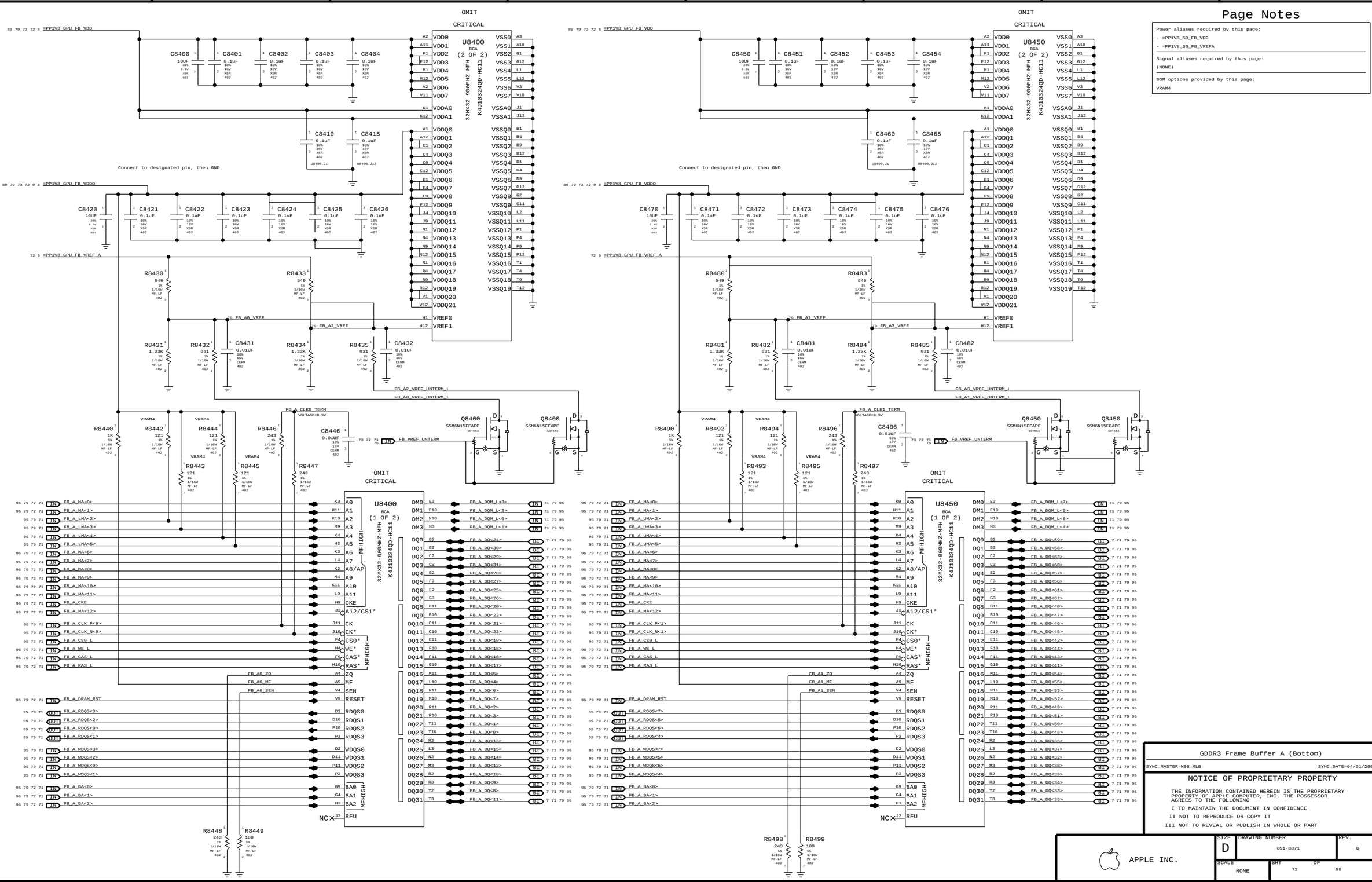


NV G96 FRAME BUFFER I/F

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE NONE	SHT 71	OF 98



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA

Signal aliases required by this page:
(NONE)

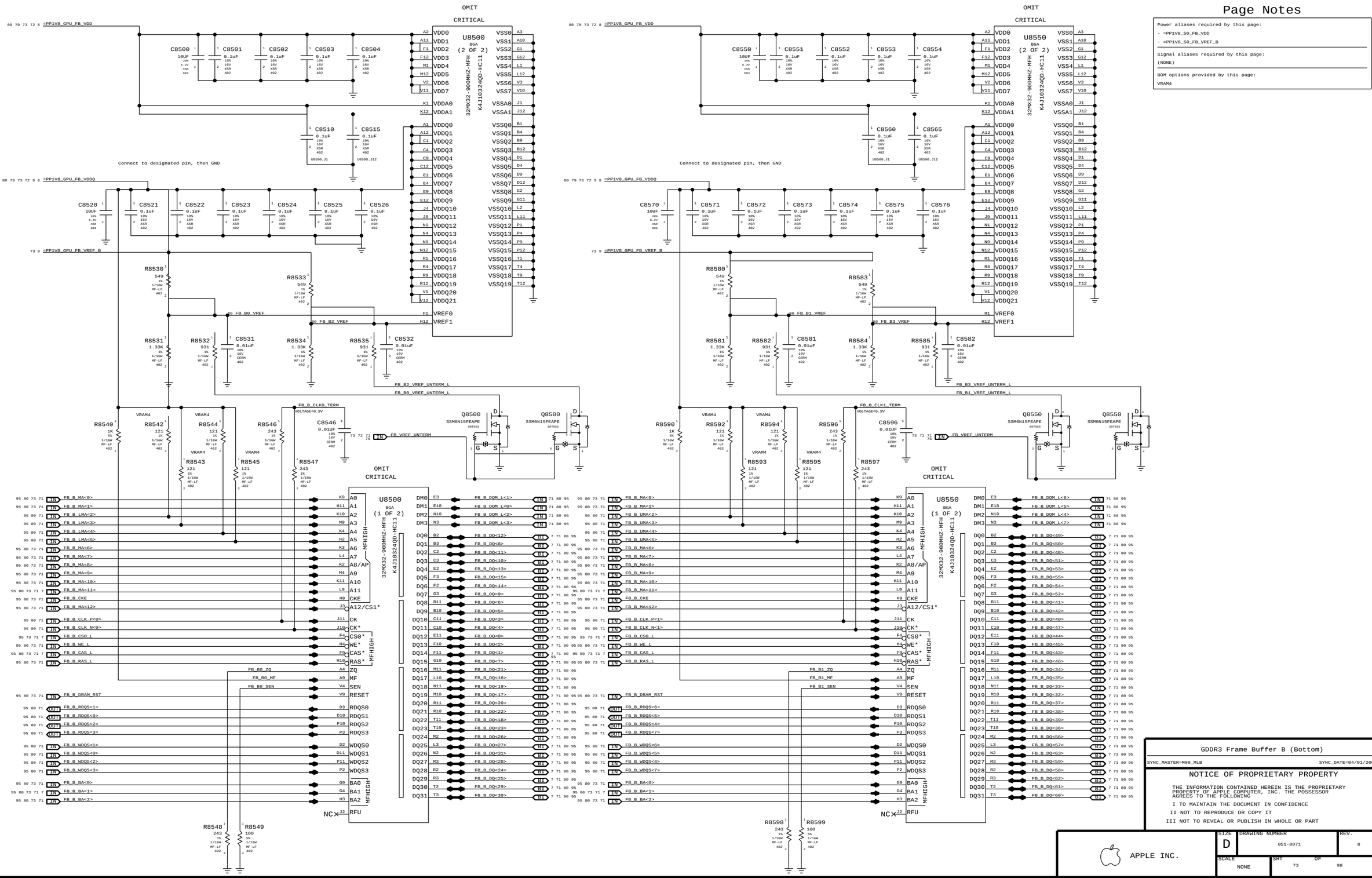
BOM options provided by this page:
VRAM4

GDDR3 Frame Buffer A (Bottom)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 72 OF 98	



Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

110mA
75 74 8 6 =PP3V3_GPU_VDD33

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C8690 0.022UF 10% 16V CERM-X5R 402
C8692 0.022UF 10% 16V CERM-X5R 402
C8694 0.1UF 20% 10V CERM 402
C8696 0.47UF 10% 6.3V CERM-X5R 402
C8698 1UF 10% 6.3V CERM 402
C8691 0.022UF 10% 16V CERM-X5R 402
C8693 0.022UF 10% 16V CERM-X5R 402
C8695 0.1UF 20% 10V CERM 402
C8697 0.47UF 10% 6.3V CERM-X5R 402

VDD33_1 J9
VDD33_2 J10
VDD33_3 J11
VDD33_4 J12
VDD33_5 J13

75 =PP3V3_GPU_VDD33
Typically <??mA
C8600 0.47UF 10% 6.3V CERM-X5R 402
C8601 0.47UF 10% 6.3V CERM-X5R 402
C8602 0.47UF 10% 6.3V CERM-X5R 402

NC RFU0 J25
NC RFU1 J26
RFU0_GND AK14
RFU1_GND K9

75 GPU_ROM_CS_L → ROM_CS* C3
75 GPU_ROM_SCLK → ROM_SCLK D4
75 GPU_ROM_SI → ROM_SI D3
75 GPU_ROM_SO → ROM_SO C4

R8696 40.2K 1% 1/16W MF-LF 402
R8697 40.2K 1% 1/16W MF-LF 402

GPU_STRAP_REF_3V3_PD → STRAP_REF_3V3 N9
GPU_STRAP_REF_MIOB_PD → STRAP_REF_MIOB (IPD) M9

75 74 8 =PP3V3_GPU_MIO

MIOA_VDDQ_1 P9
MIOA_VDDQ_2 R9
MIOA_VDDQ_3 T9
MIOA_VDDQ_4 U9
MIOB_VDDQ_1 AA9
MIOB_VDDQ_2 AB9
MIOB_VDDQ_3 W9
MIOB_VDDQ_4 Y9

C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402

75 74 8 =PP3V3_GPU_MIO
R8620 49.9 1% 1/16W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ 74
GPU_MIOB_PD_VDDQ 74
GPU_MIOA_PU_GND 74
GPU_MIOB_PU_GND 74
R8622 49.9 1% 1/16W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402

R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
C8617 0.1uF 10% 16V X5R 402
R8619 10K 5% 1/16W MF-LF 402
C8619 0.1uF 10% 16V X5R 402
R8660 10K 5% 1/16W MF-LF 402

GPU_TESTMODE_PD → TESTMODE AP35
GPU_MIOA_VREF → MIOA_VREF N5
GPU_MIOB_VREF → MIOB_VREF AF1
74 GPU_MIOA_PD_VDDQ
74 GPU_MIOA_PU_GND → MIOA_CAL_PD_VDDQ U5, MIOA_CAL_PU_GND T5
74 GPU_MIOB_PD_VDDQ → MIOB_CAL_PD_VDDQ AA7
74 GPU_MIOB_PU_GND → MIOB_CAL_PU_GND AA6

CRITICAL
L8630 FERR-220-OHM 0402
8 =PP1V1_GPU_PLLVDD
PP1V1_GPU_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
65mA
C8633 4.7UF 20% 6.3V CERM 603
C8630 4.7UF 20% 6.3V CERM 603
C8631 0.1uF 10% 16V X5R 402

CRITICAL
L8635 FERR-220-OHM 0402
8 =PP1V1_GPU_H_PLLVDD
PP1V1_GPU_H_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
25mA
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 0.1uF 10% 16V X5R 402

CRITICAL
L8640 FERR-220-OHM 0402
8 =PP1V1_GPU_VID_PLLVDD
PP1V1_GPU_VID_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
50mA
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 0.1uF 10% 16V X5R 402

SP_PLLVDD AF9
PLLVDD AE9
VID_PLLVDD AD9

75 IN GPU_XTALIN → XTAL_IN B1
75 OUT GPU_XTALOUT → XTAL_OUT B2
75 OUT GPU_XTALOUTBUFF → XTAL_OUTBUFF D1
75 IN GPU_XTALSSIN → XTAL_SSIN D2

GPIO0	K1	GPU_GPIO_0	B1		75
GPIO1	K2	GPU_GPIO_1	B1		75
GPIO2	K3	GPU_GPIO_2	B1		75
GPIO3	H3	GPU_GPIO_3	B1		75
GPIO4	H2	GPU_GPIO_4	B1		75
GPIO5	H1	GPU_GPIO_5	B1		75
GPIO6	H4	GPU_GPIO_6	B1		75
GPIO7	H5	GPU_GPIO_7	B1		75
GPIO8	H6	GPU_GPIO_8	B1		75
GPIO9	J7	GPU_GPIO_9	B1		75
GPIO10	K4	GPU_GPIO_10	B1		75
GPIO11	K5	GPU_GPIO_11	B1		75
GPIO12	H7	GPU_GPIO_12	B1		75
GPIO13	J4	GPU_GPIO_13	B1		75
GPIO14	J6	GPU_GPIO_14	B1		75
GPIO15	L1	GPU_GPIO_15	B1		75
GPIO16	L2	GPU_GPIO_16	B1		75
GPIO17	L4	GPU_GPIO_17	B1		75
GPIO18	M4	GPU_GPIO_18	B1		75
GPIO19	L7	GPU_GPIO_19	B1		75
GPIO20	L5	GPU_GPIO_20	B1		75
GPIO21	K6	GPU_GPIO_21	B1		75
GPIO22	L6	GPU_GPIO_22	B1		75
GPIO23	M6	GPU_GPIO_23	B1		75
HDA_SDI	C7	GPU_HDA_SDI		OUT	75
HDA_SDO	B7	GPU_HDA_SDO		OUT	75
HDA_SYNC	A7	GPU_HDA_SYNC		OUT	75
HDA_BCLK	D7	GPU_HDA_BCLK		OUT	75
HDA_RST*	D6	GPU_HDA_RST_L		OUT	75
SPDIF	A5	GPU_SPDIF		IN	75
BUFRST*	A4	TP_GPU_BUFRST_L		OUT	7
JTAG_TCK	AP14	GPU_JTAG_TCK		IN	6
JTAG_TDI	AN14	GPU_JTAG_TDI		IN	6
JTAG_TDO	AN16	GPU_JTAG_TDO		OUT	6
JTAG_TMS	AR14	GPU_JTAG_TMS		IN	6
JTAG_TRST*	AP16	GPU_JTAG_TRST_L		IN	6
MIOA_CLKIN	N4	GPU_MIOA_CLKIN		IN	75
MIOA_CLKOUT	R4	GPU_MIOA_CLKOUT_P	B1		75
MIOA_CLKOUT*	T4	GPU_MIOA_CLKOUT_N	B1		75
MIOA_CTL3	P5	GPU_MIOA_CTL3	B1		75
MIOA_DE	N2	GPU_MIOA_DE	B1		75
MIOA_D0	N1	GPU_MIOA_D<0>	B1		75
MIOA_D1	P4	GPU_MIOA_D<1>	B1		75
MIOA_D2	P1	GPU_MIOA_D<2>	B1		75
MIOA_D3	P2	GPU_MIOA_D<3>	B1		75
MIOA_D4	P3	GPU_MIOA_D<4>	B1		75
MIOA_D5	T3	GPU_MIOA_D<5>	B1		75
MIOA_D6	T2	GPU_MIOA_D<6>	B1		75
MIOA_D7	T1	GPU_MIOA_D<7>	B1		75
MIOA_D8	U4	GPU_MIOA_D<8>	B1		75
MIOA_D9	U1	GPU_MIOA_D<9>	B1		75
MIOA_D10	U2	GPU_MIOA_D<10>	B1		75
MIOA_D11	U3	GPU_MIOA_D<11>	B1		75
MIOA_D12	R6	GPU_MIOA_D<12>	B1		75
MIOA_D13	T6	GPU_MIOA_D<13>	B1		75
MIOA_D14	N6	GPU_MIOA_D<14>	B1		75
MIOA_HSYNC	N3	GPU_MIOA_HSYNC	B1		75
MIOA_VSYNC	L3	GPU_MIOA_VSYNC	B1		75
MIOB_CLKIN	AE1	GPU_MIOB_CLKIN		IN	75
MIOB_CLKOUT	V4	GPU_MIOB_CLKOUT_P	B1		75
MIOB_CLKOUT*	W4	GPU_MIOB_CLKOUT_N	B1		75
MIOB_CTL3	W3	GPU_MIOB_CTL3	B1		75
MIOB_DE	Y5	GPU_MIOB_DE	B1		75
MIOB_D0	Y1	GPU_MIOB_D<0>	B1		75
MIOB_D1	Y2	GPU_MIOB_D<1>	B1		75
MIOB_D2	Y3	GPU_MIOB_D<2>	B1		75
MIOB_D3	AB3	GPU_MIOB_D<3>	B1		75
MIOB_D4	AB2	GPU_MIOB_D<4>	B1		75
MIOB_D5	AB1	GPU_MIOB_D<5>	B1		75
MIOB_D6	AC4	GPU_MIOB_D<6>	B1		75
MIOB_D7	AC1	GPU_MIOB_D<7>	B1		75
MIOB_D8	AC2	GPU_MIOB_D<8>	B1		75
MIOB_D9	AC3	GPU_MIOB_D<9>	B1		75
MIOB_D10	AE3	GPU_MIOB_D<10>	B1		75
MIOB_D11	AE2	GPU_MIOB_D<11>	B1		75
MIOB_D12	U6	GPU_MIOB_D<12>	B1		75
MIOB_D13	W6	GPU_MIOB_D<13>	B1		75
MIOB_D14	Y6	GPU_MIOB_D<14>	B1		75
MIOB_D15	W5	GPU_STRAP<0>	B1		75
MIOB_D16	W7	GPU_STRAP<1>	B1		75
MIOB_D17	V7	GPU_STRAP<2>	B1		75
MIOB_HSYNC	W1	GPU_MIOB_HSYNC	B1		75
MIOB_VSYNC	W2	GPU_MIOB_VSYNC	B1		75
THERMDP	B5	GPU_THERMD_P		IN	75
THERMDN	B4	GPU_THERMD_N		OUT	75
PGOOD_OUT*	C5	TP_GPU_PGOOD_OUT_L		OUT	7

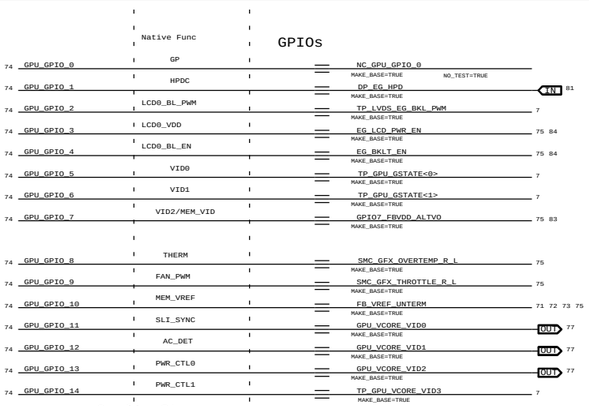
NV G96 GPIO/MIO/MISC

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

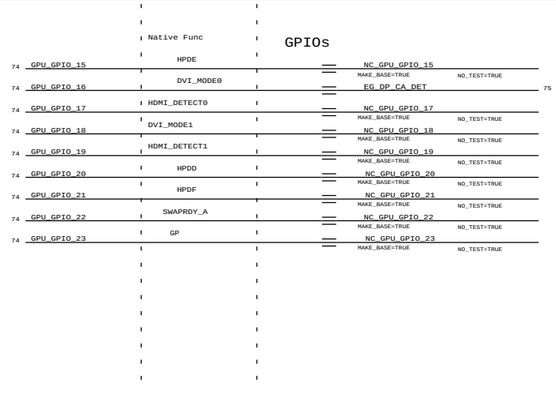
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE	SHT	OF
NONE	74	98

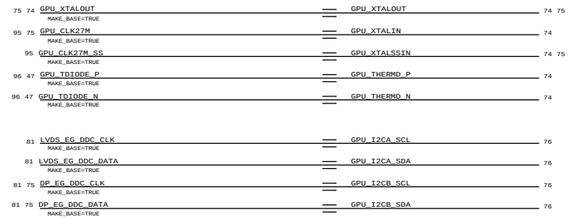
GPIOs



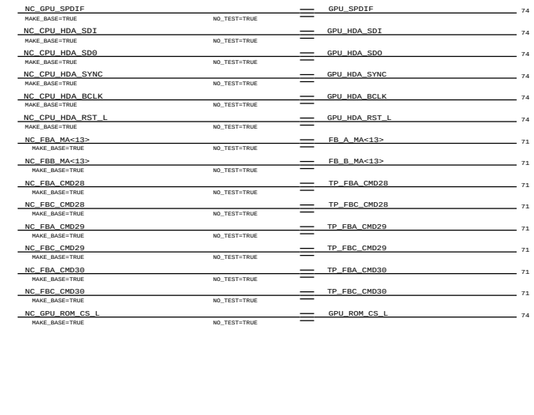
GPIOs



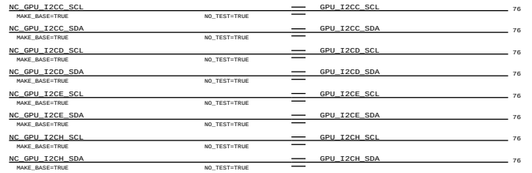
Renamed signals



Unused signals



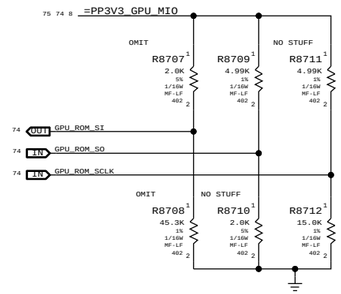
Unused I2C Buses



I2CS ties into SMBus connection page

(I2CS requires pullups even if not used)

Config Straps



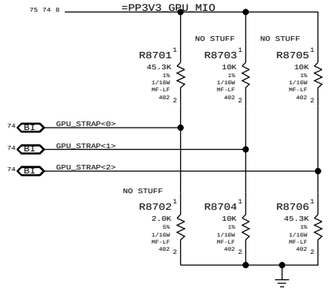
Physical Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

Strap S1/S2 Bit[3:0] PU/PD Rval

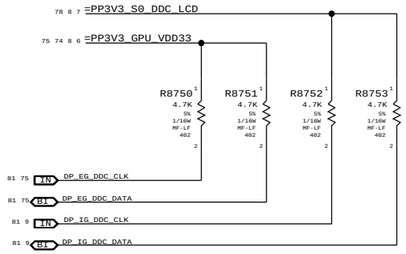
0 0000 PD 5k
1 0001 PD 10k
2 0010 PD 15k
3 0011 PD 20k
4 0100 PD 25k
5 0101 PD 30k
6 0110 PD 35k
7 0111 PD 45k

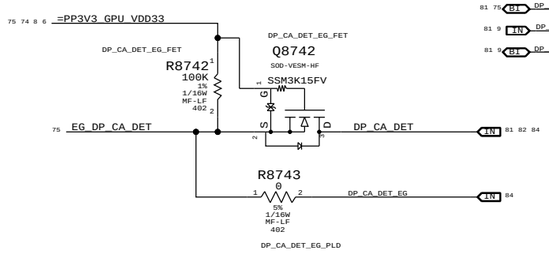
Strap S1/S2 Bit[3:0] PU/PD Rval

8 1000 PU 5k
9 1001 PU 10k
A 1010 PU 15k
B 1011 PU 20k
C 1100 PU 25k
D 1101 PU 30k
E 1110 PU 35k
F 1111 PU 45k



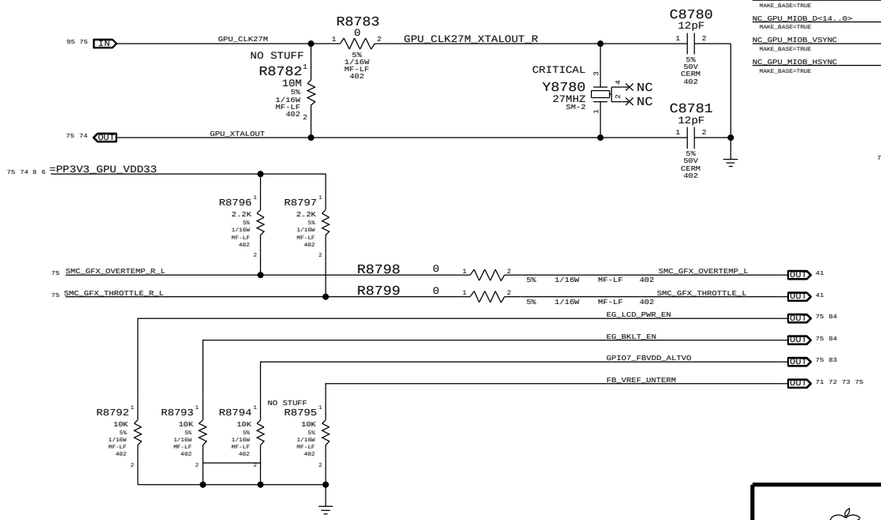
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8707		VRAM_1024_SAMSUNG
114S0368	1	RES,MTL FILM,1/16W,35.7K,1,0402,SMD,LF	R8708		VRAM_512_HYNIX



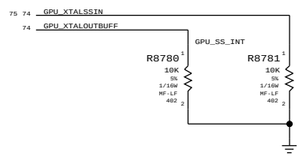


Isolation FETs for DP MUX inputs

GPU 27MHz Crystal



Unused Clocks



G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

G96 GPIOs & Straps

SYNC_MASTER=M98_MLB

SYNC_DATE=05/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 75 OF 98	

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

=PP1V8_GPU_IFPX

CRITICAL
L8800
FERR-220-OHM
0402

?mA peak per diff pair
?mA peak for all pairs

C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402

Place at AG9
Place at AG10

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

CRITICAL
L8805
FERR-220-OHM
0402

80mA peak

C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPEF_RSET 76
GPU_IFPCD_RSET 76
GPU_IFPAB_RSET 76

R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402

CRITICAL
L8810
FERR-220-OHM
0402

=PP1V1_GPU_IFPCD_IOVDD

?mA peak per diff pair
?mA peak for all pairs

C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402

Place at AJ8
Place at AK8

PP1V1_GPU_IFPCD_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

CRITICAL
L8815
FERR-220-OHM
0402

160mA peak

C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPCD_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

PP1V1_GPU_IFPEF_IOVDD_F 76
PP1V8_GPU_IFPEF_PLLVDD_F 76

Power inputs must be pulled down if not used

R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

OMIT

U8000
NB9P-GS
BGA
SYMBOL 5 OF 9

AG9	IFPA_IOVDD	IFPA_TXC	AM11
AG10	IFPB_IOVDD	IFPA_TXC*	AM12
AJ8	IFPC_IOVDD	IFPA_TXD0	AM8
AK8	IFPD_IOVDD	IFPA_TXD0*	AL8
AE7	IFPE_IOVDD	IFPA_TXD1	AM10
AD7	IFPF_IOVDD	IFPA_TXD1*	AM9
AK9	IFPAB_PLLVDD	IFPA_TXD2	AK10
AJ11	IFPAB_RSET	IFPA_TXD2*	AL10
AJ9	IFPCD_PLLVDD	IFPA_TXD3	AK11
AK7	IFPCD_RSET	IFPA_TXD3*	AL11
AJ6	IFPEF_PLLVDD	IFPB_TXC	AP13
AL1	IFPEF_RSET	IFPB_TXC*	AN13
		IFPB_TXD4	AN8
		IFPB_TXD4*	AP8
		IFPB_TXD5	AP10
		IFPB_TXD5*	AN10
		IFPB_TXD6	AR11
		IFPB_TXD6*	AR10
		IFPB_TXD7	AN11
		IFPB_TXD7*	AP11
		IFPC_AUX	AP2
		IFPC_AUX*	AN3
		IFPC_L0	AM7
		IFPC_L0*	AM6
		IFPC_L1	AL5
		IFPC_L1*	AM5
		IFPC_L2	AM3
		IFPC_L2*	AM4
		IFPC_L3	AP1
		IFPC_L3*	AR2
		IFPD_AUX	AP4
		IFPD_AUX*	AN4
		IFPD_L0	AR6
		IFPD_L0*	AP6
		IFPD_L1	AK4
		IFPD_L1*	AK5
		IFPD_L2	AN5
		IFPD_L2*	AP5
		IFPD_L3	AR5
		IFPD_L3*	AR4
		IFPE_AUX	AE4
		IFPE_AUX*	AD4
		IFPE_L0	AH6
		IFPE_L0*	AH5
		IFPE_L1	AH4
		IFPE_L1*	AG4
		IFPE_L2	AF4
		IFPE_L2*	AF5
		IFPE_L3	AE6
		IFPE_L3*	AE5
		IFPF_AUX	AF3
		IFPF_AUX*	AG3
		IFPF_L0	AL2
		IFPF_L0*	AL3
		IFPF_L1	AJ3
		IFPF_L1*	AJ4
		IFPF_L2	AJ2
		IFPF_L2*	AK2
		IFPF_L3	AK3
		IFPF_L3*	AK1
AJ12	DACA_VDD	DACA_RED	AM15
		DACA_GREEN	AM14
		DACA_BLUE	AL14
AK12	DACA_VREF	DACA_HSYNC	AM13
AK13	DACA_RSET	DACA_VSYNC	AL13
AC6	DACB_VDD	DACB_RED	AA4
		DACB_GREEN	AB4
AC5	DACB_VREF	DACB_BLUE	Y4
AD6	DACB_RSET	DACB_CSYNC	AB5
AG7	DACC_VDD	DACC_RED	AK8
		DACC_GREEN	AL8
		DACC_BLUE	AJ8
AK6	DACC_VREF	DACC_HSYNC	AM1
AD7	DACC_RSET	DACC_VSYNC	AK9

GPU_DACA_VDD
GPU_DACB_VDD
GPU_DACC_VDD

R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

75 B1	GPU_I2CA_SCL	G1	I2CA_SCL
75 B1	GPU_I2CA_SDA	G4	I2CA_SDA
75 B1	GPU_I2CC_SCL	E3	I2CC_SCL
75 B1	GPU_I2CC_SDA	E4	I2CC_SDA
44 B1	=GPU_I2CS_SCL	E2	I2CS_SCL
44 B1	=GPU_I2CS_SDA	E1	I2CS_SDA
75 B1	GPU_I2CH_SCL	F6	I2CH_SCL
75 B1	GPU_I2CH_SDA	G6	I2CH_SDA
75 B1	GPU_I2CB_SCL	G3	I2CB_SCL
75 B1	GPU_I2CB_SDA	G2	I2CB_SDA
75 B1	GPU_I2CD_SCL	F4	I2CD_SCL
75 B1	GPU_I2CD_SDA	G5	I2CD_SDA
75 B1	GPU_I2CE_SCL	D5	I2CE_SCL
75 B1	GPU_I2CE_SDA	E5	I2CE_SDA

IFPA_TXC	LVDS_EG_A_CLK_P	OUT	84 95
IFPA_TXC*	LVDS_EG_A_CLK_N	OUT	84 95
IFPA_TXD0	LVDS_EG_A_DATA_P<0>	OUT	84 95
IFPA_TXD0*	LVDS_EG_A_DATA_N<0>	OUT	84 95
IFPA_TXD1	LVDS_EG_A_DATA_P<1>	OUT	84 95
IFPA_TXD1*	LVDS_EG_A_DATA_N<1>	OUT	84 95
IFPA_TXD2	LVDS_EG_A_DATA_P<2>	OUT	84 95
IFPA_TXD2*	LVDS_EG_A_DATA_N<2>	OUT	7 84 95
IFPA_TXD3	LVDS_EG_A_DATA_P<3>	OUT	75
IFPA_TXD3*	LVDS_EG_A_DATA_N<3>	OUT	75
IFPB_TXC	LVDS_EG_B_CLK_P	OUT	75
IFPB_TXC*	LVDS_EG_B_CLK_N	OUT	75
IFPB_TXD4	LVDS_EG_B_DATA_P<0>	OUT	84 95
IFPB_TXD4*	LVDS_EG_B_DATA_N<0>	OUT	84 95
IFPB_TXD5	LVDS_EG_B_DATA_P<1>	OUT	84 95
IFPB_TXD5*	LVDS_EG_B_DATA_N<1>	OUT	84 95
IFPB_TXD6	LVDS_EG_B_DATA_P<2>	OUT	84 95
IFPB_TXD6*	LVDS_EG_B_DATA_N<2>	OUT	84 95
IFPB_TXD7	LVDS_EG_B_DATA_P<3>	OUT	75
IFPB_TXD7*	LVDS_EG_B_DATA_N<3>	OUT	75
IFPC_AUX	DP_EG_AUX_CH_P	OUT	81 95
IFPC_AUX*	DP_EG_AUX_CH_N	OUT	81 95
IFPC_L0	DP_EG_ML_P<0>	OUT	81 95
IFPC_L0*	DP_EG_ML_N<0>	OUT	81 95
IFPC_L1	DP_EG_ML_P<1>	OUT	81 95
IFPC_L1*	DP_EG_ML_N<1>	OUT	81 95
IFPC_L2	DP_EG_ML_P<2>	OUT	81 95
IFPC_L2*	DP_EG_ML_N<2>	OUT	81 95
IFPC_L3	DP_EG_ML_P<3>	OUT	81 95
IFPC_L3*	DP_EG_ML_N<3>	OUT	81 95

R8861 1K 5% 1/16W MF-LF 402
R8860 1K 5% 1/16W MF-LF 402
NO STUFF

NV G96 Video Interfaces

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

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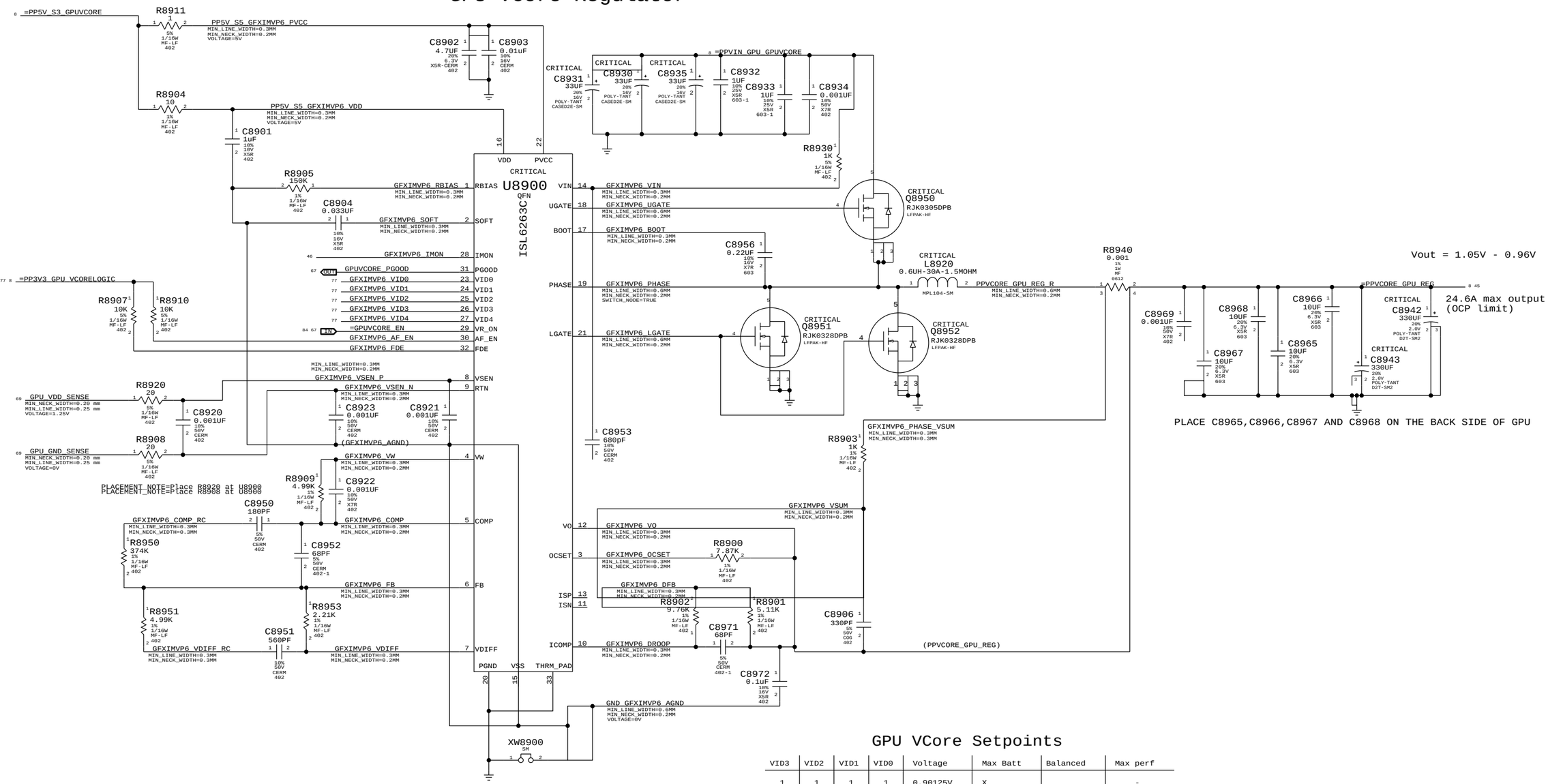
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 76 OF 98	

GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	1	1	1	0.90125V	X		-
1	1	1	0	0.92700V	-	X	-
1	0	1	1	1.00425V	-	-	X

Other VID states may not be valid

Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1,GPUVID1_1,GPUVID0_1
GPUVID_1P00V	GPUVID2_0,GPUVID1_1,GPUVID0_1

GPU (G96) CORE SUPPLY

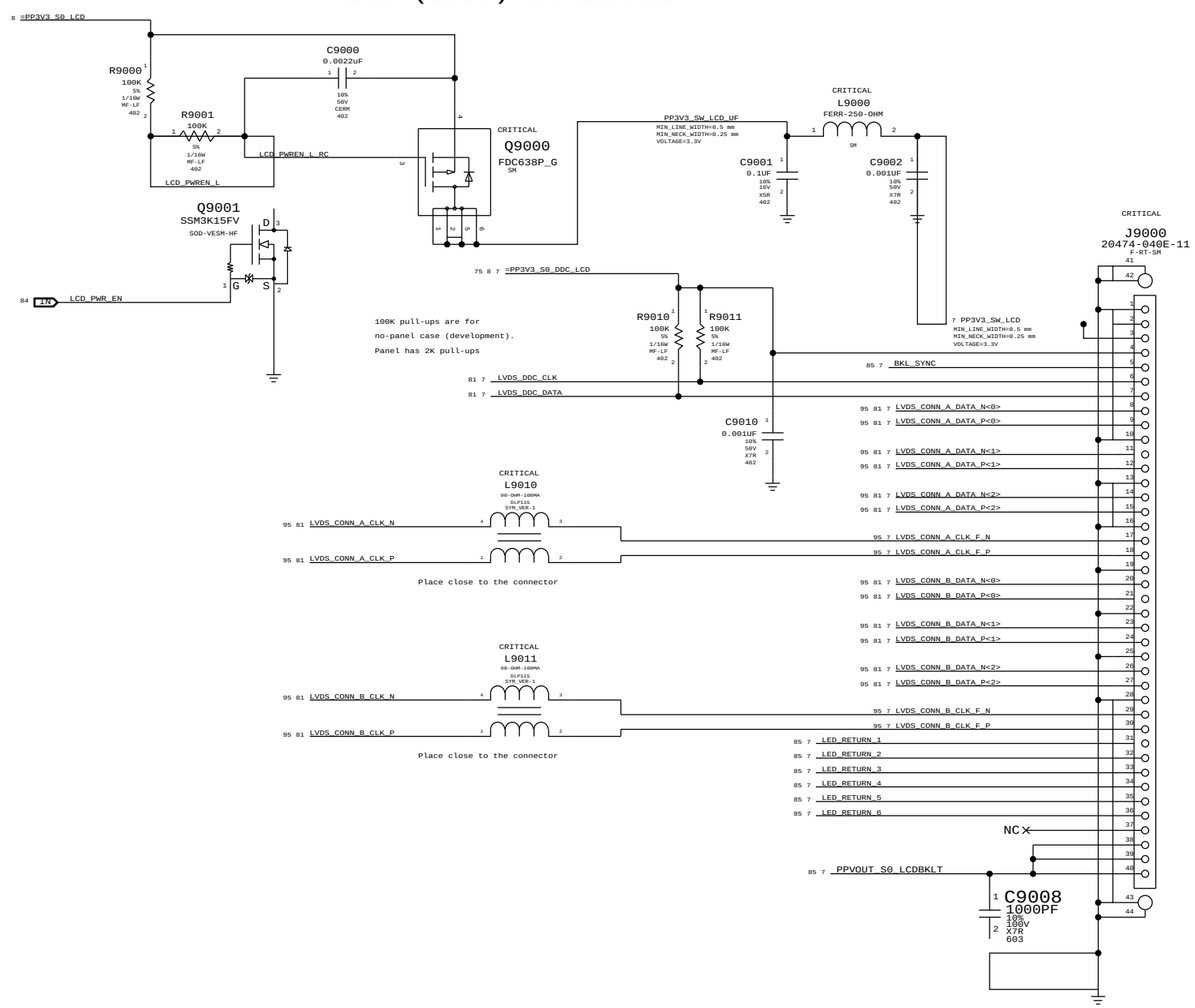
SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8

SCALE: NONE SHT 77 OF 98

LCD (LVDS) INTERFACE



518S0651

LVDS Display Connector

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

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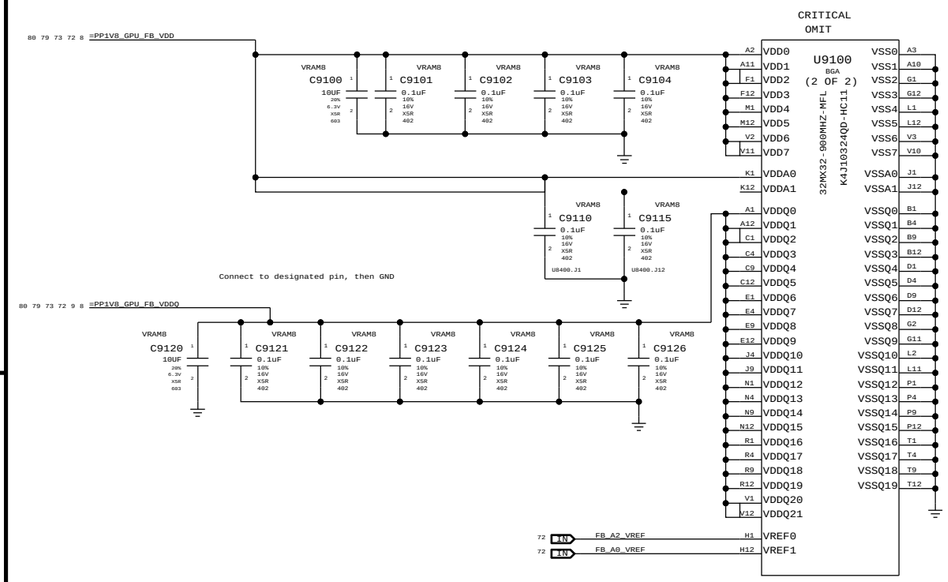
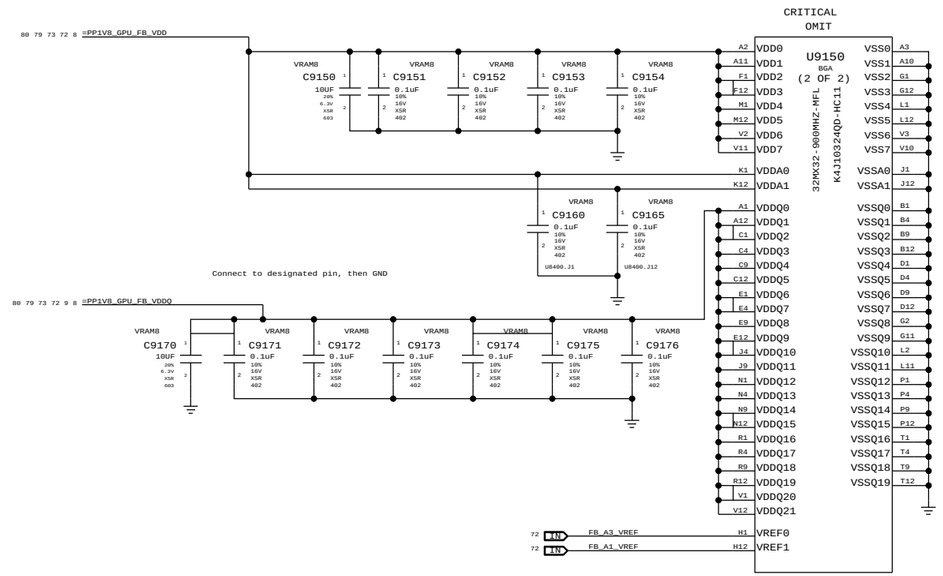
D	051-8071	8
SCALE: NONE	SHT 78 OF 98	





Page Notes

Power aliases required by this page:

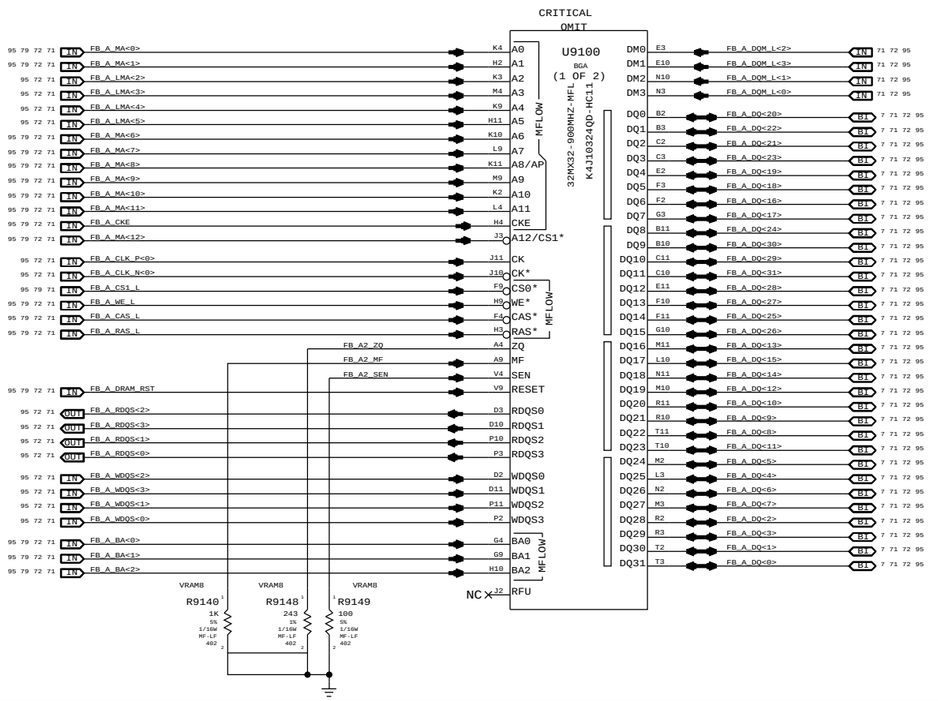
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

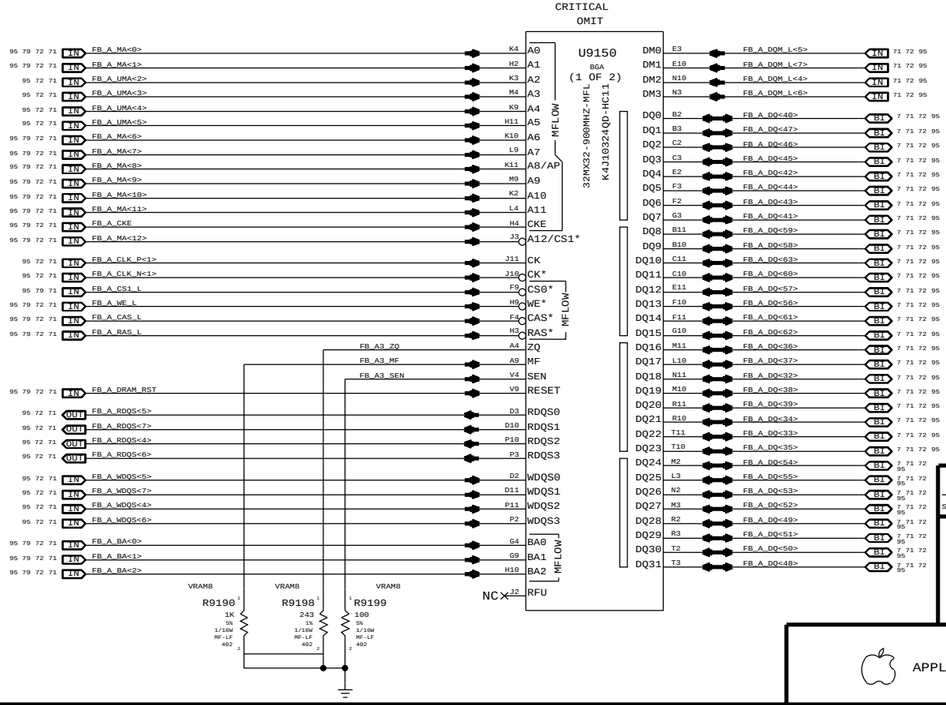
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM8



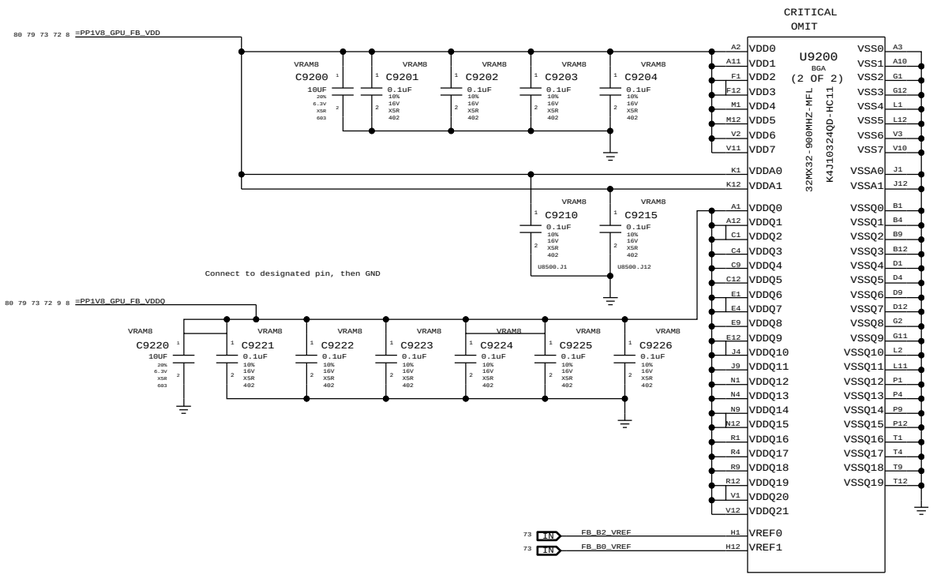


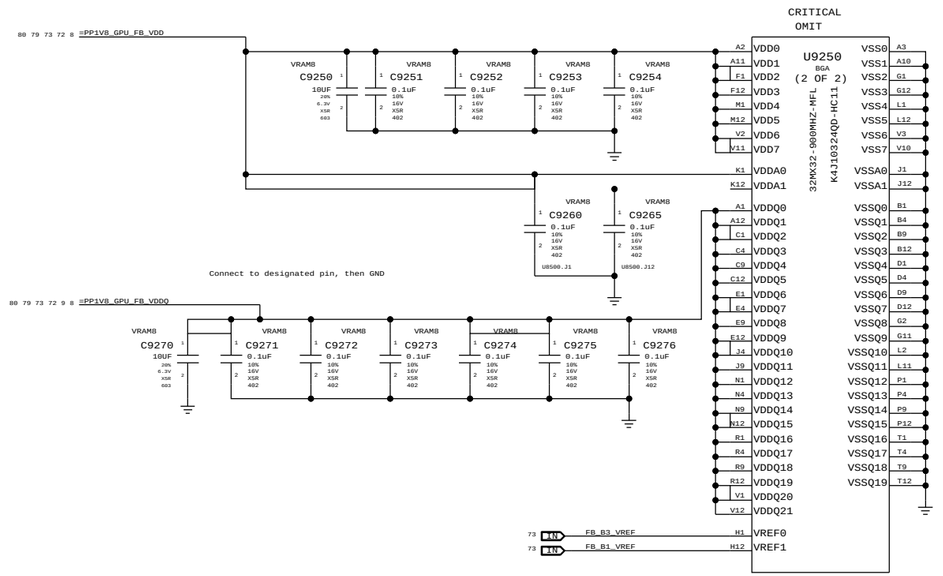
GDDR3 Frame Buffer A (Top)

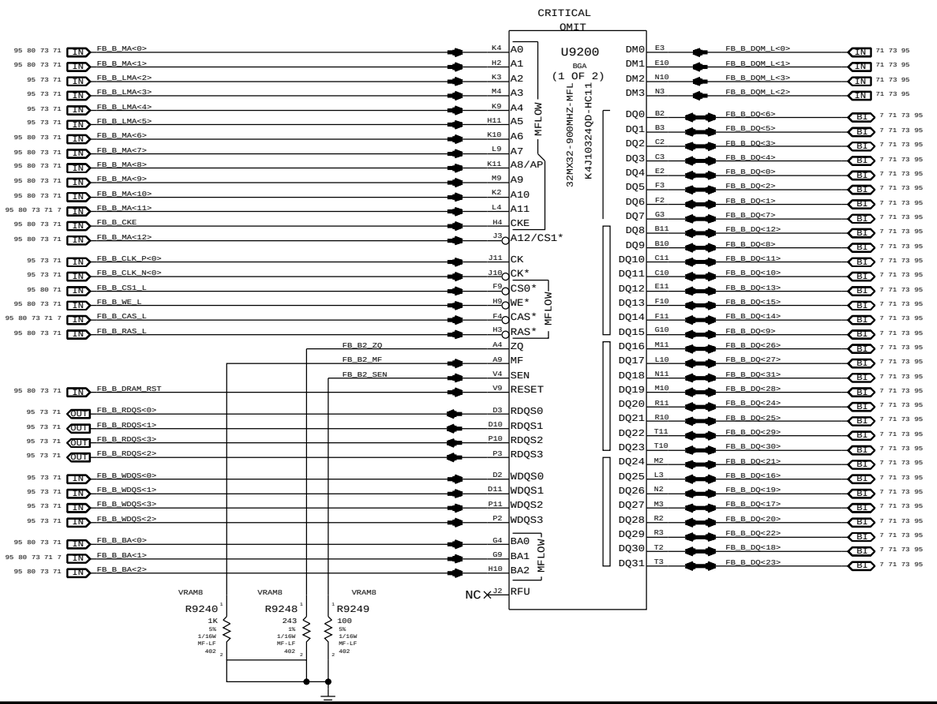
SYNC_MASTER=M99_MLB SYNC_DATE=04/04/2008

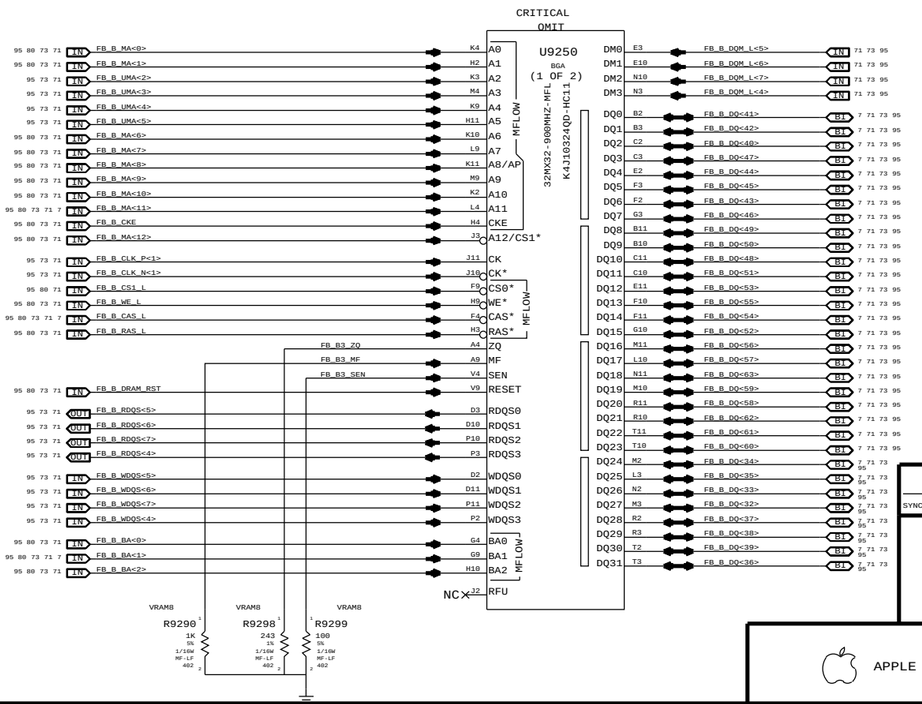
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 79 OF 98	









Page Notes

Power aliases required by this page:

- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM8

GDDR3 Frame Buffer B (Top)

SYNC_MASTER=M88_MLB SYNC_DATE=11/01/2007

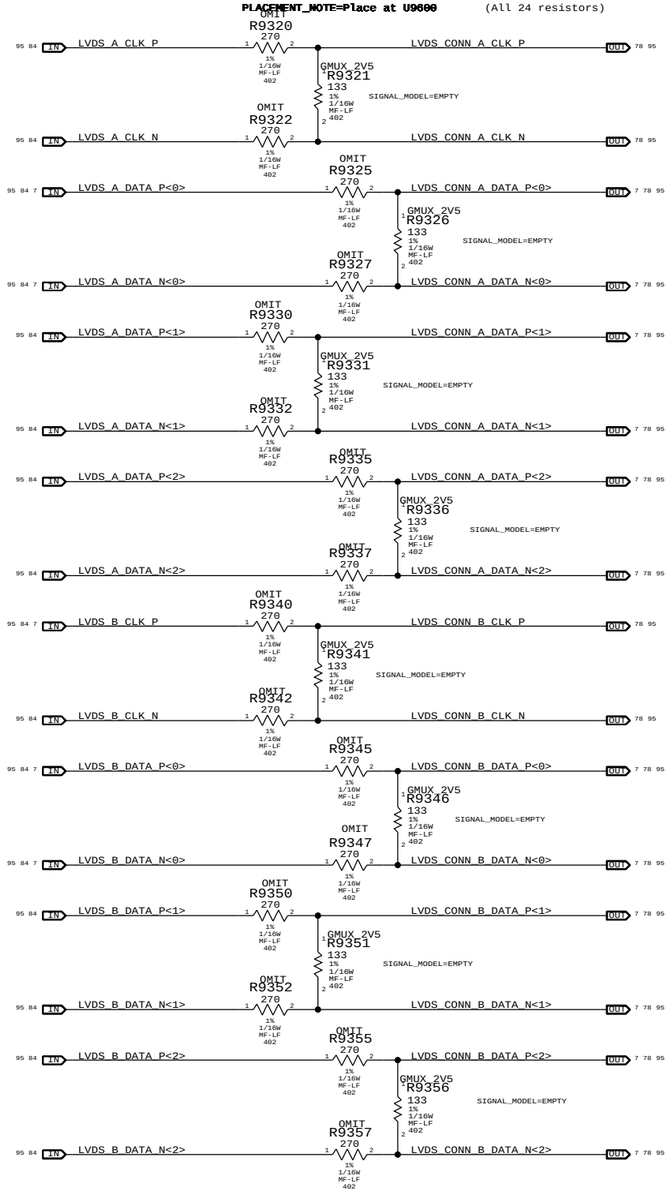
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT	OF
NONE	80	98

LVDS Transmitter Termination

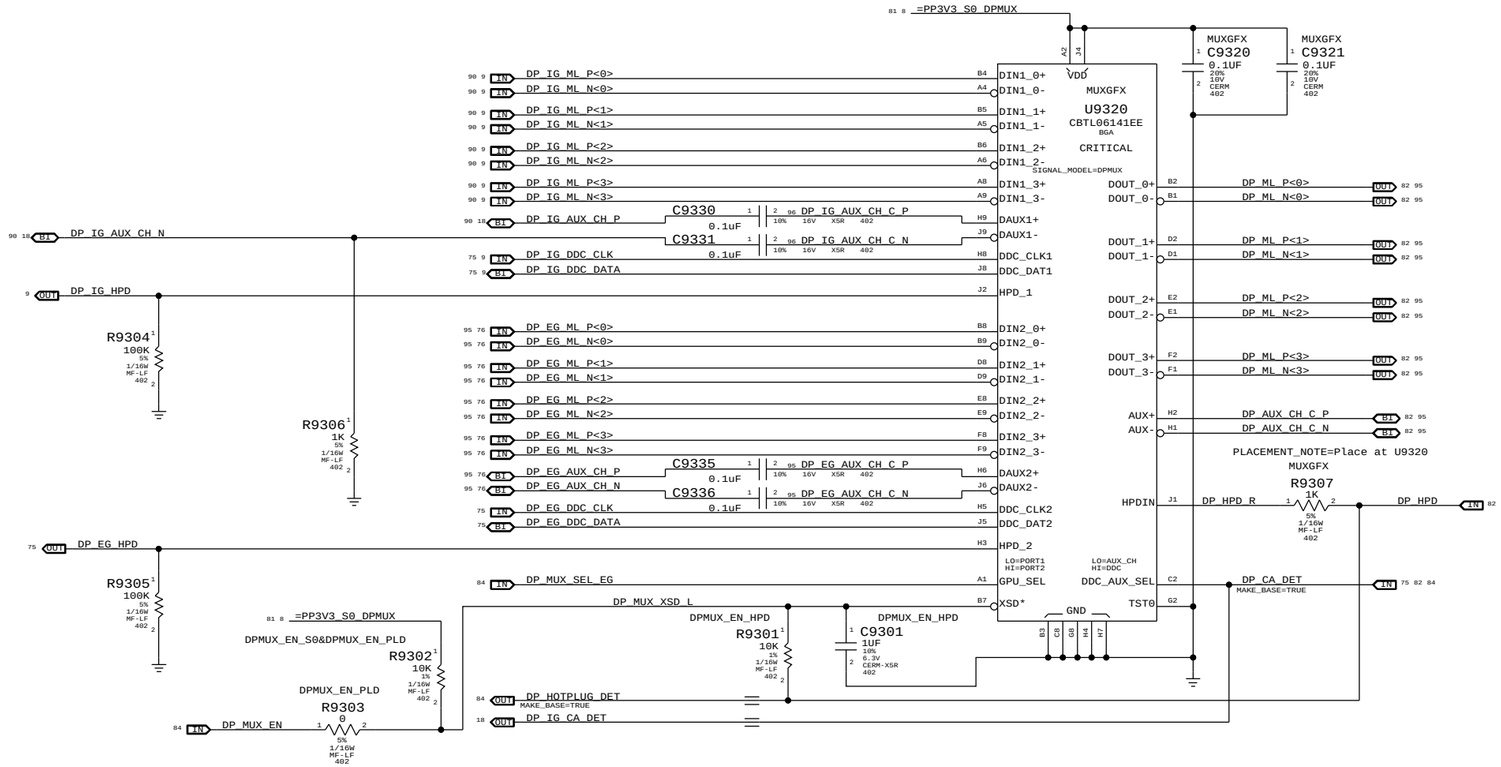
All emulated LVDS outputs require this termination

PLACEMENT_NOTE=Place at U9600 (All 24 resistors)

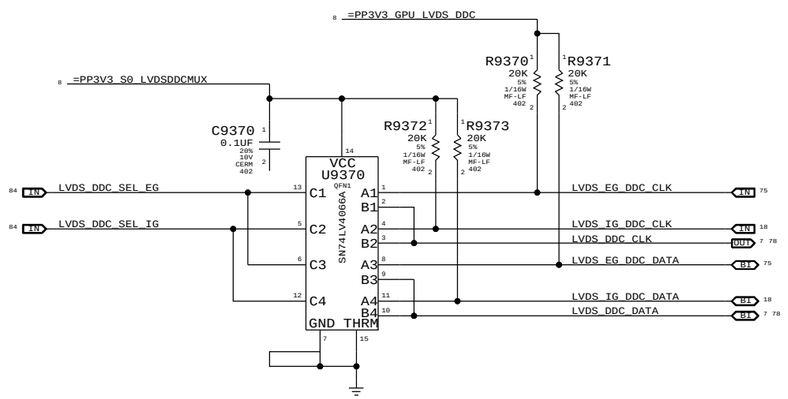


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0517	16	RES,MTL FILM,270 OHM,1%,1/16W,0402,SMD,L			GMUX_2V5
114S0174	16	RES,MTL FILM,1/16W,357 OHM,1,0402,SMD,LF			GMUX_1V8

DisplayPort Mux



LVDS DDC MUX



Muxed Graphics Support

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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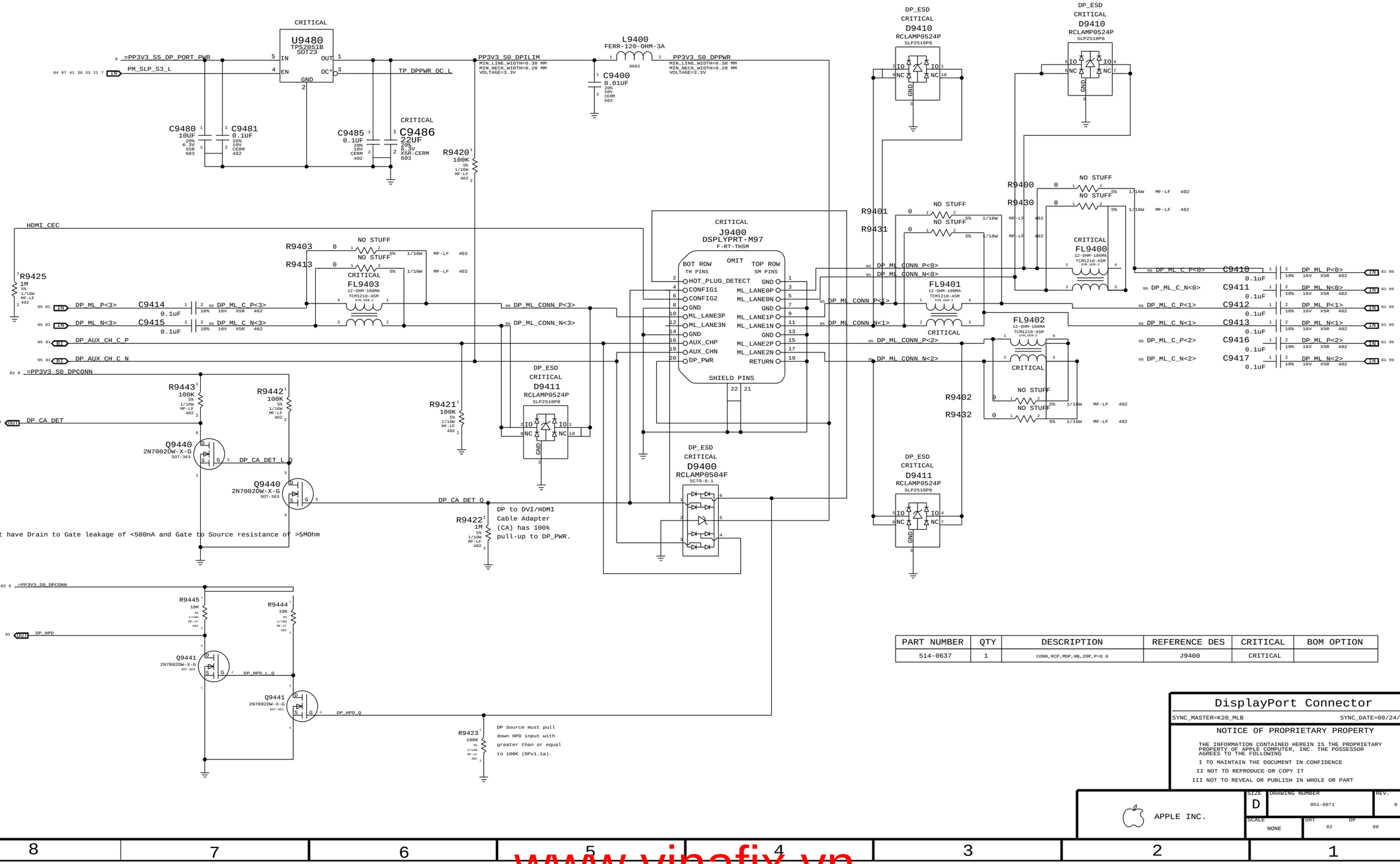
D	051-8071	8
SCALE: NONE	SHT 81 OF 98	

Port Power Switch



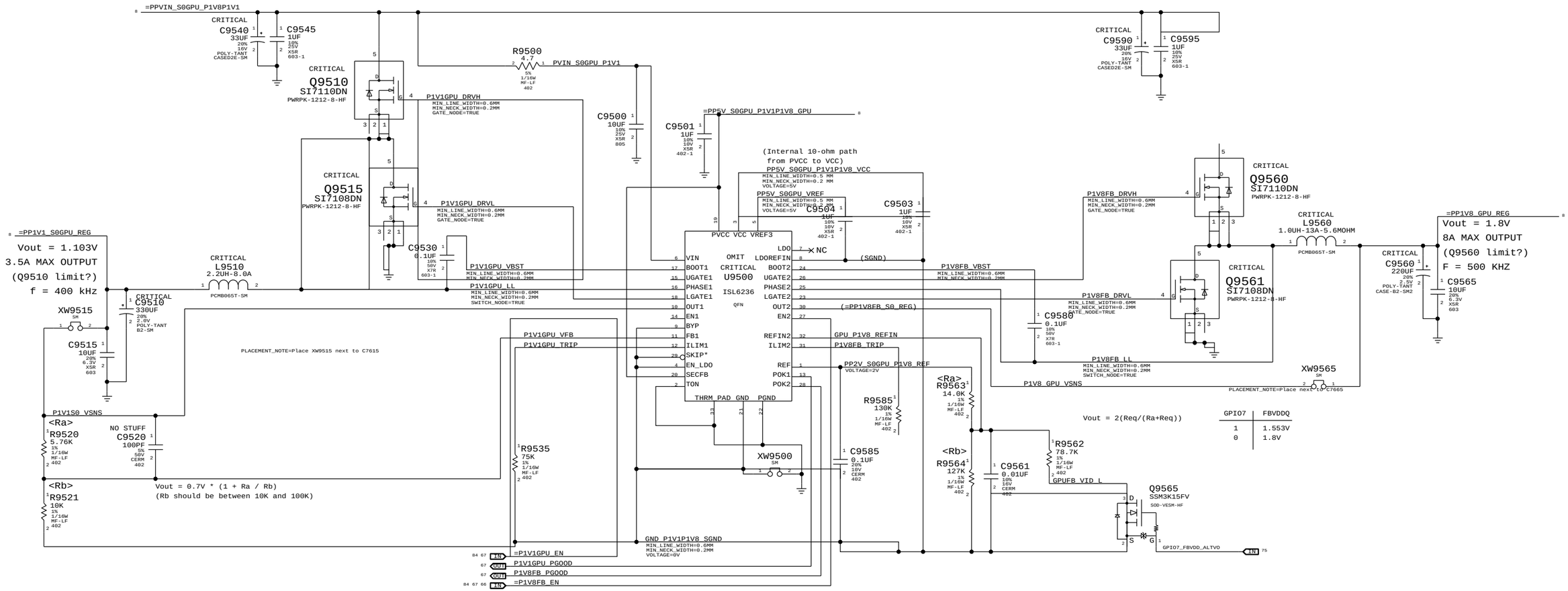
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0637	1	CONN,RCP,MDP,HB,20P,P=0.6	J9400	CRITICAL	

DisplayPort Connector

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 82 OF 98	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2312	1	IC,ISL6236,DUAL PWM CNTRL,QFN32	U9500	CRITICAL	

1.1V / 1V8 FB Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 83 OF 98	

GMUX CPLD

=PP3V3_S0_GMUX
C9610 0.1UF 20% 10V CERM 402
C9621 0.1UF 20% 10V CERM 402
C9622 0.1UF 20% 10V CERM 402
C9623 0.1UF 20% 10V CERM 402
C9624 0.1UF 20% 10V CERM 402
C9625 0.1UF 20% 10V CERM 402
C9626 0.1UF 20% 10V CERM 402
C9627 0.1UF 20% 10V CERM 402
C9628 0.1UF 20% 10V CERM 402
C9629 0.1UF 20% 10V CERM 402

=PP2V5_S0_GMUX
C9611 0.1UF 20% 10V CERM 402
C9612 0.1UF 20% 10V CERM 402
C9613 0.1UF 20% 10V CERM 402
C9614 0.1UF 20% 10V CERM 402
C9615 0.1UF 20% 10V CERM 402
C9616 0.1UF 20% 10V CERM 402
C9617 0.1UF 20% 10V CERM 402

=PP1V2_S0_GMUX
C9600 4.7UF 20% 4V X5R 402
C9604 0.1UF 20% 10V CERM 402
C9605 0.1UF 20% 10V CERM 402
C9606 0.1UF 20% 10V CERM 402
C9607 0.1UF 20% 10V CERM 402
C9608 0.1UF 20% 10V CERM 402
C9609 0.1UF 20% 10V CERM 402

=PP3V3_S0_GMUX
R9640 10K 1% 1/16W MF-LF 402
R9645 10K 1% 1/16W MF-LF 402

NO STUFF
R9641 10K 1% 1/16W MF-LF 402
NO STUFF
R9646 10K 1% 1/16W MF-LF 402

NO STUFF
R9647 10K 1% 1/16W MF-LF 402

PP3V3_S0_GMUX_ULC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
L9621 FERR-220-OHM 0402
C9631 0.1UF 20% 10V CERM 402

PP3V3_S0_GMUX_LRC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
L9620 FERR-220-OHM 0402
C9630 0.1UF 20% 10V CERM 402

VCC VCCAUX VCCIO6 VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCJ ULC_VCCPLL LRC_VCCPLL

OMIT
CRITICAL

U9600
XP28
CSBGA-HF

JTAG_GMUX_TCK	K14	TCK	
JTAG_GMUX_TDI	L13	TDI	IN
JTAG_GMUX_TDO	K13	TDO	OUT
JTAG_GMUX_TMS	L12	TMS	IN
GMUX_TOE	K2	TOE	
GMUX_CFG0	K1	CFG0	
LCD_BKLT_EN	P2	PB2A	OUT
LCD_BKLT_PWM	N2	PB2B	OUT
LVDS_DDC_SEL_EG	P4	PB14A	OUT
LVDS_DDC_SEL_IG	N4	PB14B	OUT
DP_MUX_EN	N3	PB15A (dd)	OUT
DP_MUX_SEL_EG	M4	PB15B	OUT
EG_RESET_L	P5	PB16A	OUT
EG_RAIL1_EN	M5	PB16B	OUT
EG_RAIL2_EN	P6	PB17A	OUT
EG_RAIL3_EN	M6	PB17B	OUT
EG_RAIL4_EN	P7	PB18A	OUT
EG_CLKREQ_OUT_L	M7	PB18B (dd)	OUT
DP_CA_DET_EG	N7	PB19A	OUT
LCD_PWR_EN	N8	PB19B	OUT
LPC_AD<0>	P9	PB20A	BI
LPC_AD<1>	N9	PB20B	BI
LPC_AD<2>	P10	PB30A	BI
LPC_AD<3>	M10	PB30B	BI
LPC_FRAME_L	P12	PB31A	BI
LPC_RESET_L	P13	PB31B	IN
LPC_CLK33M_GMUX	N12	PB32A	IN
GMUX_INT	P14	PB32B	OUT
LVDS_IG_B_DATA_P<2>	B1	PL2A	IN
LVDS_IG_B_DATA_N<2>	B2	PL2B	IN
TP_GMUX_PL10A	C2	PL10A	
TP_GMUX_PL10B	D3	PL10B	
LVDS_IG_A_DATA_P<0>	D1	PL11A	IN
LVDS_IG_A_DATA_N<0>	E1	PL11B	IN
LVDS_IG_A_DATA_P<1>	D2	PL12A	IN
LVDS_IG_A_DATA_N<1>	E3	PL12B	IN
LVDS_IG_A_DATA_P<2>	F1	PL13A	IN
LVDS_IG_A_DATA_N<2>	G1	PL13B	IN
LVDS_IG_B_DATA_P<0>	F3	PL14A	IN
LVDS_IG_B_DATA_N<0>	G2	PL14B	IN
LVDS_IG_B_DATA_P<1>	H2	PL15A	IN
LVDS_IG_B_DATA_N<1>	G3	PL15B	IN
LVDS_IG_A_CLK_P	H1	PL16A	IN
LVDS_IG_A_CLK_N	H3	PL16B	IN
LVDS_MUX_SEL_EG	L1	PL18A	OUT
TP_GMUX_PL18B_VSYNC	L3	PL18B	
=GMUX_PCIE_RESET_L	K3	PL19A	IN
GMUX_PM_SLP_S3_L	L2	PL19B	IN
ALL_EG_PGOOD	N1	PL32A	IN
EG_CLKREQ_IN_L	P1	PL32B	IN

BANK5 BANK4 BANK7 BANK6

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

GND GNDIO0 GNDIO1 GNDIO2 GNDIO3 GNDIO4 GNDIO5 GNDIO6 GNDIO7 ULC_GNDPLL LRC_GNDPLL

PT2A	LVDS_B_DATA_P<0>	OUT	7 81 95
PT2B	LVDS_B_DATA_N<0>	OUT	7 81 95
PT3A	LVDS_B_DATA_P<1>	OUT	81 95
PT3B	LVDS_B_DATA_N<1>	OUT	81 95
PT4A	LVDS_B_DATA_P<2>	OUT	81 95
PT4B	LVDS_B_DATA_N<2>	OUT	81 95
PT14A	EG_PWRSEQ_EN	IN	84
PT14B	GMUX_DEBUG_RESET_L	IN	84
PT15A	LVDS_A_CLK_P	OUT	81 95
PT15B	LVDS_A_CLK_N	OUT	81 95
PT16A	LVDS_B_CLK_P	OUT	7 81 95
PT16B	LVDS_B_CLK_N	OUT	81 95
PT17A	LVDS_A_DATA_P<0>	OUT	7 81 95
PT17B	LVDS_A_DATA_N<0>	OUT	7 81 95
PT18A	LVDS_A_DATA_P<1>	OUT	81 95
PT18B	LVDS_A_DATA_N<1>	OUT	81 95
PT19A	LVDS_A_DATA_P<2>	OUT	81 95
PT19B	LVDS_A_DATA_N<2>	OUT	81 95
PT20A	TP_GMUX_PT20A		
PT20B	TP_GMUX_PT20B		
PT32A	TP_GMUX_PT32A		
PT32B	TP_GMUX_PT32B		

BANK0 BANK1

PR2A	DP_CA_DET	IN	75 81 82
PR2B	DP_HOTPLUG_DET	IN	81
PR10A	LVDS_EG_A_DATA_P<0>	IN	76 84 95
PR10B	LVDS_EG_A_DATA_N<0>	IN	76 84 95
PR11A	LVDS_EG_A_DATA_P<1>	IN	76 84 95
PR11B	LVDS_EG_A_DATA_N<1>	IN	76 84 95
PR12A	LVDS_EG_A_DATA_P<2>	IN	76 84 95
PR12B	LVDS_EG_A_DATA_N<2>	IN	7 76 84 95
PR13A	LVDS_EG_B_DATA_P<0>	IN	76 84 95
PR13B	LVDS_EG_B_DATA_N<0>	IN	76 84 95
PR14A	LVDS_EG_B_DATA_P<1>	IN	76 84 95
PR14B	LVDS_EG_B_DATA_N<1>	IN	76 84 95
PR15A	LVDS_EG_B_DATA_P<2>	IN	76 84 95
PR15B	LVDS_EG_B_DATA_N<2>	IN	76 84 95
PR16A	LVDS_EG_A_CLK_P	IN	76 84 95
PR16B	LVDS_EG_A_CLK_N	IN	76 84 95
PR18A	IG_LCD_PWR_EN	IN	9
PR18B	EG_LCD_PWR_EN	IN	75
PR30A	IG_BKLT_EN	IN	9
PR30B	EG_BKLT_EN	IN	75

BANK2 BANK3

GMUX_JTAG_TCK Inversion

JTAG_GMUX_TCK
Q9670 SSM6N15FEAPE SOT563
GMUX_JTAG_TCK_L

PM_SLP_S3_L Isolation

=PP3V3_S0_GMUX
Q9670 SSM6N15FEAPE SOT563
R9670 10K 1% 1/16W MF-LF 402
PM_SLP_S3_L
EG_PWRSEQ_EN
GMUX_PM_SLP_S3_L
MAKE_BASE=TRUE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
336S0027	1	IC,XP2-8,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_BK_BLANK
341S2501	1	IC,CPLD,LATTICE,132CSBGA,REV,K20	U9600	CRITICAL	GMUX_PROG

=PP3V3_S3_GMUX
R9676 100K 5% 1/16W MF-LF 402
GMUX_S3_PD_EN
Q9607 SSM6N15FEAPE SOT563

=PP3V3_S0_GMUX
NO STUFF
R9677 10K 1% 1/16W MF-LF 402
GMUX_S0_PD_DIS_BC
NO STUFF
C9695 1UF 10% 6.3V CERM 402
Q9607 SSM6N15FEAPE SOT563
ALL_SYS_PWRGD
R9684 0 5% 1/16W MF-LF 402

LVDS Receiver Termination

PLACEMENT_NOTE=Place at U9600 (All 14 resistors)

LVDS_IG_A_CLK_P	R9650	100	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>	R9651	100	LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>	R9652	100	LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>	R9653	100	LVDS_IG_A_DATA_N<2>
LVDS_IG_B_DATA_P<0>	R9654	100	LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>	R9655	100	LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>	R9656	100	LVDS_IG_B_DATA_N<2>
LVDS_EG_A_CLK_P	R9660	100	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>	R9661	100	LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>	R9662	100	LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>	R9663	100	LVDS_EG_A_DATA_N<2>
LVDS_EG_B_DATA_P<0>	R9664	100	LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>	R9665	100	LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>	R9666	100	LVDS_EG_B_DATA_N<2>

SIGNAL_MODEL=EMPTY

Required Pullups

=PP3V3_S0_GMUX
GMUX_DEBUG_RESET_L R9680 1K
JTAG_GMUX_TCK R9690 4.7K
EG_CLKREQ_OUT_L R9695 10K
NO STUFF R9679 10K 1% 1/16W MF-LF 402
SILK_PART=GMUX_RST
PLACEMENT_NOTE=Place on top side at U9600

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K
LVDS_DDC_SEL_IG	R9682	10K
LVDS_DDC_SEL_EG	R9683	10K

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

NO STUFF

EG_RESET_L	R9691	100K
GMUX_INT	R9692	20K
LCD_BKLT_PWM	R9693	100K
EG_CLKREQ_IN_L	R9694	100K

EG_PWRSEQ_HW
R9630 0 5% 1/16W MF-LF 402 EXTGPU_PWR_EN OUT 67
EG_PWRSEQ_GMUX
R9631 0 5% 1/16W MF-LF 402 =P1V1GPU_EN OUT 67 83
EG_PWRSEQ_GMUX
R9632 0 5% 1/16W MF-LF 402 P3V3GPU_EN OUT 67 68
EG_PWRSEQ_GMUX
R9633 0 5% 1/16W MF-LF 402 GPUVCORE_EN OUT 67 77
EG_PWRSEQ_GMUX
R9634 0 5% 1/16W MF-LF 402 =P1V8FB_EN OUT 66 67 83

The MAKE BASE properties for these signals are on the POWER CONTROL page.

EG_RAIL1_EN
EG_RAIL2_EN
EG_RAIL3_EN
EG_RAIL4_EN
LCD_PWR_EN

EG_PWRSEQ_GMUX R9671 4.7K 5% 1/16W MF-LF 402
EG_PWRSEQ_GMUX R9672 4.7K 5% 1/16W MF-LF 402
EG_PWRSEQ_GMUX R9673 4.7K 5% 1/16W MF-LF 402
EG_PWRSEQ_GMUX R9674 4.7K 5% 1/16W MF-LF 402
R9678 4.7K 5% 1/16W MF-LF 402
GMUX_S3_PD_GND
NO STUFF R9675 0 5% 1/16W MF-LF 402
NO STUFF C9691 0.1UF 20% 10V CERM 402
NO STUFF C9692 0.1UF 20% 10V CERM 402
NO STUFF C9693 0.1UF 20% 10V CERM 402
NO STUFF C9694 0.1UF 20% 10V CERM 402

Graphics MUX (GMUX)

SYNC_MASTER=T18_MXMGMUX SYNC_DATE=02/13/2008

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SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 84 OF 98	

*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.
*BOOST_FET_CNTL AND PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.

PPBUS_S0_LCDBKLT_PWR
R9730 0 5% 1/10W MF-LF 603
PPVIN_S0_LCDBKLT_BUF
CRITICAL L9701 22UH-2.5A IHLP2525CZ-SM
PPVOUT_S0_LCDBKLT_SW
R9701 49.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=L9701 PLACE NEAR Q9701
CRITICAL C9701 10UF 10% 25V X5R 805
PLACEMENT_NOTE=C9701 PLACE NEAR L9701
XW9701 SM
GND_BKL_PWRGND
PLACEMENT_NOTE=XW9701 PLACE NEAR C9701
C9702 0.1UF 10% 25V X5R 402
BKL_VIN
BOOST_FET_CNTL
CRITICAL Q9701 SI7308DN PWRPK-1212-8
PLACEMENT_NOTE=D9701 PLACE NEAR Q9701
D9701 SOD-123 RB160M-60G CRITICAL
PLACEMENT_NOTE=C9709 PLACE NEAR C9710
PLACEMENT_NOTE=C9710 PLACE NEAR J9000
CRITICAL NO STUFF C9709 2.2UF 10% 100V X7R 1210
CRITICAL C9710 1.0UF 10% 100V X7R 1210
BOOST_SINK
GND_BKL_PWRGND
PLACEMENT_NOTE=R9715 PLACE NEAR C9709 AND Q9701
R9704 100 1% 1/16W MF-LF 402
R9702 0.4 1% 1/6W MF 402
R9715 0.4 1% 1/6W MF 402
XW9702 SM
GND_BKL_PWRGND_X
PLACEMENT_NOTE=R9702 PLACE NEAR C9709 AND Q9701
*R9702 AND R9715 PIN 1 SHOULD BE PLACED NEAR C9709 PIN 2
PPVOUT_S0_LCDBKLT

BKL_VREF_4V9
R9731 187K 1% 1/16W MF-LF 402
PPBUS_S0_LCDBKLT_PWR
BKLT_EN
BKL_SYNC
BKLT_PLL
R9734 0 5% 1/16W MF-LF 402
BKL_VSYNC
OMIT
CRITICAL
U9700 APP001 QFN
VIN
R9707 2.67K 1% 1/16W MF-LF 402
C9703 1UF 10% 10V X5R 402
C9713 0.1UF 10% 25V X5R 402
R9705 100K 1% 1/16W MF-LF 402
R9706 10K 5% 1/16W MF-LF 402
C9712 47PF 5% 50V CERM 402 NO STUFF
PLACEMENT_NOTE=R9707 AWAY FROM Q9701
BKL_ISET
PLACEMENT_NOTE=R9708 AWAY FROM Q9701
BKL_RT
PLACEMENT_NOTE=R9709 AWAY FROM Q9701
BKL_SSTCMP
BKL_DIM
BKL_LPF
BKL_LRT
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6
BKL_SSTCMP_RC
R9708 100K 1% 1/16W MF-LF 402
R9709 10K 1% 1/16W MF-LF 402
R9703 5.1M 5% 1/16W MF-LF 402
C9705 0.0022UF 10% 50V CERM 402
BKLT_PWM_RC
R9733 4.7K 5% 1/16W MF-LF 402
C9706 0.0022UF 10% 50V CERM 402
C9714 1UF 10% 10V X5R 402
GNDA
THRM_PAD
GND_BKL_PWRGND
BKL_VREF_4V9
R9713 0 5% 1/16W MF-LF 402
PLACEMENT_NOTE=R9713 AWAY FROM Q9701
PLACEMENT_NOTE=R9714 AWAY FROM Q9701
BKLT_PLL_NOT
BKLT_PLL
R9714 10K 5% 1/16W MF-LF 402
R9727 75K 1% 1/16W MF-LF 402
PLACEMENT_NOTE=R9727 AWAY FROM Q9701
C9707 2.2UF 20% 6.3V CERM 402-LF
BKL_LRT_RC
C9708 0.1UF 10% 25V X5R 402

CRITICAL Q9702 NTUD3127CXXG SOT-963 P-CHN
BKL_VREF_4V9
BKL_VREF_IN_4V9
R9700 10K 1% 1/16W MF-LF 402
BKL_PWR_EN
R9710 4.02K 1% 1/16W MF-LF 402
CRITICAL Q9702 NTUD3127CXXG SOT-963 N-CHN
LCD_BKLT_PWM
R9711 8.06K 1% 1/16W MF-LF 402

R9717 10.2 0.1% 1/16W TF 402 LED_RETURN_6
R9718 10.2 0.1% 1/16W TF 402 LED_RETURN_5
R9719 10.2 0.1% 1/16W TF 402 LED_RETURN_4
R9720 10.2 0.1% 1/16W TF 402 LED_RETURN_3
R9721 10.2 0.1% 1/16W TF 402 LED_RETURN_2
R9722 10.2 0.1% 1/16W TF 402 LED_RETURN_1
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm

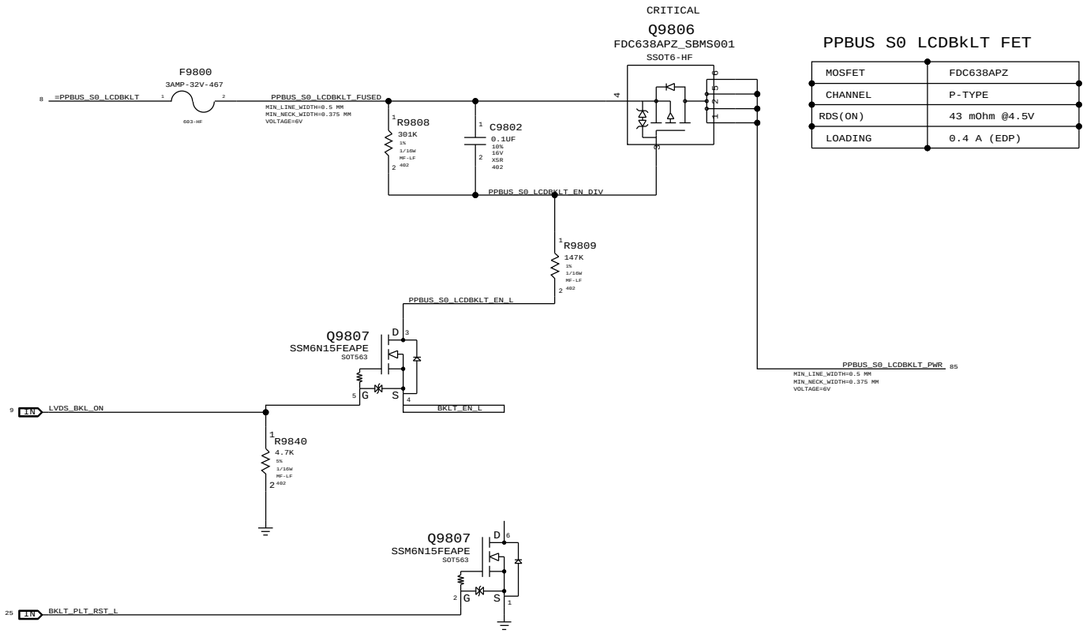
THRESHOLD=2.5V
BKL_VSEN
50.4*R9724/(R9723+R9724)=2.4V
R9723 1.2M 1% 1/10W MF-LF 603
R9724 60.4K 1% 1/16W MF-LF 402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2413	1	IC,APP001A,WHT LED BKLGHT CTR,SCRN,QFN20	U9700	CRITICAL	

*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT

LCD BACKLIGHT DRIVER
SYNC_MASTER=KIRAN_K20
SYNC_DATE=03/19/2009

APPLE INC.
SIZE D | DRAWING NUMBER 051-8071 | REV. B
SCALE NONE | SHT 85 OF 98



PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

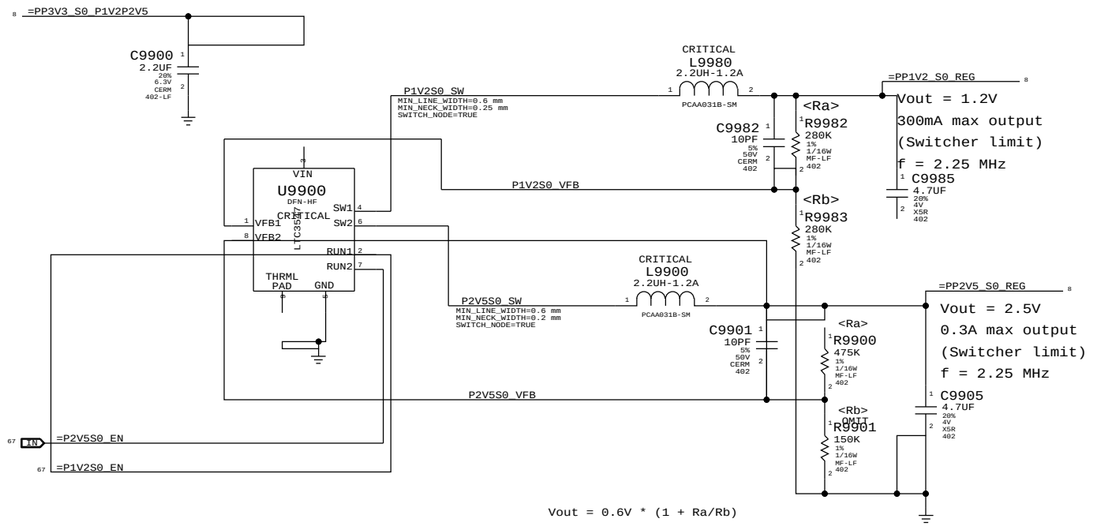
LCD Backlight Support

SYNC_MASTER=YLEE_K20 SYNC_DATE=07/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE	SHT	OF
NONE	86	98

GMUX 1.8V/1.2V S0 Switcher



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0428	1	RES,MTL FILM,1/16W,150K,1,0402,SMD,LF	R9901		GMUX_2V5
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R9901		GMUX_1V8

Misc Power Supplies

SYNC_MASTER=RXU_K20 SYNC_DATE=05/07/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 87 OF 98	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	7 10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9 10 14
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	7 10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9 10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9 10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9 10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 42 61
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 14 42
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9 10 14 61
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 61
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	61
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 26
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6 10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	6 10
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6 10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6 10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6 10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	9 11
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	9 61
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 61
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 61
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	61
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	61

CPU/FSB Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 88 OF 98	

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 27
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 27
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

Memory Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 89 OF 98	

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	69
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	69
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9 69
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9 69
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	9 69
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	9 69
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	69
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	69
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	7 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	7 30
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 30
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	7 17 30
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	7 17 30
	PCIE_90D	PCIE	PCIE_FW_R2D_P	35
	PCIE_90D	PCIE	PCIE_FW_R2D_N	35
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17 35
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17 35
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	17 35
	PCIE_90D	PCIE	PCIE_FW_D2R_N	17 35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	35
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	7 31
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	7 31
PCIE_EXCARD_R2D	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P	17 31
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N	17 31
PCIE_EXCARD_D2R	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P	7 17 31
	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N	7 17 31
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	17 69
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	17 69
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 30
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 35
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 35
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	17 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	17 31
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	18 24
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	18 24
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	18 24
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	18 24
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	18 24
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	18 24
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	18 24
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	9 81
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	9 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18 81
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18 24
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 84
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 84
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	9 18
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	9 18
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 84
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 84
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	9 18
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	9 18
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	18 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	18 24
SATA_HDD_R2D	SATA_100D	SATA	SATA_HDD_R2D_C_P	20 38
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20 38
	SATA_100D	SATA	SATA_HDD_R2D_P	7 38
	SATA_100D	SATA	SATA_HDD_R2D_N	7 38
SATA_HDD_D2R	SATA_100D	SATA	SATA_HDD_D2R_P	20 38
	SATA_100D	SATA	SATA_HDD_D2R_N	20 38
	SATA_100D	SATA	SATA_HDD_D2R_C_P	7 38
	SATA_100D	SATA	SATA_HDD_D2R_C_N	7 38
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 38
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 38
	SATA_100D	SATA	SATA_ODD_R2D_P	7 38
	SATA_100D	SATA	SATA_ODD_R2D_N	7 38
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	20 38
	SATA_100D	SATA	SATA_ODD_D2R_N	20 38
	SATA_100D	SATA	SATA_ODD_D2R_C_P	7 38
	SATA_100D	SATA	SATA_ODD_D2R_C_N	7 38
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20

MCP Constraints 1

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 90 OF 98	

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	7 19 41 43 84
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	7 19 41 43 84
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 25 84
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	25 41
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	7 25 43
USB_EXTA	USB_90D	USB	USB_EXTA_P	20 39
	USB_90D	USB	USB_EXTA_N	20 39
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	9 20
	USB_90D	USB	USB_MINI_N	9 20
USB_EXTD	USB_90D	USB	USB_EXTD_P	9 20
	USB_90D	USB	USB_EXTD_N	9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	20 30
	USB_90D	USB	USB_CAMERA_N	20 30
USB_BT	USB_90D	USB	USB_BT_P	20 30
	USB_90D	USB	USB_BT_N	20 30
USB_TPAD	USB_90D	USB	USB_TPAD_P	20 49
	USB_90D	USB	USB_TPAD_N	20 49
USB_IR	USB_90D	USB	USB_IR_P	20 40
	USB_90D	USB	USB_IR_N	20 40
USB_EXTB	USB_90D	USB	USB_EXTB_P	20 39
	USB_90D	USB	USB_EXTB_N	20 39
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	20 31
	USB_90D	USB	USB_EXCARD_N	20 31
USB_EXTC	USB_90D	USB	USB_EXTC_P	20 96 98
	USB_90D	USB	USB_EXTC_N	20 96 98
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	7 13 21 44
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	7 13 21 44
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	21 44
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	21 44
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	9 21
	HDA_55S	HDA	HDA_BIT_CLK_R	21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21 53
	HDA_55S	HDA	HDA_SYNC_R	21
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	21
	HDA_55S	HDA	HDA_RST_L	21 53
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	21 53
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21 53
	HDA_55S	HDA	HDA_SDOUT_R	21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	21 25
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	25 41
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	21 43
	SPI_55S	SPI	SPI_CLK	52
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	21 43
	SPI_55S	SPI	SPI_MOSI	52
SPI_MISO	SPI_55S	SPI	SPI_MISO	21 43
	SPI_55S	SPI	SPI_MISO_R	52
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	21 43
	SPI_55S	SPI	SPI_CS0_L	

MCP Constraints 2

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 33
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	32 33
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 32
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18 32
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	32
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 32
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 32
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 32
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 32
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 32
	ENET_MII_55S	ENET_MII	ENET_RESET_L	18 32
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	32 34
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	32 34

Ethernet Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING
FW_P0_TPA	FW_110D	FW_TP
FW_P0_TPA	FW_110D	FW_TP
FW_P0_TPB	FW_110D	FW_TP
FW_P0_TPB	FW_110D	FW_TP
FW_P1_TPA	FW_110D	FW_TP
FW_P1_TPA	FW_110D	FW_TP
FW_P1_TPB	FW_110D	FW_TP
FW_P1_TPB	FW_110D	FW_TP

Port 2 Not Used

FW_P0_TPA_P 35 37
FW_P0_TPA_N 35 37
FW_P0_TPB_P 35 37
FW_P0_TPB_N 35 37
FW_P1_TPA_P 35 37
FW_P1_TPA_N 35 37
FW_P1_TPB_P 35 37
FW_P1_TPB_N 35 37

FireWire Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	7 44
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	7 44
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	44
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	44
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	44
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	44
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	7 44
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	7 44
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	44
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	60
	1TO1_DIFFPAIR		CHGR_CSI_N	60
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	60
	1TO1_DIFFPAIR		CHGR_CSO_N	60

SMC Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	0.095 MM	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

From T18 MXM:

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
				NET_TYPE
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	81 84
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	81 84
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	7 81 84
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	7 81 84
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	7 81 84
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	81 84
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	7 81 84
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	7 81 84
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_P	7 78
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_N	7 78
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_P	7 78
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_N	7 78
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_P	78 81
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_N	78 81
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_P<2..0>	7 78 81
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_N<2..0>	7 78 81
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_P	78 81
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_N	78 81
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_P<2..0>	7 78 81
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_N<2..0>	7 78 81
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	82
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	82
DP_ML	DP_100D	DISPLAYPORT	**DP_ML_P<3..0>**	81 82
	DP_100D	DISPLAYPORT	**DP_ML_N<3..0>**	81 82
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	82
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	82
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	81 82
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	81 82

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
				NET_TYPE
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>	71 72 79
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>	71 72 79
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>	71 72 79
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>	7 71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>	7 71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L	71 72 79
FB_AB_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_A_CKE	71 72 79
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS0_L	71 72
FB_AB_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST	71 72 79
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>	71 72 79
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>	71 72 79
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>	71 72 79
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>	71 72 79
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>	71 72 79
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>	71 72 79
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>	71 72 79
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>	71 72 79
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>	71 72 79
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>	71 72 79
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>	7 71 72 79
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>	7 71 72 79
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>	7 71 72 79
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>	7 71 72 79
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>	71 72 79
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>	71 72 79
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>	71 72 79
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>	71 72 79
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>	71 72 79
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>	71 72 79
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>	71 72 79
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>	71 72 79
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>	71 72 79
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>	71 72 79
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>	71 72 79
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>	71 72 79
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>	7 71 72 79
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>	7 71 72 79
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>	7 71 72 79
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>	7 71 72 79
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>	71 72 79
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>	71 72 79
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>	71 72 79
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>	71 72 79
U200 FB_AB_CS1	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS1_L	71 79

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
				NET_TYPE
(CK505_DOT96)	CLK_SLOW_555	CLK_SLOW	GPU_CLK27M	75
CK505_CLK27MSS	CLK_SLOW_555	CLK_SLOW	GPU_CLK27M_SS	75
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_P	76 84
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_N	76 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<2..0>	76 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<2..0>	7 76 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<2..0>	76 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<2..0>	76 84
DP_ML	DP_100D	DISPLAYPORT	**DP_EG_ML_P<3..0>**	76 81
DP_ML	DP_100D	DISPLAYPORT	**DP_EG_ML_N<3..0>**	76 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_P	76 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_N	76 81
	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_P	81
	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_N	81

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
				NET_TYPE
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>	71 73 80
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>	71 73 80
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>	71 73 80
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>	71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>	71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>	7 71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>	7 71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L	71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L	7 71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L	71 73 80
FB_CD_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_B_CKE	71 73 80
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS0_L	7 71 73
FB_CD_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST	71 73 80
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>	71 73 80
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>	71 73 80
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>	71 73 80
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>	71 73 80
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>	71 73 80
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>	71 73 80
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>	71 73 80
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>	71 73 80
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>	71 73 80
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>	71 73 80
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>	7 71 73 80
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>	7 71 73 80
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>	7 71 73 80
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>	7 71 73 80
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>	71 73 80
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>	71 73 80
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>	71 73 80
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>	71 73 80
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>	71 73 80
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>	71 73 80
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>	71 73 80
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>	71 73 80
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>	71 73 80
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>	71 73 80
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>	71 73 80
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>	71 73 80
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>	7 71 73 80
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>	7 71 73 80
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>	7 71 73 80
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>	7 71 73 80
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>	71 73 80
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>	71 73 80
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>	71 73 80
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>	71 73 80
U200 FB_CD_CS1	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS1_L	71 80

GPU (G96) Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 95 OF 98	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	FSB_DSTB	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island.
Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

FLASH MEMORY BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FLSH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_MDI_100D	ENETCONN	ENETCONN_P<3..0>	34
	ENET_MDI_100D	ENETCONN	ENETCONN_N<3..0>	34
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	38
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	38
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	38
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	38
	SATA_100D	SATA	SATA_HDD_D2R_UF_P	38
	SATA_100D	SATA	SATA_HDD_D2R_UF_N	38
	SATA_100D	SATA	SATA_HDD_R2D_UF_P	38
	SATA_100D	SATA	SATA_HDD_R2D_UF_N	38
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCOREISNS_P	46 64
	SENSE_1TO1_55S	SENSE	MCPCOREISNS_N	46 64
CPUTHMSNS_D2_DP	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	47
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	47
CPU_THERMD_DP	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 47
	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 47
GPUTHMSNS_D_DP	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	47
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	47
GPU_THERMD_DP	THERM_1TO1_55S	THERM	GPU_TDIODE_P	47 75
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	47 75
MCPTHMSNS_D_DP	THERM_1TO1_55S	THERM	MCPTHMSNS_D_P	7 47
	THERM_1TO1_55S	THERM	MCPTHMSNS_D_N	7 47
MCP_THERMD_DP	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	21 47
	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	21 47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_P	46
	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_R_P	46
	SENSE_1TO1_55S	SENSE	DDRISNS_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_P	46
	SENSE_1TO1_55S	SENSE	GPUISENS_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPU_P	46 65
	SENSE_1TO1_55S	SENSE	1V05CPU_N	46 65
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_P	46
	SENSE_1TO1_55S	SENSE	DDRISNS_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPU_P	46
	SENSE_1TO1_55S	SENSE	P1V8GPU_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	45
	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	45
		GND	GND	
		SB_POWER	PP3V3_S5	7 8
		SB_POWER	PP3V3_S0	7 8 9
		SB_POWER	PP1V5_S0	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_P	
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_P	46
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_N	46
ASIC_CNTRLMEM1	FLSH_55S		NF_CLE_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_ALE_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_CE0_L_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_CE1_L_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_RE0_L_R	96
ASIC_CNTRLMEM1	FLSH_55S		NF_WE0_L_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CLE_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_ALE_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CE0_L_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CE1_L_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_RE0_L_R	96
ASIC_CNTRLMEM2	FLSH_55S		NF_WE0_L_R	96
ASIC_CNTRLMEM3	FLSH_55S		NF_CLE	96
ASIC_CNTRLMEM3	FLSH_55S		NF_ALE	96
ASIC_CNTRLMEM3	FLSH_55S		NF_CE0_L	96
ASIC_CNTRLMEM3	FLSH_55S		NF_CE1_L	96
ASIC_CNTRLMEM3	FLSH_55S		NF_RE0_L	96
ASIC_CNTRLMEM3	FLSH_55S		NF_WE0_L	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CLE	96
ASIC_CNTRLMEM2	FLSH_55S		NF_ALE	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CE0_L	96
ASIC_CNTRLMEM2	FLSH_55S		NF_CE1_L	96
ASIC_CNTRLMEM2	FLSH_55S		NF_RE0_L	96
ASIC_CNTRLMEM2	FLSH_55S		NF_WE0_L	96

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	7 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	7 30
	1TO1_DIFFPAIR		CHGR_CSI_R_P	60
	1TO1_DIFFPAIR		CHGR_CSI_R_N	60
	1TO1_DIFFPAIR		CHGR_CSO_R_P	45 60
	1TO1_DIFFPAIR		CHGR_CSO_R_N	45 60
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	39
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	39
(USB_EXTA)	USB_90D	USB	USB2_LT1_P	7 39
(USB_EXTA)	USB_90D	USB	USB2_LT1_N	7 39
(USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_P	
(USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_N	
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P	7 30
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N	7 30
	USB_90D	USB	CONN_USB2_BT_P	7 30
	USB_90D	USB	CONN_USB2_BT_N	7 30
	USB_90D	USB	USB_LT2_P	7 39
	USB_90D	USB	USB_LT2_N	7 39
	USB_90D	USB	USB2_EXCARD_CONN_P	7 31
	USB_90D	USB	USB2_EXCARD_CONN_N	7 31
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_P	81
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_N	81
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
PCIE_FC_R2D	PCIE_90D	PCIE	PCIE_FC_R2D_C_P	
	PCIE_90D	PCIE	PCIE_FC_R2D_C_N	
PCIE_FC_D2R	PCIE_90D	PCIE	PCIE_FC_D2R_P	
	PCIE_90D	PCIE	PCIE_FC_D2R_N	
	PCIE_90D	PCIE	PCIE_FC_R2D_P	
	PCIE_90D	PCIE	PCIE_FC_R2D_N	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N	7 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P	7 31
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_N	7 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_N	7 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_N	7 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_N	7 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_P	7 56 57
	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_N	7 56 57
	USB_90D	USB	USB_EXTC_P	20 91 98
	USB_90D	USB	USB_EXTC_N	20 91 98
	USB_90D	USB	USB_LT3_P	7 98
	USB_90D	USB	USB_LT3_N	7 98

Project Specific Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE: NONE	SHT 96 OF 98	

M99 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE:From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

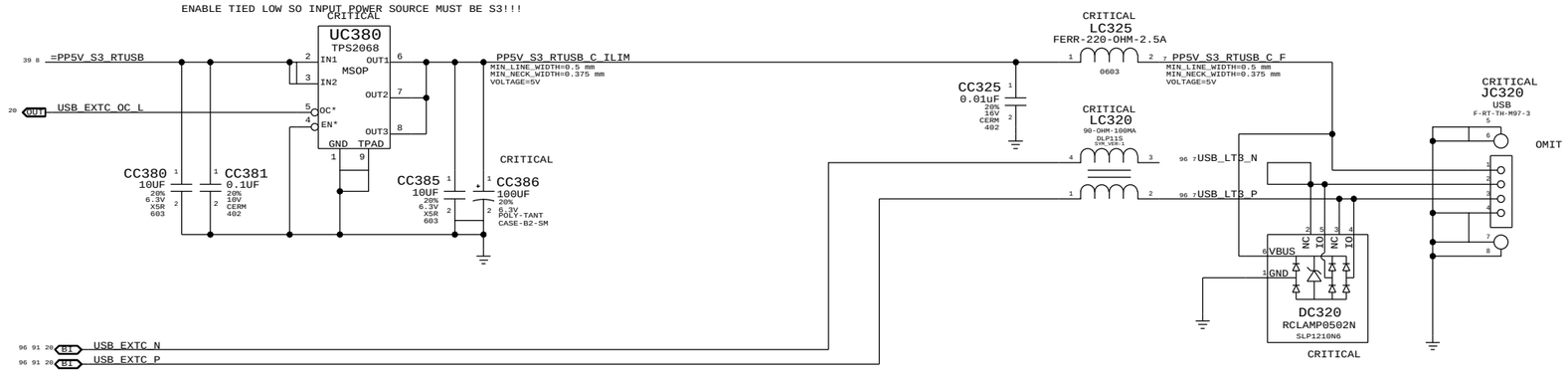
SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE D | DRAWING NUMBER 051-8071 | REV. 8

SCALE NONE | SHT 97 OF 98

Port Power Switch



LEFT USB PORT C

PLACE LC320 AND LC325 AT CONNECTOR PIN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0638	1	CONN,RCPT,USB,HB,4P	JC320	CRITICAL	

PROJECT SPECIFIC CONNS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	8
SCALE: NONE	SHT 98 OF 98	