1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
C	0000734528	PRODUCTION RELEASED	2009-06-04

K24 MLB SCHEMATIC

6/12/2009

Page (.csa)		Contents	Sync Date
1	1	Table of Contents	T17_MLB 08/22/2007
2	2	System Block Diagram	T18_MLB 12/12/2007
3	3	Power Block Diagram	DRAGON 03/13/2008
4	4	BOM Configuration	M97_MLB
5	5	Revision History	M97_MLB
6	7	FUNC TEST	M97_MLB
7	8	Power Aliases	BEN 04/21/2008
8	9	SIGNAL ALIAS	M97_MLB
9	10	CPU FSB	T18_MLB 12/12/2007
10	11	CPU Power & Ground	T18_MLB 12/12/2007
11	12	CPU Decoupling	RAYMOND 03/31/2008
12	13	eXtended Debug Port(MiniXDP)	K19_MLB 11/07/2008
13	14	MCP CPU Interface	T18_MLB 04/04/2008
14	15	MCP Memory Interface	T18_MLB 04/04/2008
15	16	MCP Memory Misc	T18_MLB 04/04/2008
16	17	MCP PCIe Interfaces	T18_MLB 04/04/2008
17	18	MCP Ethernet & Graphics	T18_MLB 04/04/2008
18	19	MCP PCI & LPC	T18_MLB 04/04/2008
19	20	MCP SATA & USB	T18_MLB 04/04/2008
20	21	MCP HDA & MISC	T18_MLB 06/26/2008
21	22	MCP Power & Ground	T18_MLB 04/04/2008
22	25	MCP Standard Decoupling	T18_MLB 04/04/2008
23	26	MCP Graphics Support	T18_MLB 12/12/2007
24	28	SB Misc	RAYMOND 04/05/2008
25	29	FSB/DDR3 Vref Margining	BEN 03/31/2008
26	31	DDR3 SO-DIMM Connector A	BEN 06/30/2008
27	32	DDR3 SO-DIMM Connector B	BEN 05/09/2008
28	33	DDR3 Support	T18_MLB 04/04/2008
29	34	Right Clutch Connector	YITE 04/22/2008
30	35	SECUREDIGITAL CARD READER	VEMURI 01/30/2009
31	37	Ethernet PHY (RTL8211CL)	SUMA 05/23/2008
32	38	Ethernet & AirPort Support	SUMA 07/01/2008
33	39	ETHERNET CONNECTOR	SUMA 04/04/2008
34	41	FireWire LLC/PHY (FW643)	K19_MLB 11/02/2008
35	42	FireWire Port Power	YUN_K19_MLB 12/22/2008
36	43	FireWire Ports	K19_MLB 11/02/2008
37	45	SATA Connectors	K19_MLB 12/04/2008
38	46	External USB Connectors	YUAN.MA 01/18/2008
39	48	Front Flex Support	YUAN.MA 05/28/2008
40	49	SMC	T18_MLB 06/26/2008
41	50	SMC Support	YUAN.MA 05/28/2008
42	51	LPC+SPI Debug Connector	CHANGZHANG 05/09/2008
43	52	K24 SMBUS CONNECTIONS	BEN 04/21/2008
44	53	VOLTAGE SENSING	YUNWU 02/04/2008
45	54	Current Sensing	YUNWU 12/17/2008
46	55	Thermal Sensors	YUNWU 03/20/2008
47	56	Fan	CHANGZHANG 01/18/2008
48	57	WELLSPRING 1	YUAN.MA 04/22/2008
49	58	WELLSPRING 2	YUAN.MA 05/09/2008
50	59	SMS	YUNWU 06/26/2008
51	61	SPI ROM	CHANGZHANG 05/02/2008
52	62	AUDIO: CODEC/REGULATOR	AUDIO 03/04/2009
53	63	AUDIO: LINE INPUT FILTER	AUDIO 01/31/2009
54	65	AUDIO: HEADPHONE FILTER	AUDIO 02/03/2009
55	66	AUDI0: SPEAKER AMP	AUDIO 12/18/2008
56	67	AUDIO: JACK	AUDIO 03/20/2009
57	68	AUDIO: JACK TRANSLATORS	AUDIO 03/20/2009
58	69	DC-In & Battery Connectors	YUNWU 12/11/2008
59	70	PBUS Supply/Battery Charger	RAYMOND 01/31/2008
60	72	5V/3.3V SUPPLY	RAYMOND 02/08/2008
61	73	1.5V/0.75V DDR3 SUPPLY	RAYMOND 01/31/2008
62	74	IMVP6 CPU VCore Regulator	RAYMOND 01/31/2008
63	75	MCP CORE REGULATOR	K19_MLB 12/10/2008
64	76	CPU VTT(1.05V) SUPPLY	RAYMOND 02/08/2008
65	77	MISC POWER SUPPLIES	RAYMOND 01/23/2008
66	78	POWER SEQUENCING	YUAN.MA 12/11/2008
67	79	POWER FETS	YUAN.MA 12/11/2008
68	90	LVDS CONNECTOR	NMARTIN 04/04/2008
69	93	DISPLAYPORT SUPPORT	AMASON 04/18/2008
70	94	DisplayPort Connector	AMASON 06/30/2008
71	97	LCD BACKLIGHT DRIVER	KIRAN 12/05/2008
72	98	LCD Backlight Support	YITE 06/30/2008
73	100	CPU/FSB Constraints	T18_MLB 01/04/2008
74	101	Memory Constraints	T18_MLB 01/04/2008
75	102	MCP Constraints 1	T18_MLB 01/04/2008
76	103	MCP Constraints 2	T18_MLB 12/14/2007
77	104	Ethernet Constraints	T18_MLB 03/19/2008
78	105	FireWire Constraints	K19_MLB 12/01/2008
79	106	SMC Constraints	T18_MLB 01/04/2008
80	107	K24 SPECIAL CONSTRAINTS	M97_MLB
81	109	K24 RULE DEFINITIONS	M97_MLB

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7898	1	SCHEM,MLB,K24	SCH	CRITICAL	
820-2530	1	PCBF,MLB,K24	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,K24

Apple Inc.

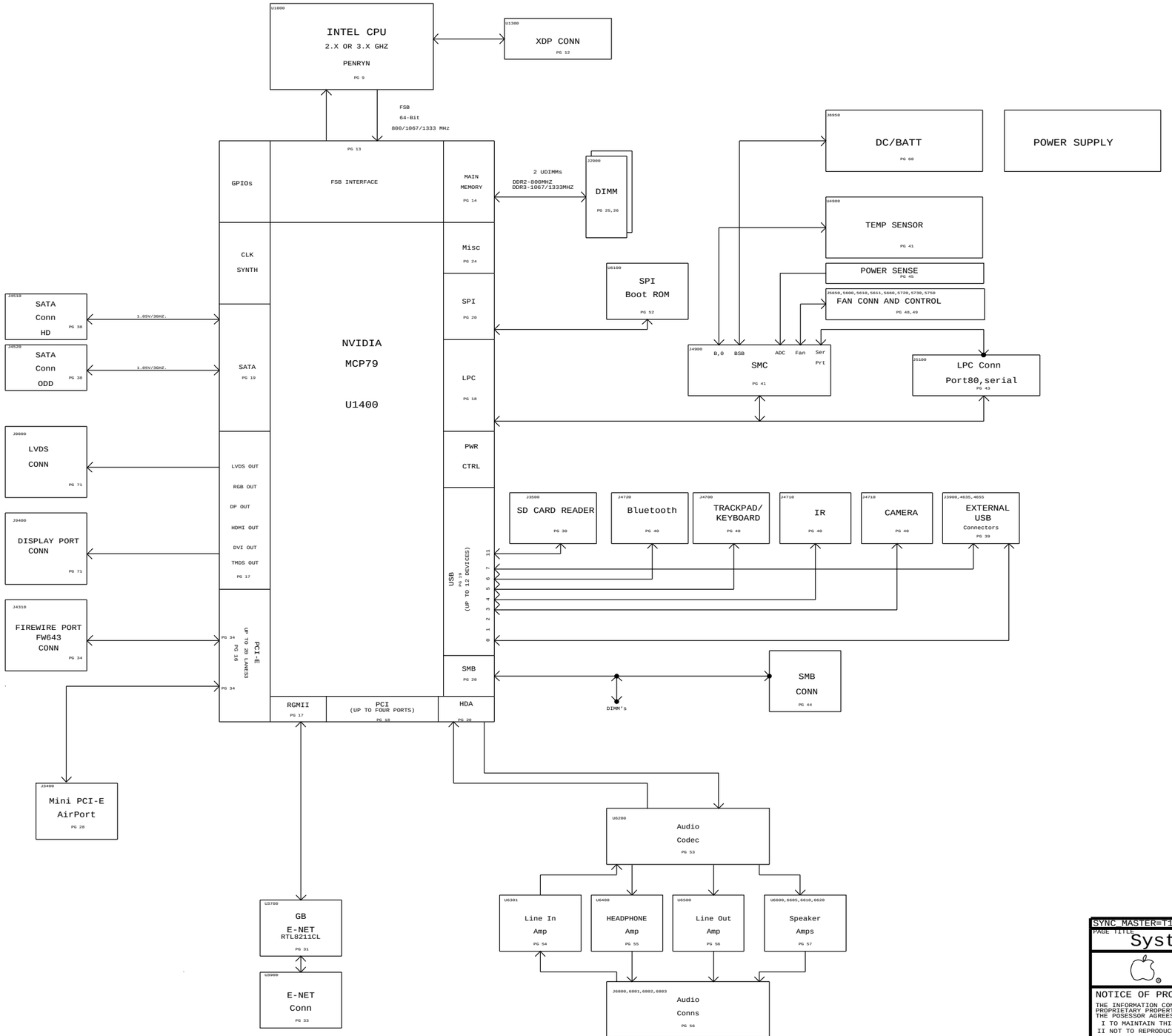
DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 1 OF 109

SHEET: 1 OF 81



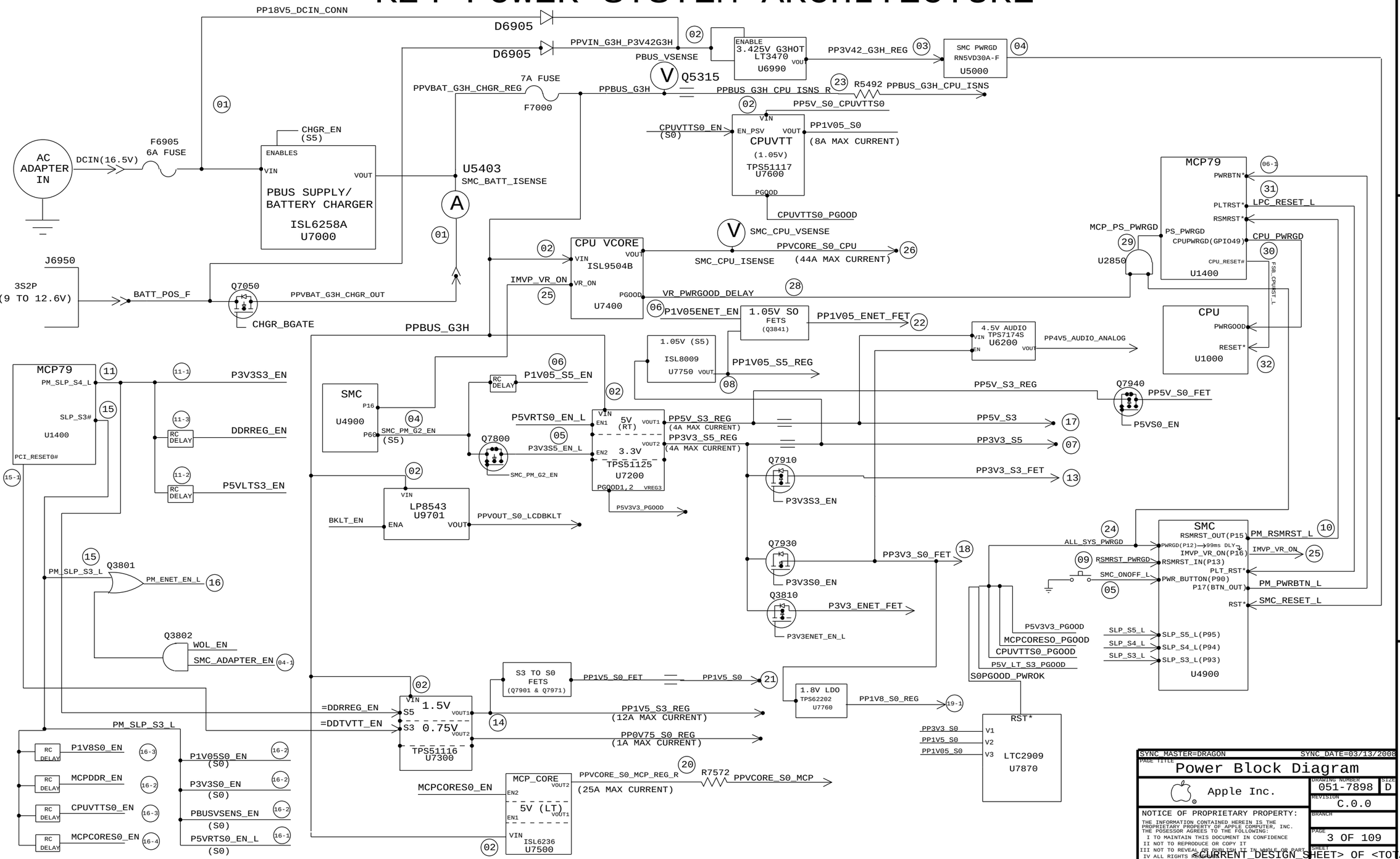
SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

PAGE TITLE
System Block Diagram

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 2 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

K24 POWER SYSTEM ARCHITECTURE



SYNC_MASTER=DRAGON SYNC_DATE=03/13/2008

PAGE TITLE: Power Block Diagram

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 3 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9923	PCBA,MLB,BETTER,K24	K24_COMMON,CPU_2_26GHZ,EEE_6GC,KB_BL
630-9924	PCBA,MLB,BEST,K24	K24_COMMON,CPU_2_53GHZ,EEE_6GD,KB_BL

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6G4]	CRITICAL	EEE_6G4
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6GC]	CRITICAL	EEE_6GC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6GD]	CRITICAL	EEE_6GD

BOM Groups

BOM GROUP	BOM OPTIONS
K24_COMMON	COMMON,ALTERNATE,K24_MCP,K24_MISC,K24_DEBUG_PROD,K24_PROGPARTS
K24_MCP	MCP_B03,BOOT_MODE_USER,MCPSEQ_SMC
K24_MISC	ONEWIRE_PU,DP_ESD,MIKEY,BKLT_PROD,SUPERCAP_NO,LDO_NO
K24_PROGPARTS	BOOTROM_PROG,SMC_PROG,IR_PROG,WELLSPRING_PROG
K24_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K24_DEBUG_PVT	DEVEL_BOM,BMON_PROD,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K24_DEBUG_PROD	BMON_PROD,SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K24_DEVEL_ENG	BMON_ENG,XDP_CONN,LPCPLUS,VREFMRGN,FWPHY_WAKE_YES
K24_DEVEL_PVT	LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3646	1	PDC,SLGBE,PRQ,2.0,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3704	1	PDC,SLGE2,PRQ,2.26,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3639	1	PDC,SLB4N,PRQ,2.4,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3756	1	PDC,SLGFG,PRQ,2.53,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3761	1	PDC,SLGLA,PRQ,2.66,25W,1066,E0,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
338S0710	1	IC,GMCP,MCP79,35X35MM,BGA1437,B03	U1400	CRITICAL	MCP_B03

Programmable Parts

338S0563	1	IC,SMC,HSB/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341S2445	1	IC,SMC,K24	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2441	1	IC,PRGRM,EFI BOOTROM,UNLOCK,K24	U6100	CRITICAL	BOOTROM_PROG
338S0375	1	IC,CY7C63833,ENCORE II,USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093	1	IC,IR CONTROLLER,M97	U4800	CRITICAL	IR_PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2503	1	IC,PRGRM,WELLSPRING CONTROLLER	U5701	CRITICAL	WELLSPRING_PROG

LOCKED BOOTROM APN IS 341S2443

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
152S1025	152S1024		ALL	TOKO AS ALTERNATE
337S3769	337S3704		ALL	INTEL P7550 CPU AS ALTERNATE
353S2718	353S2310		ALL	INTERSIL AS ALTERNATE

K24 BOARD STACK-UP

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0741	1	K24 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM

SYNC MASTER=M97 MLB

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 4 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Revision History

SYNC MASTER=M97 MLB
PAGE TITLE
Revision History

Apple Inc.

DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
BRANCH
PAGE 5 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Functional Test Points

Fan Connectors

H42	TRUE	PP5V_S0	(NEED 3 TP) 6D3 7D5
H43	TRUE	FAN_RT_PWM	47B4
H45	TRUE	FAN_RT_TACH	47C4

(NEED TO ADD 3 GND TP)

MIC FUNC_TEST

H38	TRUE	BI_MIC_LO	56C2 57B1
H39	TRUE	BI_MIC_HI	56C2 57B1
H40	TRUE	BI_MIC_SHIELD	56C2 57B1

SPEAKER FUNC_TEST

H42	TRUE	SPKRAMP_L_N_OUT	55A2 56B2
H43	TRUE	SPKRAMP_L_P_OUT	55B2 56B2
H44	TRUE	SPKRAMP_R_N_OUT	55C2 56A2
H46	TRUE	SPKRAMP_R_P_OUT	55C2 56B2
H47	TRUE	SPKRAMP_SUB_N_OUT	55B2 56B2
H48	TRUE	SPKRAMP_SUB_P_OUT	55C2 56B2

THERMAL FUNC_TEST

H50	TRUE	MCPTHMSNS_D2_P	46B5 80D3
H51	TRUE	MCPTHMSNS_D2_N	46B5 80D3

LVDS FUNC_TEST

H60	TRUE	PP3V3_LCDVDD_SW_F	6C3 68C2
H61	TRUE	PP3V3_S0_LCD_F	68C3
H62	TRUE	PPVOUT_S0_LCDBKLT	6C3 68B2 71C1
H63	TRUE	LVDS_IG_DDC_CLK	17B3 68C5
H64	TRUE	LVDS_IG_DDC_DATA	17A3 68C5
H65	TRUE	LVDS_IG_A_DATA_N<0>	17B3 68C2 75B3
H66	TRUE	LVDS_IG_A_DATA_P<0>	17B3 68C2 75B3
H67	TRUE	LVDS_IG_A_DATA_N<1>	17B3 68C2 75B3
H68	TRUE	LVDS_IG_A_DATA_P<1>	17B3 68C2 75B3
H69	TRUE	LVDS_IG_A_DATA_N<2>	17B3 68C2 75B3
H70	TRUE	LVDS_IG_A_DATA_P<2>	17B3 68C2 75B3
H71	TRUE	LVDS_IG_A_CLK_F_N	68C2 75B3
H72	TRUE	LVDS_IG_A_CLK_F_P	68C2 75B3
H73	TRUE	LED_RETURN_1	68B3 71B1
H74	TRUE	LED_RETURN_2	68B3 71B1
H75	TRUE	LED_RETURN_3	68B3 71B1
H76	TRUE	LED_RETURN_4	68B3 71B1
H77	TRUE	LED_RETURN_5	68B3 71B1
H78	TRUE	LED_RETURN_6	68B3 71A1
H80	TRUE	TP_BKL_SYNC	68C2

(NEED TO ADD 5 GND TP)

SATA ODD CONN

H85	TRUE	PP5V_SW_ODD	(NEED 4 TP) 6C3 37D3
H86	TRUE	SMC_ODD_DETECT	37C7 40B8
H87	TRUE	SATA_ODD_D2R_C_P	37C6 75A3
H88	TRUE	SATA_ODD_D2R_C_N	37C6 75A3
H89	TRUE	SATA_ODD_R2D_P	37C6 75A3
H90	TRUE	SATA_ODD_R2D_N	6A7 37C6 75A3

(NEED TO ADD 4 GND TP)

SATA HDD/IR/SIL

H91	TRUE	PP5V_S0_HDD_FLT	(NEED 4 TP) 6C3 37B6
H92	TRUE	SATA_HDD_R2D_P	37A5 75A3
H93	TRUE	SATA_HDD_R2D_N	37A5 75A3
H94	TRUE	SATA_HDD_D2R_C_P	37B5 75A3
H95	TRUE	SATA_HDD_D2R_C_N	37B5 75A3
H97	TRUE	SYS_LED_ANODE_R	37A7
H98	TRUE	IR_RX_OUT	37A7 39D4
H99	TRUE	PP5V_S3_IR_R	37A7

(NEED TO ADD 4 GND TP)

BATT POWER CONN

H82	TRUE	SMBUS_SMC_BSA_SCL	6A7 43C5 79D3
H83	TRUE	SMBUS_SMC_BSA_SDA	43C5 79D3
H84	TRUE	SYS_DETECT_L	58A8
H85	TRUE	BATT_POS_F	(NEED 3 TP) 58A7 58B8 59A3

(NEED TO ADD 3 GND TP)

BATT SIGNAL CONN

H52	TRUE	PP3V42_G3H	(NEED 3 TP) 6B5 6D3 7D1
H53	TRUE	SMBUS_SMC_BSA_SCL	6A7 43C5 79D3
H54	TRUE	SMBUS_SMC_BSA_SCL	6A7 43C5 79D3
H55	TRUE	SMC_BIL_BUTTON_L	40C5 58C4
H56	TRUE	SMC_LID_R	58C2

(NEED TO ADD 5 GND TP)

RIGHT CLUTCH CONN

H30	TRUE	PP5V_S3_BTCAMERA_F	29C7
H31	TRUE	PCIE_MINI_D2R_P	16B6 29C7 75D3
H32	TRUE	PCIE_MINI_D2R_N	16B6 29C7 75D3
H33	TRUE	PCIE_MINI_R2D_P	29C7 75D3
H34	TRUE	PCIE_MINI_R2D_N	29C7 75D3
H35	TRUE	PCIE_CLK100M_MINI_CONN_P	29C7 75D3
H36	TRUE	PCIE_CLK100M_MINI_CONN_N	29C7 75D3
H37	TRUE	USB_CAMERA_CONN_P	29B7 76C3
H38	TRUE	USB_CAMERA_CONN_N	29B7 76C3
H39	TRUE	PP5V_WLAN	(NEED 2 TP) 6C3 29C5
H40	TRUE	PCIE_WAKE_L	16B6 29C7
H42	TRUE	SMBUS_SMC_A_S3_SCL	6C5 43D2 79D3
H43	TRUE	SMBUS_SMC_A_S3_SDA	6C5 43D2 79D3
H44	TRUE	CONN_USB2_BT_P	29B7 76C3
H45	TRUE	CONN_USB2_BT_N	29B7 76B3
H46	TRUE	MINI_CLKREQ_O_L	29C7
H47	TRUE	MINI_RESET_CONN_L	29A7

(NEED TO ADD 6 GND TP)

IPD_FLEX_CONN

H70	TRUE	PP3V3_S3_LDO	6C3 49B4 49C3
H71	TRUE	PP18V5_S3	6C3 49C1 49D3
H72	TRUE	Z2_CS_L	48C8 49C3
H73	TRUE	Z2_DEBUG3	48C8 49C3
H74	TRUE	Z2_MOSI	48C8 49C3
H75	TRUE	Z2_MISO	48C8 49C3
H76	TRUE	Z2_SCLK	48C8 49C3
H77	TRUE	Z2_BOOST_EN	49C3 49C5
H78	TRUE	Z2_HOST_INTN	48D8 49C3
H79	TRUE	Z2_CLKIN	48C6 49C3
H80	TRUE	Z2_KEY_ACT_L	48C8 49C1
H81	TRUE	Z2_RESET	48C8 49C1
H82	TRUE	PSOC_MISO	48C8 49C1
H83	TRUE	PSOC_MOSI	48C8 49C1
H84	TRUE	PSOC_SCLK	48C8 49C1
H85	TRUE	SMBUS_SMC_A_S3_SDA	6D5 43D2 79D3
H87	TRUE	SMBUS_SMC_A_S3_SCL	6D5 43D2 79D3
H88	TRUE	PSOC_F_CS_L	48C8 49C1
H89	TRUE	PICKB_L	48D8 49C1

KEYBOARD CONN

H34	TRUE	PP3V3_S3	6D3 7D3
H35	TRUE	PP3V42_G3H	6A7 6D3 7D1
H14	TRUE	WS_KBD1	48C6 48D2
H15	TRUE	WS_KBD2	48C6 48D2
H16	TRUE	WS_KBD3	48C6 48D2
H17	TRUE	WS_KBD4	48C6 48D2
H18	TRUE	WS_KBD5	48C6 48D2
H19	TRUE	WS_KBD6	48C6 48D2
H20	TRUE	WS_KBD7	48C6 48D2
H21	TRUE	WS_KBD8	48C6 48D2
H24	TRUE	WS_KBD9	48C6 48D2
H25	TRUE	WS_KBD10	48C6 48D2
H26	TRUE	WS_KBD11	48C6 48D2
H27	TRUE	WS_KBD12	48C6 48D2
H28	TRUE	WS_KBD13	48C6 48D2
H29	TRUE	WS_KBD14	48C2 48C6
H30	TRUE	WS_KBD15_CAP	48C2
H31	TRUE	WS_KBD16_NUM	48C2
H32	TRUE	WS_KBD17	48C2 48D6
H33	TRUE	WS_KBD18	48C2 48D7
H36	TRUE	WS_KBD19	48C2 48D7
H38	TRUE	WS_KBD20	48C2 48D7
H39	TRUE	WS_KBD21	48C2 48D7
H37	TRUE	WS_KBD22	48C2 48D7
H40	TRUE	WS_KBD23	48C2 48D7
H41	TRUE	WS_KBD_ONOFF_L	48C2
H42	TRUE	WS_LEFT_SHIFT_KBD	48B3 48B5 48C2
H97	TRUE	WS_LEFT_OPTION_KBD	48B3 48B5 48C2
H96	TRUE	WS_CONTROL_KBD	48B3 48B5 48C2

(NEED TO ADD 1 GND TP)

KBD BACKLIGHT CONN

H45	TRUE	KBDLED_ANODE	(NEED 2 TP) 49A4
H92	TRUE	SMC_KDBLED_PRESENT_L	49A4 49A6

(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

H28	TRUE	PPVCORE_S0_CPU	7D7
H30	TRUE	PPVCORE_S0_MCP	7C7
H34	TRUE	PP0V75_S0	7C7
H36	TRUE	PP1V05_S0	7D7
H38	TRUE	PP1V5_S0	7C6
H39	TRUE	PP1V8_S0	78G
H40	TRUE	PP5V_S0	6D7 7D5
H41	TRUE	PP3V3_S0	7D5
H42	TRUE	PP1V5_S3	7D3
H43	TRUE	PP3V3_S3	68B 7D3
H44	TRUE	PP5V_S3	7C3
H45	TRUE	PP1V1R1V05_S5	78J
H46	TRUE	PP3V3_S5	78J
H47	TRUE	PP3V42_G3H	6A7 68B 7D1
H48	TRUE	PPBUS_G3H	7C1
H49	TRUE	PP3V3_ENET_PHY	78S
H50	TRUE	PP1V2R1V05_ENET	78S
H52	TRUE	PP3V3_G3_RTC	20C8 21A5 24D4
H53	TRUE	PP5V_WLAN	6D5 29C5
H55	TRUE	PP5V_SW_ODD	6B7 37D3
H56	TRUE	PP5V_S0_HDD_FLT	6B7 37B6
H58	TRUE	PP3V3_S5_AVREF_SMC	48D4 41C6
H59	TRUE	PP18V5_S3	6C5 49C1 49D3
H60	TRUE	PP3V3_S3_LDO	6C5 49B4 49C3
H61	TRUE	PP3V3_LCDVDD_SW_F	6C7 68C2
H62	TRUE	PPVOUT_S0_LCDBKLT	6C7 68B2 71C1
H63	TRUE	PP4V5_AUDIO_ANALOG	52A5 52D2 52D7
H64	TRUE	SM_PM_G2_EN	40D5 60C5 66D8
H65	TRUE	PM_SLP_S4_L	20C3 40C5 41A2 66C8
H66	TRUE	PM_SLP_S3_L	20C3 32B7 35A5 40C5 66D5 70D8

(NEED TO ADD 4 GND TP)

DC POWER CONN

H57	TRUE	PP18V5_DCIN_FUSE	(NEED 3 TP) 58D6
H58	TRUE	ADAPTER_SENSE	58D7

(NEED TO ADD 4 GND TP)

SYNC_MASTER=M97_MLB

PAGE TITLE: FUNC TEST

Apple Inc.

DRAWING NUMBER: 051-7898 | SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 7 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

"S0,S0M" RAILS

62D1 =PPVCORE_S0_CPU_REG (CPU VCORE PWR)
PPVCORE_S0_CPU — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.3 MM, VOLTAGE=1.25V, MAKE_BASE=TRUE — 6D3
=PPVCORE_S0_CPU — 10B5 10D6 11D6
=PPVCORE_S0_CPU_VSENSE — 44D8

64C2 =PPCPUVTT_S0_REG
PP1V05_S0 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE — 6D3
=PP1V05_S0_CPU — 9D5 10C6 11B6 12D6
=PP1V05_S0_MCP_FSB — 13A2 13B7 21D3 22C8
=PP1V05_S0_SMC_LS
=PP1V05_S0_MCP_PEX_DVDD — 7A8 22D8
=PP1V05_S0_MCP_AVDD_UF — 22D4
=PP1V05_S0_MCP_SATA_DVDD — 7A8 22D6
=PP1V05_S0_MCP_HDMI_VDD — 17A6 23D7
=PP1V05_S0_VMON — 66A8
=PP1V05_S0_MCP_PLL_UF_R — 65B3
=PP1V05_FW_P1V05FWFET — 35C6
=PP1V05_FWPWRCTL — 35B4

63C7 63C1 63B8 =PPMCPCORE_S0_REG (MCP VCORE AFTER SENSE RES)
PPVCORE_S0_MCP — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.25V, MAKE_BASE=TRUE — 6D3
=PPVCORE_S0_MCP — 21D5 22D8
=PPVCORE_S0_MCP_VSENSE — 44D8

61C8 =PP0V75_S0_REG
PP0V75_S0 — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0.75V, MAKE_BASE=TRUE — 6D3
=PPVTT_S0_VTTCLAMP — 67B3
=PP0V75_S0_MEM_VTT_A — 26A4
=PP0V75_S0_MEM_VTT_B — 27A4

67D1 =PP1V5_S0_FET
PP1V5_S0 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE — 6D3
=PP1V5_S0_CPU — 10B6 11B6
=PP1V5_S0_VMON — 66A8
=PP1V8R1V5_S0_MCP_MEM — 15C3 15C7 22C8
=PP1V5_S0_MEM_MCP — 27B3
=PP1V5_S0_MCP_PLL_VLDO — 65B6

65C5 =PP1V8_S0_REG
PP1V8_S0 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.8V, MAKE_BASE=TRUE — 6D3
=PP3V3R1V8_S0_MCP_IFP_VDD — 17B6 23D7
=PP1V8_S0_AUDIO — 52D7

65B1 22C4 =PP1V05_S0_MCP_PLL_UF
PP1V05_S0_MCP_PLL_UF — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V, MAKE_BASE=TRUE

67B6 =PP5V_S0_FET
PP5V_S0 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V, MAKE_BASE=TRUE — 6D3 6D7
=PP5V_S0_HDD — 37B3
=PP5V_S0_LPCPLUS — 42D5
=PP5V_S0_FAN_RT — 47C5
=PP5V_S0_CPU_IMVP — 42D8
=PP5V_S0_KBDLED — 49A5
=PP5V_S0_DP_AUX_MUX — 69B6
=PP5V_S0_CPUVTTS0 — 64C8
=PP5V_S0_BKL — 71D4
=PP5V_S0_MCPREG — 63D4
=PP5V_S0_VMON — 66B5

67C6 =PP3V3_S0_FET
PP3V3_S0 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE — 6D3
=PP3V3_S0_XDP — 12D6
=PP3V3_S0_MCP — 20C2 21B3 22B8
=PP3V3_S0_MCP_DAC_UF — 23D4
=PP3V3_S0_MCP_VPLL_UF — 23C7
=PP3V3_S0_ODD — 37C7 37D6
=PP3V3_S0_SMBUS_SMC_0_S0 — 43D5
=PP3V3_S0_SMBUS_SMC_B_S0 — 43C3
=PP3V3_S0_SMBUS_MCP_0 — 43D8
=PP3V3_S0_FAN_RT — 47C5
=PP3V3_S0_AUDIO — 52A8 52D2 56D8 57B8 57D3
=PP3V3_S0_IMVP — 62D8
=PP3V3_S0_LCD — 68C5
=PP3V3_S0_MCP_GPIO — 17C1 18D1 20A4
=PP3V3_S0_MCP_PLL_UF — 22B6
=PP3V3R1V5_S0_MCP_HDA — 20D3 20D8 22A8
=PP3V3_S0_SMC — 41A1 41D3
=PP3V3_S0_MCPTHMSNS — 46B6
=PP3V3_S0_CPUTHMSNS — 46D6
=PP3V3_S0_DPCONN — 70B8 70C8
=PPSPD_S0_MEM_A — 26A8
=PPSPD_S0_MEM_B — 27A8
=PP3V3_S0_PWRCTL — 66A5
=PP3V3_S0_VMON — 66A8
=PP3V3_S0_CPUVTTISNS — 45C7
=PP3V3_S0_TPAD — 49A6
=PP3V3_S0_SMBUS_MCP_1 — 43C8
=PP3V3_S0_P1V8S0 — 65D8
=PP3V3_S0_BKL_VDDIO — 71C7
=PP3V3_S0_MCPDDRISNS — 45D8
=PP3V3_S0_MCP_PLL_VLDO — 65C6
=PP3V3_S0_P3V3FWFET — 35D6
=PP3V3_S0_FWPWRCTL — 35B1 35D2

"ENET" RAILS

32D2 =PP3V3_ENET_FET
PP3V3_ENET_PHY — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE — 6C3
=PP3V3_ENET_MCP_RMGT — 17D3 17D7 22A5 22B6
=PP3V3_ENET_PHY — 31D7

32B2 =PP1V05_ENET_FET
PP1V2R1V05_ENET — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE — 6C3
=PP1V05_ENET_MCP_PLL_MAC — 22A8
=PP1V05_ENET_MCP_RMGT — 17D3 22D6
=PP1V05_ENET_PHY — 31D2

PEX & SATA AVDD/DVDD aliases

22D1 PP1V05_S0_MCP_PEX_AVDD (MAKE_BASE=TRUE) — 206 mA (A01)
22D8 7D7 =PP1V05_S0_MCP_PEX_DVDD — 206 mA (A01)
22D2 PP1V05_S0_MCP_SATA_AVDD (MAKE_BASE=TRUE) — 127 mA (A01)
22D6 7D7 =PP1V05_S0_MCP_SATA_DVDD — 127 mA (A01)

=PP1V05_S0_MCP_PEX_AVDD0 — 16B3
=PP1V05_S0_MCP_PEX_AVDD1 — 16A3 — 206 mA (A01)
=PP1V05_S0_MCP_PEX_DVDD0 — 16B6
=PP1V05_S0_MCP_PEX_DVDD1 — 16A6 — 57 mA (A01)
=PP1V05_S0_MCP_SATA_AVDD0 — 19B6
=PP1V05_S0_MCP_SATA_AVDD1 — 19B6 — 127 mA (A01)
=PP1V05_S0_MCP_SATA_DVDD0 — 19B6
=PP1V05_S0_MCP_SATA_DVDD1 — 19B6 — 43 mA (A01)

"S3" RAILS

61C1 =PP1V5_S3_REG
PP1V5_S3 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.5V, MAKE_BASE=TRUE — 6D3
=PP1V5_S3_P1V5S0FET — 67D3
=PP1V5_S3_MEM_A — 26D7
=PP1V5_S3_MEM_B — 27D7
=PP1V5_S3_MEMRESET — 28C6
=PP1V5_S3_HDD — 37B8

67D6 =PP3V3_S3_FET
PP3V3_S3 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE — 6B5 6D3
=PP3V3_S3_SMBUS_SMC_A_S3 — 43D3
=PP3V3_S3_PDCISENS — 61B3
=PP3V3_S3_SMBUS_SMC_MGMT — 43B5
=PP3V3_S3_VREFMRGN — 25D8
=PP3V3_S3_WLAN — 29A6
=PP3V3_S3_MCP_GPIO — 20A3
=PP3V3_S3_TPAD — 48A6 48B5 48C5 48D2
=PP3V3_S3_SMS — 50B7
=PP3V3_S3_CARDREADER — 30D7

60B8 =PP5V_S3_REG
PP5V_S3 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V, MAKE_BASE=TRUE — 6D3
=PP5V_S3_EXTUSB — 38C7
=PP5V_S3_IR — 37A8 39D7
=PP5V_S3_BTCAMERA — 29C3
=PP5V_S3_VTTCLAMP — 67A3
=PP5V_S3_MCPDDRFET — 67D4
=PP5V_S3_SYSLED — 41B8
=PP5V_S3_TPAD — 49B6 49D7
=PP5V_S3_WLAN — 29C1
=PP5V_S3_1V5S30V75S0 — 61C5
=PP5V_S3_AUDIO — 52A8 52D2 54D5 56B6
=PP5V_S3_AUDIO_AMP — 55B7 55C7 55D7
=PP5V_S3_P5VS0FET — 67B8
=PP5V_S3_ODD — 37D5

61D8 25D3 =PPVTT_S3_DDR_BUF
PPVTT_S3_DDR_BUF — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0.75V, MAKE_BASE=TRUE

"S5" RAILS

65A5 =PP1V05_S5_REG
PP1V1R1V05_S5 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE — 6D3
=PP1V05_S5_MCP_VDD_AUXC — 21A3 22D8
=PP1V05_ENET_P1V05ENETFET — 32C4

60B1 =PP3V3_S5_REG
PP3V3_S5 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE — 6D3
=PP3V3_S5_MCP_GPIO — 17C7 19C1
=PP3V3_S5_ROM — 42B5 42C7 51C6
=PP3V3_S5_LCD — 68C8
=PP3V3_S5_MCP — 21B3 22B8
=PP3V3_S5_MCPPWRGD — 24B8
=PP3V3_S5_PWRCTL — 66B3
=PP3V3_S5_P1V05ENETFET — 32C5
=PP3V3_S5_P3V3S3FET — 67D8
=PP3V3_S5_P3V3S0FET — 67C8
=PP3V3_S5_P1V05S5 — 65B8
=PP3V3_S5_MEMRESET — 28C4
=PP3V3_S5_P3V3ENETFET — 32D5
=PP3V3_S5_DP_PORT_PWR — 70D8
=PP3V3_FW_LATEVG — 36A7
=PP3V3_FW_LATEVG_ACTIVE — 35A8
=PP3V3_S5_P1V05FWFET — 35C7

"G3H" RAILS

58B4 =PP3V42_G3H_REG
PP3V42_G3H — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.42V, MAKE_BASE=TRUE — 6A7 6B5 6D3
=PPVIN_S5_SMCVREF — 41C8
=PP3V42_G3H_SMBUS_SMC_BSA — 43C5
=PP3V42_G3H_PWRCTL — 66B3 66C8 66D8
=PP3V42_G3H_CHGR — 59A8 59C6 59D5
=PP3V42_G3H_SMCUSBMUX — 38B8
=PP3V42_G3H_TPAD — 48B5 48C2 48C3 48C6
=PP3V42_G3H_BATT — 58C2 58C4
=PP3V3_S5_SMC — 40D4 41C1 41C3 41C7 41D8
=PP3V3_S5_LPCPLUS — 42C7 42C8 42D5
=PP3V42_G3H_RTC_D — 24D8
=PP3V42_G3H_BMON_ISNS — 45B8
=PP3V42_G3H_ONEWIRE — 58D2
=PP3V42_G3H_AUDIO — 66B6

58D1 58C8 =PP18V5_DCIN_CONN
PP18V5_G3H — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.3 MM, VOLTAGE=18.5V, MAKE_BASE=TRUE
=PP18V5_G3H_CHGR — 59D8

59C1 =PPBUS_G3H
PPBUS_G3H — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.3 MM, VOLTAGE=12.6V, MAKE_BASE=TRUE — 6C3
=PPBUS_S0_LCDBKLT — 72D8
=PPVIN_S0_MCPCORE — 63D5
=PPVIN_S5_1V5S30V75S0 — 61C2
=PPVIN_S5_3V3S5 — 60C3
=PPVIN_S3_5VS3 — 60C6 60C7
=PPBUS_G3HRS5 — 44B8
=PPBUS_S5_FWPWRSW — 35B7
=PPCPUVCORE_VTT_ISNS_R — 45B8
(BEFORE HIGH SIDE SENSING RES.)

45B7 =PPCPUVCORE_VTT_ISNS (AFTER HIGH SIDE CPU VCORE & CPU VTT SENSING RES.)
PPBUS_G3H_CPU_ISNS — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.3 MM, VOLTAGE=12.6V, MAKE_BASE=TRUE
=PPVIN_S0_CPUVTTS0 — 64C6
=PPVIN_S5_CPU_IMVP — 62C3 62D4 62D8

"FIREWIRE" RAILS

35D4 =PP3V3_FW_FET
PP3V3_FW — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE — 36D5 36D6 36D8 34B1 34D2
=PP3V3_FW_FWPHY — 34B1
=PP3V3_S0_P1V05FWFET — 35C7

35B1 =PPBUS_S5_FW_FET
PPVP_FW — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=12.6V, MAKE_BASE=TRUE
=PPVP_FW_PORT1 — 36C3
=PPVP_FW_PHY_CPS_FET — 36C6

35C5 =PP1V0_FW_FET
PP1V05_FW — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE
=PP1V0_FW_FWPHY — 34D6 35D3

SYNC_MASTER=BEN SYNC_DATE=04/21/2008
PAGE TITLE: Power Aliases
Apple Inc.
DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 8 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

HEATSINK STANDOFFS

Z0902 STDOFF-4.50D.98H-1.1-3.48-TH — LEFT OF CPU

Z0901 STDOFF-4.50D.98H-1.1-3.48-TH — ABOVE CPU

Z0903 STDOFF-4.50D.98H-1.1-3.48-TH — BELOW MCP

Z0904 STDOFF-4.50D.98H-1.1-3.48-TH — BELOW CPU

FAN STANDOFF

Z0905 STDOFF-4.50D.98H-1.1-3.48-TH

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

Z0906 OMIT 3R2P5

Z0907 OMIT 3R2P5

MLB MOUNTING (TO TOPCASE) SCREW HOLES

Z0908 OMIT 3R2P5

Z0909 OMIT 3R2P5

Z0910 OMIT 3R2P5

Z0911 OMIT 3R2P5

Z0912 OMIT 3R2P5

EMI IO POGO PINS

ZS0900 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

ZS0901 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

ZS0902 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

ZS0903 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

ZS0908 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

ZS0909 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-1801	6	POGO PIN,SHORT,EMI,MLB,K19/K24	ZS0900,ZS0901,ZS0902,ZS0903,ZS0908,ZS0909	CRITICAL	

EMI POGO PINS

ZS0904 2.0DIA-TALL-EMI-MLB-M97-M98 SM

ZS0905 2.0DIA-TALL-EMI-MLB-M97-M98 SM

ZS0906 2.0DIA-TALL-EMI-MLB-M97-M98 SM

ZS0907 2.0DIA-TALL-EMI-MLB-M97-M98 SM

PCI-E ALIASES

UNUSED GPU LANES

16D6 16C6	=PEG_D2R_N<15:0>	NC_PEG_D2R_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
16D6 16C6	=PEG_D2R_P<15:0>	NC_PEG_D2R_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
16D3 16C3	=PEG_R2D_C_N<15:0>	NC_PEG_R2D_C_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
16D3 16C3	=PEG_R2D_C_P<15:0>	NC_PEG_R2D_C_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
16C6	PEG_PRSNT_L	TP_PEG_PRSNT_L	MAKE_BASE=TRUE
16C3	PEG_CLK100M_P	TP_PEG_CLK100M_P	MAKE_BASE=TRUE
16C3	PEG_CLK100M_N	TP_PEG_CLK100M_N	MAKE_BASE=TRUE

UNUSED EXPRESS CARD LANE

16B6	PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE
16B6	PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE
16B3	PCIE_EXCARD_R2D_C_P	TP_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE
16B3	PCIE_EXCARD_R2D_C_N	TP_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE
16C6	PCIE_EXCARD_PRSNT_L	TP_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE
16C6	EXCARD_CLKREQ_L	TP_EXCARD_CLKREQ_L	MAKE_BASE=TRUE
16C3	PCIE_CLK100M_EXCARD_P	TP_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE
16C3	PCIE_CLK100M_EXCARD_N	TP_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE

FIREWIRE PRESENT SIGNALS

35D3 16C6 PCIE_FW_PRSNT_L — R0950 0 5% 1/16W MF-LF 402 — NOSTUFF

USB ALIASES

UNUSED USB PORTS

19C3	USB_EXTC_P	TP_USB_EXTC_P	MAKE_BASE=TRUE
19C3	USB_EXTC_N	TP_USB_EXTC_N	MAKE_BASE=TRUE
19D3	USB_EXTD_P	TP_USB_EXTD_P	MAKE_BASE=TRUE
19D3	USB_EXTD_N	TP_USB_EXTD_N	MAKE_BASE=TRUE
19C3	USB_EXCARD_P	TP_USB_EXCARD_P	MAKE_BASE=TRUE
19C3	USB_EXCARD_N	TP_USB_EXCARD_N	MAKE_BASE=TRUE
19D3	USB_MINI_P	TP_USB_MINI_P	MAKE_BASE=TRUE
19D3	USB_MINI_N	TP_USB_MINI_N	MAKE_BASE=TRUE

DAC ALIASES

UNUSED CRT & TV-OUT INTERFACE

17C6	MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	NO_TEST=TRUE, MAKE_BASE=TRUE
17C6	MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	NO_TEST=TRUE, MAKE_BASE=TRUE
17C6	MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	NO_TEST=TRUE, MAKE_BASE=TRUE
17C6	MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_HSYNC	NC_CRT_IG_HSYNC	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_VSYNC	NC_CRT_IG_VSYNC	NO_TEST=TRUE, MAKE_BASE=TRUE

LVDS ALIASES

UNUSED LVDS SIGNALS

17B3	LVDS_IG_A_DATA_P<3>	NC_LVDS_IG_A_DATA_P3	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_A_DATA_N<3>	NC_LVDS_IG_A_DATA_N3	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_B_CLK_P	NC_LVDS_IG_B_CLK_P	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_B_CLK_N	NC_LVDS_IG_B_CLK_N	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_B_DATA_P<3:0>	NC_LVDS_IG_B_DATA_P<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_B_DATA_N<3:0>	NC_LVDS_IG_B_DATA_N<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE

MISC MCP79 ALIASES

13B6	CPU_PECI_MCP	TP_CPU_PECI_MCP	MAKE_BASE=TRUE
16B6	GMUX_JTAG_TCK_L	TP_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE
16B6	GMUX_JTAG_TDO	TP_GMUX_JTAG_TDO	MAKE_BASE=TRUE
18D4	GMUX_JTAG_TDI	TP_GMUX_JTAG_TDI	MAKE_BASE=TRUE
18D4	GMUX_JTAG_TMS	TP_GMUX_JTAG_TMS	MAKE_BASE=TRUE

LAN ALIASES

17D6 =MCP_MII_RXER — MCP_MII_PD MAKE_BASE=TRUE

17D6 =MCP_MII_COL

17D6 =MCP_MII_CRS

R0930 47K 5% 1/16W MF-LF 402

DP HOTPLUG PULL-DOWN

17B6 =DVI_HPD_GMUX_INT — HPLUG_DET2 MAKE_BASE=TRUE

R0940 20K 5% 1/10W MF-LF 402

SO-DIMM ALIASES

UNUSED ADDRESS PINS

26D5	MEM_A_A<15>	TP_MEM_A_A15	MAKE_BASE=TRUE
27D5	MEM_B_A<15>	TP_MEM_B_A15	MAKE_BASE=TRUE

ETHERNET ALIASES

32C5	=P3V3ENET_EN	PM_SLP_RMGT_L 29C3	MAKE_BASE=TRUE
32B5	=P1V05ENET_EN		
31C2	=PP3V3_ENET_PHY_VDDREG	TP_PP3V3_ENET_PHY_VDDREG	MAKE_BASE=TRUE
31C2	=RTL8211_REGOUT	NC_RTL8211_REGOUT	MAKE_BASE=TRUE
31C6	=RTL8211_ENSWREG		MAKE_BASE=TRUE
31B6	TP_RTL8211_CLK125		

R0931 22 5% 1/16W MF-LF 402

FW ALIASES

18B7	FW_PME_L	FW_PLUG_DET_L 35B1 35D7	MAKE_BASE=TRUE
35C8 34B2	=FW_PME_L	FW643_WAKE_L	MAKE_BASE=TRUE

CPU FSB FREQUENCY STRAPS

73C3 9B4 IN CPU_BSEL<0:2> MAKE_BASE=TRUE — =MCP_BSEL<0:2> OUT 13A7

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(RSVD)
1 0 0	166
1 0 1	333
1 1 0	(400)
1 1 1	(RSVD)

SYNC_MASTER=M97_MLB

PAGE TITLE: SIGNAL ALIAS

Apple Inc.

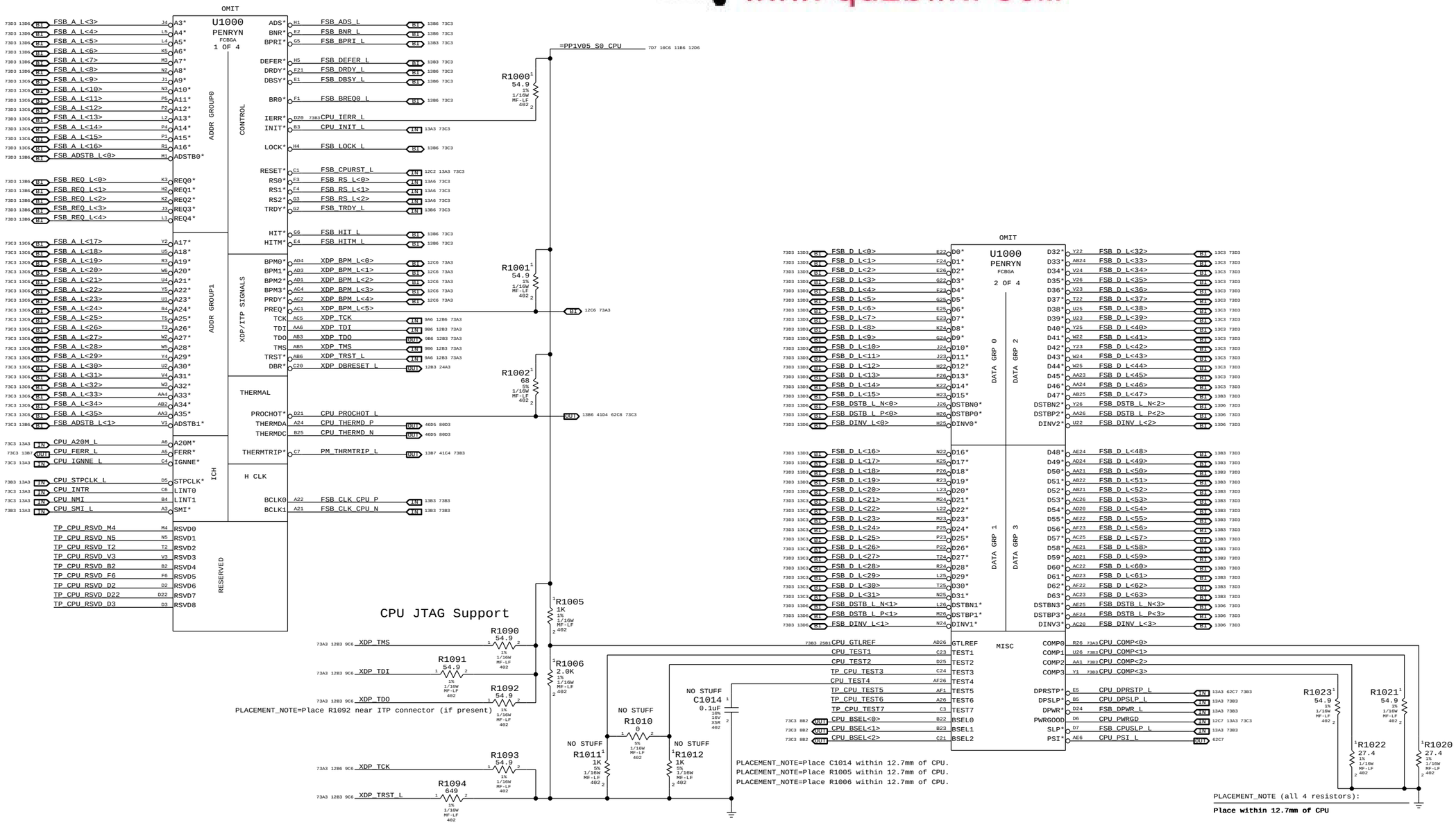
DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 9 OF 109

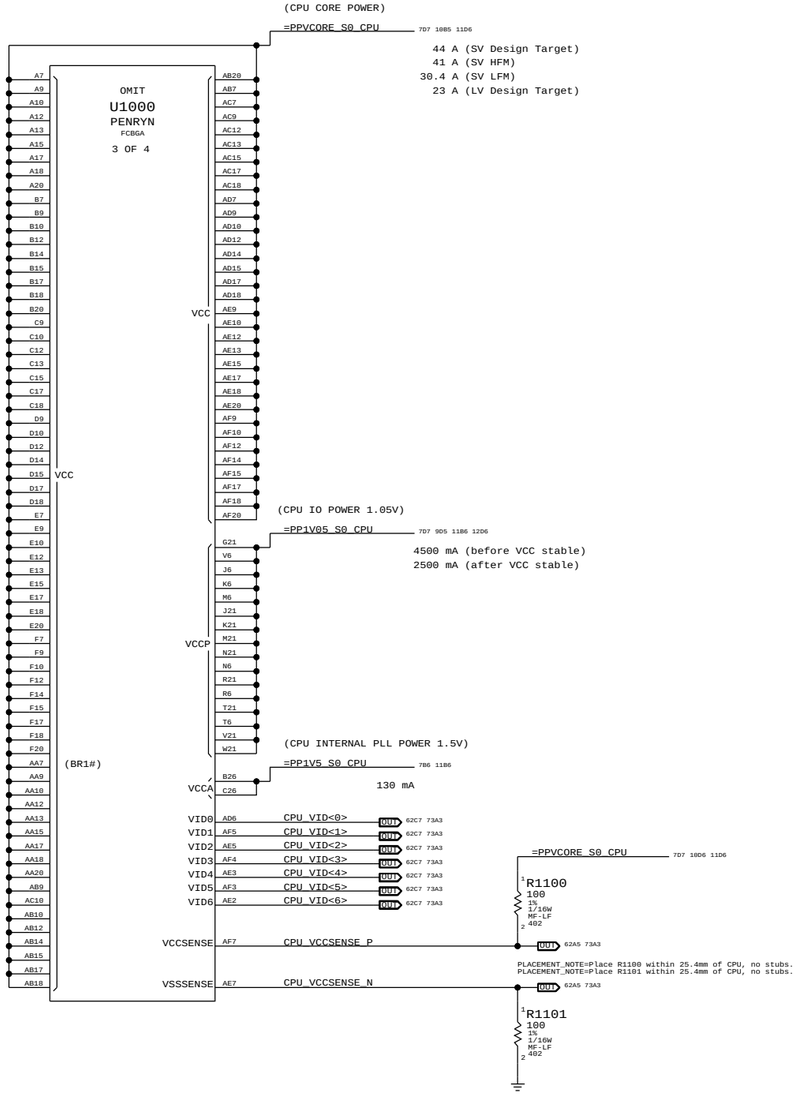
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

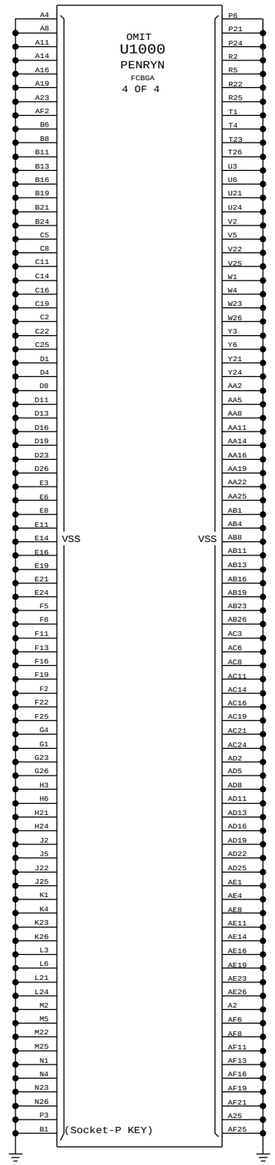


SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC_MASTER=T18_MLB	SYNC_DATE=12/12/2007
PAGE TITLE	CPU FSB
Apple Inc.	DRAWING NUMBER 051-7898 · SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 10 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED





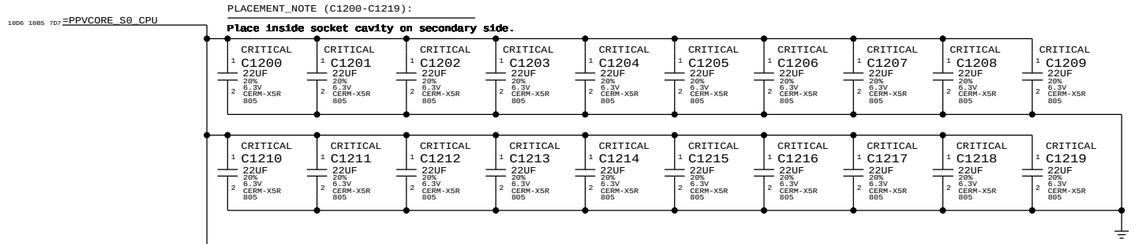
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

SYNC MASTER=T18_MLB	SYNC DATE=12/12/2007
PAGE TITLE: CPU Power & Ground	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH
	PAGE: 11 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

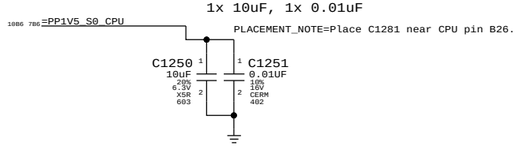
CPU VCore HF and Bulk Decoupling

4X 330UF. 20X 22UF 0805



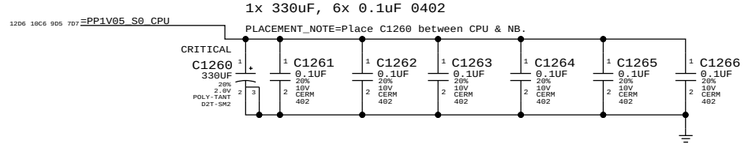
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC FROM T18
REMOVE NO STUFF CAPS C1220 TO C1231
REMOVE C1244 & C1245
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

SYNC_MASTER=RAYMOND SYNC_DATE=03/31/2008

PAGE TITLE: CPU Decoupling

Apple Inc.

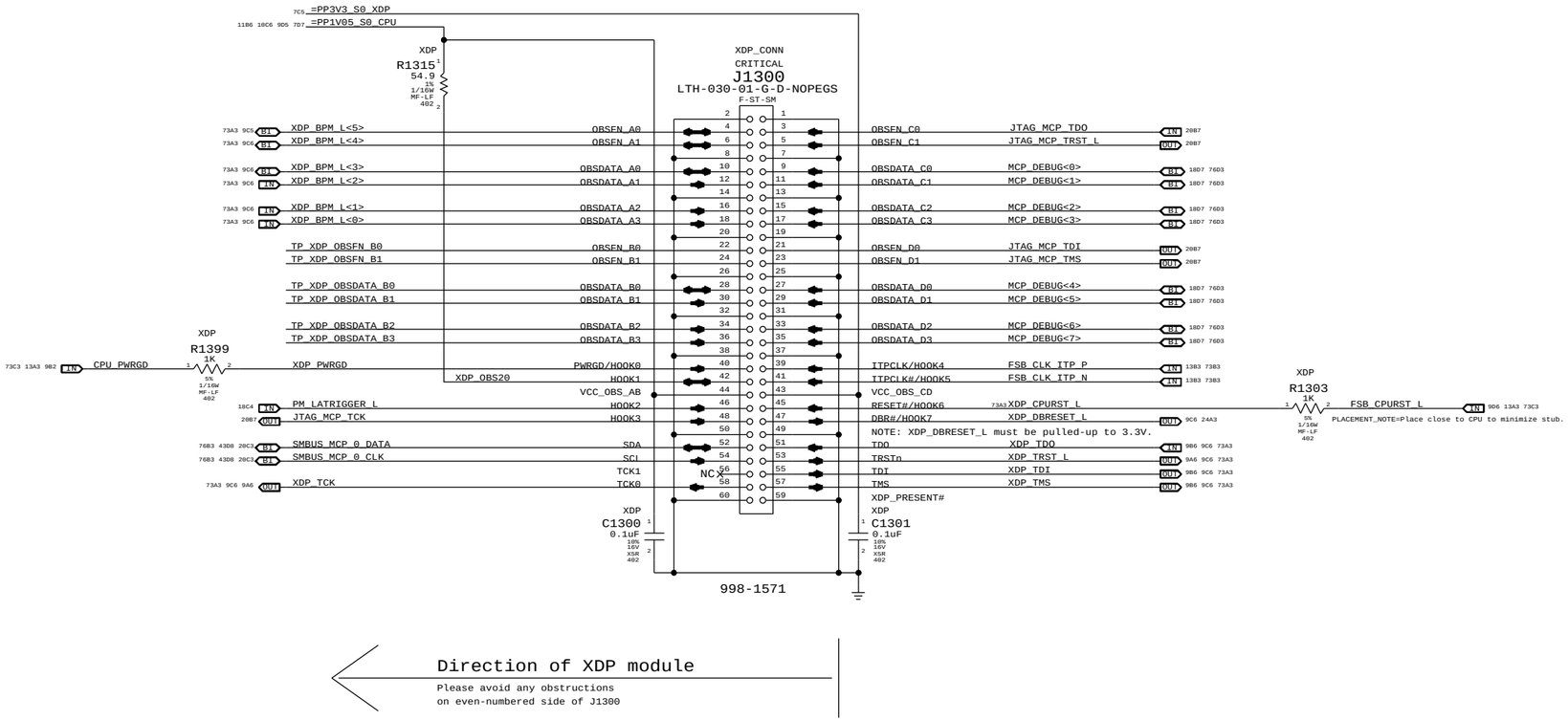
DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 12 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

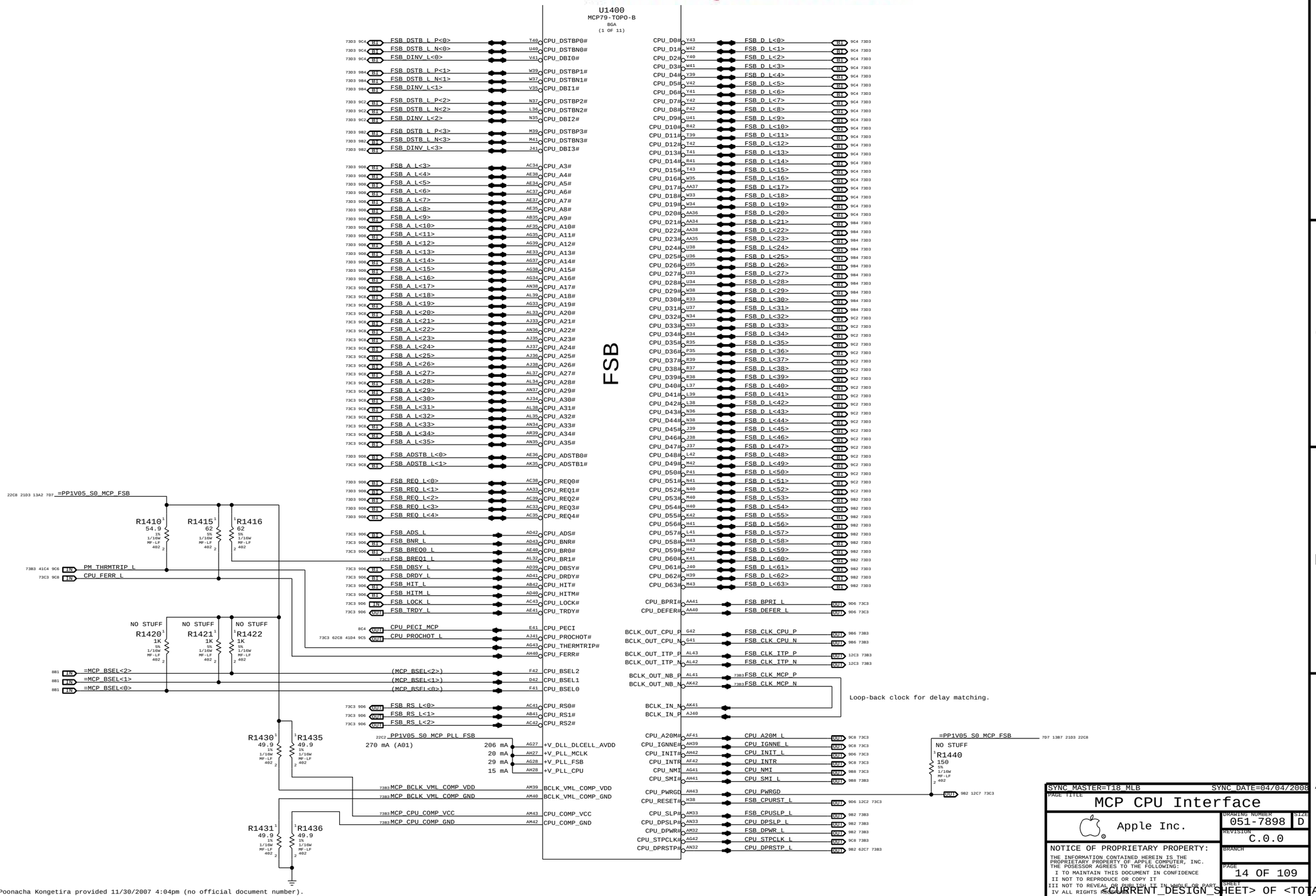
Please avoid any obstructions
on even-numbered side of J1300

SYNC_MASTER=K19_MLB SYNC_DATE=11/07/2008

PAGE TITLE
eXtended Debug Port(MiniXDP)

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 13 OF 109
SHEET



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE: MCP CPU Interface

Apple Inc.

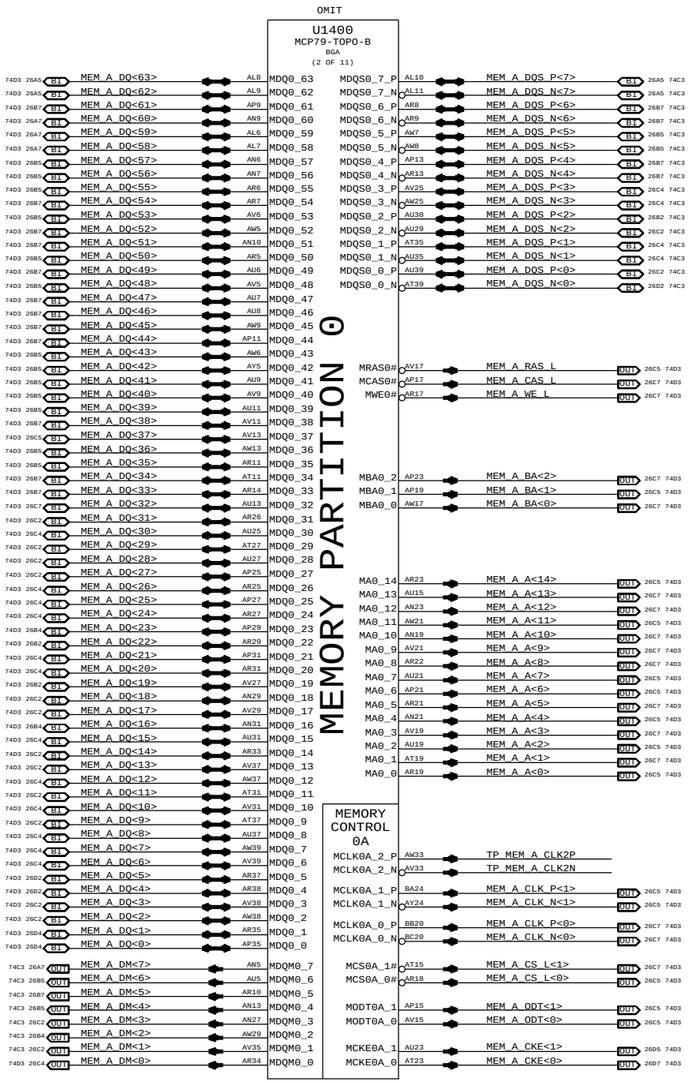
DRAWING NUMBER: 051-7898 SIZE: D

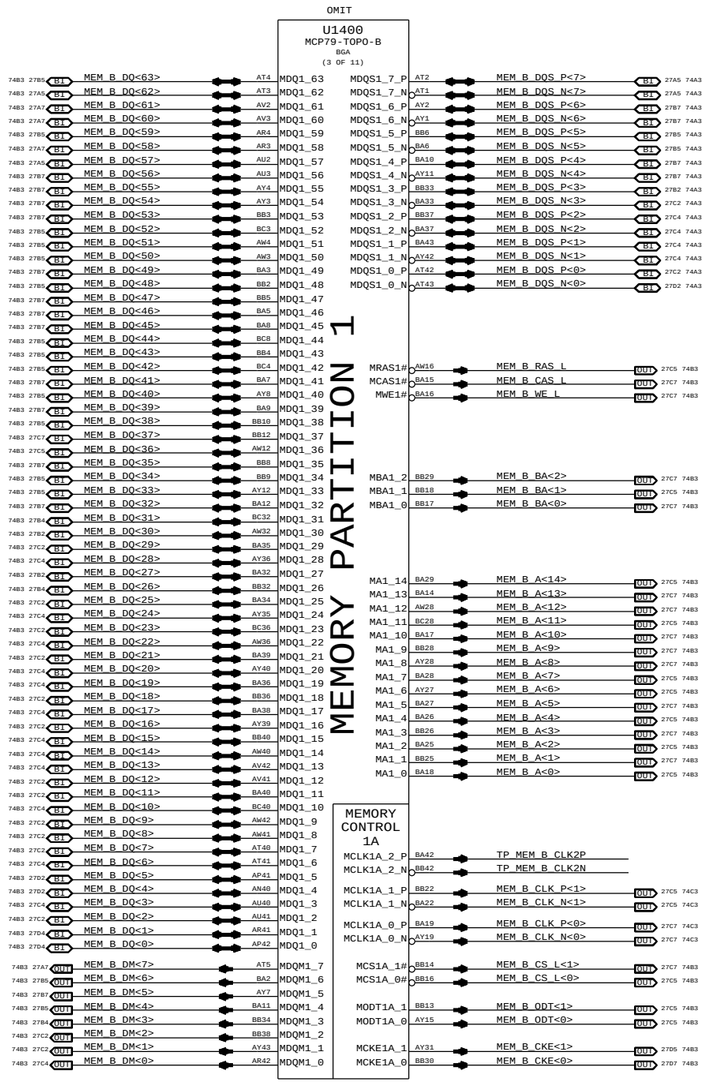
REVISION: C.0.0

BRANCH:

PAGE: 14 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



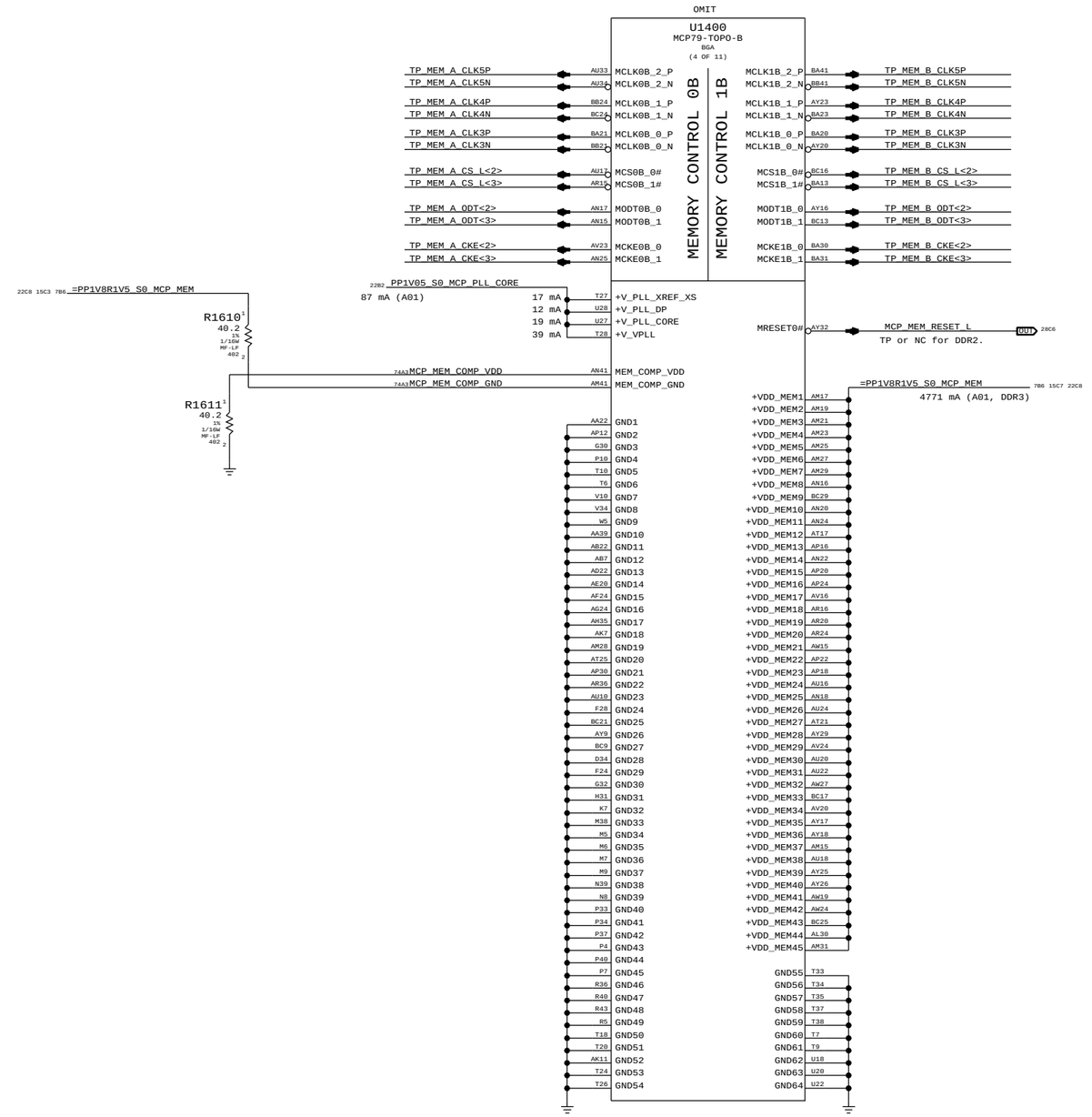


SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE
MCP Memory Interface

Apple Inc.

DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
BRANCH
PAGE 15 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE: MCP Memory Misc

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

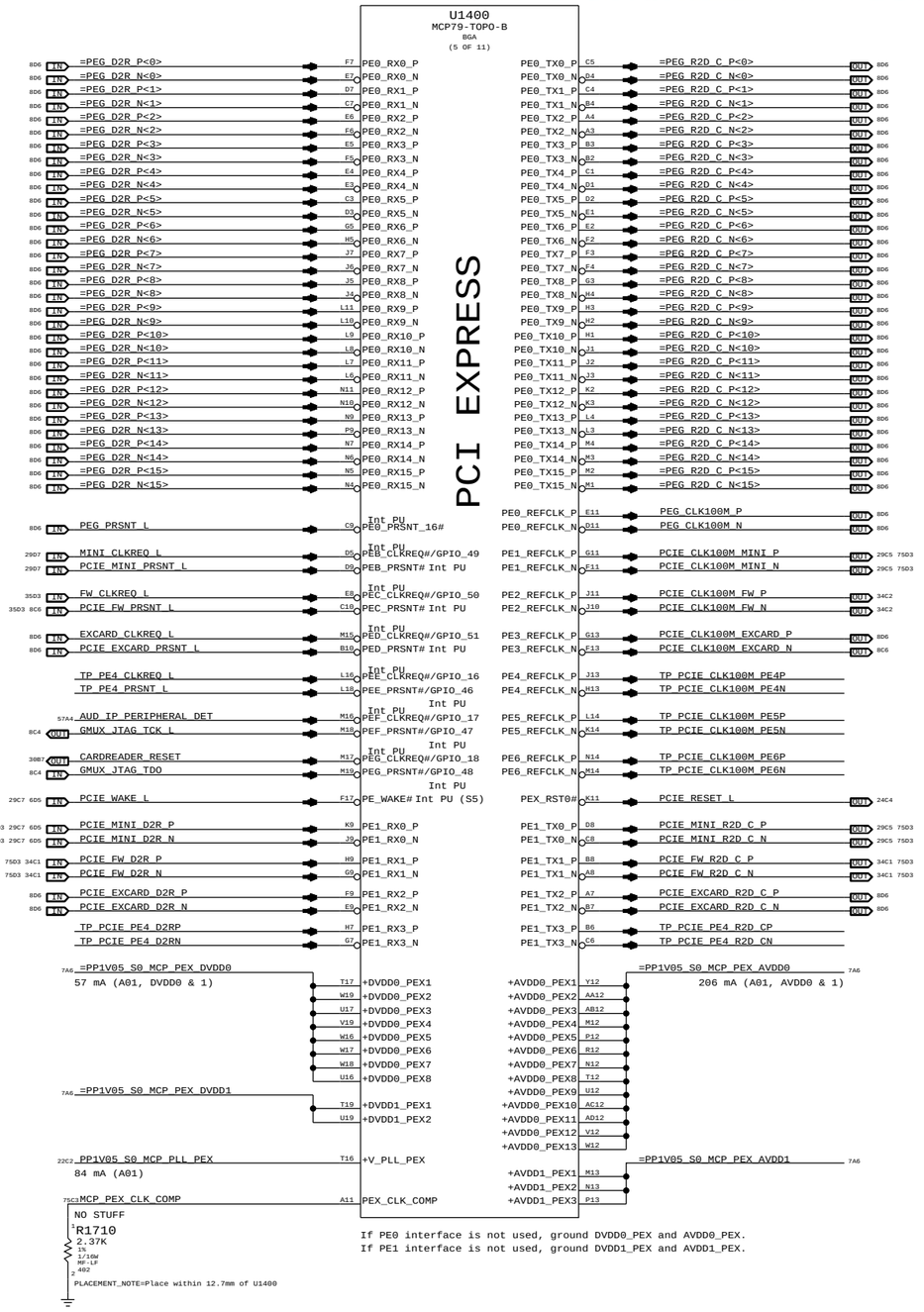
REVISION: C.0.0

BRANCH:

PAGE: 16 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE: MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 17 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE: MCP Ethernet & Graphics

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 18 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

OMIT

U1400
MCP79-TOPO-B
BGA
(7 OF 11)

PCI

PCI_REQ0_L	T2	PCI_REQ0#	
PCI_REQ1_L	V5	PCI_REQ1#/FANRPM2	
FW_PWR_EN	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	
AUD_IPHS_SWITCH_EN	U5	PCI_REQ3#/GPIO_38/RS232_CTS#	
MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	
MCP_DEBUG<0>	AC3	PCI_AD0	
MCP_DEBUG<1>	AE10	PCI_AD1	
MCP_DEBUG<2>	AC4	PCI_AD2	
MCP_DEBUG<3>	AE11	PCI_AD3	
MCP_DEBUG<4>	AB3	PCI_AD4	
MCP_DEBUG<5>	AC6	PCI_AD5	
MCP_DEBUG<6>	AB2	PCI_AD6	
MCP_DEBUG<7>	AC7	PCI_AD7	
TP_PCI_AD<8>	AC8	PCI_AD8	
TP_PCI_AD<9>	AA2	PCI_AD9	
TP_PCI_AD<10>	AC9	PCI_AD10	
TP_PCI_AD<11>	AC10	PCI_AD11	
TP_PCI_AD<12>	AC11	PCI_AD12	
TP_PCI_AD<13>	AA1	PCI_AD13	
TP_PCI_AD<14>	AA5	PCI_AD14	
TP_PCI_AD<15>	Y5	PCI_AD15	
TP_PCI_AD<16>	W3	PCI_AD16	
TP_PCI_AD<17>	W6	PCI_AD17	
TP_PCI_AD<18>	W4	PCI_AD18	
TP_PCI_AD<19>	W7	PCI_AD19	
TP_PCI_AD<20>	V3	PCI_AD20	
TP_PCI_AD<21>	W8	PCI_AD21	
TP_PCI_AD<22>	V2	PCI_AD22	
TP_PCI_AD<23>	W9	PCI_AD23	
TP_PCI_AD<24>	U3	PCI_AD24	
TP_PCI_AD<25>	W11	PCI_AD25	
TP_PCI_AD<26>	U2	PCI_AD26	
TP_PCI_AD<27>	U5	PCI_AD27	
TP_PCI_AD<28>	U1	PCI_AD28	
TP_PCI_AD<29>	U6	PCI_AD29	
TP_PCI_AD<30>	T5	PCI_AD30	
TP_PCI_AD<31>	U7	PCI_AD31	
TP_PCI_INTW_L	P2	PCI_INTW#	
TP_PCI_INTX_L	N3	PCI_INTX#	
TP_PCI_INTY_L	N2	PCI_INTY#	
TP_PCI_INTZ_L	N1	PCI_INTZ#	
TP_PCI_TRDY_L	Y3	PCI_TRDY#	
PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42	
FW_PME_L	AE3	LPC_DRQ1#/GPIO_19 Int PU	
TP_LPC_DRQ0_L	AE1	LPC_DRQ0# Int PU	
LPC_SERIRQ	AE6	LPC_SERIRQ Int PU	

PCI_GNT0#	R3	TP_PCI_GNT0_L	
PCI_GNT1#/FANCTL2	U10	TP_PCI_GNT1_L	
PCI_GNT2#/GPIO_41/RS232_DTR#	R4	GMUX_JTAG_TMS	OUT 8C4
PCI_GNT3#/GPIO_39/RS232_RTS#	U11	GMUX_JTAG_TDI	OUT 8C4
PCI_GNT4#/GPIO_53/RS232_SOUT#	P3	MCP_RS232_SOUT_L	OUT 18D2
PCI_CBE0#	AA3	TP_PCI_C_BE_L<0>	
PCI_CBE1#	AA6	TP_PCI_C_BE_L<1>	
PCI_CBE2#	AA11	TP_PCI_C_BE_L<2>	
PCI_CBE3#	W10	TP_PCI_C_BE_L<3>	
PCI_DEVSEL#	AA9	TP_PCI_DEVSEL_L	
PCI_FRAME#	Y4	TP_PCI_FRAME_L	
PCI_IRDY#	AA10	TP_PCI_IRDY_L	
PCI_PAR	Y1	TP_PCI_PAR	
PCI_PERR#/GPIO_43/RS232_DCD#	AB9	TP_PCI_PERR_L	
PCI_SERR#	AA7	TP_PCI_SERR_L	
PCI_STOP#	Y2	TP_PCI_STOP_L	
PCI_PME#/GPIO_30 Int PU (S5)	T1	PM_LATRIGGER_L	OUT 12C6
PCI_RESET0#	R10	MEM_VTT_EN_R	OUT 24C4
PCI_RESET1#	R11	TP_PCI_RESET1_L	
PCI_CLK0	R6	TP_PCI_CLK0	
PCI_CLK1	R7	TP_PCI_CLK1	
PCI_CLK2	R8	76C3 PCI_CLK33M_MCP_R	
PCI_CLKIN	R9	76C3 PCI_CLK33M_MCP	

R1910
22
5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

LPC

LPC_FRAME#	AD4	LPC_FRAME_R_L	R1960	22	LPC_FRAME_L OUT 40C8 42D5 76C3
LPC_PWRDWN#/GPIO_54/EXT_NMI#	AE12	LPC_PWRDWN_L			OUT 40C5 42D3
LPC_RESET0#	AE5	LPC_RESET_L			OUT 24D4 76C3
LPC_AD0	AD3	LPC_AD_R<0>	R1950	22	LPC_AD<0> BI 40C8 42D5 76C3
LPC_AD1	AD2	LPC_AD_R<1>	R1951	22	LPC_AD<1> BI 40C8 42D5 76C3
LPC_AD2	AD1	LPC_AD_R<2>	R1952	22	LPC_AD<2> BI 40C8 42D3 76C3
LPC_AD3	AD5	LPC_AD_R<3>	R1953	22	LPC_AD<3> BI 40C8 42D3 76C3
LPC_CLK0	AE9	LPC_CLK33M_SMC_R			OUT 24B4 76C3

5% 1/16W MF-LF 402

R1961
10K
5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

GND65	U24	GND98	Y26
GND66	U26	GND99	Y27
GND67	U39	GND100	AB18
GND68	U4	GND101	H34
GND69	U8	GND102	AB20
GND70	V16	GND103	AB21
GND71	V17	GND104	AB23
GND72	V18	GND105	AB24
GND73	V20	GND106	AB25
GND74	V22	GND107	AB26
GND75	V24	GND108	AB27
GND76	V26	GND109	AB28
GND77	V27	GND110	AB34
GND78	V28	GND111	AB37
GND79	V33	GND112	AB4
GND80	V37	GND113	AB40
GND81	V4	GND114	AC22
GND82	V40	GND115	AC36
GND83	V7	GND116	AC40
GND84	W20	GND117	AB33
GND85	W22	GND118	AC5
GND86	W24	GND119	AD16
GND87	W36	GND120	AD17
GND88	W40	GND121	AD18
GND89	W43	GND122	AD19
GND90	Y16	GND123	AD20
GND91	Y17	GND124	AD24
GND92	Y18	GND125	AD25
GND93	Y19	GND126	AD26
GND94	Y20	GND127	AD27
GND95	Y22	GND128	AD28
GND96	Y24	GND129	AD33
GND97	Y25	GND130	AD34

20A4 17C1 7C5 =PP3V3_S0_MCP_GPIO

18D4 MCP_RS232_SOUT_L	R1989	8.2K	5% 1/16W MF-LF 402
76D3 18D7 PCI_REQ0_L	R1990	8.2K	5% 1/16W MF-LF 402
76D3 18D7 PCI_REQ1_L	R1991	8.2K	5% 1/16W MF-LF 402
35D6 35C7 35C4 35A4 18D7 FW_PWR_EN	R1992	8.2K	5% 1/16W MF-LF 402
18D7 MCP_RS232_SIN_L	R1994	8.2K	5% 1/16W MF-LF 402

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE: MCP PCI & LPC

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 19 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

OMIT

U1400
MCP79-TOPO-B
BGA
(8 OF 11)

SATA

75A3 37A2 OUT	SATA_HDD_R2D_C_P	AJ7	SATA_A0_TX_P
75A3 37A2 OUT	SATA_HDD_R2D_C_N	AJ6	SATA_A0_TX_N
75A3 37B2 IN	SATA_HDD_D2R_N	AJ5	SATA_A0_RX_N
75A3 37B2 IN	SATA_HDD_D2R_P	AJ4	SATA_A0_RX_P
75A3 37C3 OUT	SATA_ODD_R2D_C_P	AJ11	SATA_A1_TX_P
75A3 37C3 OUT	SATA_ODD_R2D_C_N	AJ10	SATA_A1_TX_N
75A3 37C3 IN	SATA_ODD_D2R_N	AJ9	SATA_A1_RX_N
75A3 37C3 IN	SATA_ODD_D2R_P	AK9	SATA_A1_RX_P
	TP_SATA_C_R2D_CP	AK2	SATA_B0_TX_P
	TP_SATA_C_R2D_CN	AJ3	SATA_B0_TX_N
	TP_SATA_C_D2RN	AJ2	SATA_B0_RX_N
	TP_SATA_C_D2RP	AJ1	SATA_B0_RX_P
	TP_SATA_D_R2D_CP	AM4	SATA_B1_TX_P
	TP_SATA_D_R2D_CN	AL3	SATA_B1_TX_N
	TP_SATA_D_D2RN	AL4	SATA_B1_RX_N
	TP_SATA_D_D2RP	AK3	SATA_B1_RX_P
	TP_SATA_E_R2D_CP	AN1	SATA_C0_TX_P
	TP_SATA_E_R2D_CN	AM1	SATA_C0_TX_N
	TP_SATA_E_D2RN	AM2	SATA_C0_RX_N
	TP_SATA_E_D2RP	AM3	SATA_C0_RX_P
	TP_SATA_F_R2D_CP	AP3	SATA_C1_TX_P
	TP_SATA_F_R2D_CN	AP2	SATA_C1_TX_N
	TP_SATA_F_D2RN	AN3	SATA_C1_RX_N
	TP_SATA_F_D2RP	AN2	SATA_C1_RX_P
	TP_MCP_SATALED_L	E12	SATA_LED#
22B2	PP1V05_S0_MCP_PLL_SATA 84 mA (A01)	AE16	+V_PLL_SATA
7A6	=PP1V05_S0_MCP_SATA_DVDD0 43 mA (A01, DVDD0 & 1)	AF19	+DVDD0_SATA1
		AG16	+DVDD0_SATA2
		AG17	+DVDD0_SATA3
		AG19	+DVDD0_SATA4
7A6	=PP1V05_S0_MCP_SATA_DVDD1	AH17	+DVDD1_SATA1
		AH19	+DVDD1_SATA2
7A6	=PP1V05_S0_MCP_SATA_AVDD0 127 mA (A01, AVDD0 & 1)	AJ12	+AVDD0_SATA1
		AN11	+AVDD0_SATA2
		AK12	+AVDD0_SATA3
		AK13	+AVDD0_SATA4
		AL12	+AVDD0_SATA5
		AM11	+AVDD0_SATA6
		AM12	+AVDD0_SATA7
		AN12	+AVDD0_SATA8
		AL13	+AVDD0_SATA9
7A6	=PP1V05_S0_MCP_SATA_AVDD1	AN14	+AVDD1_SATA1
		AL14	+AVDD1_SATA2
		AM13	+AVDD1_SATA3
		AM14	+AVDD1_SATA4
75A3	MCP_SATA_TERMP	AE3	SATA_TERMP

R2010
2.49K
1%
1/16W
MF-LF
402

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

USB

	External A		
USB0_P	C29	USB_EXTA_P	38A8 76C3
USB0_N	D29	USB_EXTA_N	38A8 76C3
	AirPort (PCIe Mini-Card)		
USB1_P	C28	USB_MINI_P	8C6
USB1_N	D28	USB_MINI_N	8C6
	External D		
USB2_P	A28	USB_EXTD_P	8C6
USB2_N	B28	USB_EXTD_N	8C6
	Camera		
USB3_P	F29	USB_CAMERA_P	29B5 76C3
USB3_N	G29	USB_CAMERA_N	29B5 76C3
	IR		
USB4_P	K27	USB_IR_P	39D7 76B3
USB4_N	L27	USB_IR_N	39D7 76B3
	Geyser Trackpad/Keyboard		
USB5_P	J26	USB_TPAD_P	48B8 76B3
USB5_N	J27	USB_TPAD_N	48B8 76B3
	Bluetooth		
USB6_P	F27	USB_BT_P	29B5 76C3
USB6_N	G27	USB_BT_N	29B5 76C3
	External B		
USB7_P	D27	USB_EXTB_P	38A4 76B3
USB7_N	E27	USB_EXTB_N	38B4 76B3
	ExpressCard		
USB8_P	K25	USB_EXCARD_P	8C6
USB8_N	L25	USB_EXCARD_N	8C6
	External C		
USB9_P	H25	USB_EXTC_P	8C6
USB9_N	J25	USB_EXTC_N	8C6
USB10_P	F25	TP_USB_10P	
USB10_N	G25	TP_USB_10N	
USB11_P	K23	USB_CARDREADER_P	39C7 76B3
USB11_N	L23	USB_CARDREADER_N	39C7 76B3

USB_OC0#/GPIO_25	L21	USB_EXTA_OC_L	39C7
USB_OC1#/GPIO_26	K21	USB_EXTB_OC_L	39C7
USB_OC2#/GPIO_27/MGPIO	J21	USB_EXTC_OC_L	41C4
USB_OC3#/GPIO_28/MGPIO	H21	EXCARD_OC_L	41C4

=PP3V3_S5_MCP_GPIO 7A3 17C7

R2051 8.2K 5% 1/16W MF-LF 402
R2053 8.2K 5% 1/16W MF-LF 402
R2050 8.2K 5% 1/16W MF-LF 402
R2052 8.2K 5% 1/16W MF-LF 402

+V_PLL_USB	L28	PP3V3_S0_MCP_PLL_USB 19 mA (A01)	22B4
USB_RBIAS_GND	A27	76B3 MCP_USB_RBIAS_GND	

R2060
806
1%
1/16W
MF-LF
402

GND131	AD35	GND146	AF28
GND132	AD37	GND147	AF33
GND133	AD38	GND148	AF34
GND134	AE22	GND149	AF37
GND135	AE24	GND150	AF40
GND136	AE39	GND151	AG18
GND137	AE4	GND152	AG20
GND138	AD6	GND153	AG22
GND139	AF16	GND154	AG26
GND140	AF17	GND155	AG36
GND141	AF18	GND156	AG40
GND142	AF20	GND157	AH18
GND143	AF22	GND158	AH20
GND144	AF26	GND159	AH22
GND145	AF27	GND160	AH24

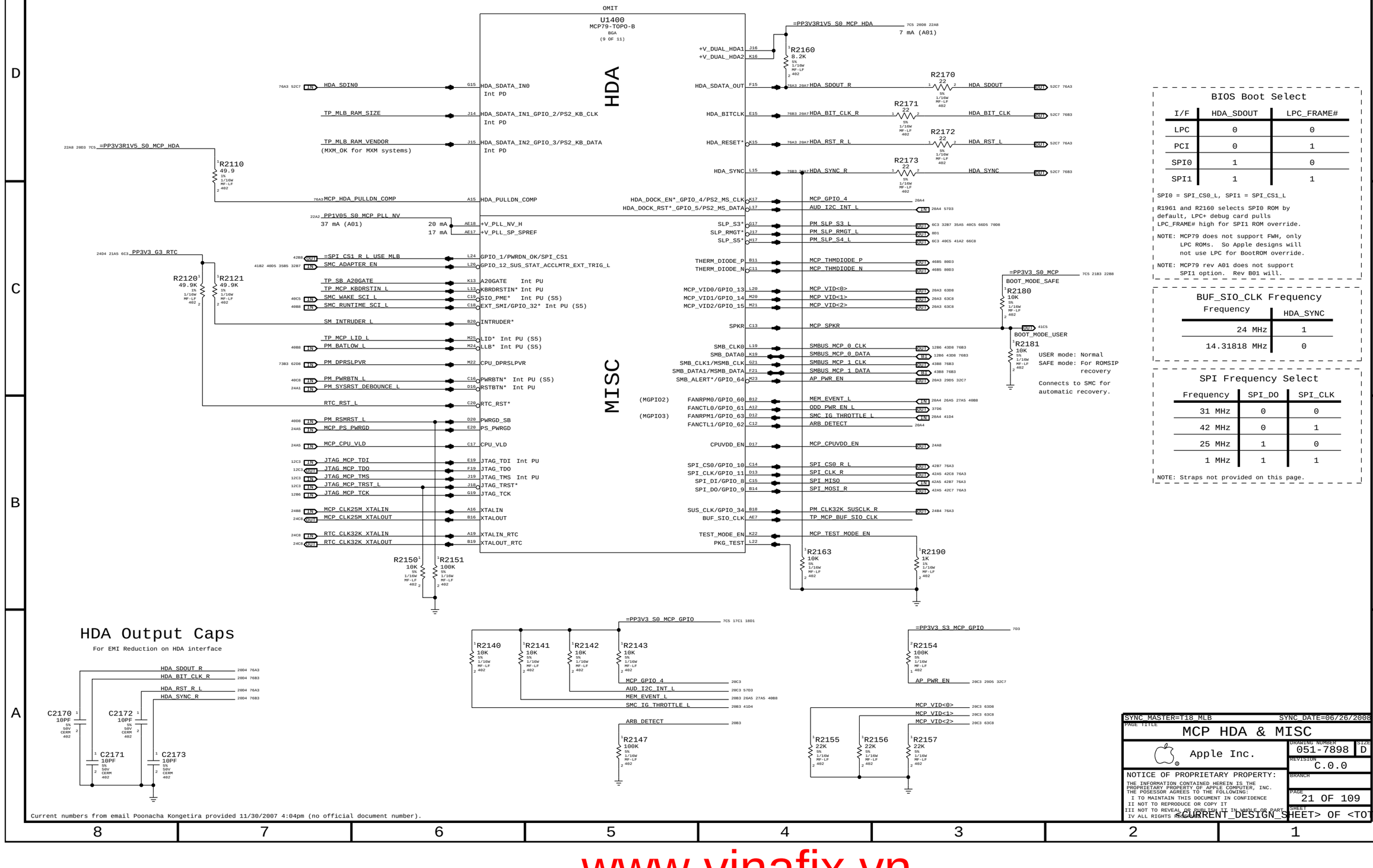
SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE
MCP SATA & USB

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 20 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



OMIT

U1400
MCP79-TOPO-B
BGA
(11 OF 11)

GND

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR36	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

=PPVCORE_S0_MCP
22D8 7C6
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

AA25	+VDD_CORE1	+VTT_CPU1	R32	
AC23	+VDD_CORE2	+VTT_CPU2	AC32	
U25	+VDD_CORE3	+VTT_CPU3	E40	
AH12	+VDD_CORE4	+VTT_CPU4	J36	
AG10	+VDD_CORE5	+VTT_CPU5	N32	
AG5	+VDD_CORE6	+VTT_CPU6	T32	
Y21	+VDD_CORE7	+VTT_CPU7	U32	
Y23	+VDD_CORE8	+VTT_CPU8	V32	
AA16	+VDD_CORE9	+VTT_CPU9	W32	
AA26	+VDD_CORE10	+VTT_CPU10	P31	
AA27	+VDD_CORE11	+VTT_CPU11	AF32	
AA28	+VDD_CORE12	+VTT_CPU12	AE32	
AC16	+VDD_CORE13	+VTT_CPU13	AH32	
AC17	+VDD_CORE14	+VTT_CPU14	AJ32	
AC18	+VDD_CORE15	+VTT_CPU15	AK31	
AC19	+VDD_CORE16	+VTT_CPU16	AK32	
AC20	+VDD_CORE17	+VTT_CPU17	AD32	
AC21	+VDD_CORE18	+VTT_CPU18	AL31	
AA17	+VDD_CORE19	+VTT_CPU19	AB32	
AC24	+VDD_CORE20	+VTT_CPU20	B41	
AC25	+VDD_CORE21	+VTT_CPU21	B42	
AC26	+VDD_CORE22	+VTT_CPU22	C40	
AC27	+VDD_CORE23	+VTT_CPU23	C41	
AC28	+VDD_CORE24	+VTT_CPU24	C42	
AD21	+VDD_CORE25	+VTT_CPU25	D39	
AD23	+VDD_CORE26	+VTT_CPU26	D40	
W27	+VDD_CORE27	+VTT_CPU27	D41	
V25	+VDD_CORE28	+VTT_CPU28	E38	
AA18	+VDD_CORE29	+VTT_CPU29	E39	
AE19	+VDD_CORE30	+VTT_CPU30	F37	
AE21	+VDD_CORE31	+VTT_CPU31	F38	
AE23	+VDD_CORE32	+VTT_CPU32	F39	
AE25	+VDD_CORE33	+VTT_CPU33	G36	
AE26	+VDD_CORE34	+VTT_CPU34	G37	
AE27	+VDD_CORE35	+VTT_CPU35	G38	
AE28	+VDD_CORE36	+VTT_CPU36	H35	
AF10	+VDD_CORE37	+VTT_CPU37	H37	
AF11	+VDD_CORE38	+VTT_CPU38	J34	
AA19	+VDD_CORE39	+VTT_CPU39	J35	
AF2	+VDD_CORE40	+VTT_CPU40	K33	
AF21	+VDD_CORE41	+VTT_CPU41	K34	
AF23	+VDD_CORE42	+VTT_CPU42	K35	
AF25	+VDD_CORE43	+VTT_CPU43	L32	
AF3	+VDD_CORE44	+VTT_CPU44	L33	
AF4	+VDD_CORE45	+VTT_CPU45	L34	
AF7	+VDD_CORE46	+VTT_CPU46	M31	
AH23	+VDD_CORE47	+VTT_CPU47	M32	
AF9	+VDD_CORE48	+VTT_CPU48	M33	
AA28	+VDD_CORE49	+VTT_CPU49	N31	
AG11	+VDD_CORE50	+VTT_CPU50	P32	
AG12	+VDD_CORE51	+VTT_CPU51	Y32	
AG21	+VDD_CORE52	+VTT_CPU52	AA32	
AG23	+VDD_CORE53			
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32	43 mA
AG3	+VDD_CORE55			
AG4	+VDD_CORE56			
AA21	+VDD_CORE57			
AG6	+VDD_CORE58			
AG7	+VDD_CORE59			
AG8	+VDD_CORE60			
AG9	+VDD_CORE61			
AH1	+VDD_CORE62			
AH10	+VDD_CORE63			
AH11	+VDD_CORE64			
W26	+VDD_CORE65			
AH2	+VDD_CORE66			
AA23	+VDD_CORE67			
W28	+VDD_CORE68			
AH25	+VDD_CORE69			
AH21	+VDD_CORE70	+3.V_DUAL1	G18	
AH3	+VDD_CORE71	+3.V_DUAL2	H19	
AH4	+VDD_CORE72	+3.V_DUAL3	J20	
AH5	+VDD_CORE73	+3.V_DUAL4	K20	
AH6	+VDD_CORE74			
AH7	+VDD_CORE75	+3.V_DUAL_USB1	G26	250 mA
AH9	+VDD_CORE76	+3.V_DUAL_USB2	H27	
AA24	+VDD_CORE77	+3.V_DUAL_USB3	J28	
W21	+VDD_CORE78	+3.V_DUAL_USB4	K28	
W23	+VDD_CORE79			
W25	+VDD_CORE80			
AF12	+VDD_CORE81			
		+VDD_AUXC1	T21	
		+VDD_AUXC2	U21	
A20	+VBAT	+VDD_AUXC3	V21	

=PP1V05_S0_MCP_FSB
7D7 13A2 13B7 22C8
1139 mA
1182 mA (A01)

=PP3V3_S0_MCP
7C5 20C2 22B8
450 mA (A01)

+3.3V_1	AD10	
+3.3V_2	AE8	
+3.3V_3	AB10	
+3.3V_4	AD9	
+3.3V_5	Y10	
+3.3V_6	AB11	
+3.3V_7	AA8	
+3.3V_8	Y9	

=PP3V3_S5_MCP
7A3 22B8
16 mA
266 mA (A01)

=PP1V05_S5_MCP_VDD_AUXC
7B3 22D8
105 mA (A01)

=PP3V3_G3_RTC
24D4 28C8 6C9
10 uA (G3)
80 uA (S0)

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=T18_MLB
SYNC_DATE=04/04/2008

PAGE TITLE
MCP Power & Ground

Apple Inc.

DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
BRANCH
PAGE 22 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP Core Power
=PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)
NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)
C2500 4.7UF 20% 4V X5R-1 402
C2501 4.7UF 20% 4V X5R-1 402
C2502 4.7UF 20% 4V X5R-1 402
C2503 4.7UF 20% 4V X5R-1 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power
=PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)
C2515 4.7UF 20% 4V X5R-1 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power
=PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)
C2520 4.7UF 20% 4V X5R-1 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power
=PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)
C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power
=PP1V05_ENET_MCP_RMGT
131 mA (A01)
C2528 4.7UF 20% 4V X5R-1 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power
=PP1V05_S0_MCP_FSB
1182 mA (A01)
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)
C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power
=PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)
C2540 4.7UF 20% 4V X5R-1 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power
=PP3V3_S0_MCP
450 mA (A01)
NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)
C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

=PP3V3_S0_MCP_PLL_UF
19 mA (A01)
L2555 30-OHM-1.7A 0402
PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2555 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power
=PP3V3_S5_MCP
266 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power
=PP3V3_ENET_MCP_RMGT
83 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2564 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power
=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2562 2.2UF 20% 6.3V CERM 402-LF

MCP79 Ethernet VRef
=PP3V3_ENET_MCP_RMGT
R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402
MCP_MII_VREF
C2591 0.1UF 20% 10V CERM 402

=PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)
L2595 30-OHM-1.7A 0402
PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)
C2595 4.7UF 20% 4V X5R-1 402
C2596 0.1UF 20% 10V CERM 402

=PP1V05_S0_MCP_AVDD_UF
333 mA (A01)
L2570 30-OHM-5A 0603
PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)
C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

L2575 30-OHM-5A 0603
PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)
C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_S0_MCP_PLL_UF
562 mA (A01)
L2580 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)
C2592 10UF 20% 6.3V X5R 603
C2580 4.7UF 20% 4V X5R-1 402
C2581 0.1UF 20% 10V CERM 402

L2582 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)
C2582 4.7UF 20% 4V X5R-1 402
C2583 0.1UF 20% 10V CERM 402

L2584 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)
C2584 4.7UF 20% 4V X5R-2 402
C2585 0.1UF 20% 10V CERM 402

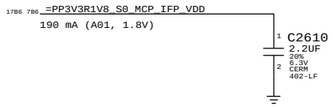
L2586 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)
C2586 4.7UF 20% 4V X5R-2 402
C2587 0.1UF 20% 10V CERM 402

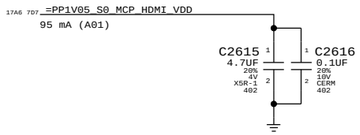
L2588 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)
C2588 4.7UF 20% 4V X5R-2 402
C2589 0.1UF 20% 10V CERM 402
C2590 0.1UF 20% 10V CERM 402

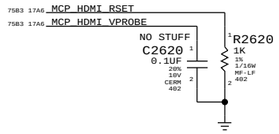
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

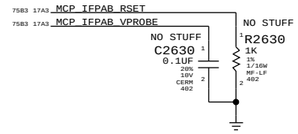
SYNC_MASTER=T18_MLB
SYNC_DATE=04/04/2008
PAGE TITLE
MCP Standard Decoupling
Apple Inc.
DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
BRANCH
PAGE 25 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

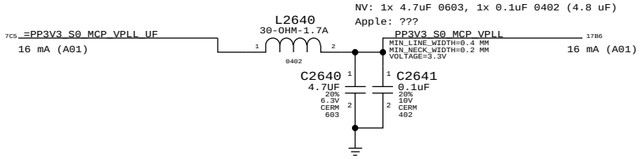




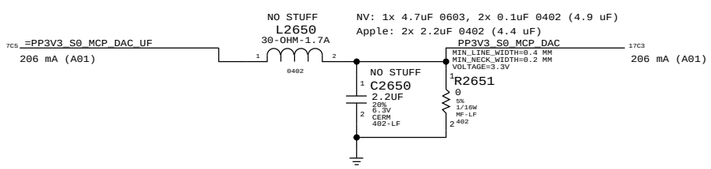




WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)



SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
REMOVE HDCP ROMS

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

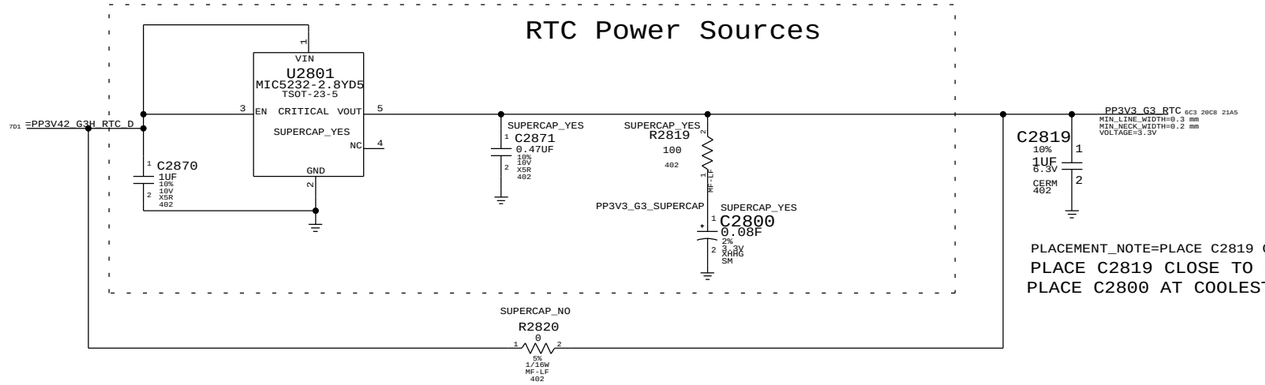
SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

PAGE TITLE: MCP Graphics Support

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 26 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

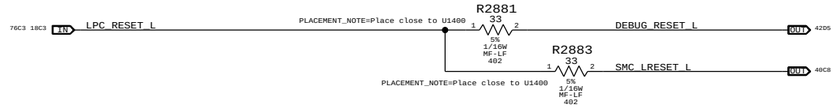
RTC Power Sources



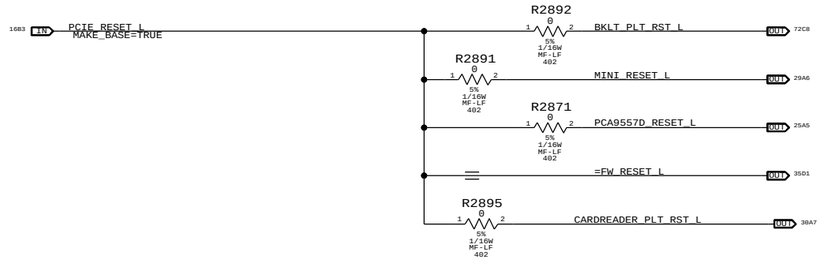
PLACEMENT_NOTE=PLACE C2819 CLOSE TO MCP79
PLACE C2819 CLOSE TO MCP79
PLACE C2800 AT COOLEST SPOT ON MLB

Platform Reset Connections

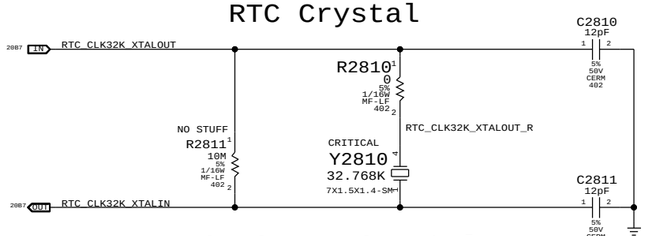
LPC Reset (Unbuffered)



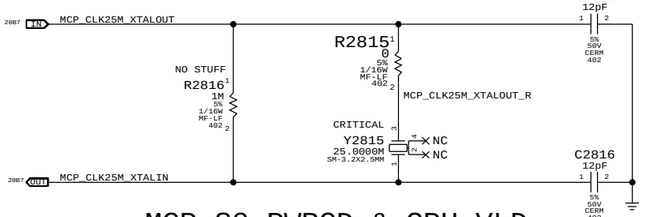
PCIE Reset (Unbuffered)



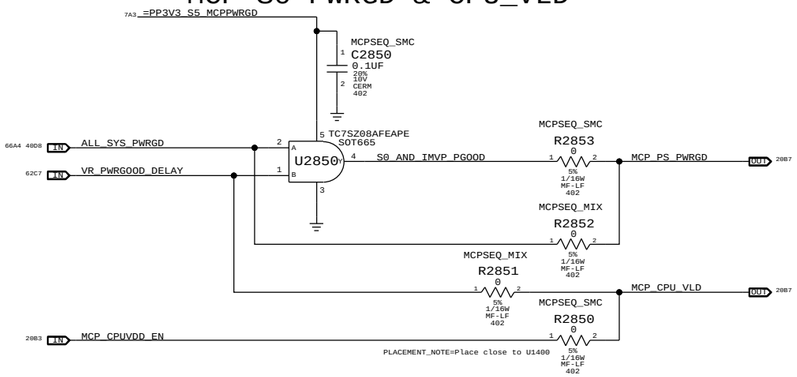
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD

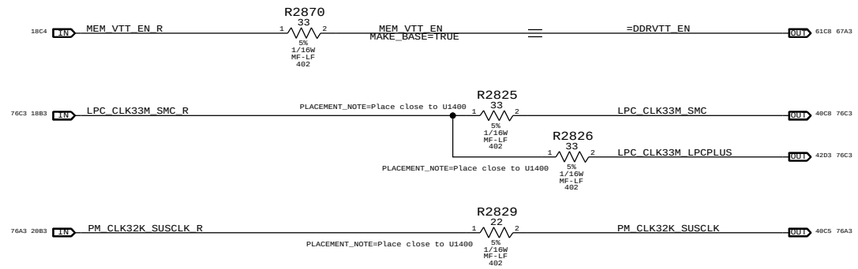


MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

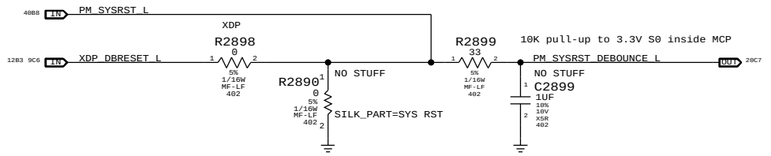
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.



Reset Button



SYNC FROM T18
CHANGE RESET BUTTOM TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

SYNC_MASTER=RAYMOND SYNC_DATE=04/05/2008

PAGE TITLE: SB Misc

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 28 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

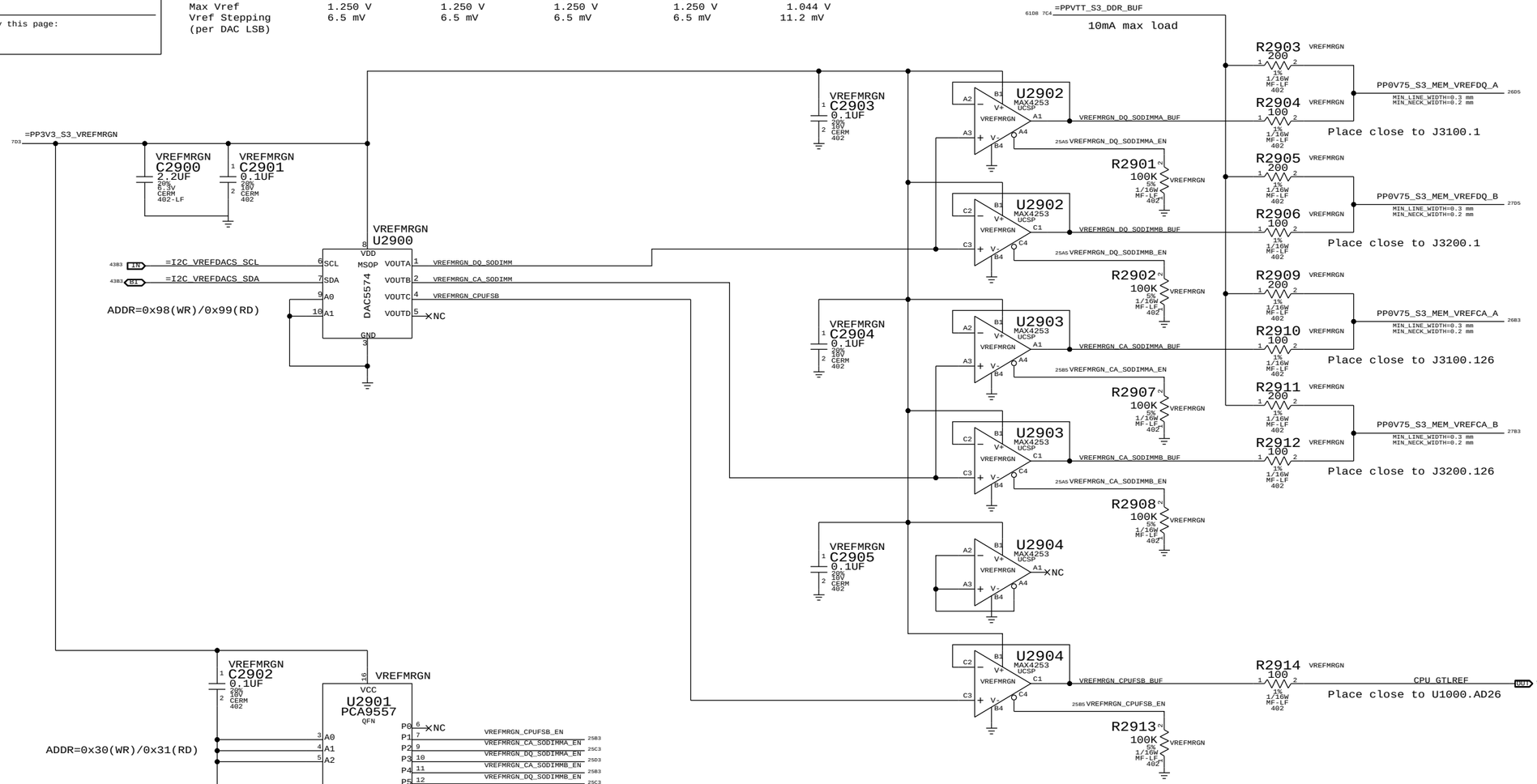
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

SYNC_MASTER=BEN SYNC_DATE=03/31/2008
PAGE TITLE
FSB/DDR3 Vref Margining
Apple Inc.
DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 29 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

7D3 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3111 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3112 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3113 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3114 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3115 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3116 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3117 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL

25D1 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)

73	CKE0	CKE1	74
75	VDD	VDD	76
77	NC	A15	78
79	BA2	A14	80
81	VDD	VDD	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD	VDD	88
89	A8	A6	90
91	A5	A4	92
93	VDD	VDD	94
95	A3	A2	96
97	A1	A0	98
99	VDD	VDD	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD	VDD	106
107	A10/AP	BA1	108
109	BA0	RAS*	110
111	VDD	VDD	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD	VDD	118
119	A13	ODT1	120
121	S1*	NC	122
123	VDD	VDD	124
125	TEST	VREFCA	126
127	VSS	VSS	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS	VSS	134
135	DQS4*	DM4	136
137	DQS4	VSS	138
139	VSS	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS	144
145	VSS	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS	150
151	VSS	DQS5*	152
153	DM5	DQS5	154
155	VSS	VSS	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS	VSS	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS	VSS	168
169	DQS6*	DM6	170
171	DQS6	VSS	172
173	VSS	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS	178
179	VSS	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS	184
185	VSS	DQS7*	186
187	DM7	DQS7	188
189	VSS	VSS	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS	VSS	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT	VTT	204

NCX
KEY

MEM_A_CKE<0> MEM_A_CKE<1>
MEM_A_BA<2>
MEM_A_A<12> MEM_A_A<11>
MEM_A_A<9> MEM_A_A<7>
MEM_A_A<8> MEM_A_A<6>
MEM_A_A<5> MEM_A_A<4>
MEM_A_A<3> MEM_A_A<2>
MEM_A_A<1> MEM_A_A<0>
MEM_A_CLK_P<0> MEM_A_CLK_P<1>
MEM_A_CLK_N<0> MEM_A_CLK_N<1>
MEM_A_A<10> MEM_A_BA<1>
MEM_A_BA<0> MEM_A_RAS_L
MEM_A_WE_L MEM_A_CS_L<0>
MEM_A_CAS_L MEM_A_ODT<0>
MEM_A_A<13> MEM_A_ODT<1>
MEM_A_CS_L<1>
MEM_A_DQ<32> MEM_A_DQ<37>
MEM_A_DQ<33> MEM_A_DQ<36>
MEM_A_DQS_N<4> MEM_A_DM<4>
MEM_A_DQS_P<4>
MEM_A_DQ<34> MEM_A_DQ<35>
MEM_A_DQ<38> MEM_A_DQ<39>
MEM_A_DQ<44> MEM_A_DQ<40>
MEM_A_DQ<45> MEM_A_DQ<41>
MEM_A_DM<5> MEM_A_DQS_N<5>
MEM_A_DQS_P<5>
MEM_A_DQ<47> MEM_A_DQ<43>
MEM_A_DQ<46> MEM_A_DQ<42>
MEM_A_DQ<49> MEM_A_DQ<53>
MEM_A_DQ<52> MEM_A_DQ<48>
MEM_A_DQS_N<6> MEM_A_DM<6>
MEM_A_DQS_P<6>
MEM_A_DQ<54> MEM_A_DQ<55>
MEM_A_DQ<51> MEM_A_DQ<50>
MEM_A_DQ<61> MEM_A_DQ<57>
MEM_A_DQ<60> MEM_A_DQ<56>
MEM_A_DM<7> MEM_A_DQS_N<7>
MEM_A_DQS_P<7>
MEM_A_DQ<58> MEM_A_DQ<62>
MEM_A_DQ<59> MEM_A_DQ<63>
MEM_A_SA<0> MEM_EVENT_L
MEM_A_SA<1> =I2C_SODIMMA_SDA
=I2C_SODIMMA_SCL

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)

1	VREFDQ	VSS	2
3	VSS	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS	8
9	VSS	DQS0*	10
11	DM0	DQS0	12
13	VSS	VSS	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS	VSS	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS	VSS	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS	VSS	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS	VSS	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS	VSS	44
45	DQS2*	DM2	46
47	DQS2	VSS	48
49	VSS	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS	54
55	VSS	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS	60
61	VSS	DQS3*	62
63	DM3	DQS3	64
65	VSS	VSS	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS	VSS	72

CRITICAL
KEY

MEM_A_DQ<0> MEM_A_DQ<4>
MEM_A_DQ<1> MEM_A_DQ<5>
MEM_A_DM<0> MEM_A_DQS_N<0>
MEM_A_DQS_P<0>
MEM_A_DQ<6> MEM_A_DQ<3>
MEM_A_DQ<7> MEM_A_DQ<2>
MEM_A_DQ<8> MEM_A_DQ<9>
MEM_A_DQ<12> MEM_A_DQ<13>
MEM_A_DQS_N<1> MEM_A_DM<1>
MEM_A_DQS_P<1> MEM_RESET_L
MEM_A_DQ<10> MEM_A_DQ<11>
MEM_A_DQ<15> MEM_A_DQ<14>
MEM_A_DQ<25> MEM_A_DQ<29>
MEM_A_DQ<24> MEM_A_DQ<28>
MEM_A_DQS_N<3> MEM_A_DM<3>
MEM_A_DQS_P<3>
MEM_A_DQ<26> MEM_A_DQ<27>
MEM_A_DQ<30> MEM_A_DQ<31>
MEM_A_DQ<20> MEM_A_DQ<18>
MEM_A_DQ<21> MEM_A_DQ<17>
MEM_A_DM<2> MEM_A_DQS_N<2>
MEM_A_DQS_P<2>
MEM_A_DQ<23> MEM_A_DQ<19>
MEM_A_DQ<16> MEM_A_DQ<22>

516-0201

PP0V75_S3_MEM_VREFCA_A 25C1

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

"Factory" (top) slot

7C5 =PPSPD_S0_MEM_A

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

=PP0V75_S0_MEM_VTT_A 7C7

C3150 2.2UF 20% 6.3V CERM 402-LF
C3151 2.2UF 20% 6.3V CERM 402-LF

516-0201
SPD ADDR=0xA0(WR)/0xA1(RD)

SYNC_MASTER=BEN SYNC_DATE=06/30/2008
PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 31 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

=PP1V5_S3_MEM_B

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603
C3210 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3211 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3212 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3213 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3214 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3215 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3216 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3217 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL

PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 F-RT-BGA3 DDR3-SODIMM (2 OF 2)

MEM_B_CKE<0>	73 CKE0	CKE1 74	MEM_B_CKE<1>
	75 VDD	VDD 76	
	77 NC	A15 78	MEM_B_A<15>
MEM_B_BA<2>	79 BA2	A14 80	MEM_B_A<14>
	81 VDD	VDD 82	
MEM_B_A<12>	83 A12/BC*	A11 84	MEM_B_A<11>
MEM_B_A<9>	85 A9	A7 86	MEM_B_A<7>
	87 VDD	VDD 88	
MEM_B_A<8>	89 A8	A6 90	MEM_B_A<6>
MEM_B_A<5>	91 A5	A4 92	MEM_B_A<4>
	93 VDD	VDD 94	
MEM_B_A<3>	95 A3	A2 96	MEM_B_A<2>
MEM_B_A<1>	97 A1	A0 98	MEM_B_A<0>
	99 VDD	VDD 100	
MEM_B_CLK_P<0>	101 CK0	CK1 102	MEM_B_CLK_P<1>
MEM_B_CLK_N<0>	103 CK0*	CK1* 104	MEM_B_CLK_N<1>
	105 VDD	VDD 106	
MEM_B_A<10>	107 A10/AP	BA1 108	MEM_B_BA<1>
MEM_B_BA<0>	109 BA0	RAS* 110	MEM_B_RAS_L
	111 VDD	VDD 112	
MEM_B_WE_L	113 WE*	S0* 114	MEM_B_CS_L<0>
MEM_B_CAS_L	115 CAS*	ODT0 116	MEM_B_ODT<0>
	117 VDD	VDD 118	
MEM_B_A<13>	119 A13	ODT1 120	MEM_B_ODT<1>
MEM_B_CS_L<1>	121 S1*	NC 122	
	123 VDD	VDD 124	
	125 TEST	VREFCA 126	
	127 VSS	VSS 128	
MEM_B_DQ<37>	129 DQ32	DQ36 130	MEM_B_DQ<36>
MEM_B_DQ<32>	131 DQ33	DQ37 132	MEM_B_DQ<33>
	133 VSS	VSS 134	
MEM_B_DQS_N<4>	135 DQS4*	DM4 136	MEM_B_DM<4>
MEM_B_DQS_P<4>	137 DQS4	VSS 138	
	139 VSS	DQ38 140	MEM_B_DQ<38>
MEM_B_DQ<35>	141 DQ34	DQ39 142	MEM_B_DQ<34>
MEM_B_DQ<39>	143 DQ35	VSS 144	
	145 VSS	DQ44 146	MEM_B_DQ<40>
MEM_B_DQ<45>	147 DQ40	DQ45 148	MEM_B_DQ<44>
MEM_B_DQ<41>	149 DQ41	VSS 150	
	151 VSS	DQS5* 152	MEM_B_DQS_N<5>
MEM_B_DM<5>	153 DM5	DQS5 154	MEM_B_DQS_P<5>
	155 VSS	VSS 156	
MEM_B_DQ<46>	157 DQ42	DQ46 158	MEM_B_DQ<42>
MEM_B_DQ<47>	159 DQ43	DQ47 160	MEM_B_DQ<43>
	161 VSS	VSS 162	
MEM_B_DQ<53>	163 DQ48	DQ52 164	MEM_B_DQ<52>
MEM_B_DQ<49>	165 DQ49	DQ53 166	MEM_B_DQ<48>
	167 VSS	VSS 168	
MEM_B_DQS_N<6>	169 DQS6*	DM6 170	MEM_B_DM<6>
MEM_B_DQS_P<6>	171 DQS6	VSS 172	
	173 VSS	DQ54 174	MEM_B_DQ<51>
MEM_B_DQ<55>	175 DQ50	DQ55 176	MEM_B_DQ<50>
MEM_B_DQ<54>	177 DQ51	VSS 178	
	179 VSS	DQ60 180	MEM_B_DQ<63>
MEM_B_DQ<56>	181 DQ56	DQ61 182	MEM_B_DQ<59>
MEM_B_DQ<58>	183 DQ57	VSS 184	
	185 VSS	DQS7* 186	MEM_B_DQS_N<7>
MEM_B_DM<7>	187 DM7	DQS7 188	MEM_B_DQS_P<7>
	189 VSS	VSS 190	
MEM_B_DQ<61>	191 DQ58	DQ62 192	MEM_B_DQ<62>
MEM_B_DQ<60>	193 DQ59	DQ63 194	MEM_B_DQ<57>
	195 VSS	VSS 196	
MEM_B_SA<0>	197 SA0	EVENT* 198	MEM_EVENT_L
	199 VDDSPD	SDA 200	=I2C_SODIMMB_SDA
MEM_B_SA<1>	201 SA1	SCL 202	=I2C_SODIMMB_SCL
	203 VTT	VTT 204	=PP0V75_S0_MEM_VTT_B
	MTG PINS		
	205 MTG PIN	MTG PIN 206	
	207 MTG PIN	MTG PIN 208	
	209 MTG PIN	MTG PIN 210	
	211 MTG PIN	MTG PIN 212	

R3240 10K 5% 1/16W MF-LF 402
C3240 2.2UF 20% 6.3V CERM 402-LF
R3241 10K 5% 1/16W MF-LF 402
C3250 2.2UF 20% 6.3V CERM 402-LF
C3251 2.2UF 20% 6.3V CERM 402-LF

=PPSPD_S0_MEM_B

516S0706
SPD ADDR=0xA2(WR)/0xA3(RD)

PP0V75_S3_MEM_VREFCA_B

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

J3200 F-RT-BGA3 DDR3-SODIMM (1 OF 2)

	1 VREFDQ	VSS 2	
MEM_B_DQ<1>	3 VSS	DQ4 4	MEM_B_DQ<4>
MEM_B_DQ<0>	5 DQ0	DQ5 6	MEM_B_DQ<5>
	7 DQ1	VSS 8	
MEM_B_DM<0>	9 VSS	DQS0* 10	MEM_B_DQS_N<0>
	11 DM0	DQS0 12	MEM_B_DQS_P<0>
MEM_B_DQ<3>	13 VSS	VSS 14	
MEM_B_DQ<6>	15 DQ2	DQ6 16	MEM_B_DQ<7>
	17 DQ3	DQ7 18	MEM_B_DQ<2>
MEM_B_DQ<13>	19 VSS	VSS 20	
MEM_B_DQ<14>	21 DQ8	DQ12 22	MEM_B_DQ<12>
	23 DQ9	DQ13 24	MEM_B_DQ<9>
	25 VSS	VSS 26	
MEM_B_DQS_N<1>	27 DQS1*	DM1 28	MEM_B_DM<1>
MEM_B_DQS_P<1>	29 DQS1	RESET* 30	MEM_RESET_L
	31 VSS	VSS 32	
MEM_B_DQ<15>	33 DQ10	DQ14 34	MEM_B_DQ<8>
MEM_B_DQ<10>	35 DQ11	DQ15 36	MEM_B_DQ<11>
	37 VSS	VSS 38	
MEM_B_DQ<20>	39 DQ16	DQ20 40	MEM_B_DQ<16>
MEM_B_DQ<17>	41 DQ17	DQ21 42	MEM_B_DQ<21>
	43 VSS	VSS 44	
MEM_B_DQS_N<2>	45 DQS2*	DM2 46	MEM_B_DM<2>
MEM_B_DQS_P<2>	47 DQS2	VSS 48	
	49 VSS	DQ22 50	MEM_B_DQ<18>
MEM_B_DQ<22>	51 DQ18	DQ23 52	MEM_B_DQ<23>
MEM_B_DQ<19>	53 DQ19	VSS 54	
	55 VSS	DQ28 56	MEM_B_DQ<29>
MEM_B_DQ<24>	57 DQ24	DQ29 58	MEM_B_DQ<25>
MEM_B_DQ<28>	59 DQ25	VSS 60	
	61 VSS	DQS3* 62	MEM_B_DQS_N<3>
MEM_B_DM<3>	63 DM3	DQS3 64	MEM_B_DQS_P<3>
	65 VSS	VSS 66	
MEM_B_DQ<26>	67 DQ26	DQ30 68	MEM_B_DQ<30>
MEM_B_DQ<31>	69 DQ27	DQ31 70	MEM_B_DQ<27>
	71 VSS	VSS 72	

516S0706

DDR3 GROUND RETURN CAPS (MCP SIDE)

=PP1V5_S0_MEM_MCP

C3222 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3223 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3224 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3225 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3226 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3227 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3228 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3229 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL

"Expansion" (bottom) slot

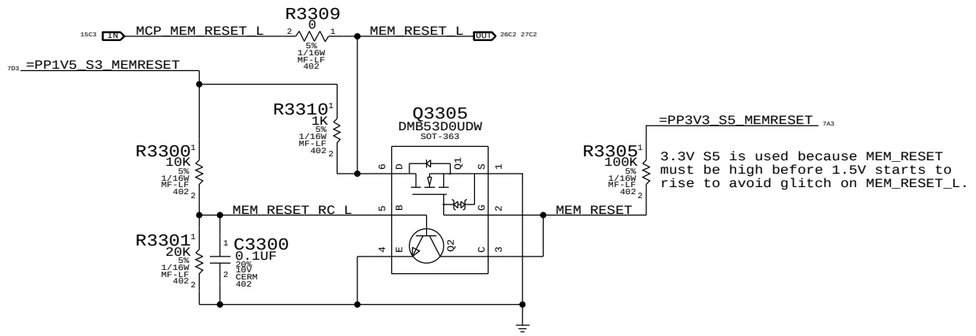
SYNC_MASTER=BEN SYNC_DATE=05/09/2008
PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 32 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

DDR3 RESET Support

Required becaues MCP79 does not meet DDR3 spec power-up reset timing requirement.



SYNC_MASTER=T18_MLB	SYNC_DATE=04/04/2008
PAGE TITLE: DDR3 Support	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 33 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

PCIE_MINI_PRSNT_L

Q3401
SSM6N15FEAPE
SOT563

AP_PWR_EN

MINI_CLKREQ_L

Q3401
SSM6N15FEAPE
SOT563

CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM

PCIE_MINI_D2R_P
PCIE_MINI_D2R_N
PCIE_MINI_R2D_P
PCIE_MINI_R2D_N
PCIE_CLK100M_MINI_CONN_P
PCIE_CLK100M_MINI_CONN_N
MINI_CLKREQ_Q_L
PCIE_WAKE_L
NC
NC

PLACEMENT_NOTE=Place close to J3401.

C3431
0.1uF
10% 16V X5R 402

C3430
0.1uF
10% 16V X5R 402

PCIE_MINI_R2D_C_P
PCIE_MINI_R2D_C_N

PLACEMENT_NOTE=Place close to J3401.

CRITICAL
L3401
90-OHM-100MA
DLP11S

PCIE_CLK100M_MINI_P
PCIE_CLK100M_MINI_N

PLACEMENT_NOTE=Place close to J3401.

AIRPORT

1000 mA peak
750 mA nominal max

PP5V_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

L3404
FERR-120-OHM-1.5A
0402-LF

C3422 0.1uF 20% 10V CERM 402
C3421 0.1uF 20% 10V CERM 402
C3420 10UF 20% 10V X5R 805

PLACEMENT_NOTE=Place close to J3401.

PP5V_WLAN_F
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

PLACEMENT_NOTE=Place close to Q3450.

5V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

CRITICAL
Q3450
TPCP8102
23V1K-SM

C3450 0.1UF 10% 16V X5R 402

P5VWLAN_SS

C3451 0.033UF 10% 16V X5R 402

R3450 100K 5% 1/16W MF-LF 402

R3451 10K 5% 1/16W MF-LF 402

=PP5V_S3_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

PM_WLAN_EN_L

PLACEMENT_NOTE=Place close to Q3450.

=PP5V_S3_BTCAMERA_F
=I2C_ALS_SDA
=I2C_ALS_SCL
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

ALS

CAMERA

USB_CAMERA_CONN_P
USB_CAMERA_CONN_N

CRITICAL
L3402
90-OHM
DLP0NS

USB_CAMERA_P
USB_CAMERA_N

PLACEMENT_NOTE=Place close to J3401.

275 mA peak
206 mA nominal max

L3405
FERR-120-OHM-1.5A
0402-LF

C3452 0.1uF 20% 10V CERM 402

=PP5V_S3_BTCAMERA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

CONN_USB2_BT_P
CONN_USB2_BT_N

BLUETOOTH

CRITICAL
L3403
90-OHM
DLP0NS

USB_BT_P
USB_BT_N

PLACEMENT_NOTE=Place close to J3401.

PP5V_WLAN_F

=PP3V3_S3_WLAN

R3453 33K 5% 1/16W MF-LF 402

U3402
74LVC1G17DRL
SOT-553

TC7SZ08AFEAPE
SOT665
U3401

MINI_RESET_CONN_L
WLAN_SMIT_BUF
MINI_RESET_L

NC
C3453 1UF 10% 6.3V CERM 402

R3454 62K 5% 1/16W MF-LF 402

WLAN_SMIT_RC

R3455 1 5% 1/16W MF-LF 402

WLAN_SMIT_DISCHRG

Q3455
SSM3K15FV
SOD-VESM-HF

PM_WLAN_EN_L

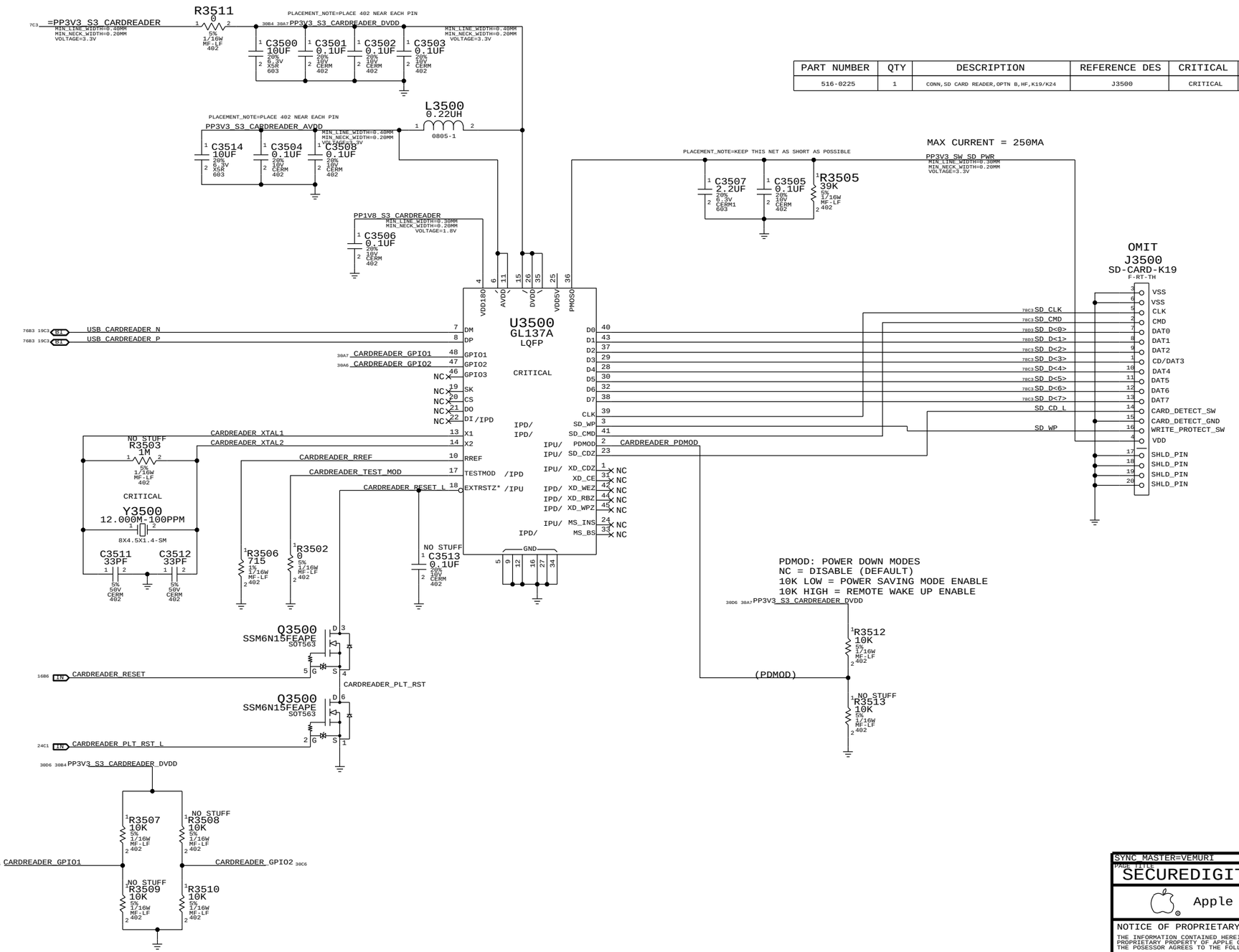
SYNC_MASTER=YITE SYNC_DATE=04/22/2008

PAGE TITLE
Right Clutch Connector

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 34 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
516-0225	1	CONN,SD CARD READER,OPTN B,HF,K19/K24	J3500	CRITICAL	

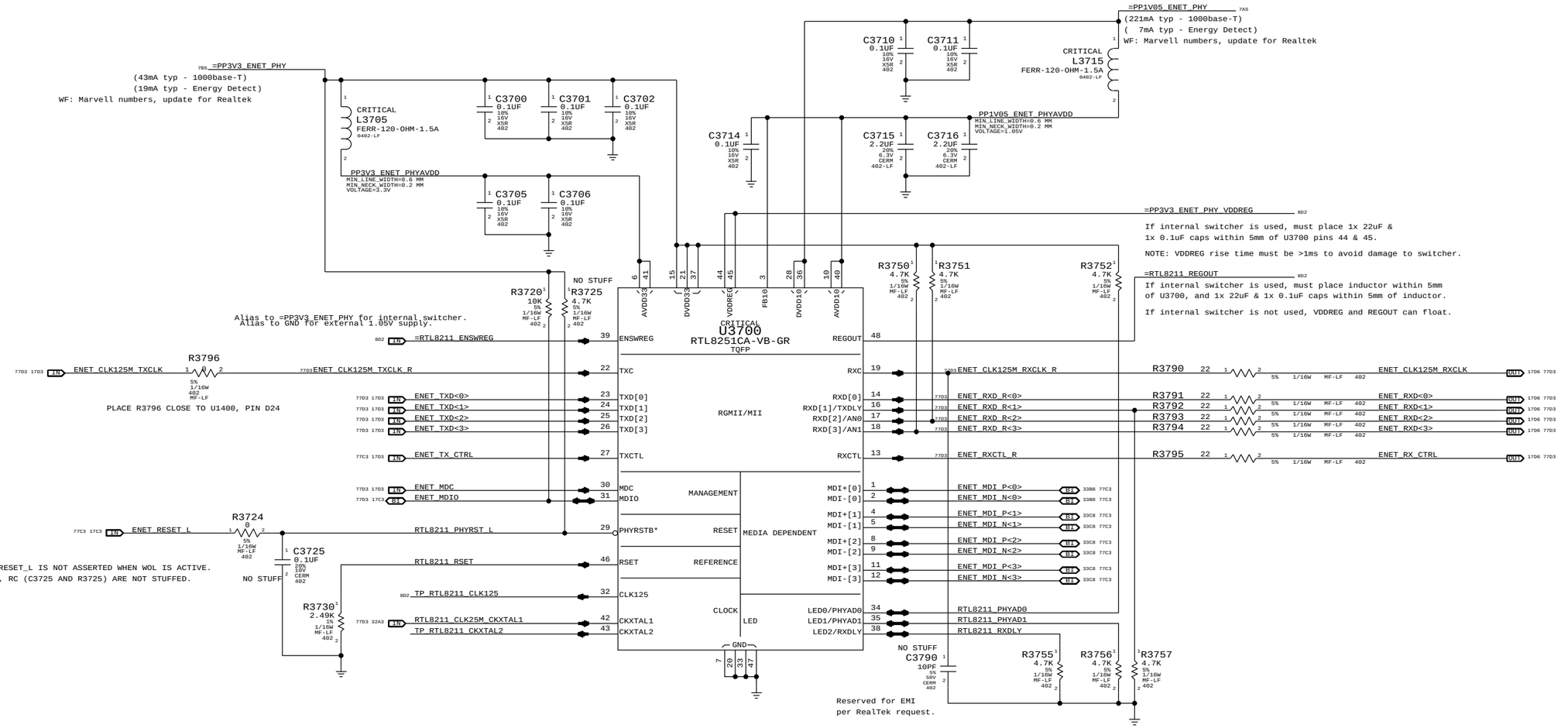


SYNC_MASTER=VEMURI SYNC_DATE=01/30/2009

PAGE TITLE
SECUREDIGITAL CARD READER

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 35 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

SYNC_MASTER=SUMA SYNC_DATE=05/23/2008

PAGE TITLE: Ethernet PHY (RTL8211CL)

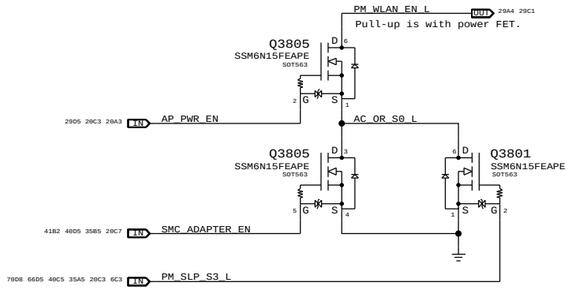
Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 37 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

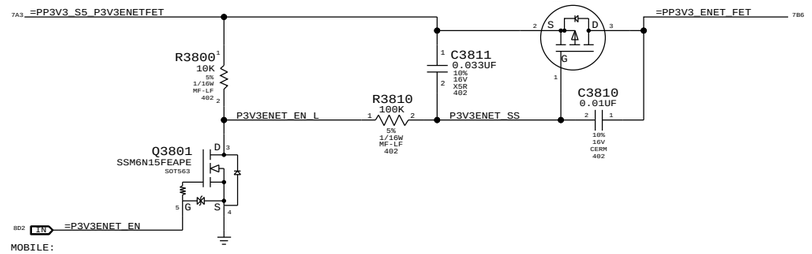


3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL

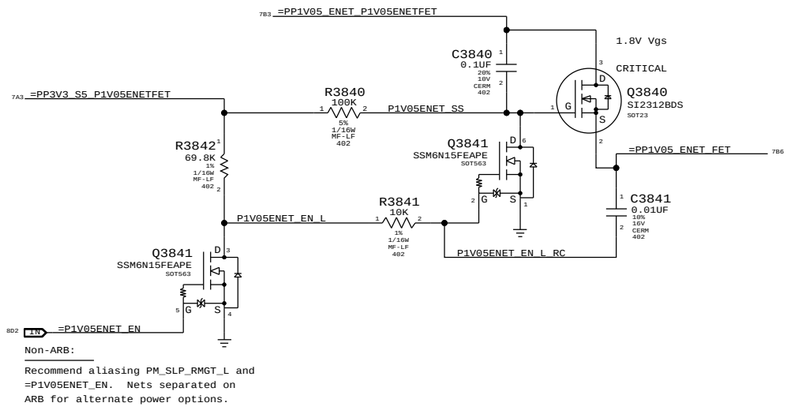
Q3810
NTR4101P
SOT-23-HF



MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

1.05V ENET FET

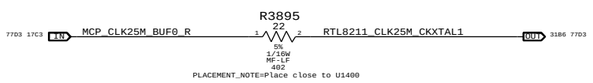


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



PLACEMENT_NOTE=Place close to U1400

SYNC MASTER=SUMA SYNC DATE=07/07/2008

PAGE TITLE
Ethernet & AirPort Support

Apple Inc.

DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
BRANCH
PAGE 38 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

- COPY THIS PAGE FROM K36 CSA.39

PLACE ONE CAP EACH NEAR PINS 3 AND 4 OF T3901 AND T3902

ENET_CONN_CTAP

C3900 0.1UF 10% 16V X5R 402
C3901 0.1UF 10% 16V X5R 402
C3902 0.1UF 10% 16V X5R 402
C3903 0.1UF 10% 16V X5R 402

CRITICAL
T3901
SM
TX → RX
TLA-6T213HF

CRITICAL
T3902
SM
TX → RX
TLA-6T213HF

77C3 31B3 B1 ENET_MDI_P<1>
77C3 31B3 B1 ENET_MDI_N<1>
77C3 31B3 B1 ENET_MDI_P<3>
77C3 31B3 B1 ENET_MDI_N<3>
77C3 31B3 B1 ENET_MDI_N<2>
77C3 31B3 B1 ENET_MDI_P<2>
77C3 31B3 B1 ENET_MDI_N<0>
77C3 31B3 B1 ENET_MDI_P<0>

77C3 ENET_MDI_TRAN_P<1>
77C3 ENET_MDI_TRAN_N<1>
77C3 ENET_MDI_TRAN_P<3>
77C3 ENET_MDI_TRAN_N<3>
77C3 ENET_MDI_TRAN_N<2>
77C3 ENET_MDI_TRAN_P<2>
77C3 ENET_MDI_TRAN_N<0>
77C3 ENET_MDI_TRAN_P<0>

ENET_CENTER_TAP<1> R3903 75 1% 1/16W MF-LF 402
ENET_CENTER_TAP<3> R3902 75 1% 1/16W MF-LF 402
ENET_CENTER_TAP<2> R3901 75 1% 1/16W MF-LF 402
ENET_CENTER_TAP<0> R3900 75 1% 1/16W MF-LF 402

C3911 10PF 5% 50V CERM 402-1 CRITICAL
C3912 10PF 5% 50V CERM 402-1 CRITICAL
C3913 10PF 5% 50V CERM 402-1 CRITICAL
C3914 10PF 5% 50V CERM 402-1 CRITICAL
C3915 10PF 5% 50V CERM 402-1 CRITICAL
C3916 10PF 5% 50V CERM 402-1 CRITICAL
C3917 10PF 5% 50V CERM 402-1 CRITICAL
C3918 10PF 5% 50V CERM 402-1 CRITICAL

PLACEMENT_NOTE=PLACE C3911-C3918 ON MDI LINES WITHOUT ANY STUBS

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

CRITICAL
C3910 1000PF 10% 2KV CERM 1206

ETHERNET CONNECTOR

CRITICAL
J3900
RJ45-M97-3
F-RT-TH

514-0636

SYNC MASTER=SUMA SYNC DATE=04/04/2008

PAGE TITLE: ETHERNET CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 39 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0558	1	RES,0.68 OHM,1%,0402,SMD	R4100	CRITICAL	

OMIT
R4100
0
5%
1/10W
MF-LF
402

35D3 7A1 =PP1V0_FW_FWPHY
135 mA
PP1V0_FW_R

L4110
120-OHM-0.3A-EMI
0402-LF
PP1V0_FW_FWPHY_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V

25 mA PCIe SerDes
C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402

110 mA Digital Core
C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402

7 mA I/O
C4120 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4124 1UF 10% 6.3V CERM 402
=PP3V3_FW_FWPHY
781 34B1 35D8 36B6 36D5
138 mA

114 mA FireWire PHY
C4130 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4132 1UF 10% 6.3V CERM 402
PP3V3_FW_FWPHY_VDDA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
L4130
120-OHM-0.3A-EMI
0402-LF

17 mA PCIe SerDes
C4135 1UF 10% 6.3V CERM 402
C4136 1UF 10% 6.3V CERM 402
PP3V3_FW_FWPHY_VP25
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
L4135
120-OHM-0.3A-EMI
0402-LF

0 mA VReg PWR
C4141 0.1UF 20% 10V CERM 402
C4140 1UF 10% 6.3V CERM 402

VDD10 VDD33 VDDH VP VP25 VREG_PWR

CRITICAL
U4100
FW643E
BGA

1394 PHY

NC ATBUSB B13
NC ATBUSH A13
NC ATBUSN A11
=FW_PHY_DS0 DS0 (IPD) NT-19 F12
=FW_PHY_DS1 DS1 (IPD) NT-20 E12
=FW_PHY_DS2 DS2 (IPD) NT-21 E13
FW_P0_TPA_N TPA0N B8
FW_P0_TPA_P TPA0P A8
FW_P1_TPA_N TPA1N B5
FW_P1_TPA_P TPA1P A5
FW_P2_TPA_N TPA2N B3
FW_P2_TPA_P TPA2P A3
FW_P0_TPB_N TPB0N B9
FW_P0_TPB_P TPB0P A9
FW_P1_TPB_N TPB1N B6
FW_P1_TPB_P TPB1P A6
FW_P2_TPB_N TPB2N B4
FW_P2_TPB_P TPB2P A4
FW_P0_TPBIAS TPBIAS0 B7
FW_P1_TPBIAS TPBIAS1 C3
FW_P2_TPBIAS TPBIAS2 A2
FW643_R0 R0 B11
FW643_TPCPS TPCPS B10
TP_FW643_NAND_TREE NAND_TREE NT-OUT K1
FW643_REXT REXT L8
FW_CLK24P576M_XO_R XO F13
FW_CLK24P576M_XI XI NT-9 G13
NOTE: NT-xx notes show NAND tree order.
TP_FW643_SE SE (IPD) M13
TP_FW643_SM SM (IPD) N13
TP_FW643_MODE_A MODE_A (IPD) NT-18 J2
TP_FW643_CE CE (IPD) L13
TP_FW643_FW620_L FW620*(IPU) D12
TP_FW643_JASI_EN JASI_EN (IPD) NT-11 D1
TP_FW643_AVREG AVREG A10
TP_FW643_VBUF VBUF H13
FW643_PU_RST_L FW_RESET* (IPU) NT-8 K13
TP_FW643_OCR10_CTL OCR_CTL_V10 J12
NC OCR_CTL_V12 (Reserved) J13

VSS VREG_VSS

PCIE_RXD0N N8 75D3 PCIE_FW_R2D_N
PCIE_RXD0P N7 75D3 PCIE_FW_R2D_P
PCIE_TXD0N N5 75D3 PCIE_FW_D2R_C_N
PCIE_TXD0P N6 75D3 PCIE_FW_D2R_C_P
REFCLKN N9 PCIE_CLK100M_FW_N IN 16C3
REFCLKP N10 PCIE_CLK100M_FW_P IN 16C3

PCI EXPRESS PHY

C4170 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_N IN 16B3 75D3
C4171 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_P IN 16B3 75D3
C4175 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_N OUT 16B6 75D3
C4176 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_P OUT 16B6 75D3
PLACEMENT_NOTE=Place C4170 close to U1400
PLACEMENT_NOTE=Place C4171 close to U1400
PLACEMENT_NOTE=Place C4175 close to U4000
PLACEMENT_NOTE=Place C4176 close to U4000

TEST CONTROLLER

NT-4 (IPU)TCK M4 TP_FW643_TCK
NT-3 (IPU)TDI N2 TP_FW643_TDI
(IPU)TDO M1 TP_FW643_TDO
NT-1 (IPU)TMS M3 TP_FW643_TMS
NT-2 (IPU)TRST* N1 FW643_TRST_L

POWER MANAGEMENT
FIXME!!! - TYPO IN SYMBOL REGCTL
NT-10 (IPD) WAKE* C2 =FW_PME_L OUT 8C2 35C8
REGCLT D13 FW643_REGCTL
VAUX_DETECT E1 FW643_VAUX_DETECT
NT-12 (IPD) VAUX_DISABLE D2 TP_FW643_VAUX_ENABLE
NT-13 (OD)CLKREQN L2 =FW_CLKREQ_L OUT 35C4

SCIF
NT-16 (IPD) SCIFCLK G2 TP_FW643_SCIFCLK
NT-14 (IPD) SCIFDAIN G1 TP_FW643_SCIFDAIN
NT-17 SCIFDOUT H1 TP_FW643_SCIFDOUT
NT-15 (IPD) SCIFMC F2 TP_FW643_SCIFMC

SERIAL EEPROM CONTROLLER
NT-7 SCL N12 FW643_SCL
NT-6 SDA M11 TP_FW643_SDA

CHIP RESET
NT-5 PERST* N4 FW_RESET_L IN 35C1

MISCELLANEOUS

=PP3V3_FW_FWPHY
781 34D2 35D8 36B6 36D5
FW643_LDO
R4165 10K 5% 1/10W MF-LF 402
R4166 10K 5% 1/10W MF-LF 402
R4164 10K 5% 1/10W MF-LF 402
R4163 10K 5% 1/10W MF-LF 402

36C4 =PPVP_FW_PHY_CPS
R4160 200K 1% 1/10W MF-LF 402
C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO
CRITICAL
Y4150 24.576MHZ SM-3.2X2.5MM
NC
NC
R4150 412 1% 1/10W MF-LF 402
R4161 2.94K 1% 1/10W MF-LF 402
R4170 191 1% 1/10W MF-LF 402
R4162 470K 5% 1/10W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402

SYNC_MASTER=K19_MLB	SYNC_DATE=11/02/2008
PAGE TITLE: FireWire LLC/PHY (FW643)	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH:
	PAGE: 41 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

3.3V FW F

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

=PP3V3_S0_P3V3FWFET
R4290 10K 5% 1/16W MF-LF 402
P3V3FW_EN_L
R4291 100K 5% 1/16W MF-LF 402
Q4290 SSM6N15FEAPE SOT563
FW_PWR_EN
C4290 0.033UF 10% 16V X5R 402
CRITICAL Q4291 NTR4101P SOT-23-HF
=PP3V3_FW_FET
C4291 0.01UF 10% 16V CERM 402
P3V3FW_SS

=PP3V3_FW_FWPHY
FWPHY_WAKE_YES
R4276 100K 5% 1/16W MF-LF 402
R4277 10K 5% 1/16W MF-LF 402
FW_WAKE
FW_PLUG_DET_L
CRITICAL Q4276 DMB53D0UV SOT-563
=FW_PME_L
CRITICAL Q4276 DMB53D0UV SOT-563
FWPHY_WAKE_YES

1.05V FW FET

=PP1V05_FW_P1V05FWFET
C4296 0.1UF 20% 16V CERM 402
=PP3V3_S0_P1V05FWFET
R4297 220K 5% 1/16W MF-LF 402
P1V05FW_SS
CRITICAL Q4295 SI2312BDS SOT23
Q4293 SSM6N15FEAPE SOT563
=PP3V3_S5_P1V05FWFET
R4295 10K 5% 1/16W MF-LF 402
R4296 100K 5% 1/16W MF-LF 402
P1V05_FW_EN_L
P1V05_FW_EN_L_RC
=PP1V0_FW_FET
C4295 0.068UF 10% 16V CERM 402
Q4293 SSM6N15FEAPE SOT563
FW_PWR_EN

PCIE_FW_PRSNT
MAKE_BASE=TRUE
Q4264 SSM6N15FEAPE SOT563
FW_CLKREQ_L
Q4264 SSM6N15FEAPE SOT563
FW_PWR_EN
=FW_CLKREQ_L
FW_CLKREQ_PHY_L
MAKE_BASE=TRUE

=PP3V3_S0_FWPWRCTL
R4281 100K 5% 1/16W MF-LF 402
R4280 10K 1% 1/16W MF-LF 402
=PP1V0_FW_FWPHY
P1V0_FW_RC
C4281 1UF 10% 10V X5R 402
CRITICAL Q4299 DMB53D0UV SOT-563
P1V0_RESET_GATE
R4283 10K 5% 1/16W MF-LF 402
=FW_RESET_L
CRITICAL Q4299 DMB53D0UV SOT-563
FW_RESET_L
PP1V05_FW PGOOD/FW_RESET_L

FireWire Port Power Switch

CRITICAL Q4260 FDC638P_G SM
=PPBUS_S5_FWPWRSW
PPBUS_FW_FWPWRSW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL F4260 1.1A-24V MINISMDC110H24
PPBUS_FW_FWPWRSW_D
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL D4260 SM CRS08-1.5A-30V
=PPBUS_S5_FW_FET

Late-VG Event Detection

CRITICAL Q4262 DMB54D0UV SOT-563
R4265 10K 1% 1/16W MF-LF 402
NOSTUFF R4263 100 1% 1/16W MF-LF 402
LATEVG_FAULT_EVENT_PNP
LATEVG_FAULT_EVENT
LATEVG_RETRY_RC
C4263 1UF 10% 10V X5R 402 NOSTUFF
R4261 470K 5% 1/16W MF-LF 402
FWPWR_EN_L_DIV
R4260 300K 5% 1/16W MF-LF 402
C4260 0.1UF 10% 25V X5R 402
FWPWR_EN_L
Q4261 2N7002DW-X-G SOT-363
Q4261 2N7002DW-X-G SOT-363
SMC_ADAPTER_EN
PM_SLP_S3_L
Enables port power when machine is running or on AC.

=PP3V3_FW_LATEVG_ACTIVE
PP2V4_FW_LATEVG
R4211 10K 5% 1/16W MF-LF 402
R4212 10K 1% 1/16W MF-LF 402
C4210 0.1UF 10% 16V CERM 402
U4210 LMC7211 SM-HF
FWLATEGV_3V_REF
P2V4_FWLATEVG_RC
LATEVG_EVENT
C4211 100PF 5% 50V CERM 402
R4213 80.6K 1% 1/16W MF-LF 402
R4210 200K 1% 1/16W MF-LF 402
FWLATEVG Hysteresis:
3.08V when port power is on
2.91V when late VG event and port power is off

=PP1V05_FW_PWRCTL
R4275 1K 5% 1/16W MF-LF 402
FW_PWR_EN_L
R4270 330K 5% 1/16W MF-LF 402
CRITICAL Q4270 BC847CDXV6TXG SOT563
FW_DET_MIRROR
FW_P1_TPBIAS_R
R4272 1K 5% 1/16W MF-LF 402
R4271 56K 5% 1/16W MF-LF 402
FW_PLUG_DET
CRITICAL Q4270 BC847CDXV6TXG SOT563
FW_DET_EMIT
R4273 12K 5% 1/16W MF-LF 402
C4270 0.1UF 10% 16V X5R 402
=PP3V3_S0_FWPWRCTL
R4274 100K 5% 1/16W MF-LF 402
FW_PLUG_DET_L
CRITICAL Q4275 DMB53D0UV SOT-563
CRITICAL Q4275 DMB53D0UV SOT-563
FW_PWR_EN
FW_P1_TPBIAS

SYNC_MASTER=YUN_K19_MLB	SYNC_DATE=12/22/2008
PAGE TITLE: FireWire Port Power	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH
	PAGE: 42 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

3686 35D8 34D2 34B1 781 =PP3V3_FW_FWPHY

R4382 10K 1% 1/16W MF-LF 402

R4380 10K 1% 1/16W MF-LF 402

FWPHY_DS0 MAKE_BASE=TRUE =FW_PHY_DS0 34C6

FWPHY_DS2 MAKE_BASE=TRUE =FW_PHY_DS2 34C6

FWPHY_DS1 MAKE_BASE=TRUE =FW_PHY_DS1 34C6

R4381 10K 1% 1/16W MF-LF 402

3486	FW_P0_TPBIAS	NC_FW0_TPBIAS	MAKE_BASE=TRUE
3486	FW_P2_TPBIAS	NC_FW2_TPBIAS	MAKE_BASE=TRUE
78D3 34C6	FW_P0_TPA_N	NC_FW0_TPAN	MAKE_BASE=TRUE
78D3 3486	FW_P0_TPA_P	NC_FW0_TPAP	MAKE_BASE=TRUE
3486	FW_P2_TPA_N	NC_FW2_TPAN	MAKE_BASE=TRUE
3486	FW_P2_TPA_P	NC_FW2_TPAP	MAKE_BASE=TRUE
78D3 3486	FW_P0_TPB_N	NC_FW0_TPBN	MAKE_BASE=TRUE
78D3 3486	FW_P0_TPB_P	NC_FW0_TPBP	MAKE_BASE=TRUE
3486	FW_P2_TPB_N	NC_FW2_TPBN	MAKE_BASE=TRUE
3486	FW_P2_TPB_P	NC_FW2_TPBP	MAKE_BASE=TRUE

Termination

Place close to FireWire PHY

35A4 3486 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 6.3V CERM-X5R 402

SIGNAL_MODEL=EMPTY SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402

R4361 56.2 1% 1/16W MF-LF 402

78D3 3486 FW_P1_TPA_P — MAKE_BASE=TRUE — FW_PORT1_TPA_P 3685

78D3 3486 FW_P1_TPA_N — MAKE_BASE=TRUE — FW_PORT1_TPA_N 3685

78D3 3486 FW_P1_TPB_P — MAKE_BASE=TRUE — FW_PORT1_TPB_P 3685

78D3 3486 FW_P1_TPB_N — MAKE_BASE=TRUE — FW_PORT1_TPB_N 3685

SIGNAL_MODEL=EMPTY SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402

R4363 56.2 1% 1/16W MF-LF 402

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

781 =PPVP_FW_PHY_CPS_FET

Q4300 BSS8402DW (SYM-VER1)

PPVP_FW_CPS MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=12.6V MAKE_BASE=TRUE =PPVP_FW_PHY_CPS 34B7

R4311 470K 5% 1/16W MF-LF 402

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

Q4300 BSS8402DW SOT-363 (SYM-VER1)

781 =PP3V3_FW_FWPHY

Snapback" & "Late VG" Protection

36A5 35A8 PP2V4_FW_LATEVG

DP4310 BAV99DW-X-G SOT-363 CRITICAL

C4311 0.01uF 10% 50V X7R 402

DP4310 BAV99DW-X-G SOT-363

C4310 0.01uF 10% 50V X7R 402

3687 FW_PORT1_TPB_N

3687 FW_PORT1_TPB_P

3687 FW_PORT1_TPA_N

3687 FW_PORT1_TPA_P

DP4311 BAV99DW-X-G SOT-363

C4312 0.01uF 10% 50V X7R 402

CRITICAL DP4311 BAV99DW-X-G SOT-363

C4313 0.01uF 10% 50V X7R 402

C4319 0.1uF 10% 50V X7R 603-1

R4319 1M 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

Cable Power

781 =PPVP_FW_PORT1

CRITICAL L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

PORT 1

BILINGUAL

CRITICAL J4310 1394B-M97 F-RT-TH

(FW_PORT1_BREF)

NC

(GND_FW_PORT1_VG)

FW_PORT1_AREF

OUTPUT

INPUT

CHASSIS GND

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

514S0605

Late-VG Protection Power

7A3 =PP3V3_FW_LATEVG

R4390 332 1% 1/16W MF-LF 402

PP2V4_FW_LATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V 35A8 36C5

CRITIICAL D4390 MMBZ5227BLT1H SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin

R4390 should be 390 Ohms max for a 3.3V rail

SYNC_MASTER=K19_MLB SYNC_DATE=11/02/2008

PAGE TITLE: FireWire Ports

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

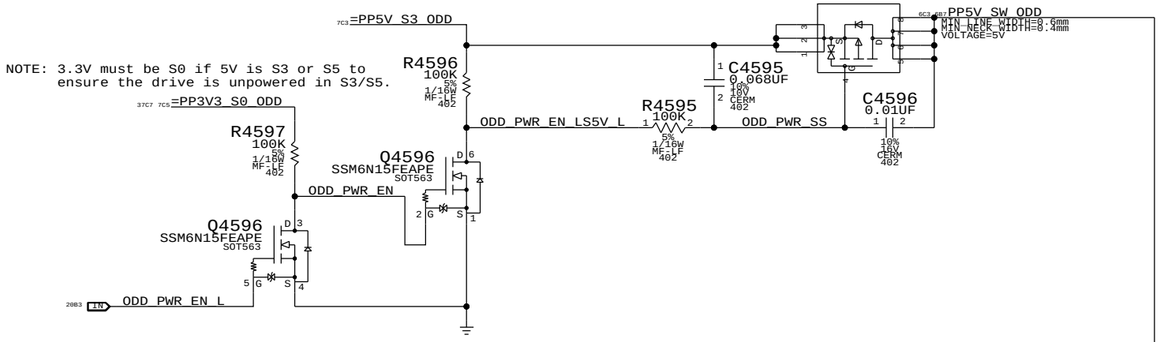
REVISION C.0.0

BRANCH

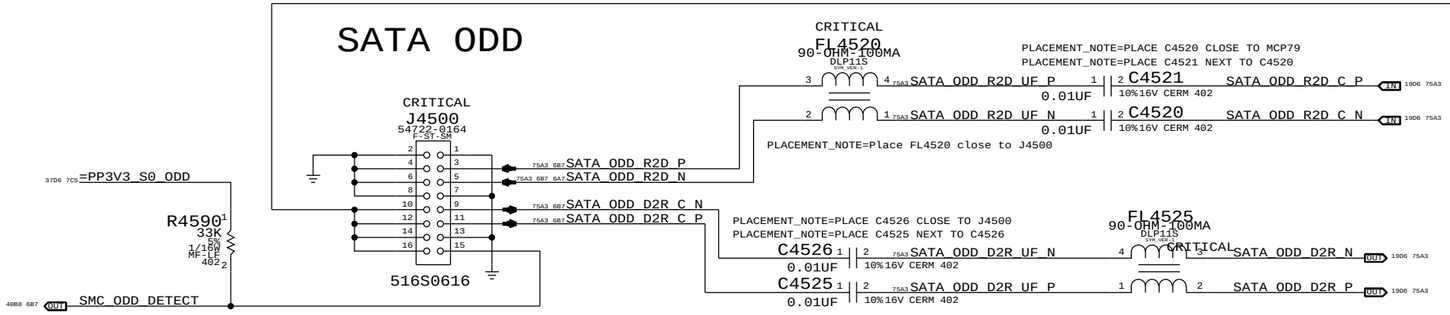
PAGE 43 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

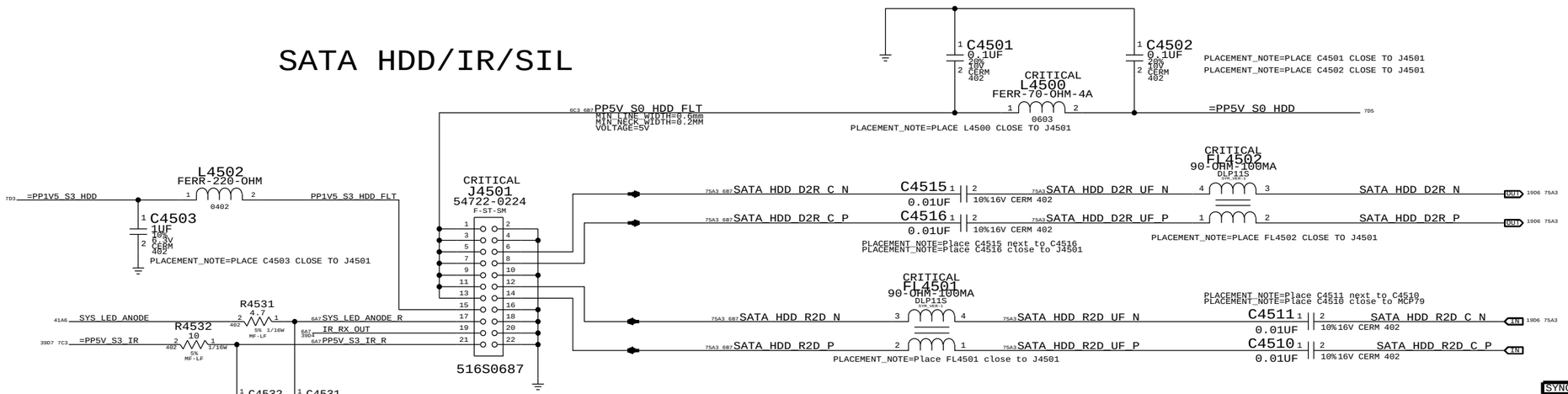
ODD Power Control



SATA ODD



SATA HDD/IR/SIL



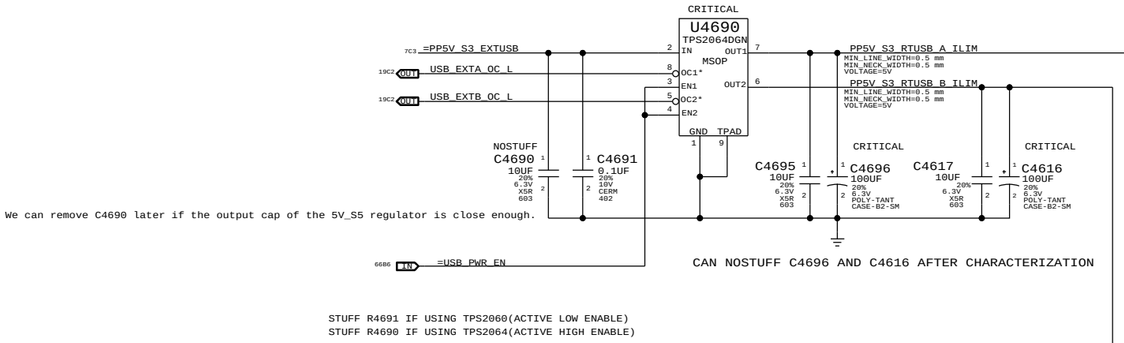
SYNC MASTER=K19 MLB SYNC DATE=12/04/2008

PAGE TITLE: SATA Connectors

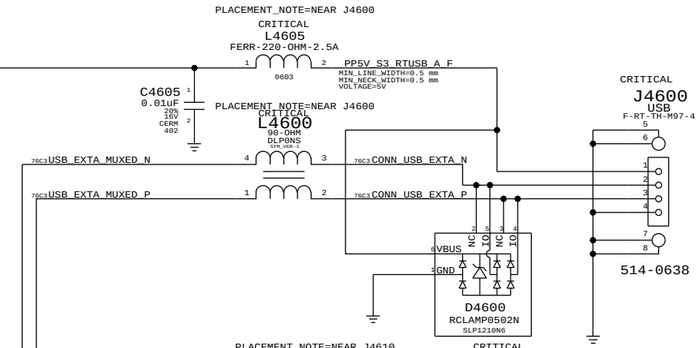
Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 45 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

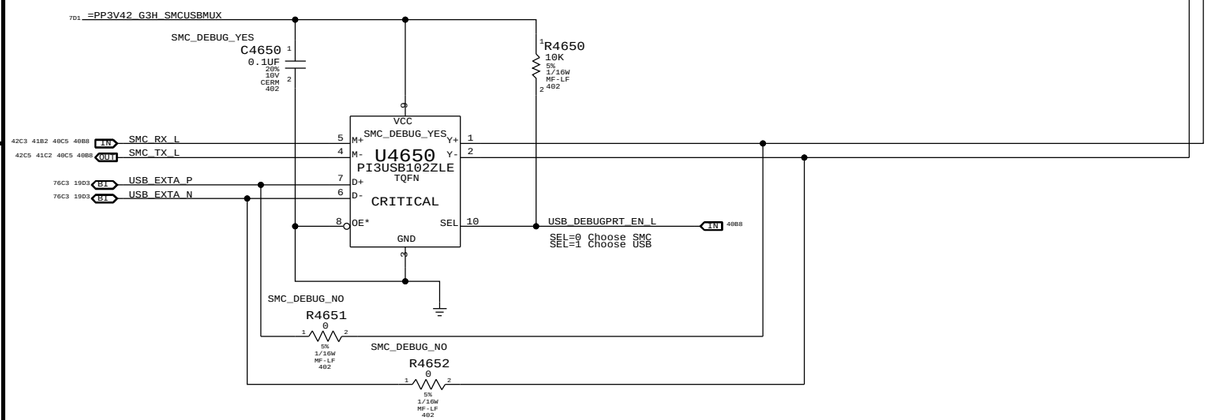
Port Power Switch



USB PORT A (FRONT PORT)

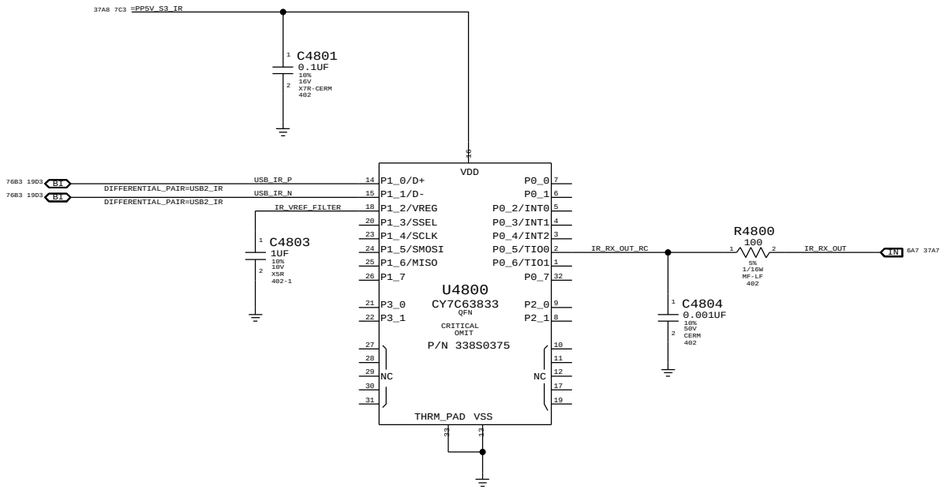


USB/SMC Debug Mux



USB PORT B (BACK PORT)

SYNC_MASTER=YUAN.MA	SYNC_DATE=01/18/2008
PAGE TITLE: External USB Connectors	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 46 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



CYPRESS 'ENCORE II' USB CONTROLLER

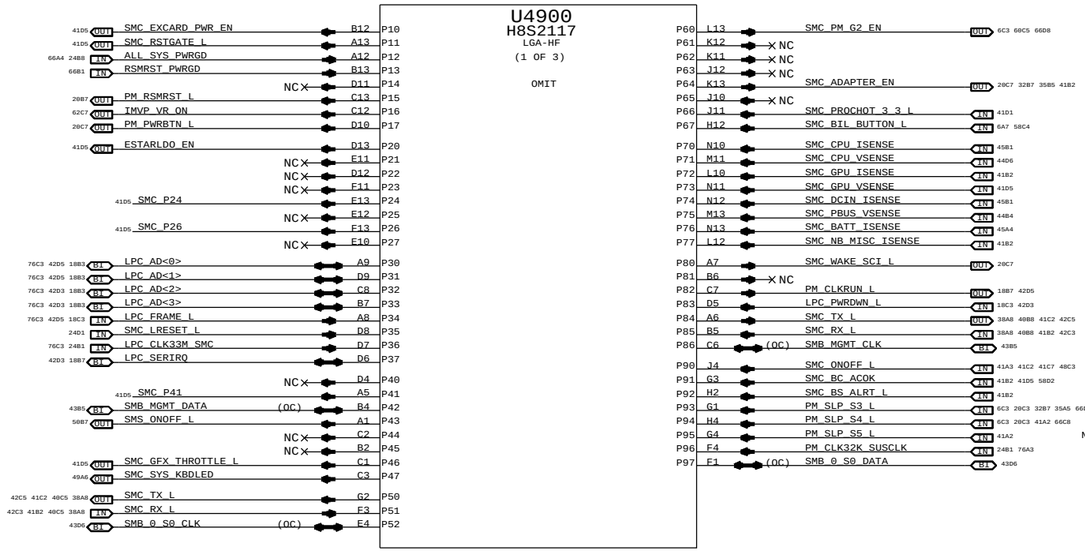
SYNC_MASTER=YUAN.MA SYNC_DATE=05/28/2008

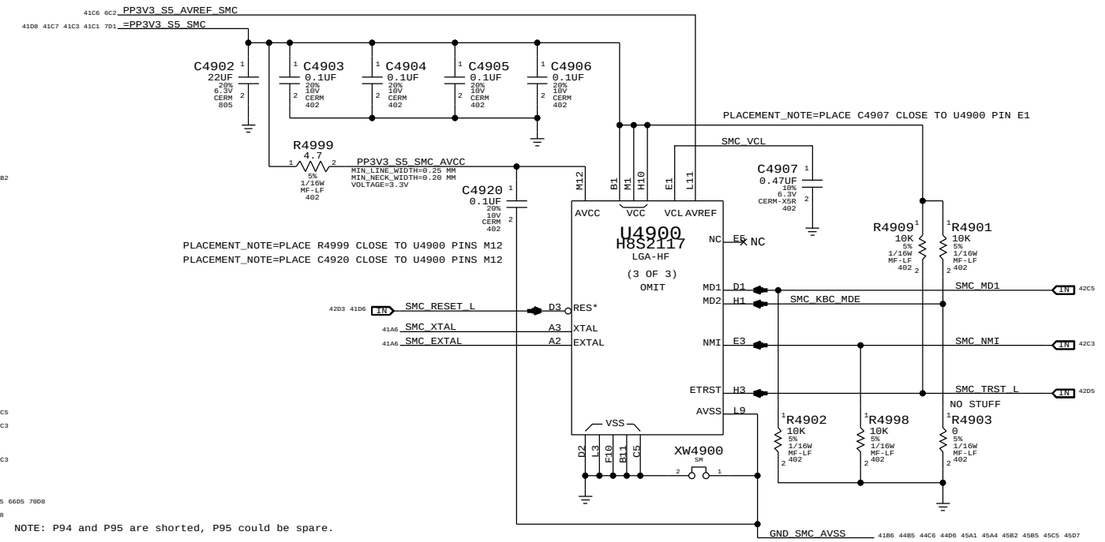
PAGE TITLE
Front Flex Support

Apple Inc.

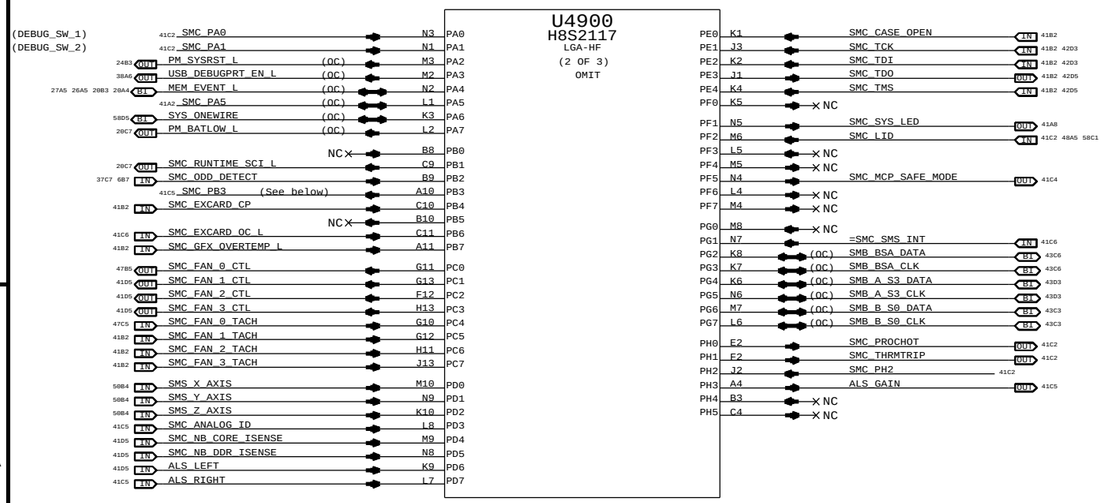
DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
BRANCH
PAGE 48 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: P94 and P95 are shorted, P95 could be spare.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

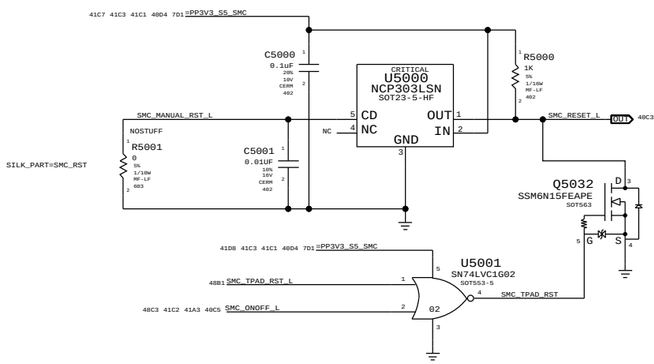
SYNC_MASTER=T18_MLB SYNC_DATE=06/26/2008

PAGE TITLE: SMC

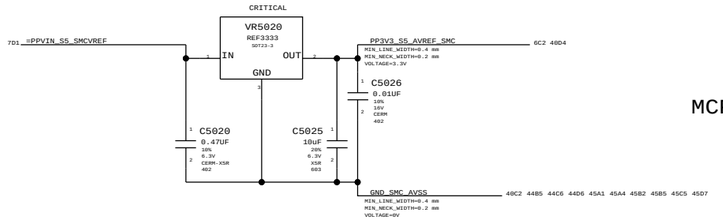
Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 49 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

SMC Reset "Button" / Brownout Detect

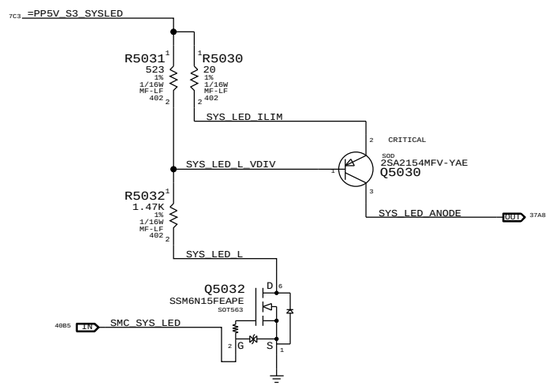


SMC AVREF Supply

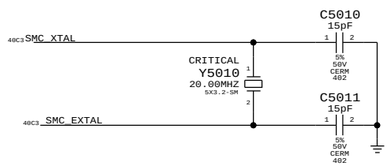


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	ISL60002-33, INTERSIL

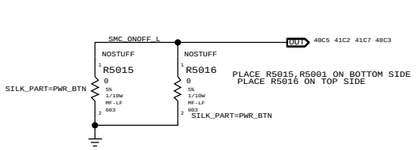
System (Sleep) LED Circuit



SMC Crystal Circuit

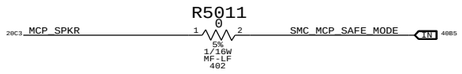


Debug Power "Button"

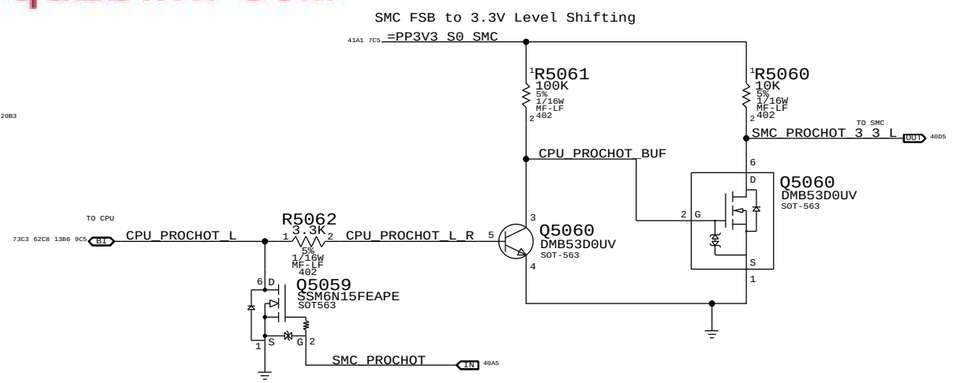


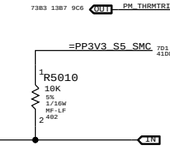
MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

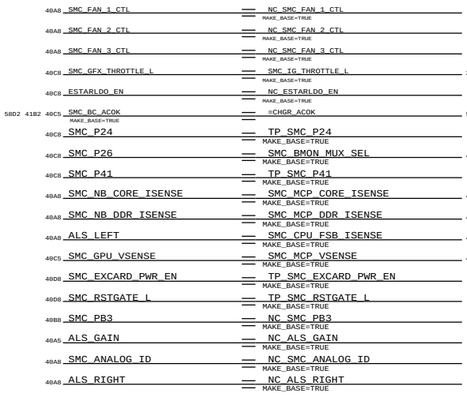
RADAR 5925345

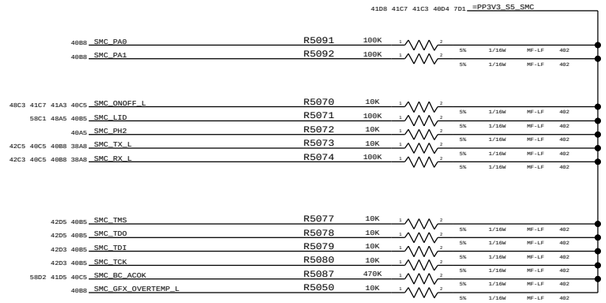


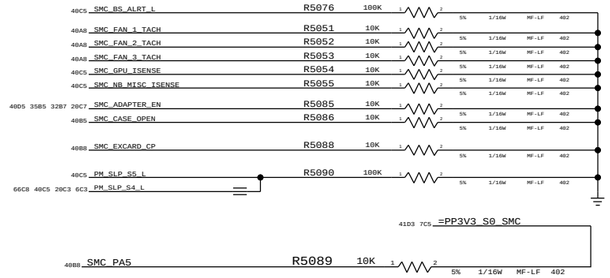
SMC FSB to 3.3V Level Shifting











SYNC_MASTER=YUAN.MA SYNC_DATE=05/28/2008

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

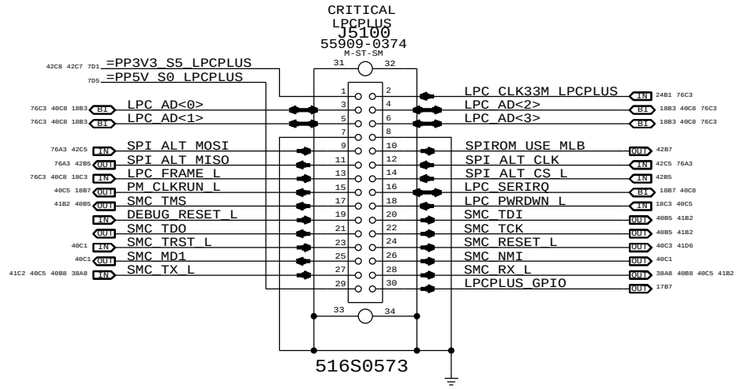
REVISION: C.0.0

BRANCH:

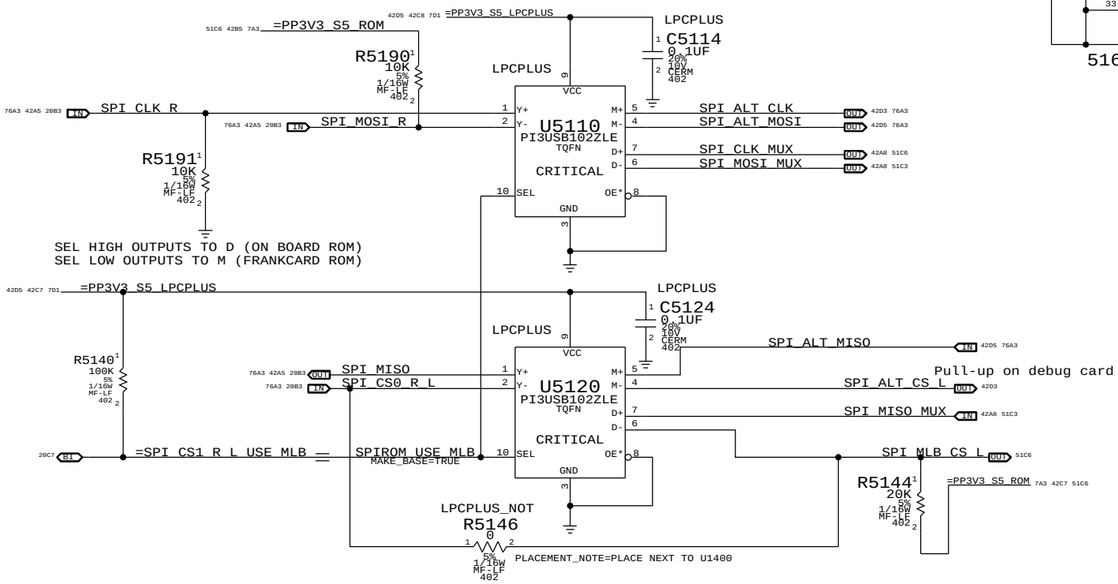
PAGE: 50 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

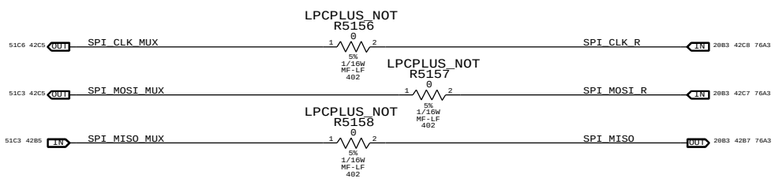
LPC+SPI Connector



Alternate SPI ROM Support



SPI MUX BYPASS



SYNC_MASTER=CHANGZHANG SYNC_DATE=05/09/2008

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

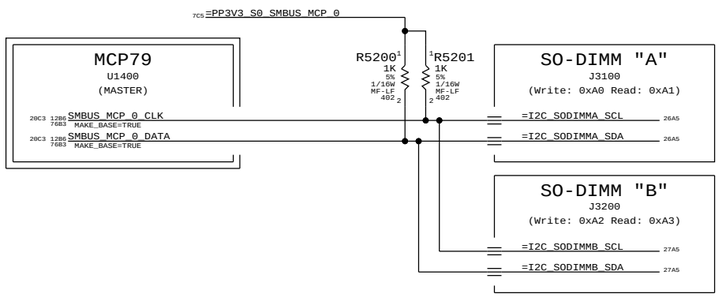
REVISION: C.0.0

BRANCH:

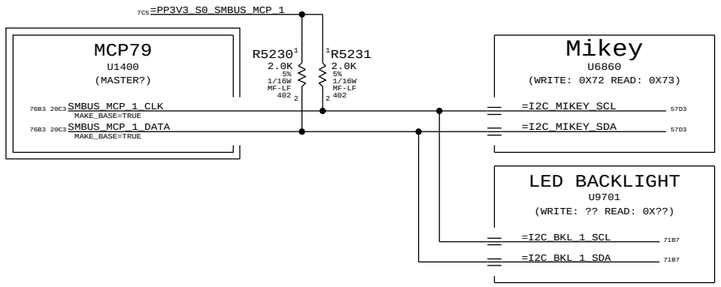
PAGE: 51 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

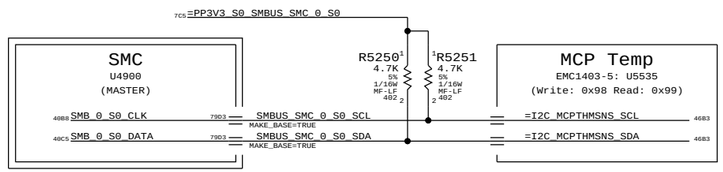
MCP79 SMBUS "0" CONNECTIONS



MCP79 SMBUS "1" CONNECTIONS

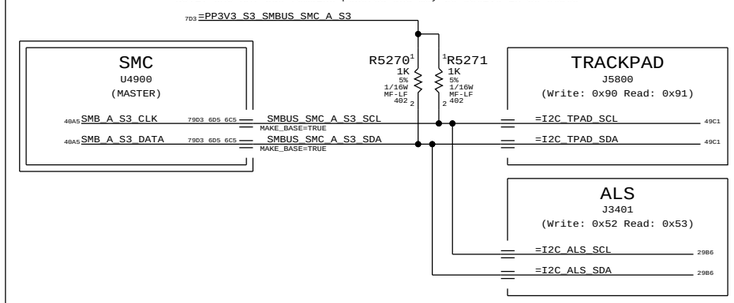


SMC "0" SMBus Connections

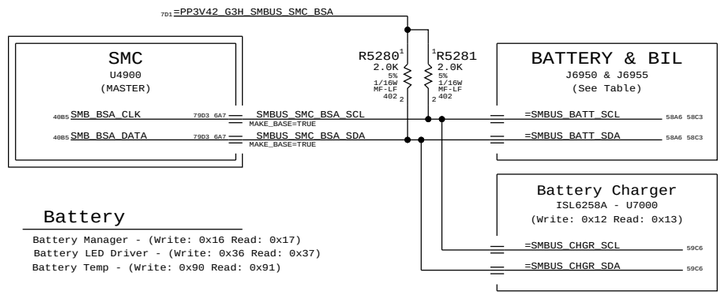


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



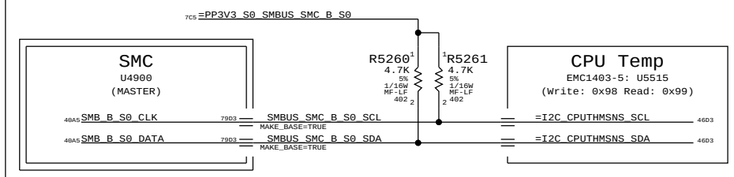
SMC "Battery A" SMBus Connections



Battery

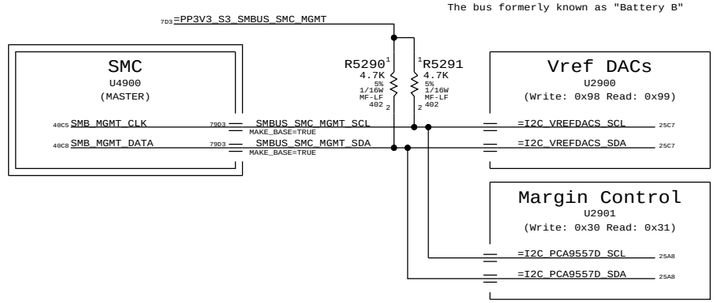
Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "B" SMBus Connections



SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



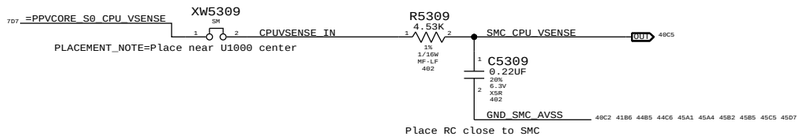
SYNC MASTER=BEN SYNC DATE=04/21/2008

PAGE TITLE: K24 SMBUS CONNECTIONS

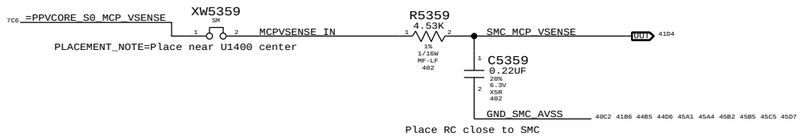
Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 52 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

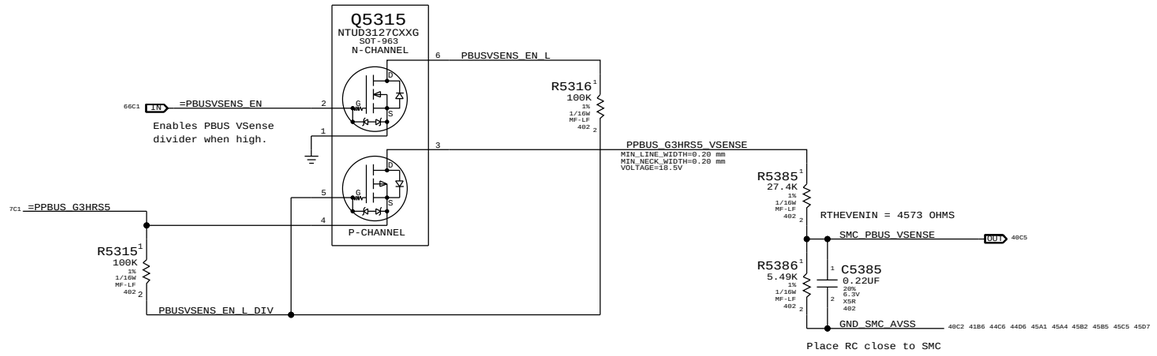
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER



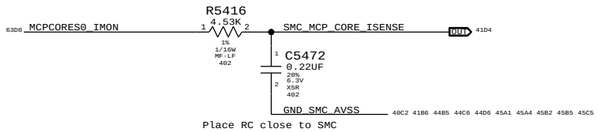
SYNC MASTER=YUNWU SYNC DATE=02/04/2008

PAGE TITLE: VOLTAGE SENSING

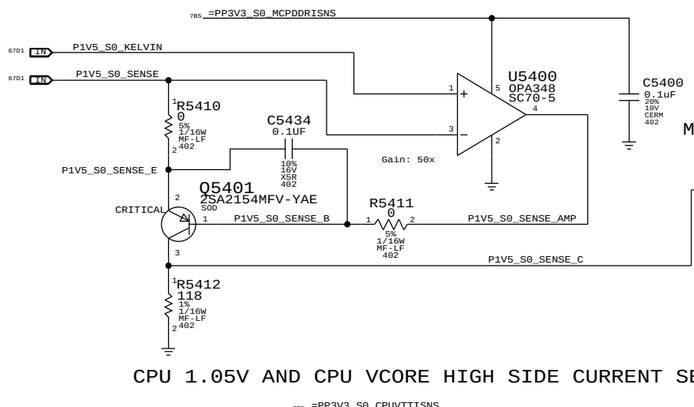
Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 53 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

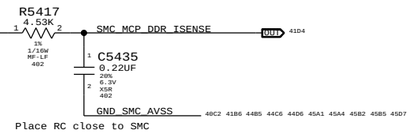
MCP VCore Current Sense Filter



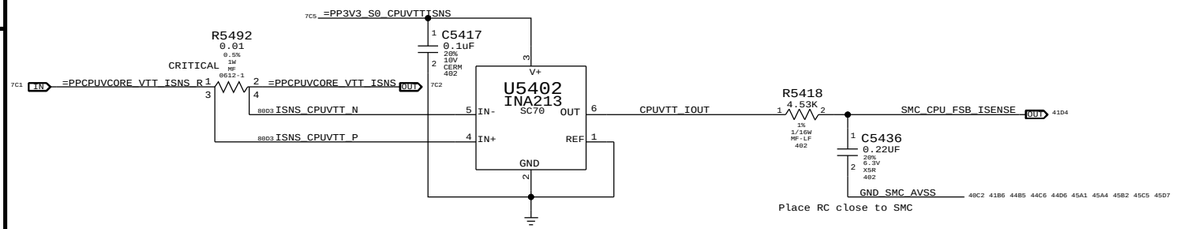
MCP MEM VDD Current Sense



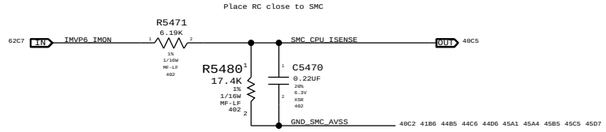
MCP MEM VDD Current Sense Filter



CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE

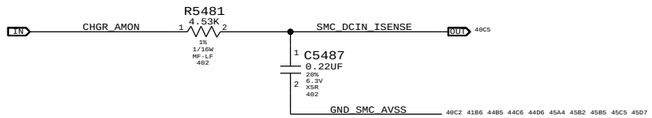


CPU VCore Load Side Current Sense / Filter



BMON CURRENT SENSE

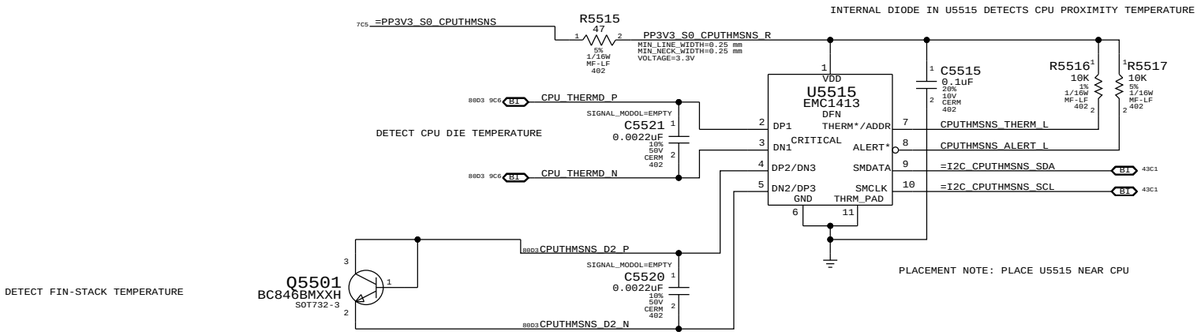
DC-IN (AMON) CURRENT SENSE



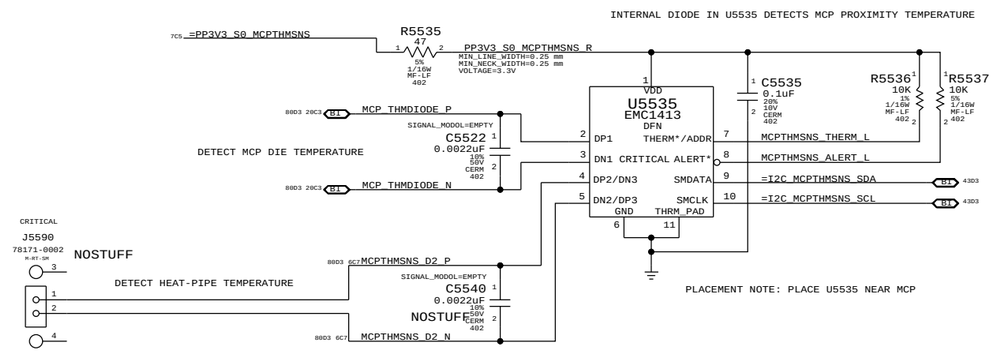
PLACE U5413, R5423, R5431, C5459 NEAR SMC (U4900)

SYNC_MASTER=YUNWU	SYNC_DATE=12/17/2008
PAGE TITLE: Current Sensing	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 54 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



REPLACED 518S0521 WITH 518S0519

SYNC_MASTER=YUNWU SYNC_DATE=03/20/2008

PAGE TITLE: Thermal Sensors

Apple Inc.

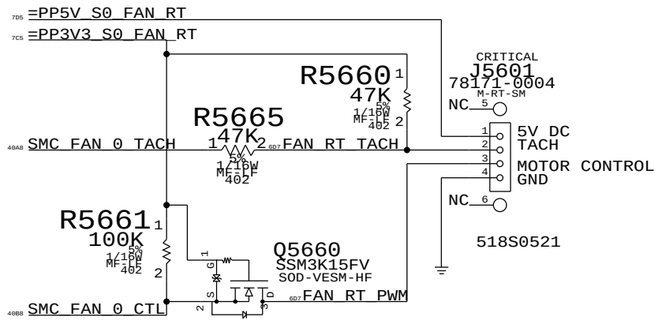
DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 55 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=CHANGZHANG SYNC_DATE=01/18/2008

PAGE TITLE

Fan

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

BRANCH

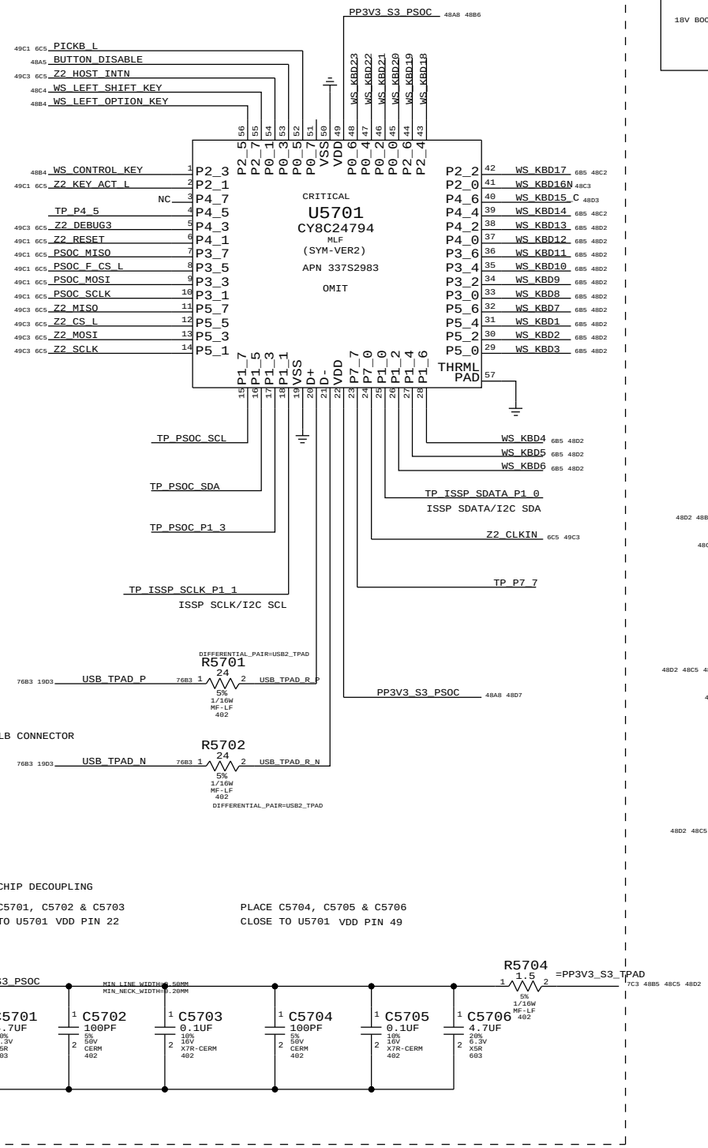
PAGE 56 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

TRACKPAD PICK BUTTONS
KEYBOARD SCANNER



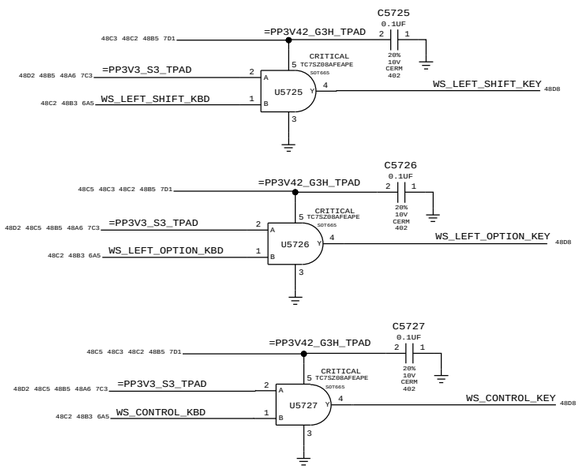
U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

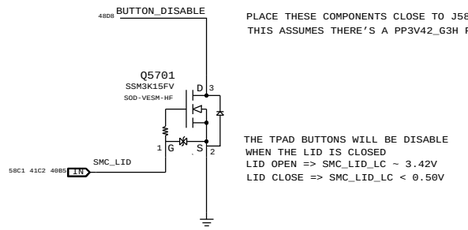
PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

ISOLATION CIRCUIT



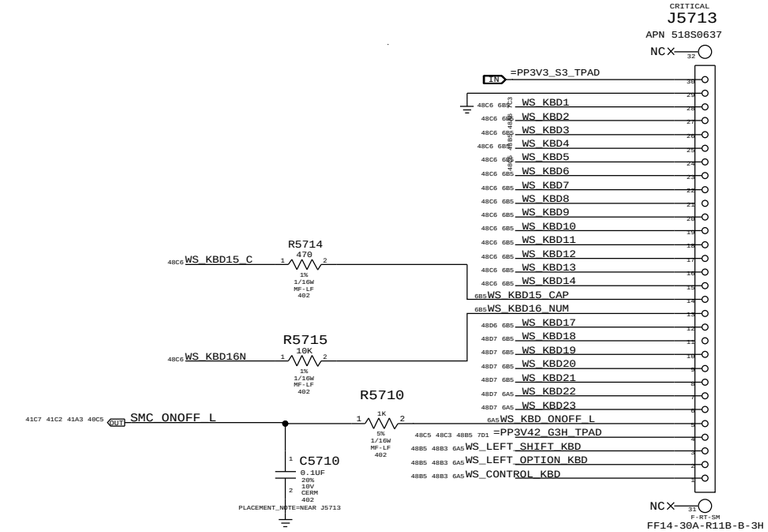
TPAD BUTTONS DISABLE



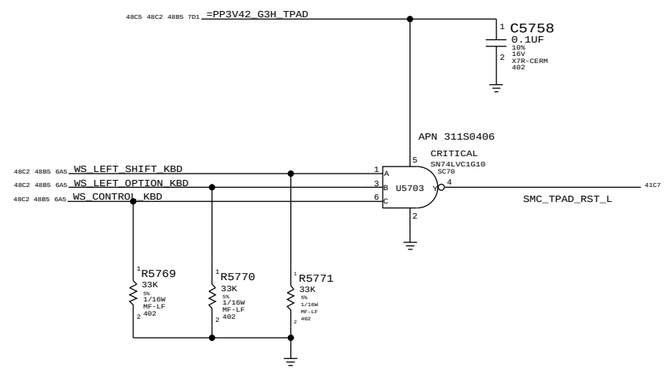
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0406	311S0447		ALL	NXP PART AS ALTERNATE

SYNC_MASTER=YUAN.MA SYNC_DATE=04/22/2008

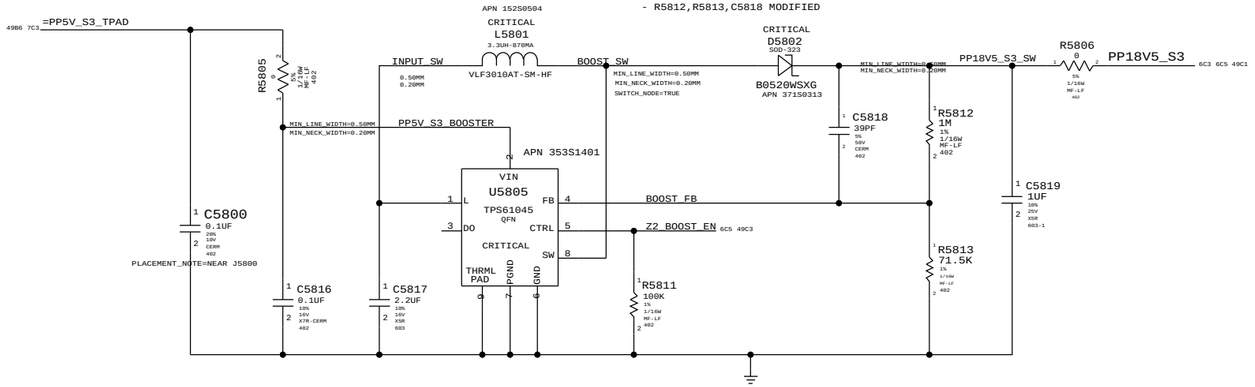
PAGE TITLE: WELLSPRING 1

Apple Inc.

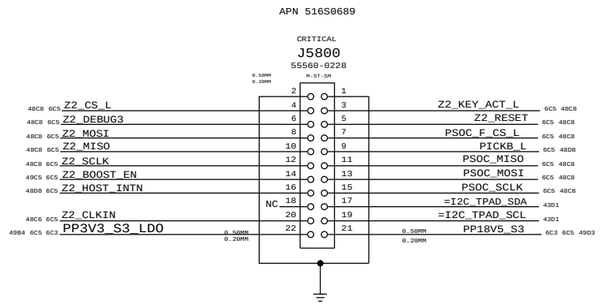
DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 57 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

BOOSTER +18.5VDC FOR SENSORS

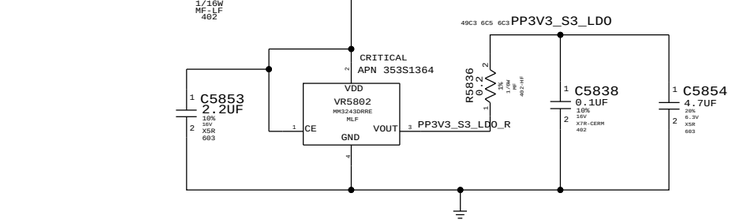
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD

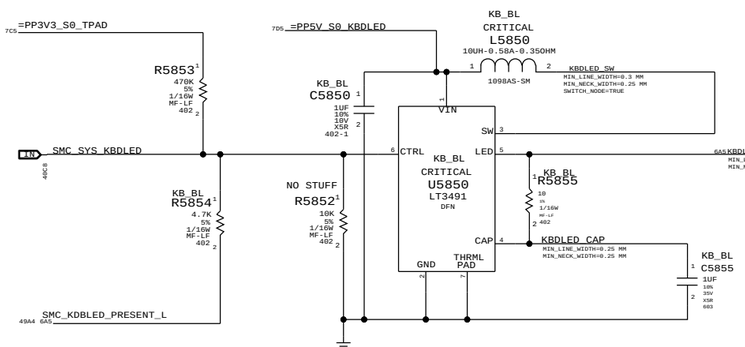


KEYBOARD BACKLIGHT DRIVNG AND DETECTION

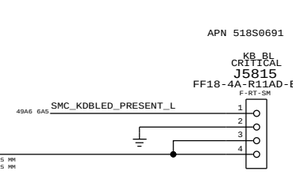
To detect Keyboard backlight, SMC will
tristate SMC_SYS_KBDLED:
LOW = keyboard backlight present
HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES
TURNED ON FOR BEST MLB CONFIG

R5853 ALWAYS PRESENT



APN 518S0691
J5815 pin 1 is grounded on keyboard backlight flex

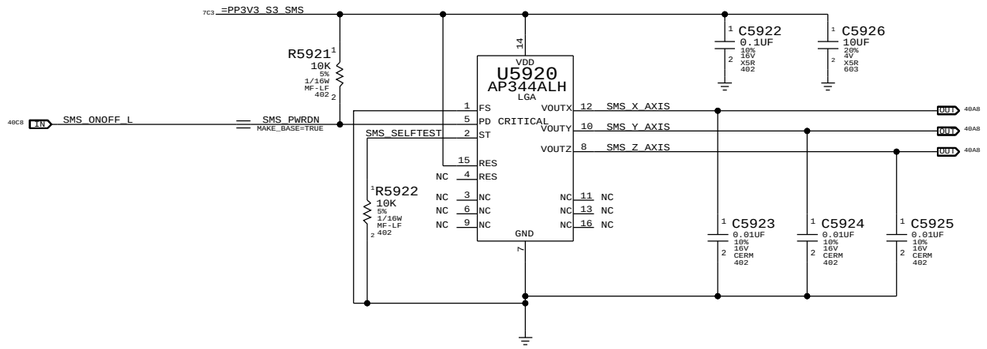


KBD BACKLIGHT CONNECTOR

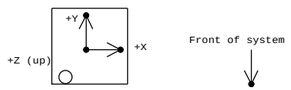
SYNC_MASTER=YUAN.MA	SYNC_DATE=05/09/2008
PAGE TITLE: WELLSPRING 2	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 58 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC

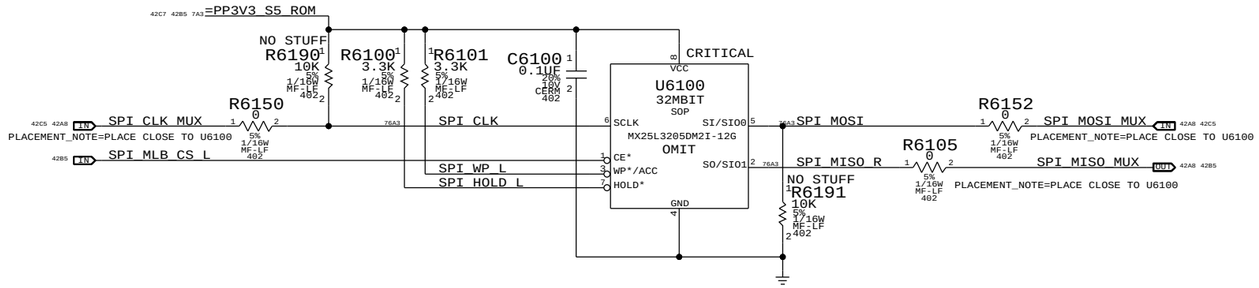


Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

SYNC_MASTER=YUNWU	SYNC_DATE=06/26/2008
PAGE TITLE: SMS	
Apple Inc.	DRAWING NUMBER 051-7898 · SIZE D · REVISION C.0.0 · BRANCH · PAGE 59 OF 109 · SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

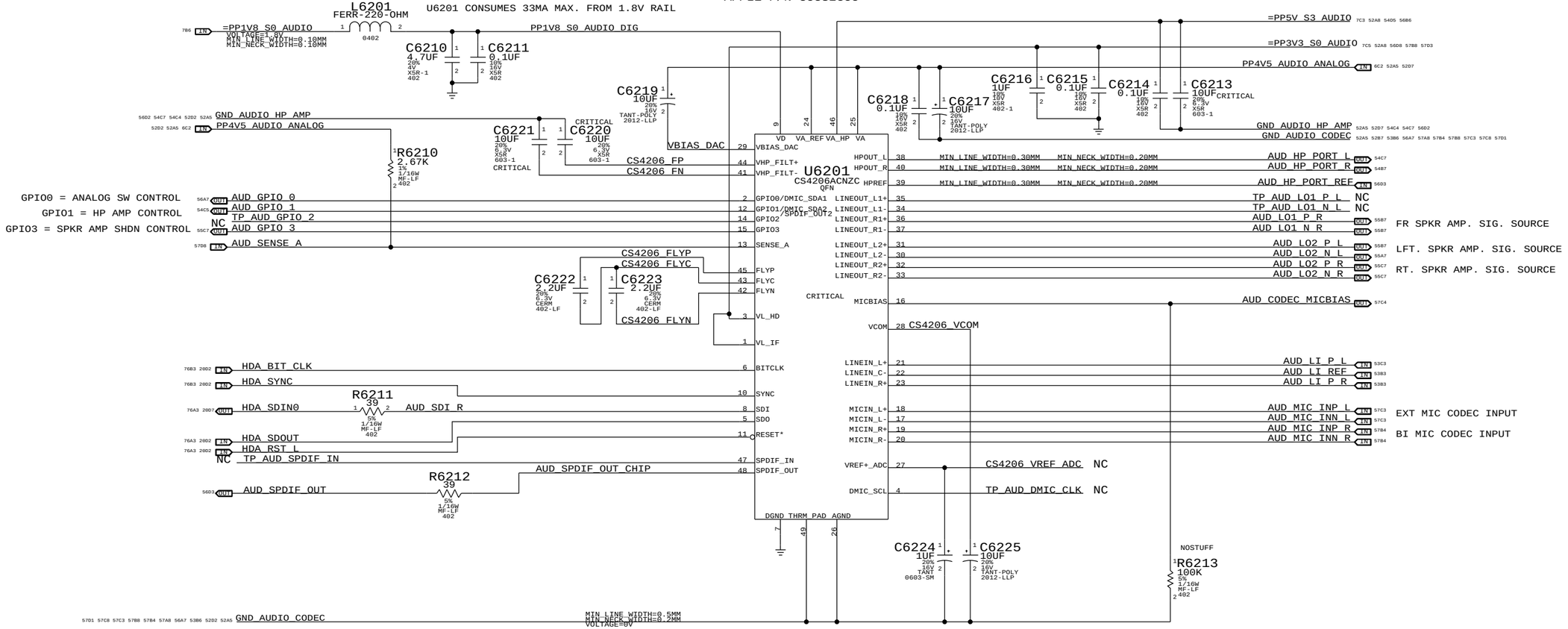
SYNC_MASTER=CHANGZHANG SYNC_DATE=05/02/2008

PAGE TITLE: SPI ROM

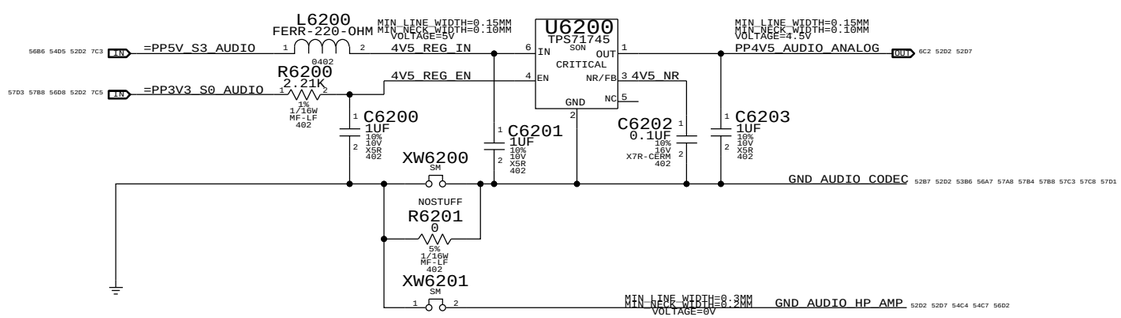
Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 61 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

AUDIO CODEC
APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=AUDIO SYNC_DATE=03/04/2009

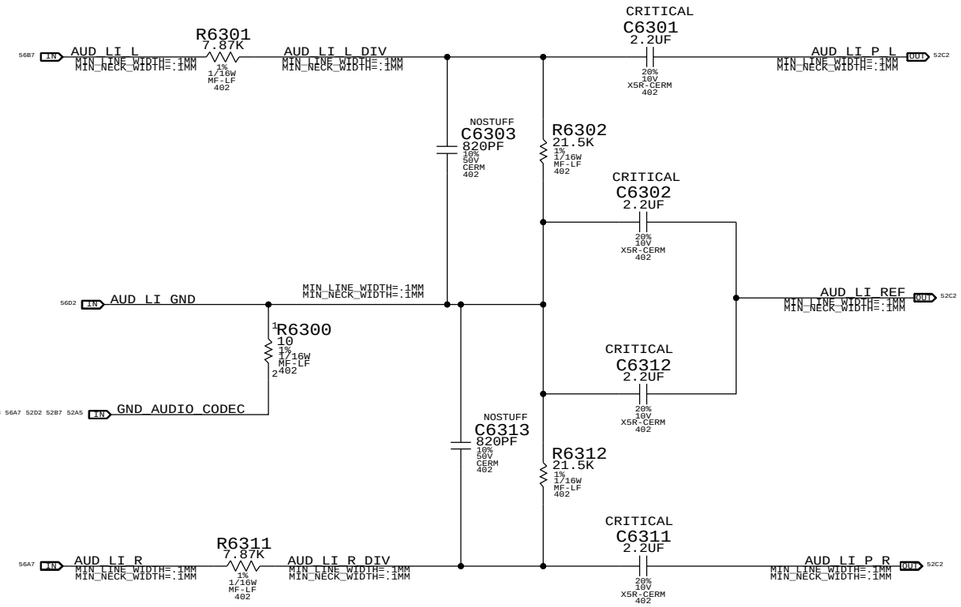
PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 62 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS

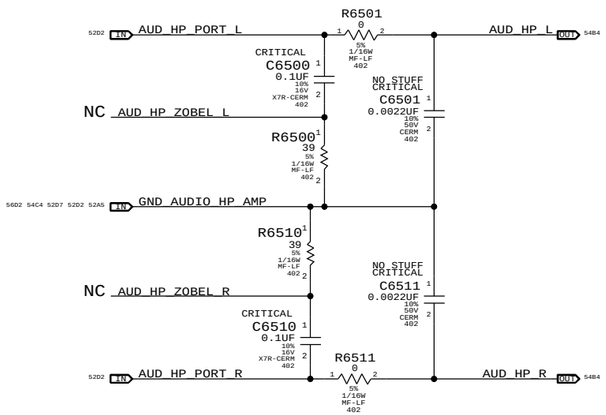


SYNC_MASTER=AUDIO SYNC_DATE=01/31/2009
PAGE TITLE
AUDIO: LINE INPUT FILTER

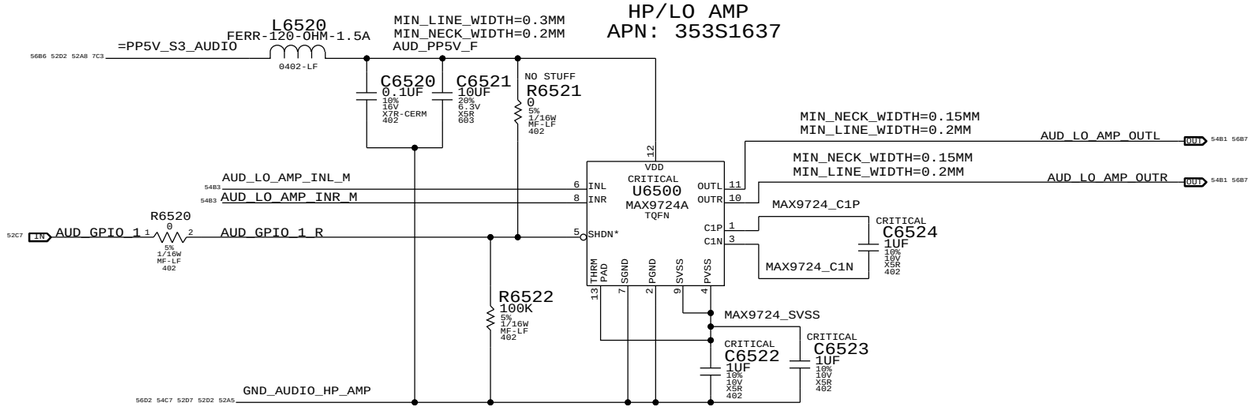
Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 63 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

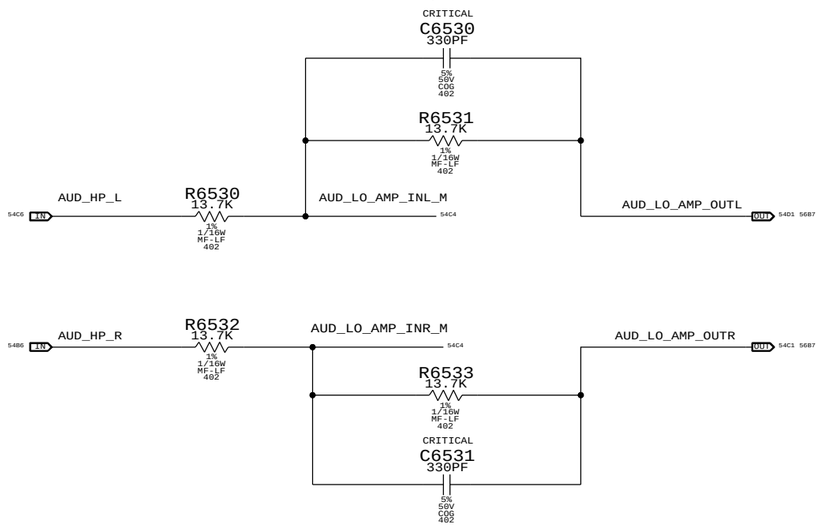
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL
RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).



MAX9724 GAIN/FILTER COMPONENTS
AV_PB = -1V/V, FC_LPF = 35.2KHZ



SYNC_MASTER=AUDIO SYNC_DATE=02/03/2009

PAGE TITLE
AUDIO: HEADPHONE FILTER

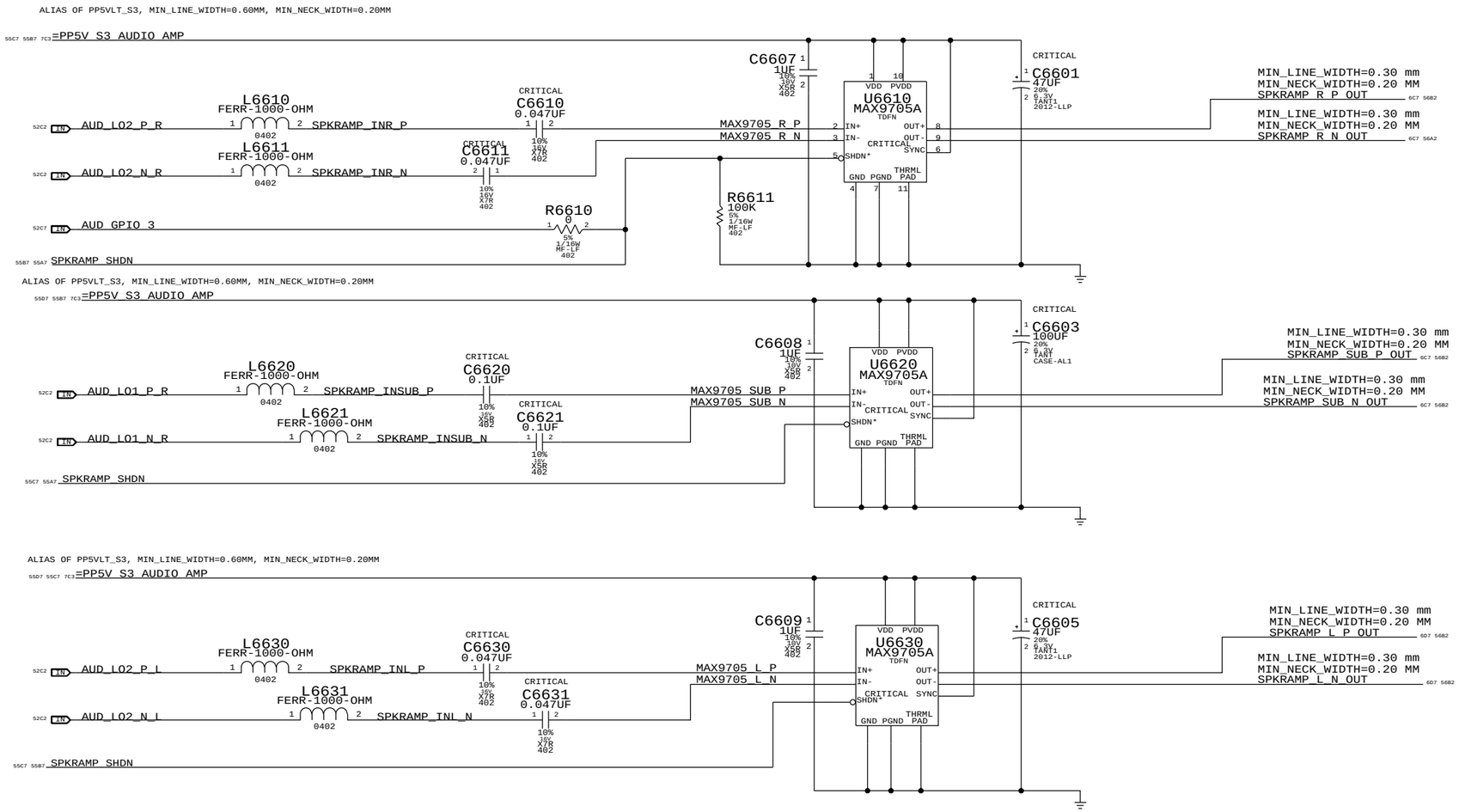
Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 65 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

SATELLITE & SUB TWEETER AMPLIFIER

APN:353S2524

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC_MASTER=AUDIO SYNC_DATE=12/18/2008

PAGE TITLE

AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER	051-7898
SIZE	D
REVISION	C.0.0
BRANCH	
PAGE	66 OF 109
SHEET	<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX

=PP3V3_S0_AUDIO

APN:514-0671
J6700
SPDIF-TXRX-K24
F-RT-TH
CRITICAL
MIC 6
DETECT 5
SWITCH 2
LEFT 1
RIGHT 3
GND 4
AUDIO

A - VIN 7
B - VCC 8
C - GND 9
OPERATING VOLTAGE 3.3
POF

SHELL 10 11 12 13
SHIELD PINS

C6700 1UF 10% 6.3V CERM 402

AUD_CONNJ1_MIC
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
AUD_CONNJ1_SLEEVE
AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_TIPDET
AUD_CONNJ1_TIP
AUD_CONNJ1_RING

AUD_SPDIF_OUT

L6701 FERR-1000-OHM 0402 — HS_MIC_HI
L6702 FERR-1000-OHM 0402 — HS_MIC_LO
L6706 CRITICAL FERR-220-OHM 0402 — AUD_HP_PORT_REF
L6703 CRITICAL FERR-120-OHM-1.5A 0402-LF — AUD_CONN_GND
L6704 CRITICAL FERR-220-OHM 0402 — AUD_CONN_L
L6705 CRITICAL FERR-220-OHM 0402 — AUD_CONN_R
R6700 10K 5% 1/10W MF-LF 402 — AUD_J1_SLEEVEDET_R
R6701 4.7 5% 1/10W MF-LF 402 — AUD_J1_TIPDET_R

DZ6701 CRITICAL 6.8V-100PF 402
DZ6704 CRITICAL 6.8V-100PF 402
DZ6705 CRITICAL 6.8V-100PF 402
DZ6703 CRITICAL 6.8V-100PF 402
DZ6700 CRITICAL 6.8V-100PF 402

C6701 100PF 5% 50V CERM 402

XW6700 SM GND_AUDIO_HP_AMP
XW6701 SM AUD_LI_GND
AUD_CONN_GND

GND_CHASSIS_AUDIO_JACK
CHASSIS_GND_STITCHES
XW6710 SM
XW6711 SM
R6760 0 5% 1/10W MF-LF 402

NOSTUFF R6723 0 5% 1/10W MF-LF 402
NOSTUFF R6722 0 5% 1/10W MF-LF 402
NOSTUFF R6725 0 5% 1/10W MF-LF 402
=PP3V42_G3H_AUDIO

R6724 0 5% 1/10W MF-LF 402
=PP5V_S3_AUDIO
PP_MAX14504_VCC

C6710 1UF 10% 10V X5R 402
NOSTUFF R6726 0 5% 1/10W MF-LF 402

APN: 353S2536

U6700 MAX14504 WLP CRITICAL
VCC A3
C4 NC1
C1 NC2
A4 NO1
A1 NO2
C2 CB
A2 NEG
COM1 B4
COM2 B1
EN* B2
GND B3 C3
SWITCH_CP

AUD_LO_AMP_OUTL — R6716 0 5% 1/10W MF-LF 402 — AUD_LO_AMP_OUTL_SWITCH
AUD_LO_AMP_OUTR — R6717 0 5% 1/10W MF-LF 402 — AUD_LO_AMP_OUTR_SWITCH
AUD_LI_L — R6718 0 5% 1/10W MF-LF 402 — AUD_LI_L_SWITCH
AUD_LI_R — R6719 0 5% 1/10W MF-LF 402 — AUD_LI_R_SWITCH
AUD_GPIO_0 — R6720 0 5% 1/10W MF-LF 402 — AUD_SWITCH_CTRL

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
R6712 24K 5% 1/10W MF-LF 402 — AUD_CONN_L
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
R6713 24K 5% 1/10W MF-LF 402 — AUD_CONN_R

C6711 0.0033UF 10% 50V CERM 402

R6721 100K 5% 1/16W MF-LF 402

AUD_CONN_GND — R6715 0 5% 1/10W MF-LF 402 — AUD_SWITCH_GND

GND STUFFING OPTIONS FOR CMOS SWITCH
GND_AUDIO_CODEC — R6714 0 5% 1/10W MF-LF 402

NOSTUFF R6727 0 5% 1/10W MF-LF 402

ANALOG AUDIO IO SWITCH

GPIO0 = 0 AND GPIO1 = 1 --> HP PATH SELECTED
GPIO0 = 1 AND GPIO1 = 0 --> LI PATH SELECTED

MIC CONNECTOR

APN:518S0520

CRITICAL J6701 78171-0003 M-RT-SM
BI_MIC_LO
BI_MIC_SHIELD
BI_MIC_HI

SPEAKER CONNECTOR

APN:518S0519

CRITICAL J6702 78171-0002 M-RT-SM
SPKRAMP_L_P_OUT
SPKRAMP_L_N_OUT
SPKRAMP_SUB_P_OUT
C6760 33PF 5% 50V CERM 402
C6761 33PF 5% 50V CERM 402
SPKRAMP_SUB_N_OUT
SPKRAMP_R_P_OUT
C6762 33PF 5% 50V CERM 402
C6763 33PF 5% 50V CERM 402
SPKRAMP_R_N_OUT

CRITICAL J6703 78171-0004 M-RT-SM

APN:518S0521

C6760 - C6763 ARE FOR FILTERING POTENTIAL FSB NOISE COUPLED ON SPKR LINES

SYNC_MASTER=AUDIO SYNC_DATE=03/20/2009
PAGE TITLE: AUDIO: JACK
Apple Inc.
DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 67 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

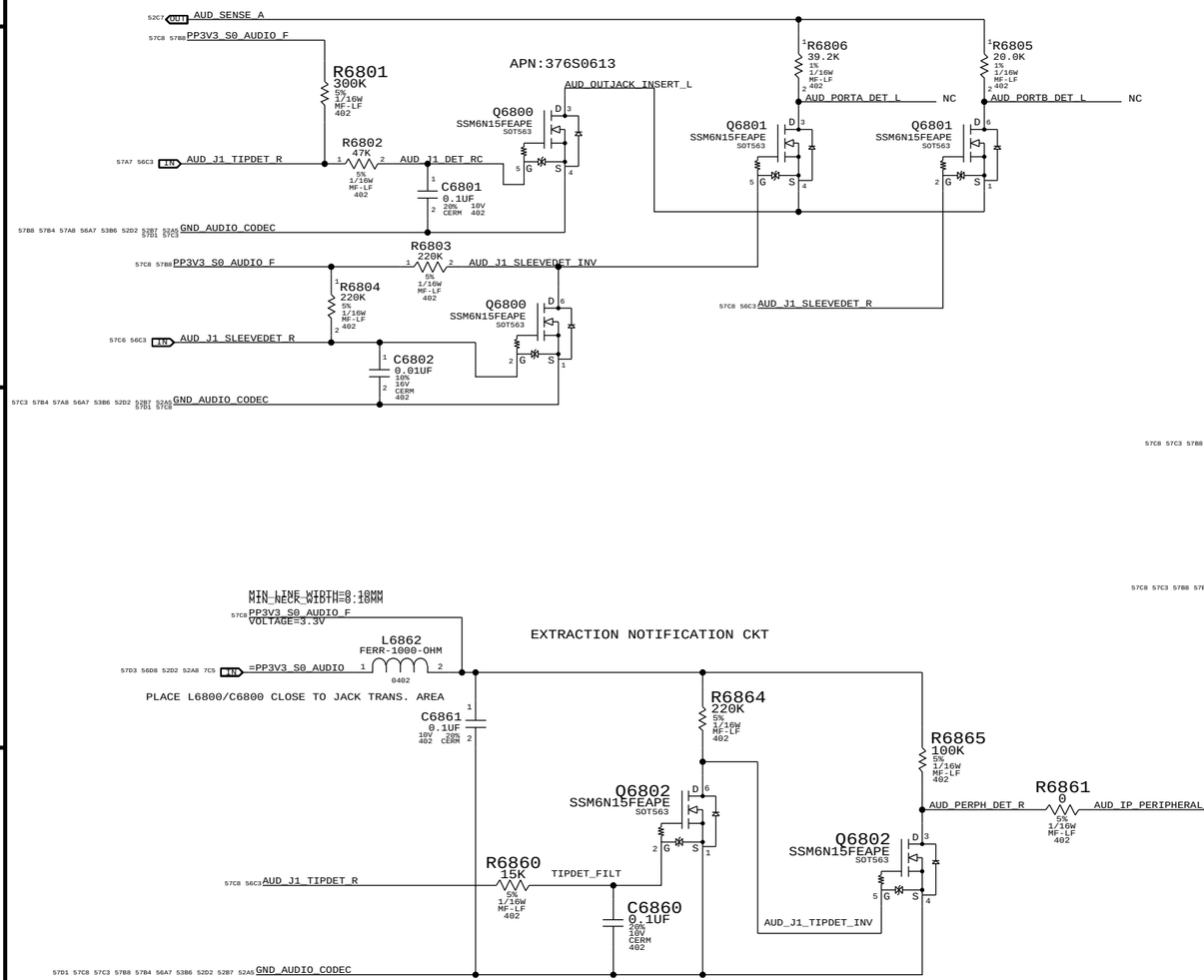
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A)AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

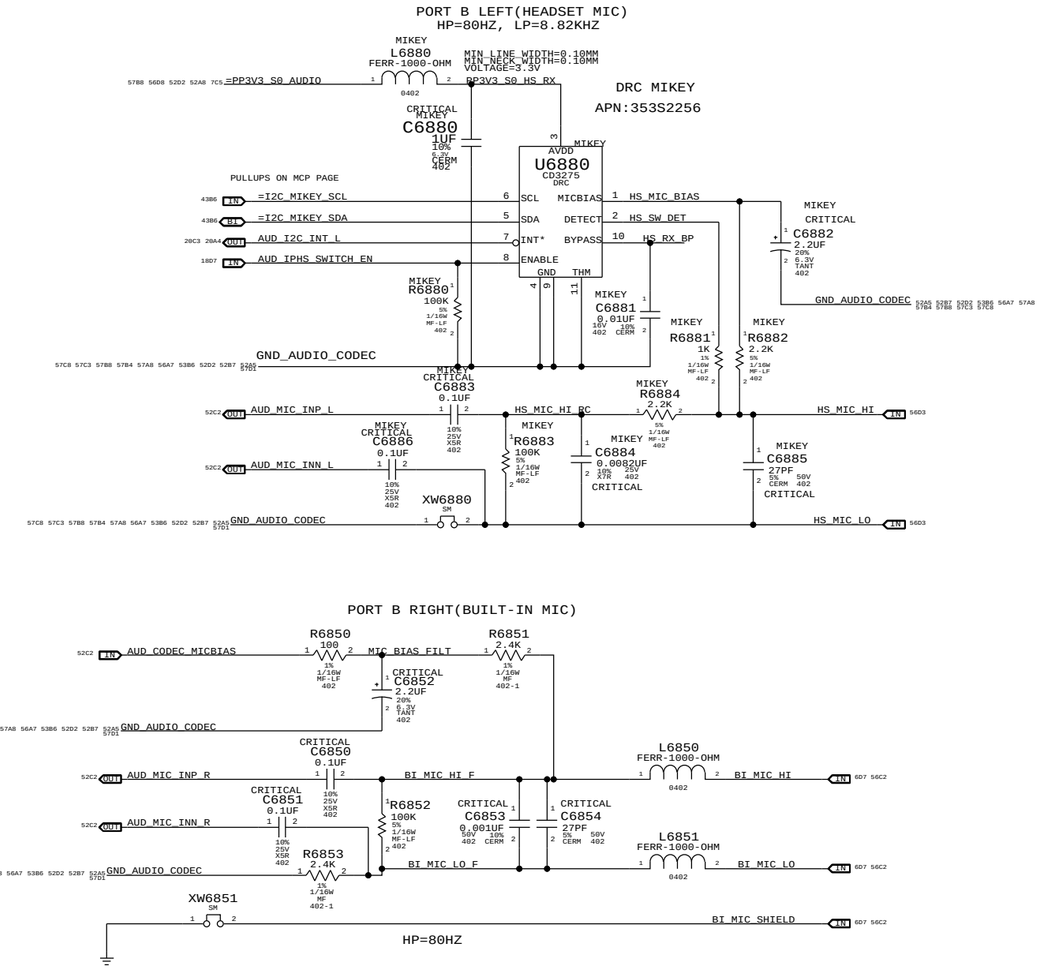
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)



PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ



PORT B RIGHT(BUILT-IN MIC)

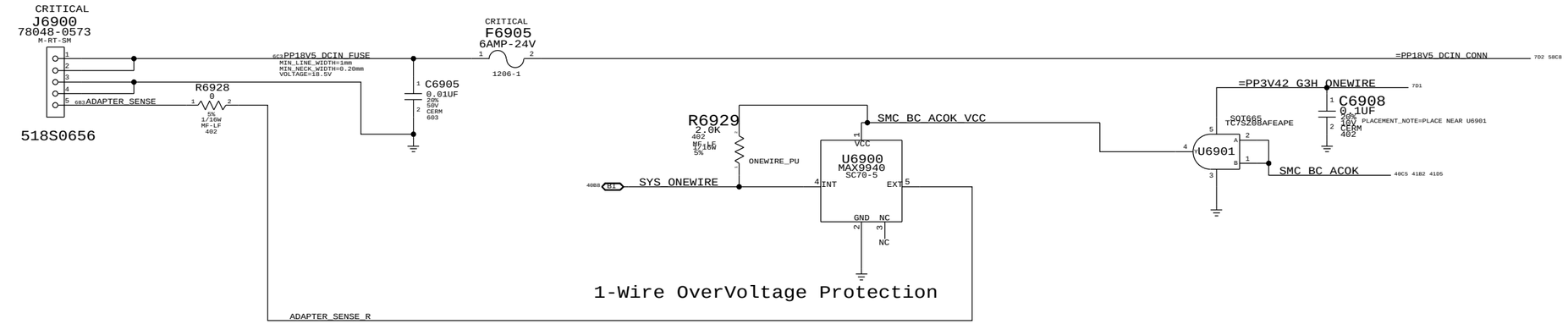
SYNC_MASTER=AUDIO SYNC_DATE=03/20/2009

PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

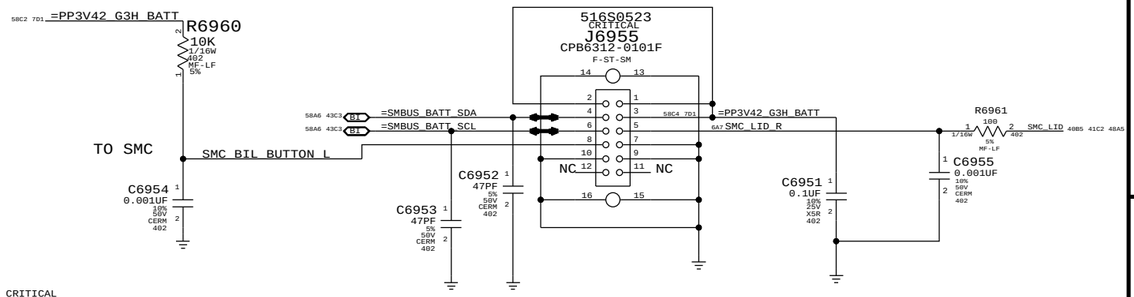
DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 68 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MagSafe DC Power Jack



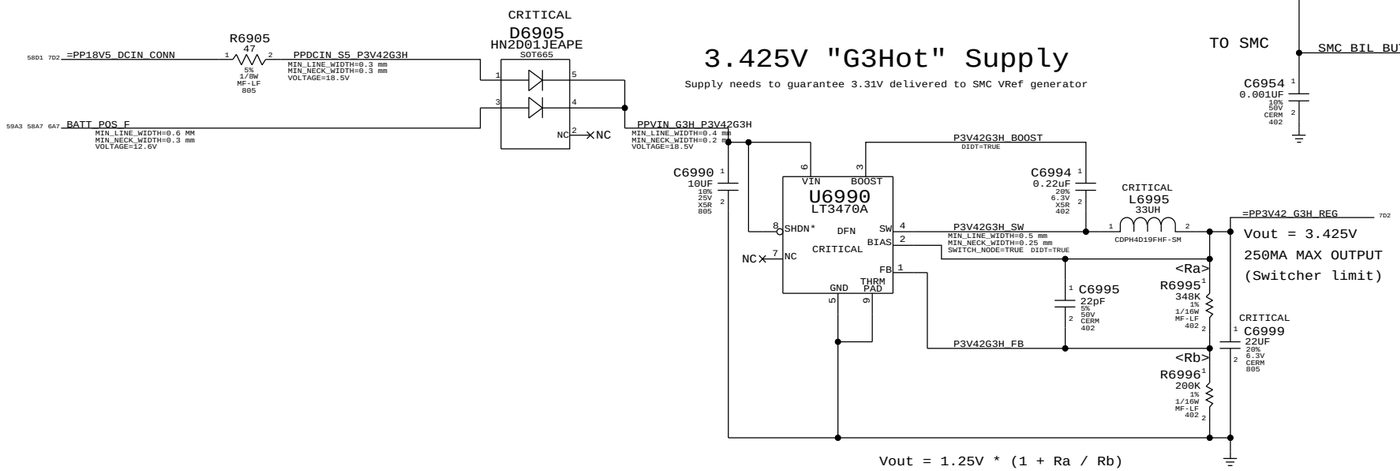
1-Wire OverVoltage Protection

BIL CONNECTOR



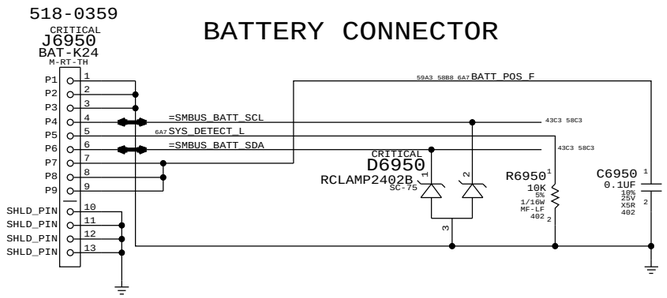
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



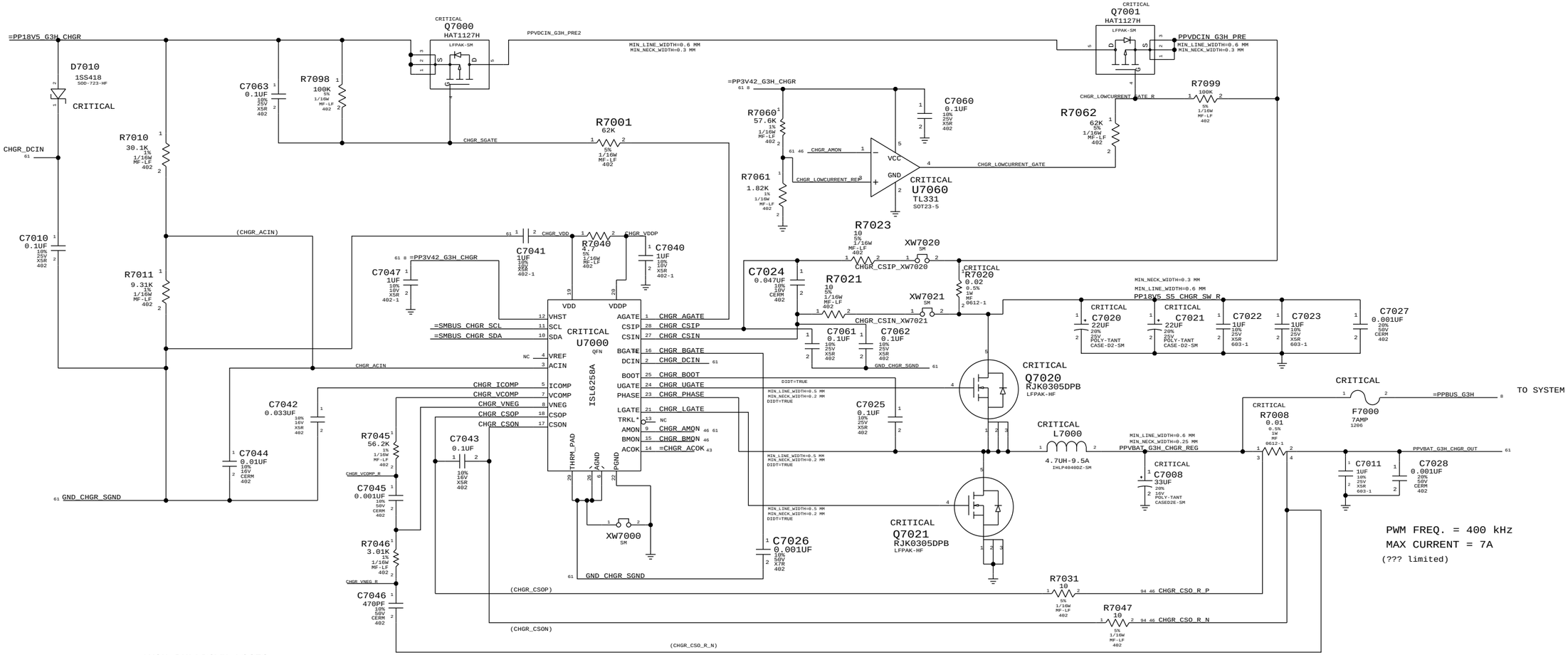
Vout = 1.25V * (1 + Ra / Rb)

BATTERY CONNECTOR

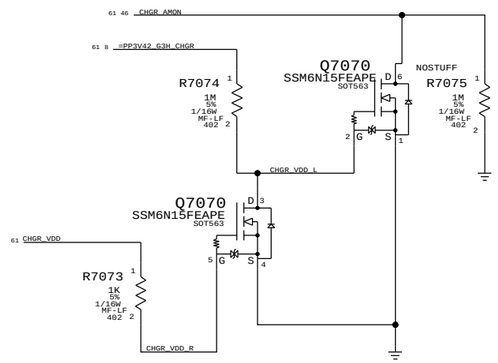


SYNC_MASTER=YUNWU	SYNC_DATE=12/11/2008
PAGE TITLE: DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 69 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

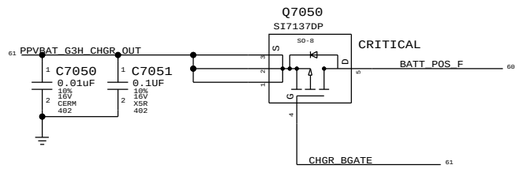
PBUS SUPPLY / BATTERY CHARGER



AMON PULLDOWN LOGIC



BATTERY CHARGE LIMITING FETS



SYNC_MASTER=K24_MLB SYNC_DATE=05/20/2009

PAGE TITLE: PBUS Supply/Battery Charger

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

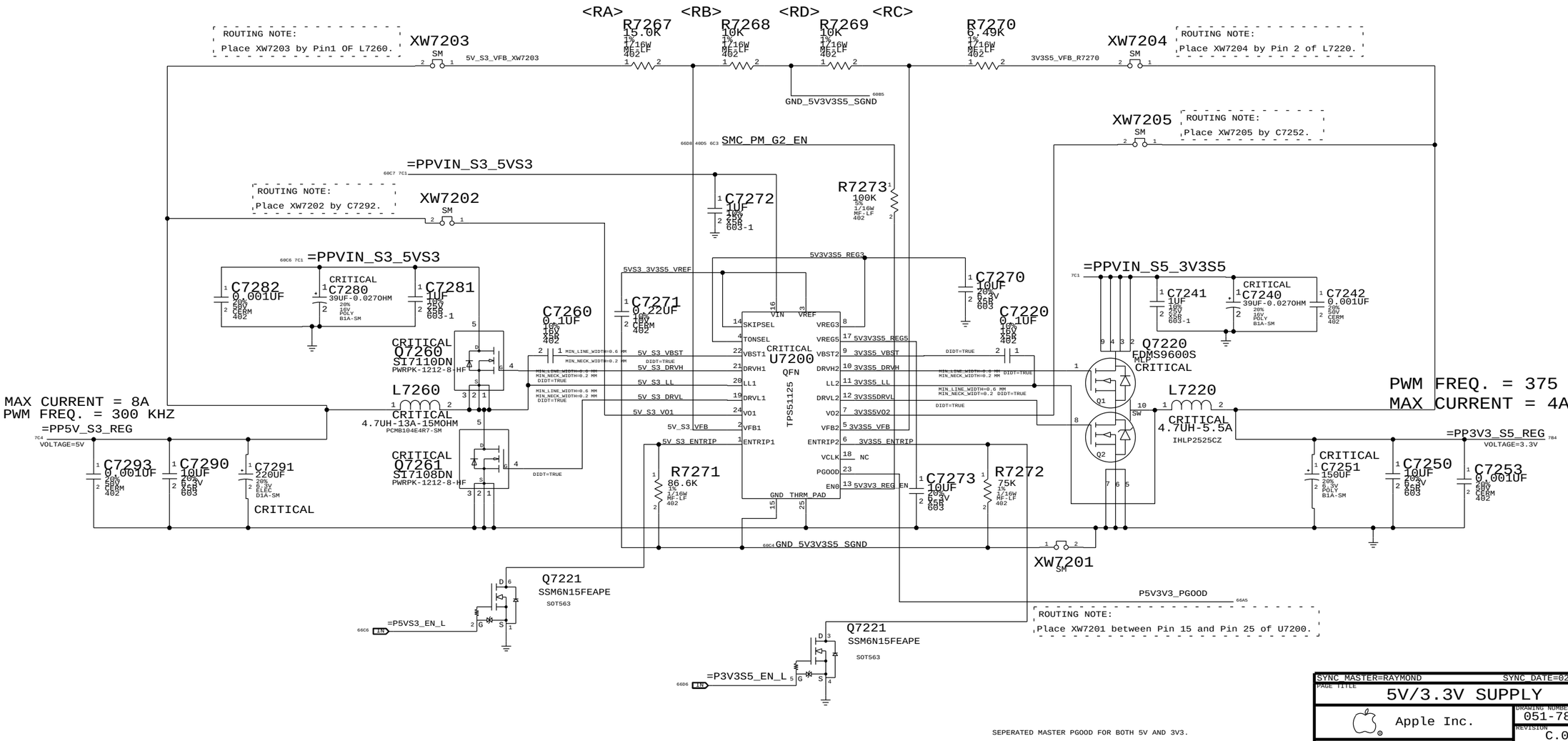
PAGE: 70 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

5V_S3/3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008

PAGE TITLE: 5V/3.3V SUPPLY

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

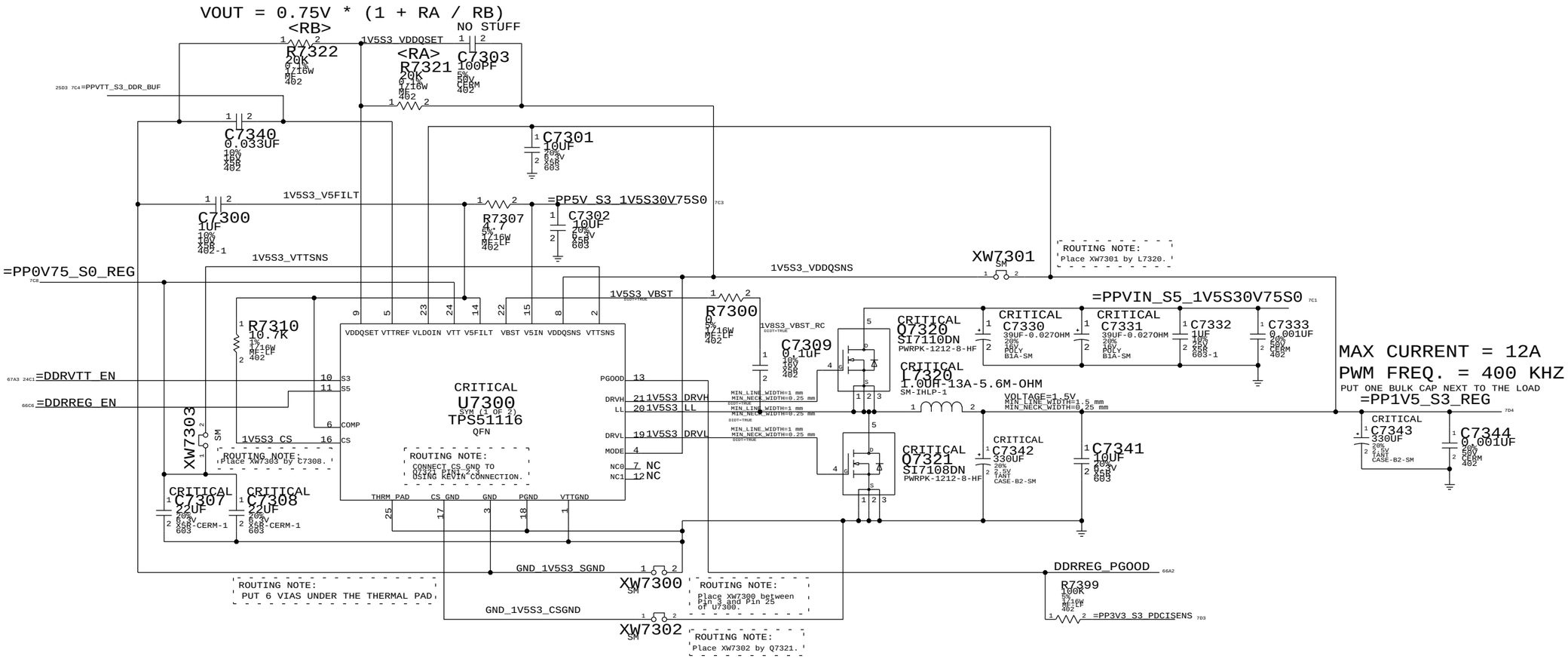
REVISION: C.0.0

BRANCH:

PAGE: 72 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1.5V/0.75V(DDR3) POWER SUPPLY



STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

PAGE TITLE: 1.5V/0.75V DDR3 SUPPLY

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 73 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

IMVP6 CPU VCORE REGULATOR

DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

PWM FREQ. = 300 KHZ
MAX CURRENT = 44A
LOAD LINE SLOPE = -2.1 MV/A

NOTE 1: C7432,C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

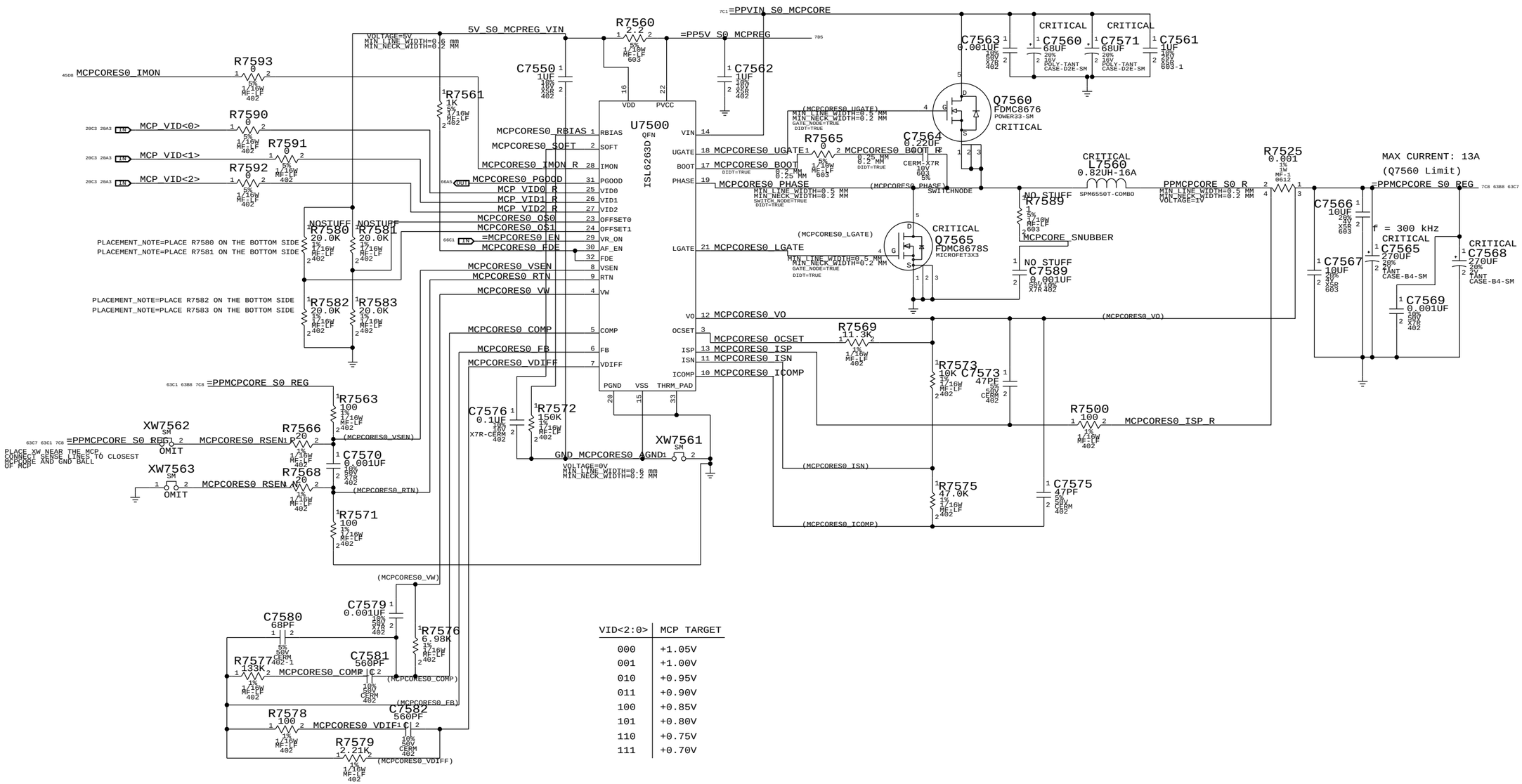
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

SYNC_MASTER=RAYMOND	SYNC_DATE=01/31/2008
PAGE TITLE: IMVP6 CPU VCore Regulator	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH
	PAGE: 74 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP VCORE POWER SUPPLY



VID<2:0>	MCP TARGET
000	+1.05V
001	+1.00V
010	+0.95V
011	+0.90V
100	+0.85V
101	+0.80V
110	+0.75V
111	+0.70V

SYNC_MASTER=K19_MLB SYNC_DATE=12/10/2008

PAGE TITLE: MCP CORE REGULATOR

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

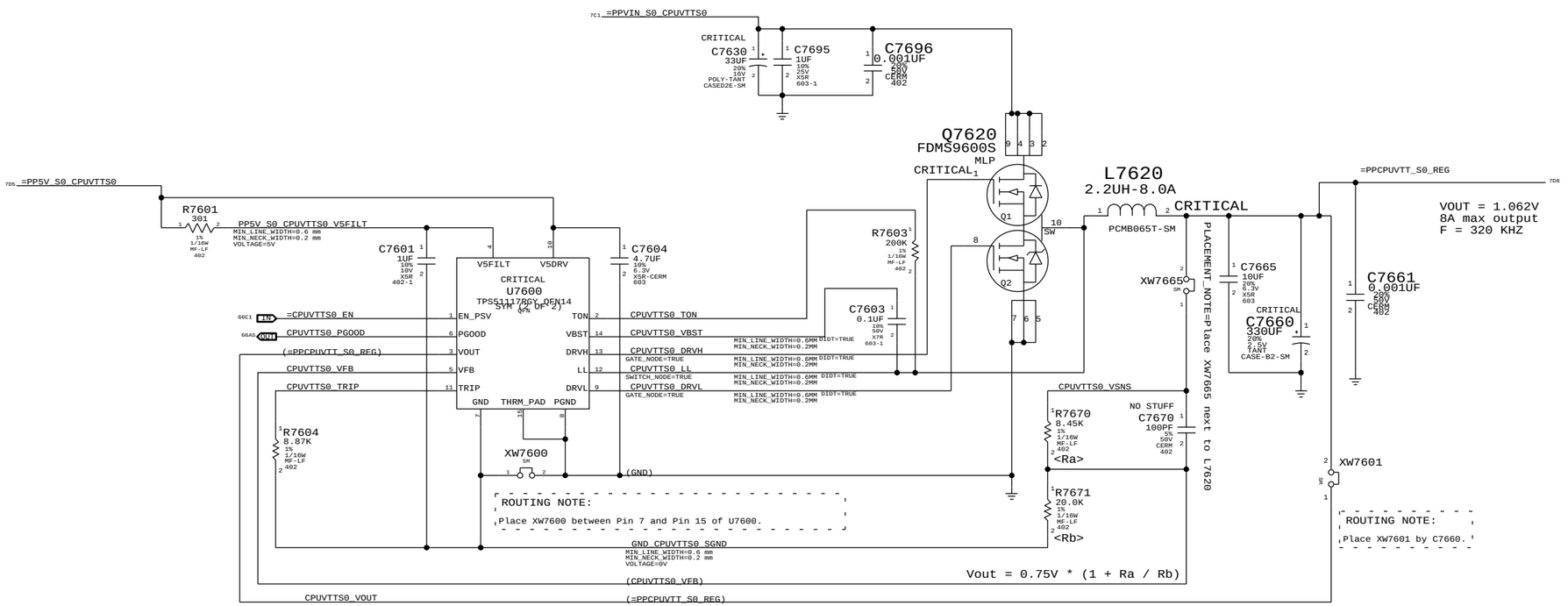
REVISION: C.0.0

BRANCH:

PAGE: 75 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CPUVTT POWER SUPPLY



SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008

PAGE TITLE: CPU VTT(1.05V) SUPPLY

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

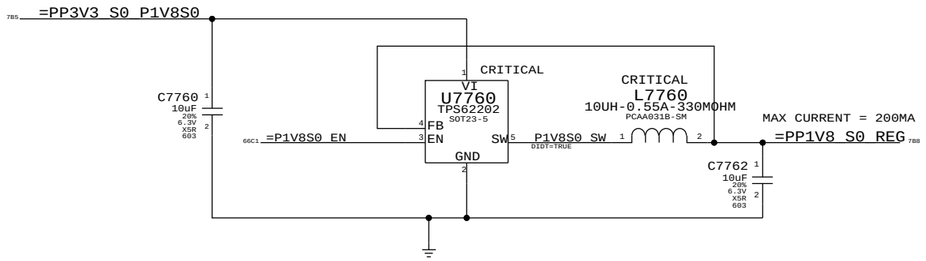
REVISION: C.0.0

BRANCH:

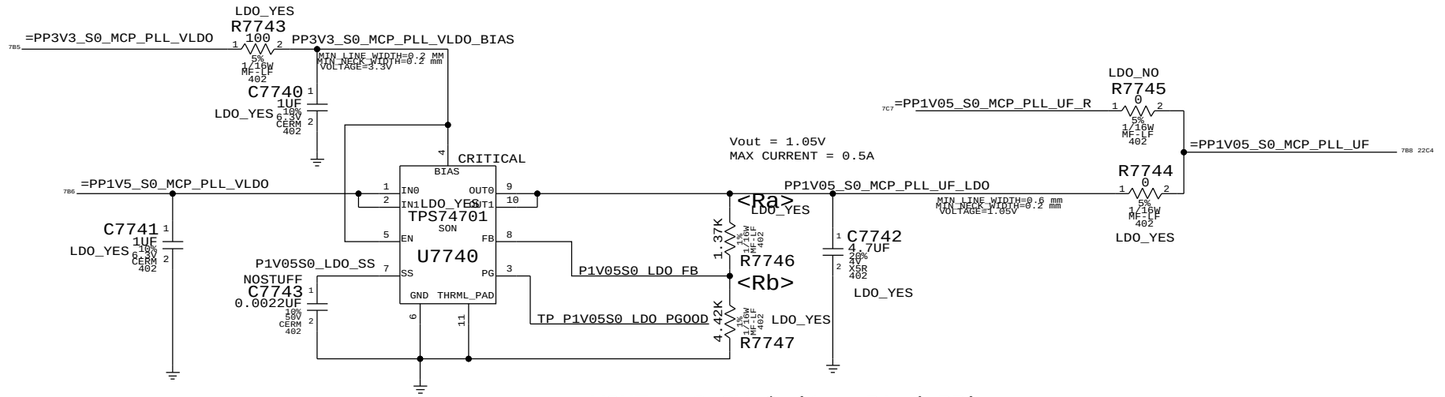
PAGE: 76 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

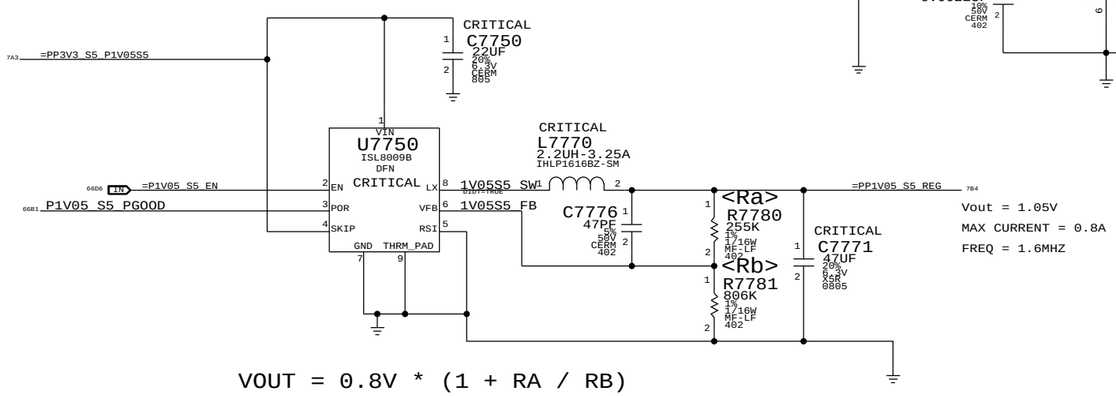
1.8V S0 SWITCHER



1.05V S0 PLL LDO



MCP 1.05V S5 (AUXC) SUPPLY

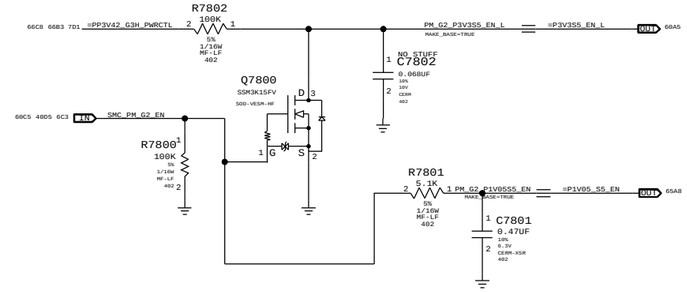


VOUT = 0.8V * (1 + RA / RB)

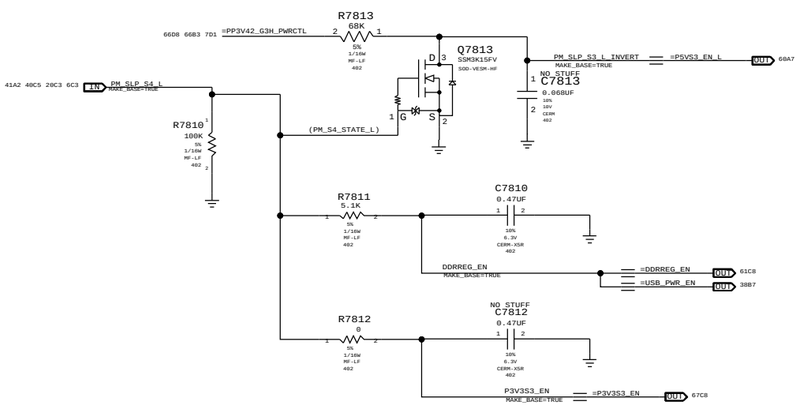
VOUT = 0.8V * (1 + RA / RB)

SYNC_MASTER=RAYMOND	SYNC_DATE=01/23/2008
PAGE TITLE: MISC POWER SUPPLIES	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH:
	PAGE: 77 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

3.3V 1.05V S5 ENABLE

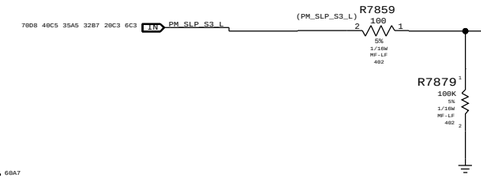


S3 ENABLE

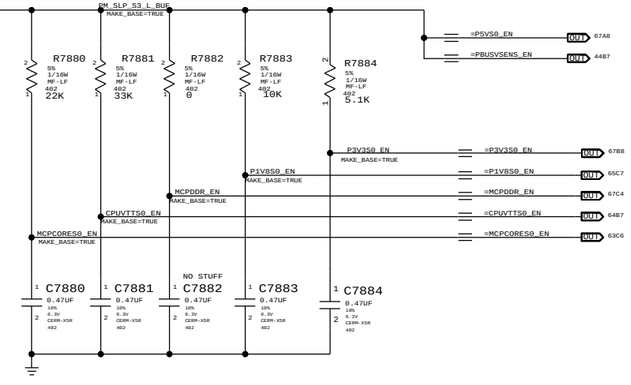


Power Control Signals

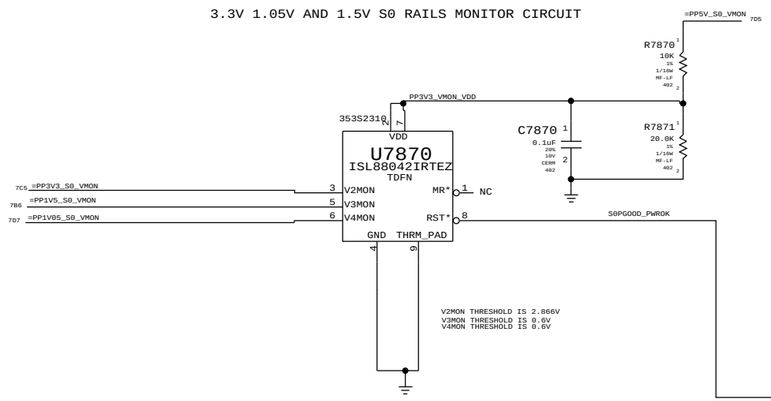
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



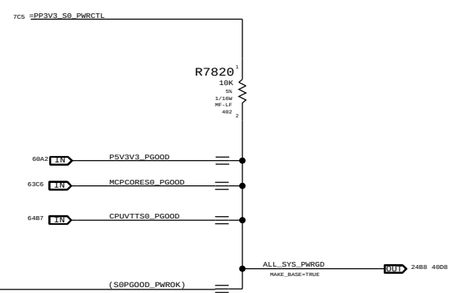
3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT,MCPCORES0 ENABLE
1.5V S0 AND 1.05V S0 ENABLE



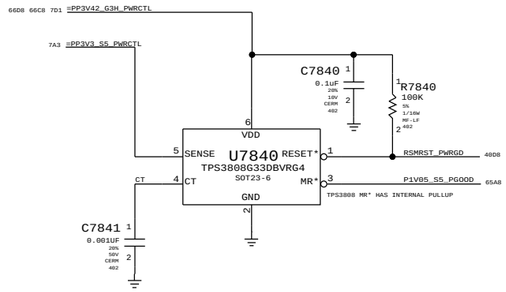
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



OTHER S0 RAILS PGOOD



VOLTAGE MONITOR



Unused PGOOD signal

SYNC_MASTER=YUAN.MA SYNC_DATE=12/11/2008

PAGE TITLE: POWER SEQUENCING

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

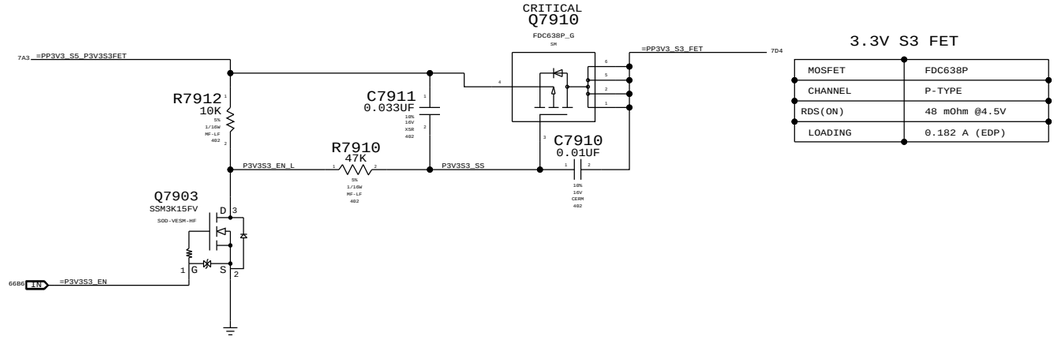
REVISION: C.0.0

BRANCH:

PAGE: 78 OF 109

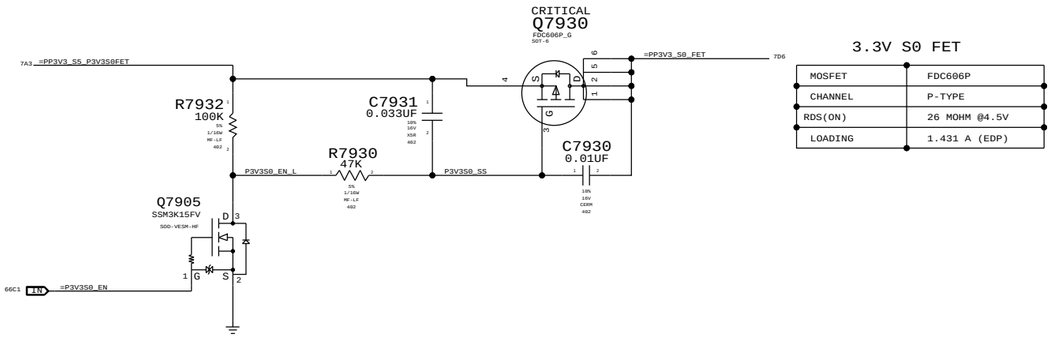
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

3.3V S3 FET



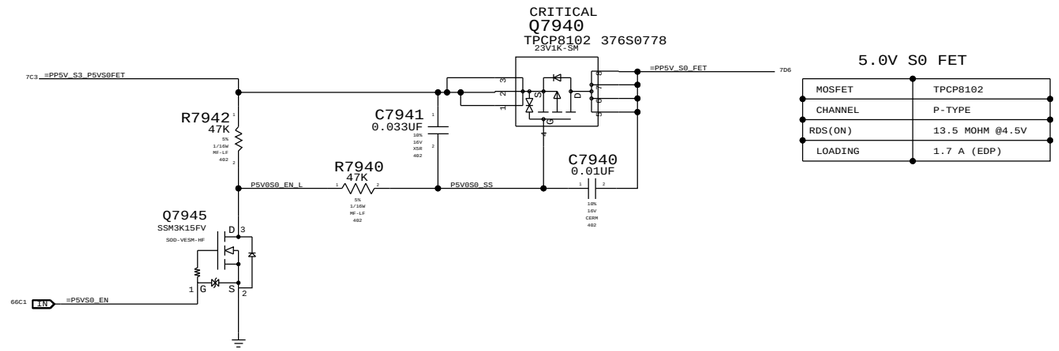
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

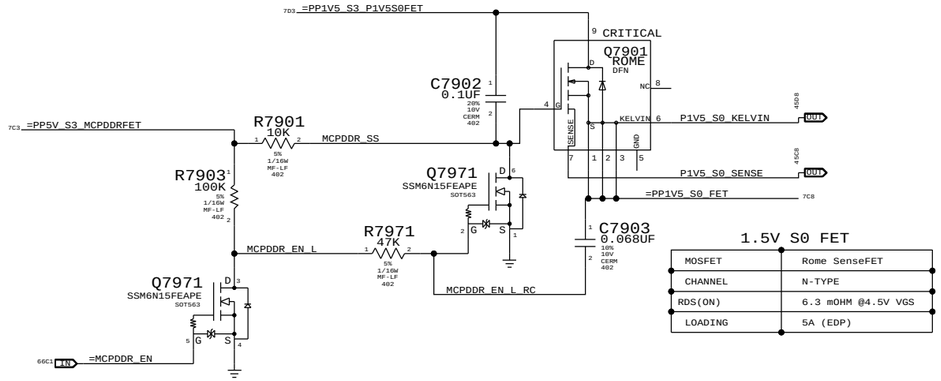
5.0V S0 FET



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.7 A (EDP)

1.5V S0 FET

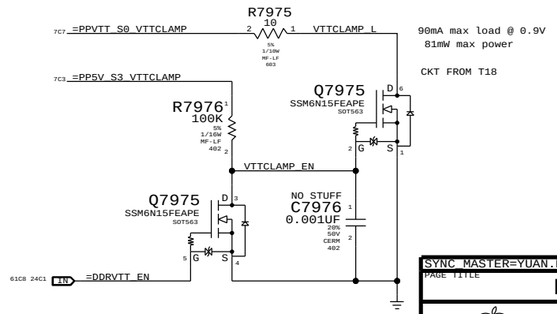
(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)



1.5V S0 FET	
MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOHM @4.5V VGS
LOADING	5A (EDP)

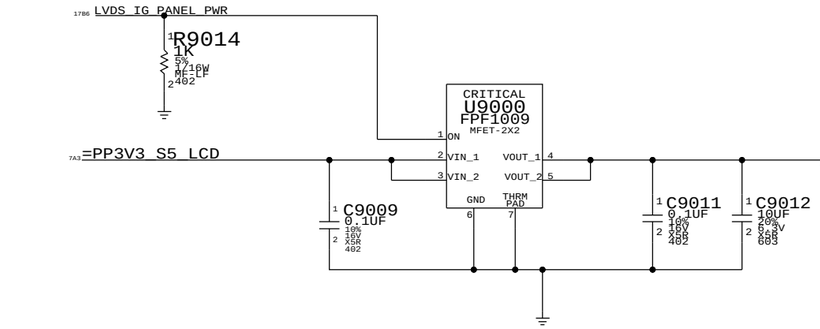
MCP79 DDRVTT FET

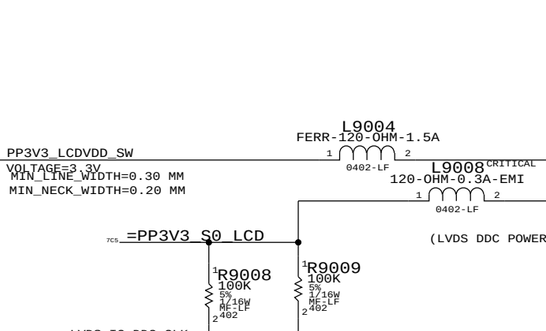
MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.

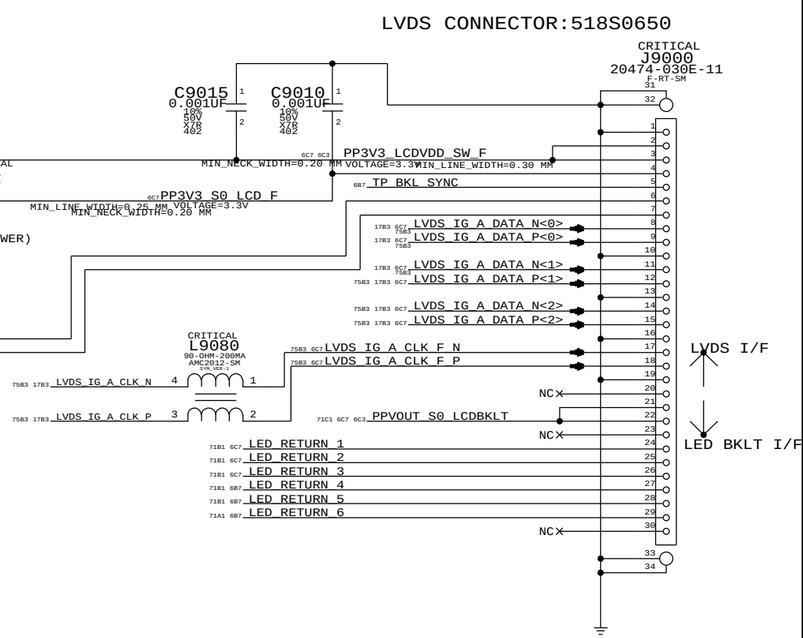


SYNC_MASTER=YUAN.MA	SYNC_DATE=12/11/2008
PAGE TITLE	POWER FETS
Apple Inc.	DRAWING NUMBER 051-7898
	SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 79 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP







SYNC_MASTER=NMARTIN SYNC_DATE=04/04/2008

PAGE TITLE: LVDS CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

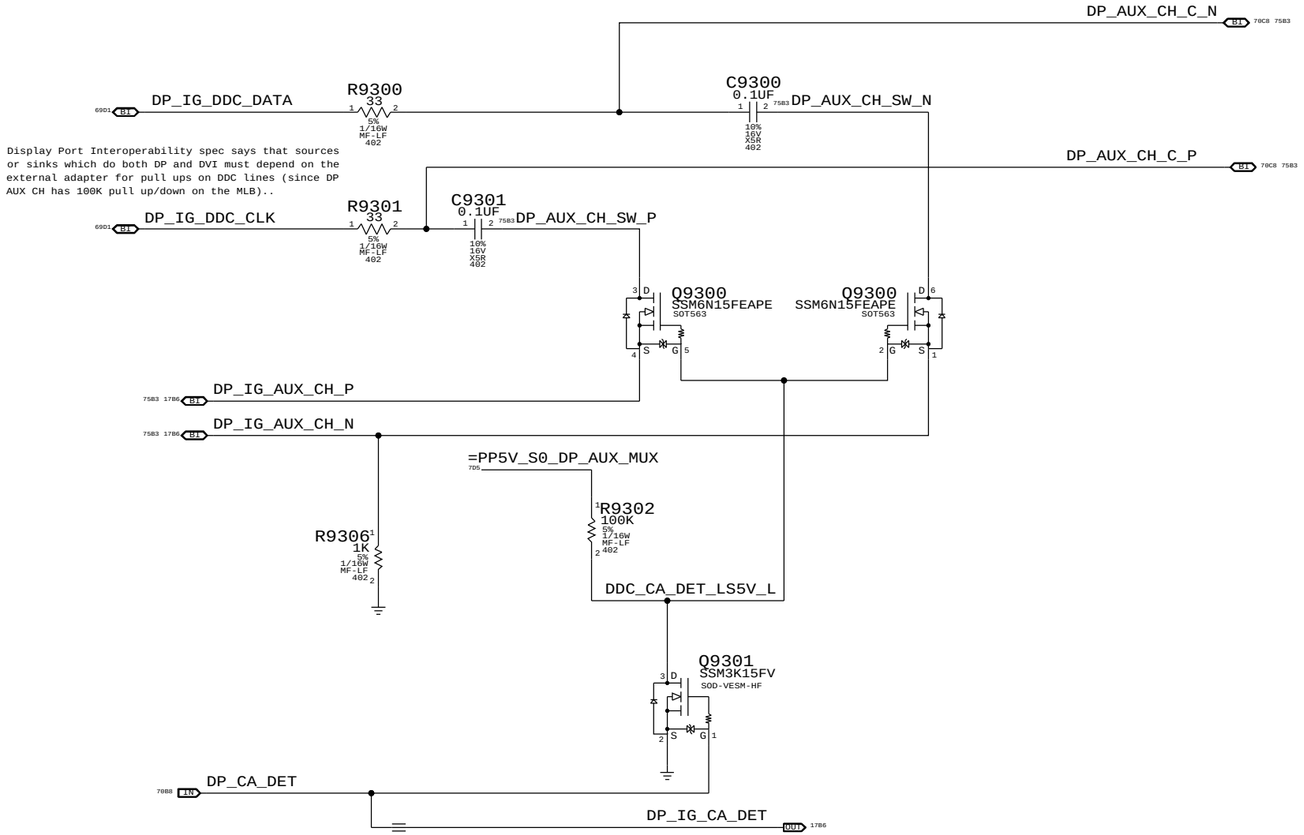
PAGE: 90 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8	7	6	5	4	3	2	1	

178G6	=MCP_HDMI_TXC_P	DP_ML_P<3>	70C8 75C3
178G6	=MCP_HDMI_TXC_N	DP_ML_N<3>	70C8 75C3
178G6	=MCP_HDMI_TXD_P<0>	DP_ML_P<2>	70C1 75C3
178G6	=MCP_HDMI_TXD_N<0>	DP_ML_N<2>	70C1 75C3
178G6	=MCP_HDMI_TXD_P<1>	DP_ML_P<1>	70C1 75C3
178G6	=MCP_HDMI_TXD_N<1>	DP_ML_N<1>	70C1 75C3
178G6	=MCP_HDMI_TXD_P<2>	DP_ML_P<0>	70C1 75C3
178G6	=MCP_HDMI_TXD_N<2>	DP_ML_N<0>	70C1 75C3
178G6	=MCP_HDMI_HPD	DP_HPD	70A8
17A3	=MCP_HDMI_DDC_CLK	DP_IG_DDC_CLK	69C8
17A3	=MCP_HDMI_DDC_DATA	DP_IG_DDC_DATA	69C8

All: MAKE_BASE=TRUE



SYNC_MASTER=AMASON	SYNC_DATE=04/18/2008
PAGE TITLE: DISPLAYPORT SUPPORT	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH:
	PAGE: 93 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

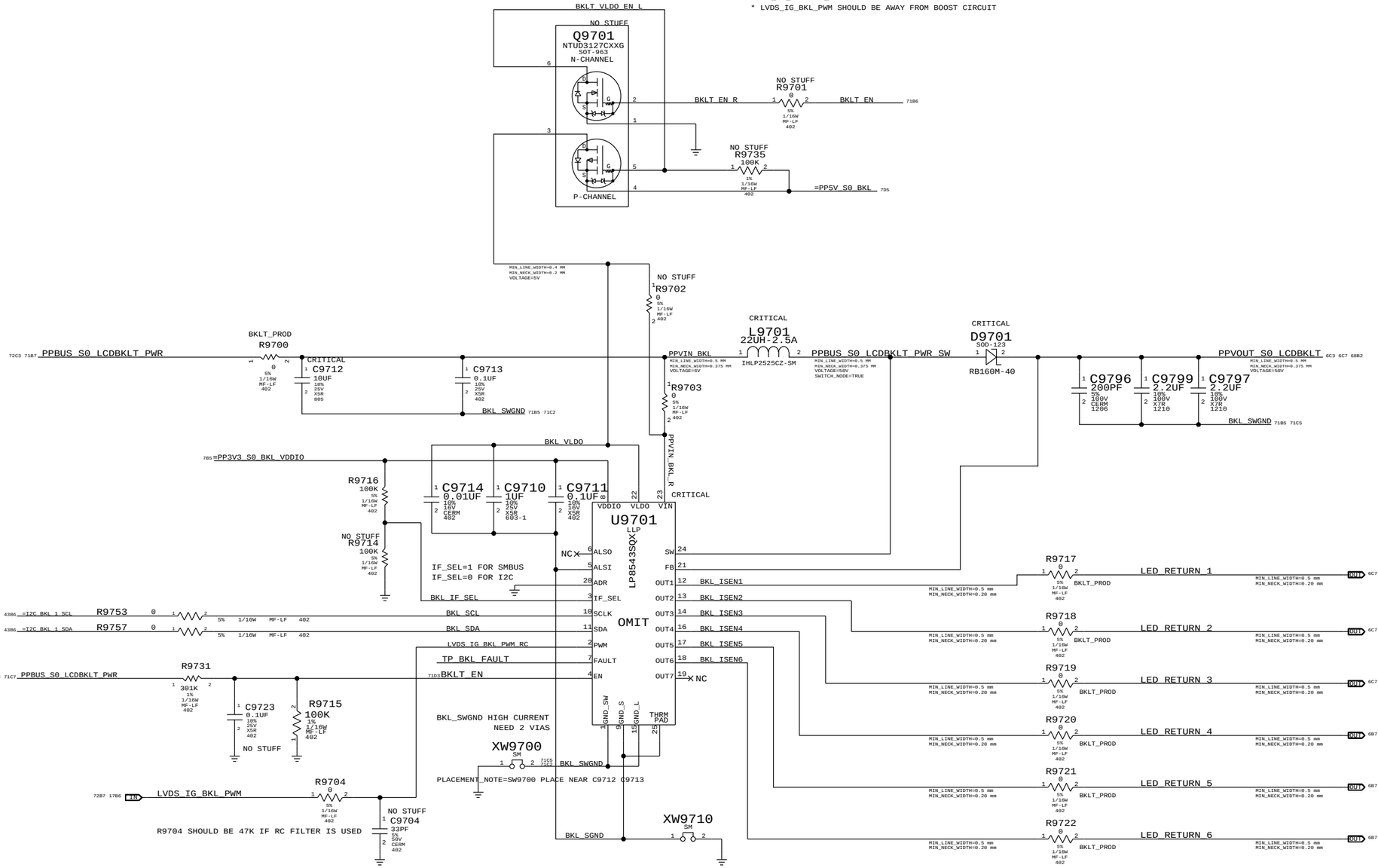
Port Power Switch

CRITICAL
U9480
TPS2051B
SOT23
=PP3V3_S5_DP_PORT_PWR
PM_SLP_S3_L
TP_DPPWR_OC_L
PP3V3_S0_DPILIM
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
L9400
FERR-120-OHM-3A
0603
PP3V3_S0_DPPWR
C9400 4.7UF 20% 6.3V X5R-CERM 402
C9480 22UF 20% 6.3V X5R-CERM-1 603
C9481 4.7UF 20% 6.3V X5R-CERM 402
C9485 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL
C9486 22UF 20% 6.3V X5R-CERM-1 603
R9420 100K 5% 1/16W MF-LF 402
HDMI_CEC
R9425 1M 5% 1/16W MF-LF 402
CRITICAL
J9400
DSPLYPRT-M97-1
F-RT-THSM
BOT ROW TH PINS
TOP ROW SM PINS
HOT_PLUG_DETECT
CONFIG1
CONFIG2
GND
ML_LANE3P
ML_LANE3N
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
ML_LANE1P
ML_LANE1N
ML_LANE2P
ML_LANE2N
RETURN
SHIELD PINS
514-0637
DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8
DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8
FL9400 12-OHM-100MA TCM1210-4SM
FL9401 12-OHM-100MA TCM1210-4SM
FL9402 12-OHM-100MA TCM1210-4SM
FL9403 12-OHM-100MA TCM1210-4SM
DP_ML_P<3> C9414 0.1uF DP_ML_C_P<3>
DP_ML_N<3> C9415 0.1uF DP_ML_C_N<3>
DP_AUX_CH_C_P
DP_AUX_CH_C_N
DP_ML_CONN_P<3>
DP_ML_CONN_N<3>
DP_ML_CONN_P<0>
DP_ML_CONN_N<0>
DP_ML_CONN_P<1>
DP_ML_CONN_N<1>
DP_ML_CONN_P<2>
DP_ML_CONN_N<2>
DP_ML_C_P<0> C9410 0.1uF DP_ML_P<0>
DP_ML_C_N<0> C9411 0.1uF DP_ML_N<0>
DP_ML_C_P<1> C9412 0.1uF DP_ML_P<1>
DP_ML_C_N<1> C9413 0.1uF DP_ML_N<1>
DP_ML_C_P<2> C9416 0.1uF DP_ML_P<2>
DP_ML_C_N<2> C9417 0.1uF DP_ML_N<2>
=PP3V3_S0_DPCONN
R9443 100K 5% 1/16W MF-LF 402
R9442 100K 5% 1/16W MF-LF 402
DP_CA_DET
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_L_Q
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q
R9421 100K 5% 1/16W MF-LF 402
DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8
DP_ESD CRITICAL D9400 RCLAMP0504F SC70-6-1
DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8
R9422 1M 5% 1/16W MF-LF 402
DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.
Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm
=PP3V3_S0_DPCONN
R9445 10K 5% 1/16W MF-LF 402
R9444 10K 5% 1/16W MF-LF 402
DP_HPD
R9446 100K 5% 1/16W MF-LF 402
MCP79 requires pull down HPD input with 100K if DP_HPD is used.
Q9441 2N7002DW-X-G SOT-363
DP_HPD_L_Q
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q
R9423 100K 5% 1/16W MF-LF 402
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

SYNC_MASTER=AMASON SYNC_DATE=06/30/2008
PAGE TITLE: DisplayPort Connector
Apple Inc.
DRAWING NUMBER: 051-7898
SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 94 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

*PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

NEAR EACHOTHER.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	6	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719,R9720,R9721,R9722		BKLT_ENG
116S0005	1	RES,1/16W,0.1 OHM,1%,0402,SM	R9700		BKLT_ENG

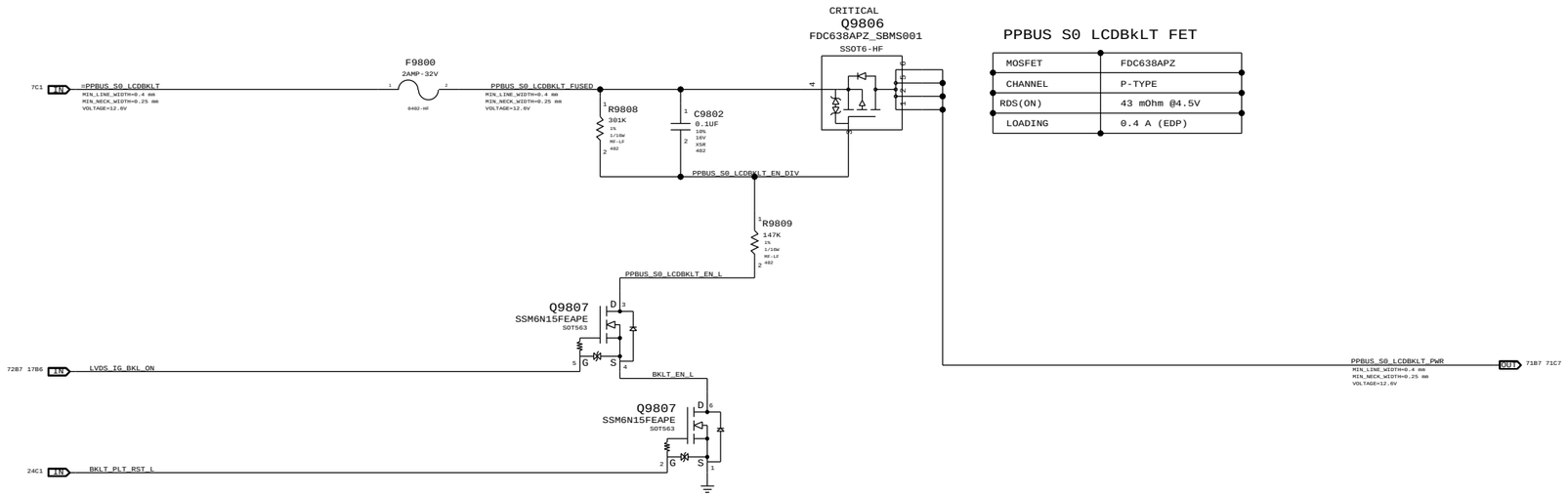
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2670	1	IC,LP8543,WHT LED BKLT CTRLR,QFN24,PROD	U9701	CRITICAL	

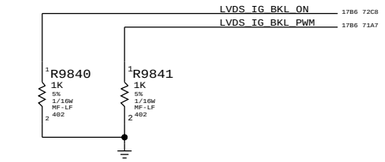
SYNC_MASTER=KIRAN SYNC_DATE=12/05/2008

PAGE TITLE: LCD BACKLIGHT DRIVER

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 97 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





MCP HAS INTERNAL 10K PULL-UP FOR THESE SIGNALS

SYNC_MASTER=YITE SYNC_DATE=06/30/2008

PAGE TITLE
LCD Backlight Support

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 98 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU 7 FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	9C4 13D3
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	9C4 13D6
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	9C4 13D6
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	9C4 13D6
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	9B4 9C4 13C3 13D3
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	9B4 13D6
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	9B4 13D6
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	9B4 13D6
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	9C2 13B3 13C3
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	9C2 13D6
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	9C2 13D6
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	9C2 13D6
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	9B2 9C2 13B3
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	9B2 13D6
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	9B2 13D6
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	9B2 13D6
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	9D8 13C6 13D6
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	9D8 13B6
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	9D8 13B6
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	9C8 9D8 13C6
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	9C8 13B6
FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	9D6 13B6
FSB_RREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9D6 13B6
FSB_RREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	13B6
FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	9D6 13B6
FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	9D6 13B3
FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	9D6 13B6
FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	9D6 13B3
FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	9D6 13B6
FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	9D6 13B6
FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	9D6 13B6
FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	9D6 13B6
FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9D6 12C2 13A3
FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	9D6 13A6
FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	9D6 13B6
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	9C8 13A3
CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	8B2 9B4
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	9C8 13B7
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	9C8 13A3
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	9D6 13A3
CPU_ASYNC_P	CPU_50S	CPU_AGTL	CPU_INTR	9C8 13A3
CPU_ASYNC_P	CPU_50S	CPU_AGTL	CPU_NMI	9B8 13A3
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	9C5 13B6 41D4 62C8
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	9B2 12C7 13A3
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	9B8 13A3
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	9C8 13A3
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	9C6 13B7 41C4
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	9B2 13A3
CPU_EROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	9B2 13A3
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9B2 13A3 62C7
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	9B2 13A3
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	13A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	13A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	13A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	13A6
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	9B6 13B3
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	9B6 13B3
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	12C3 13B3
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	12C3 13B3
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	13A4
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	13A4
CPU_IERR_L	CPU_50S		CPU_IERR_L	9D6
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	20C7 62D8
(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	62C7
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	9B4 25B1
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	9B3
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	9B3
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	9B3
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	9B3
XDP_TDI	CPU_50S	CPU_TIP	XDP_TDI	9B6 9C6 12B3
XDP_TDO	CPU_50S	CPU_TIP	XDP_TDO	9B6 9C6 12B3
XDP_TMS	CPU_50S	CPU_TIP	XDP_TMS	9B6 9C6 12B3
XDP_TCK	CPU_50S	CPU_TIP	XDP_TCK	9A6 9C6 12B6
XDP_TRST_L	CPU_50S	CPU_TIP	XDP_TRST_L	9A6 9C6 12B3
XDP_BPM_L	CPU_50S	CPU_TIP	XDP_BPM_L<4..0>	9C6 12C6
XDP_BPM_L5	CPU_50S	CPU_TIP	XDP_BPM_L<5>	9C5 12C6
(FSB_CPURST_L)	CPU_50S	CPU_TIP	XDP_CPURST_L	12C4
	CPU_50S	CPU_8MIL	CPU_VID<6..0>	10B6 62C7
	CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	10B5 62A5
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	10A5 62A5
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

FSB 4X Signal Groups

FSB 2X Signals

FSB 1X Signals

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

PAGE TITLE: CPU/FSB Constraints

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 100 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	14B5 26C5 26C7
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	14B5 26C5 26C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	14A5 26D5 26D7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	14B5 26C5 26C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	14B5 26C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	14B5 14C5 26C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	14C5 26C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	14C5 26C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	14C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	14C5 26C7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	14B7 26C2 26C4 26D2 26D4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	14B7 26C2 26C4
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	14B7 14C7 26B2 26B4 26C2 26C4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	14C7 26C2 26C4
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	14C7 26B5 26B7 26C5 26C7
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	14C7 14D7 26B5 26B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	14D7 26B5 26B7
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	14D7 26A5 26A7 26B5 26B7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	14A7 26C4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	14A7 26C2
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	14B7 26B4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	14B7 26C2
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	14B7 26B5
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	14B7 26B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	14B7 26B5
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	14B7 26A7
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	14D5 26C2
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	14D5 26D2
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	14D5 26C4
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	14D5 26C4
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	14D5 26B2
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	14D5 26C2
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	14D5 26C4
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	14D5 26C4
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	14D5 26B7
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	14D5 26B7
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	14D5 26B5
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	14D5 26B5
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	14D5 26B7
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	14D5 26B7
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	14D5 26A5
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	14D5 26A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	14B1 27C5 27C7
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	14B1 27C5 27C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	14A1 27D5 27D7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	14B1 27C5 27C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	14B1 27C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	14B1 14C1 27C5 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	14C1 27C5 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	14C1 27C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	14C1 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	14C1 27C7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	14B3 27C2 27C4 27D2 27D4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	14B3 27C2 27C4
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	14B3 14C3 27C2 27C4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	14C3 27B2 27B4 27C2 27C4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	14C3 27B5 27B7 27C5 27C7
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	14C3 14D3 27B5 27B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	14D3 27B5 27B7
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	14D3 27A5 27A7 27B5 27B7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	14A3 27C4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	14A3 27C2
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	14B3 27C2
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	14B3 27B4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	14B3 27B5
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	14B3 27B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	14B3 27B5
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	14B3 27A7
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	14D1 27C2
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	14D1 27D2
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	14D1 27C4
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	14D1 27C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	14D1 27C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	14D1 27C4
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	14D1 27B2
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	14D1 27C2
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	14D1 27B7
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	14D1 27B7
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	14D1 27B5
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	14D1 27B5
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	14D1 27B7
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	14D1 27B7
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	14D1 27A5
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	14D1 27A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15C6
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15C6

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 101 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_90D_HDD	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	6D5 29C7
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	6D5 29C7
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	16B3 29C5
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	16B3 29C5
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	6D5 16B6 29C7
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	6D5 16B6 29C7
	PCIE_90D	PCIE	PCIE_FW_R2D_P	34C3
	PCIE_90D	PCIE	PCIE_FW_R2D_N	34C3
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	16B3 34C1
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	16B3 34C1
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	16B6 34C1
	PCIE_90D	PCIE	PCIE_FW_D2R_N	16B6 34C1
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	34C3
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	34C3
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	16C3 29C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	16C3 29C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	6D5 29C7
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	6D5 29C7
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	16A6
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	69D1 70C1 70C8
	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	70C2 70C7
DP_ML	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	69D1 70C1 70C8
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	70C2 70C7
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	17B6 69C7
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	17B6 69C7
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	69C6
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	69C5
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	69C4 70C8
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	69D4 70C8
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	17A6 23C7
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	17A6 23C7
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	17B3 68B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	6C7 68C2
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	17B3 68B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	6C7 68C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	6C7 17B3 68C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	6C7 17B3 68C2
16:8 DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	70C3 70C4 70C5
16:8	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	70C3 70C4 70C5
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17A3 23C6
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17A3 23C6
SATA_HDD_R2D	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_P	19D6 37A2
	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_N	19D6 37A2
	SATA_90D_HDD	SATA	SATA_HDD_R2D_P	6B7 37A5
	SATA_90D_HDD	SATA	SATA_HDD_R2D_N	6B7 37A5
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_P	37A4
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_N	37A4
SATA_HDD_D2R	SATA_90D_HDD	SATA	SATA_HDD_D2R_P	19D6 37B2
	SATA_90D_HDD	SATA	SATA_HDD_D2R_N	19D6 37B2
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_P	6B7 37B5
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_N	6B7 37B5
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_P	37B4
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_N	37B4
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	19D6 37C3
	SATA_100D	SATA	SATA_ODD_R2D_C_N	19D6 37C3
	SATA_100D	SATA	SATA_ODD_R2D_P	6B7 37C6
	SATA_100D	SATA	SATA_ODD_R2D_N	6A7 6B7 37C6
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	37C4
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	37C4
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	19D6 37C3
	SATA_100D	SATA	SATA_ODD_D2R_N	19D6 37C3
	SATA_100D	SATA	SATA_ODD_D2R_C_P	6B7 37C6
	SATA_100D	SATA	SATA_ODD_D2R_C_N	6B7 37C6
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	37C4
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	37C4
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	19A6

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

PAGE TITLE: MCP Constraints 1

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 102 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
MCP_DEBUG	PCI_5SS	PCI	MCP_DEBUG<7..0>	12C3 18D7
PCI_AD	PCI_5SS	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_5SS	PCI	PCI_AD<24>	
PCI_AD	PCI_5SS	PCI	PCI_AD<31..25>	
PCI_AD	PCI_5SS	PCI	PCI_PAR	
PCI_C_BE_L	PCI_5SS	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_5SS	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_5SS	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_5SS	PCI	PCI_PERR_L	
PCI_CNTL	PCI_5SS	PCI	PCI_SERR_L	
PCI_CNTL	PCI_5SS	PCI	PCI_STOP_L	
PCI_CNTL	PCI_5SS	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_5SS	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_5SS	PCI	PCI_REQ0_L	18D2 18D7
PCI_GNT0_L	PCI_5SS	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_5SS	PCI	PCI_REQ1_L	18D2 18D7
PCI_GNT1_L	PCI_5SS	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_5SS	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_5SS	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_5SS	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_5SS	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_5SS	CLK_PCI	PCI_CLK33M_MCP_R	18C5
	CLK_PCI_5SS	CLK_PCI	PCI_CLK33M_MCP	18C5
LPC_AD	LPC_5SS	LPC	LPC_AD<3..0>	18B3 40C8 42D3 42D5
LPC_FRAME_L	LPC_5SS	LPC	LPC_FRAME_L	18C3 40C8 42D5
LPC_RESET_L	LPC_5SS	LPC	LPC_RESET_L	18C3 24D4
MCP_LPC_CLK0	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_SMC_R	18B3 24B4
	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_SMC	24B1 40C8
	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_LPCPLUS	24B1 42D3
USB_EXTA	USB_90D	USB	USB_EXTA_P	19D3 38A8
	USB_90D	USB	USB_EXTA_N	19D3 38A8
	USB_90D	USB	USB_EXTA_MUXED_P	38C4
	USB_90D	USB	USB_EXTA_MUXED_N	38C4
	USB_90D	USB	CONN_USB_EXTA_P	38C3
	USB_90D	USB	CONN_USB_EXTA_N	38C3
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	19D3 29B5
	USB_90D	USB	USB_CAMERA_N	19D3 29B5
	USB_90D	USB	USB_CAMERA_CONN_P	6D5 29B7
	USB_90D	USB	USB_CAMERA_CONN_N	6D5 29B7
USB_BT	USB_90D	USB	USB_BT_P	19D3 29B5
	USB_90D	USB	USB_BT_N	19C3 29B5
	USB_90D	USB	CONN_USB2_BT_P	6D5 29B7
	USB_90D	USB	CONN_USB2_BT_N	6D5 29B7
USB_TPAD	USB_90D	USB	USB_TPAD_P	19D3 48B8
	USB_90D	USB	USB_TPAD_N	19D3 48B8
	USB_90D	USB	USB_TPAD_R_P	48B7
	USB_90D	USB	USB_TPAD_R_N	48B7
USB_IR	USB_90D	USB	USB_IR_P	19D3 39D7
	USB_90D	USB	USB_IR_N	19D3 39D7
USB_EXTB	USB_90D	USB	USB_EXTB_P	19C3 38A4
	USB_90D	USB	USB_EXTB_N	19C3 38B4
	USB_90D	USB	CONN_USB_EXTB_P	38B3
	USB_90D	USB	CONN_USB_EXTB_N	38B3
USB_SD	USB_90D	USB	USB_CARDREADER_P	19C3 30C7
	USB_90D	USB	USB_CARDREADER_N	19C3 30C7
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	19C4
SMBUS_MCP_0_CLK	SMB_5SS	SMB	SMBUS_MCP_0_CLK	12B6 20C3 43D8
SMBUS_MCP_0_DATA	SMB_5SS	SMB	SMBUS_MCP_0_DATA	12B6 20C3 43D8
SMBUS_MCP_1_CLK	SMB_5SS	SMB	SMBUS_MCP_1_CLK	20C3 43B8
SMBUS_MCP_1_DATA	SMB_5SS	SMB	SMBUS_MCP_1_DATA	20C3 43B8
HDA_BIT_CLK	HDA_5SS	HDA	HDA_BIT_CLK	20D2 52C7
	HDA_5SS	HDA	HDA_BIT_CLK_R	20A7 20D4
HDA_SYNC	HDA_5SS	HDA	HDA_SYNC	20D2 52C7
	HDA_5SS	HDA	HDA_SYNC_R	20A7 20D4
HDA_RST_L	HDA_5SS	HDA	HDA_RST_R_L	20A7 20D4
	HDA_5SS	HDA	HDA_RST_L	20D2 52C7
HDA_SDIN0	HDA_5SS	HDA	HDA_SDIN0	20D7 52C7
	HDA_5SS	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_5SS	HDA	HDA_SDOUT	20D2 52C7
	HDA_5SS	HDA	HDA_SDOUT_R	20A7 20D4
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	20C7
MCP_SUS_CLK	CLK_SLOW_5SS	CLK_SLOW	PM_CLK32K_SUSCLK_R	20B3 24B4
	CLK_SLOW_5SS	CLK_SLOW	PM_CLK32K_SUSCLK	24B1 40C5
SPI_CLK	SPI_5SS	SPI	SPI_CLK_R	20B3 42A5 42C8
	SPI_5SS	SPI	SPI_CLK	51C5
	SPI_5SS	SPI	SPI_ALT_CLK	42C5 42D3
SPI_MOSI	SPI_5SS	SPI	SPI_MOSI_R	20B3 42A5 42C7
	SPI_5SS	SPI	SPI_MOSI	51C4
	SPI_5SS	SPI	SPI_ALT_MOSI	42C5 42D5
SPI_MISO	SPI_5SS	SPI	SPI_MISO	20B3 42A5 42B7
	SPI_5SS	SPI	SPI_MISO_R	51C4
	SPI_5SS	SPI	SPI_ALT_MISO	42B5 42D5
SPI_CS0	SPI_5SS	SPI	SPI_CS0_R_L	20B3 42B7
	SPI_5SS	SPI	SPI_CS0_L	
	SPI_5SS	SPI	SPI_CS1_R_L	
	SPI_5SS	SPI	SPI_CS1_R_L_USE_MLB	

SYNC_MASTER=T18_MLB SYNC_DATE=12/14/2007

PAGE TITLE: MCP Constraints 2

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 103 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	17C6
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	17C6
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	17C3 32A5
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	31B6 32A3
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	17C3 31B6
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	17D3 31B6
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	31C4
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	17D6 31C1
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	31C4
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	17D6 31C1
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	17D6 31C1
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	17D6 31B1
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	31B4
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	31C6
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	17D3 31C8
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	17D3 31C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	17D3 31C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	17D3 31B6
	ENET_MII_55S	ENET_MII	ENET_RESET_L	17C3 31B7
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31B3 33B8 33C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31B3 33B8 33C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	33B4 33C4 33C5
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	33B4 33C4 33C5

SYNC_MASTER=T18_MLB SYNC_DATE=03/19/2008

PAGE TITLE: Ethernet Constraints

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 104 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

SD CARD INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_SSS	*	=SS_OHM_SE	=SS_OHM_SE	=SS_OHM_SE	=SS_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	34B6 36C4
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	34C6 36C4
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	34B6 36C4
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	34B6 36C4
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	34B6 36B8
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	34B6 36B8
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	34B6 36B8
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	34B6 36B8
Port 2 Not Used				

SD CARD NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I23 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<0>	30C2
I24 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<1>	30C2
I25 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<2>	30C2
I26 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<3>	30C2
I27 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<4>	30C2
I28 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<5>	30C2
I29 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<6>	30C2
I30 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<7>	30C2
I32 SD_CLK	SD_SSS	SD_INTERFACE	SD_CLK	30C2
I33 SD_CMD	SD_SSS	SD_INTERFACE	SD_CMD	30C2

SYNC_MASTER=K19_MLB SYNC_DATE=12/01/2008

PAGE TITLE: FireWire Constraints

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 105 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	6C5 6D5 43D2
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	6C5 6D5 43D2
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	43C2
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	43C2
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	43D5
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	43D5
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	6A7 43C5
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	6A7 43C5
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	43B5
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	43B5

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

PAGE TITLE
SMC Constraints

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 106 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

K24 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DIFFPAIR		CHGR_CSO_R_P	45A8 59B3
	DIFFPAIR		CHGR_CSO_R_N	45A8 59B3
	DIFFPAIR		CPUTHMSNS_D2_P	46C5
	DIFFPAIR		CPUTHMSNS_D2_N	46C5
	DIFFPAIR		CPU_THERMD_P	9C6 46D5
	DIFFPAIR		CPU_THERMD_N	9C6 46D5
	DIFFPAIR		ISNS_CPUVTT_P	45B7
	DIFFPAIR		ISNS_CPUVTT_N	45B7
	DIFFPAIR		ISNS_P1V5S0MCP_P	
	DIFFPAIR		ISNS_P1V5S0MCP_N	
	DIFFPAIR		ISNS_PVCORES0MCP_P	
	DIFFPAIR		ISNS_PVCORES0MCP_N	
	DIFFPAIR		MCPTHMSNS_D2_P	6C7 46B5
	DIFFPAIR		MCPTHMSNS_D2_N	6C7 46B5
	DIFFPAIR		MCP_THMDIODE_P	20C3 46B5
	DIFFPAIR		MCP_THMDIODE_N	20C3 46B5

SYNC_MASTER=M97_MLB

PAGE TITLE
K24 SPECIAL CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
BRANCH
PAGE 107 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

K24 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD_UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	-	0.126 MM	?
3X_DIELECTRIC	-	0.189 MM	?
4X_DIELECTRIC	-	0.252 MM	?
5X_DIELECTRIC	-	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

SYNC MASTER=M97 MLB

PAGE TITLE: K24 RULE DEFINITIONS

Apple Inc.

DRAWING NUMBER: 051-7898 | SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 109 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>