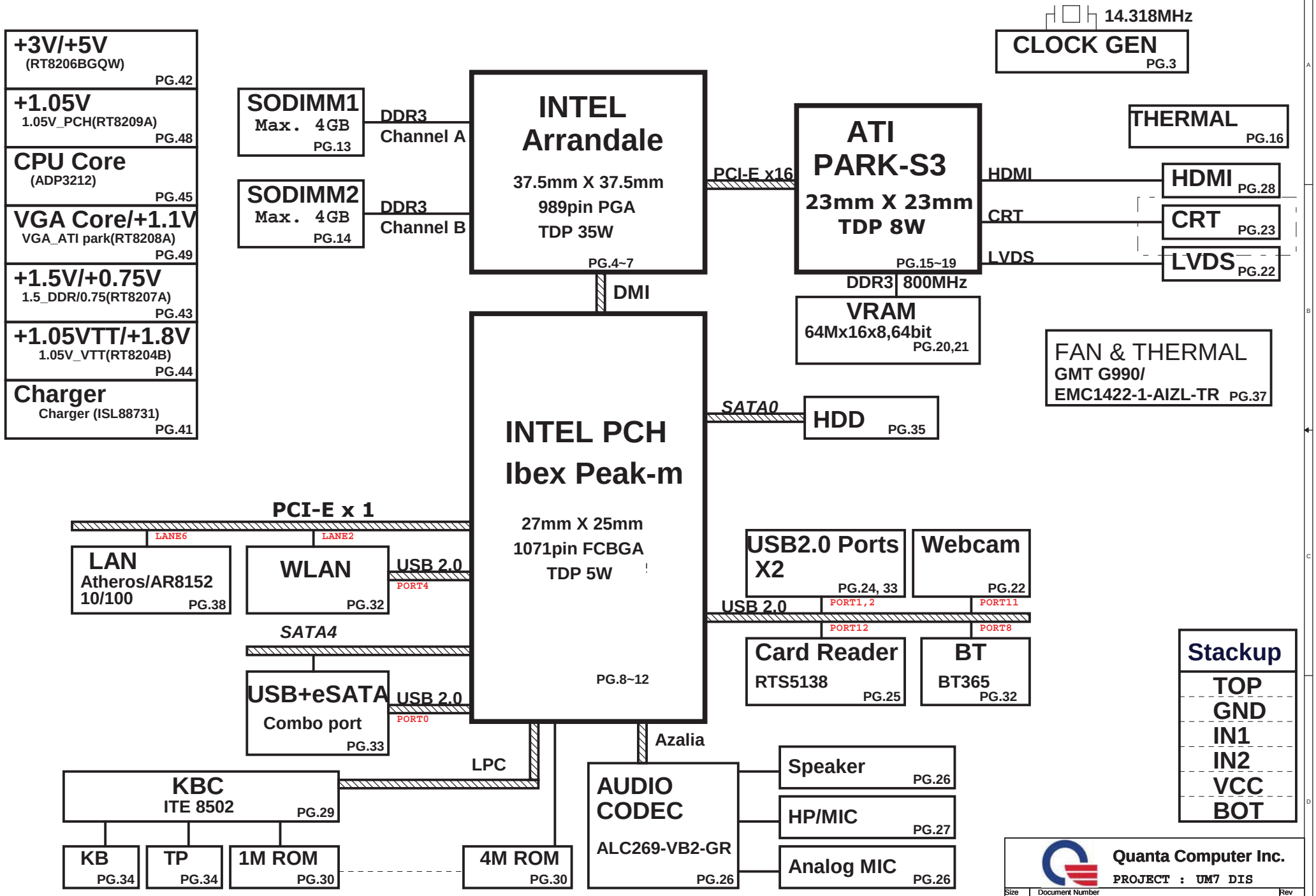
UM7B DISCRETE SYSTEM DIAGRAM



Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	BLOCK DIAGRAM	3A
Date: Wednesday, February 03, 2010	Sheet 1 of 52	

Table of Contents

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	23,42,43,44,45,46,49,50	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	09,12,30,31	RTC		S0~S5
					S0~S5
+5V_ALW	+5V	37,43,44,47,48	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	30,31,37,42,43,45,47,48	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	12,25,34,37,43,44,45,46,47,49,50	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	03,08,09,10,11,12,23,35,37,39,41,46,47,50	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	04,06,14,15,44,47	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	14,15,44	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	08,12,23,24,27,28,29,35,36,3738,47	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,4,8,9,10,11,12,14,15,23,24,26,27,28,29,30 ,31,33,34,36,37,38,39,41,47	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	6,12,45	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	4,6,11,12,45,46	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	12,33,47	PCH/Min Card	RUN_ON	
+1.05V_PCH	+1.05V	3,8,9,10,12,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	6,46	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	23	LCD Power	LCDVCC_TST_EN & ENVDD	

GND PLANE	PAGE	DESCRIPTION
GND	ALL	

Quanta Computer Inc.

PROJECT : UM7 DIS

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	BLOCK DIAGRAM	3A
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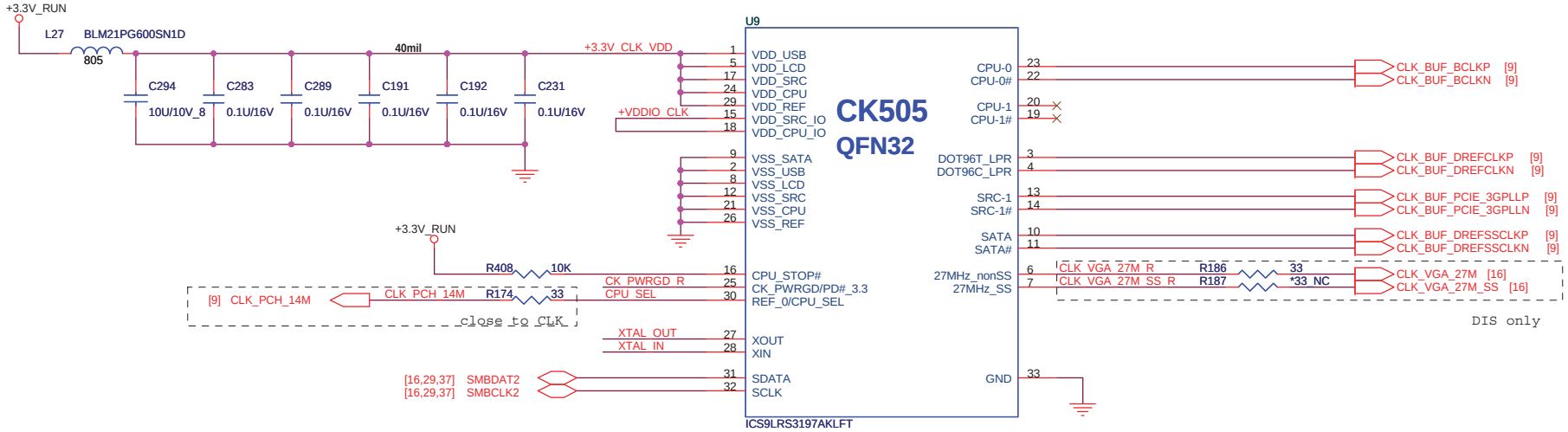
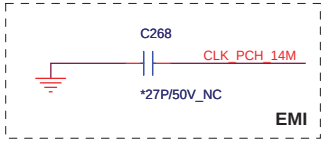
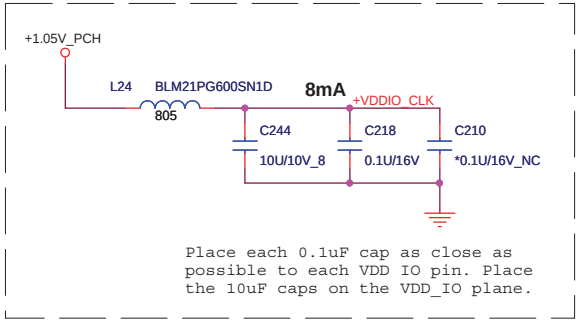
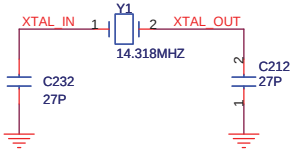
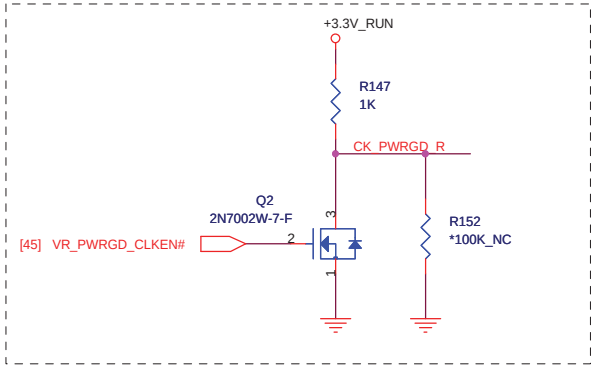


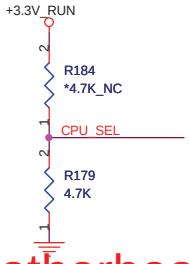
AL003197000IC OTHER(32P)ICS9LRS3197AKLFT(QFN)
~~AL8SP585000IC OTHER(32P)SLG8SP585VTR(QFN)~~
AL8SP590000IC OTHER(32P)SLG8SP590VTR(QFN)











PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	Clock Generator	3A
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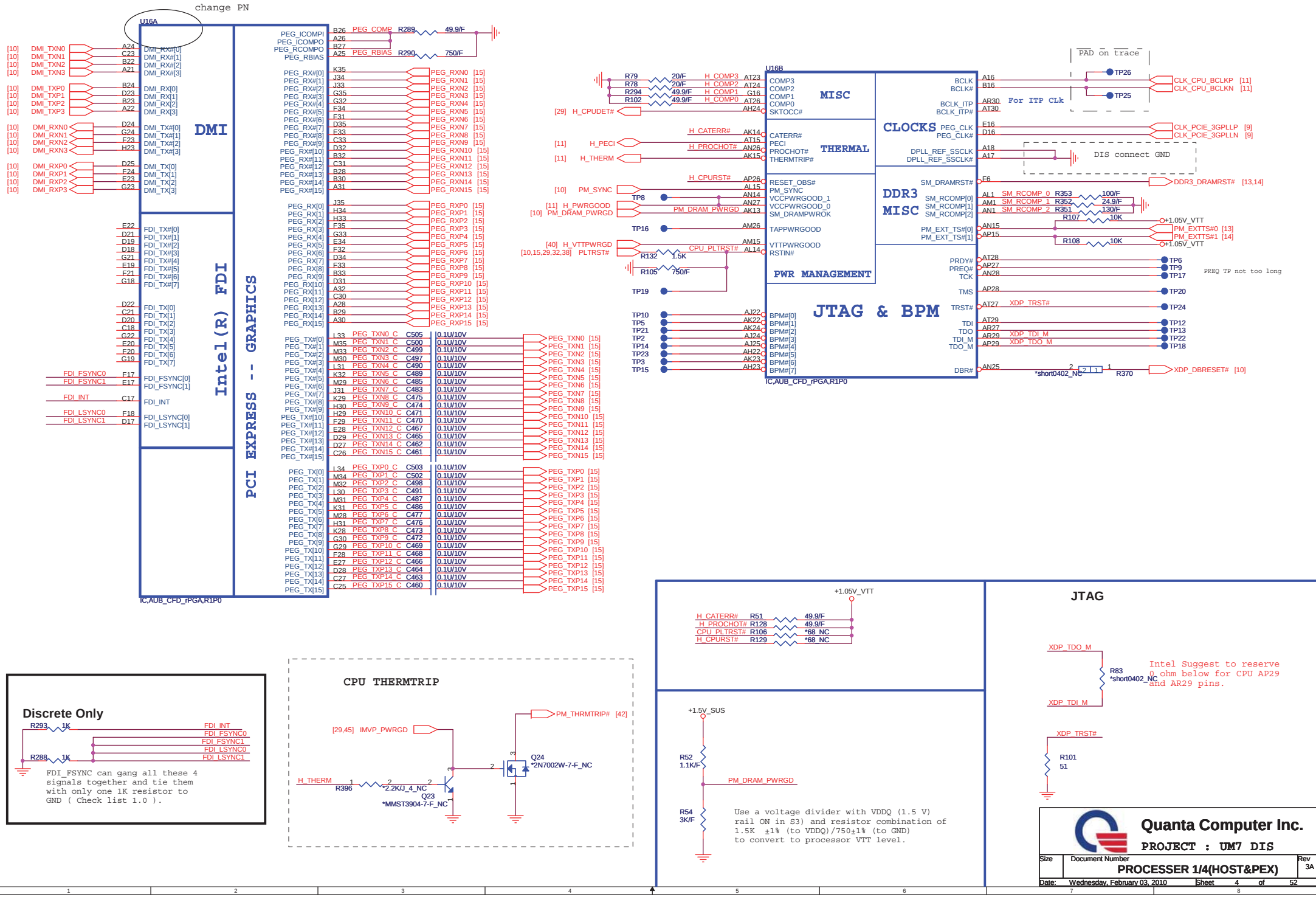
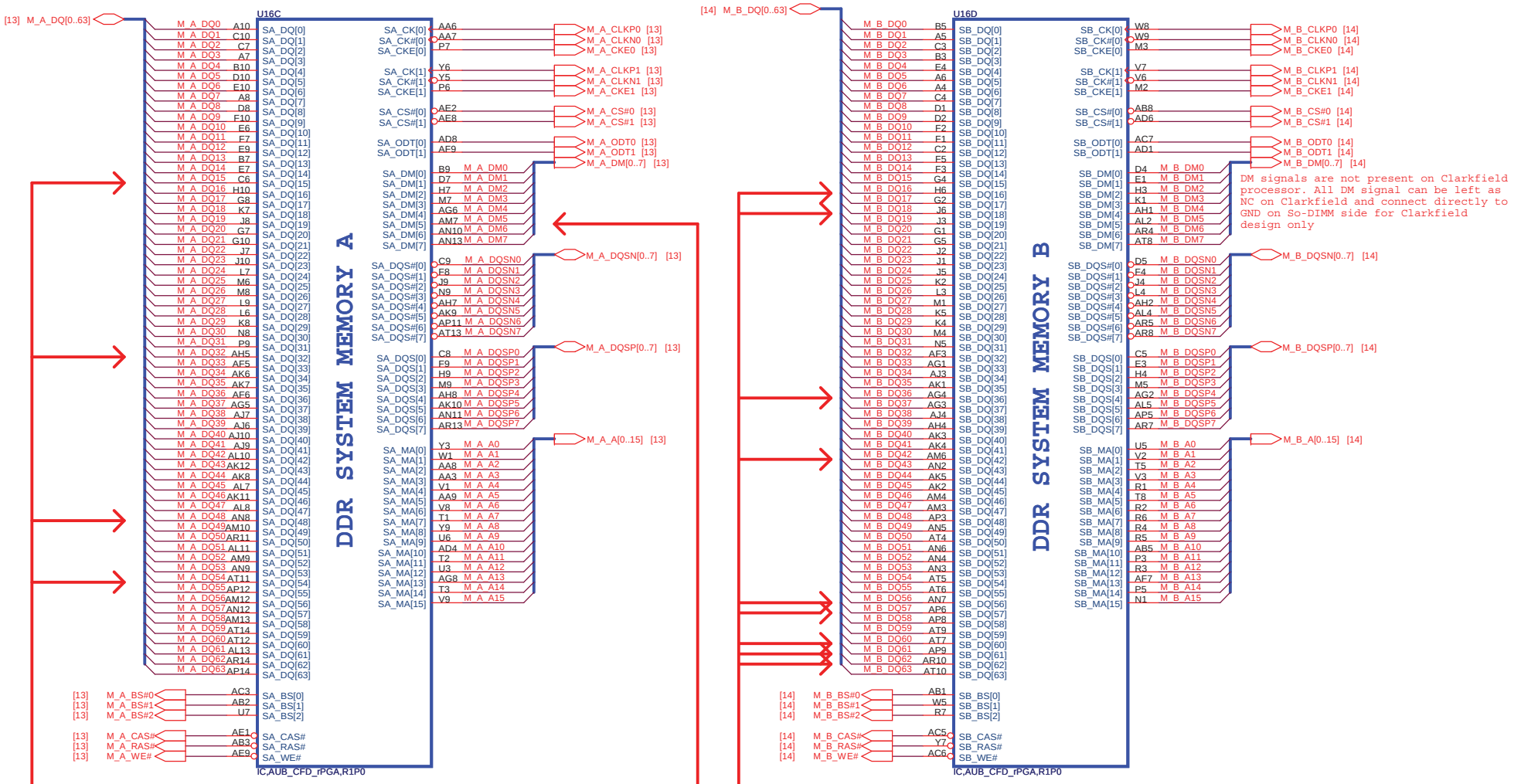


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: PROCESSER 2/4(DDR)	Rev: 3A
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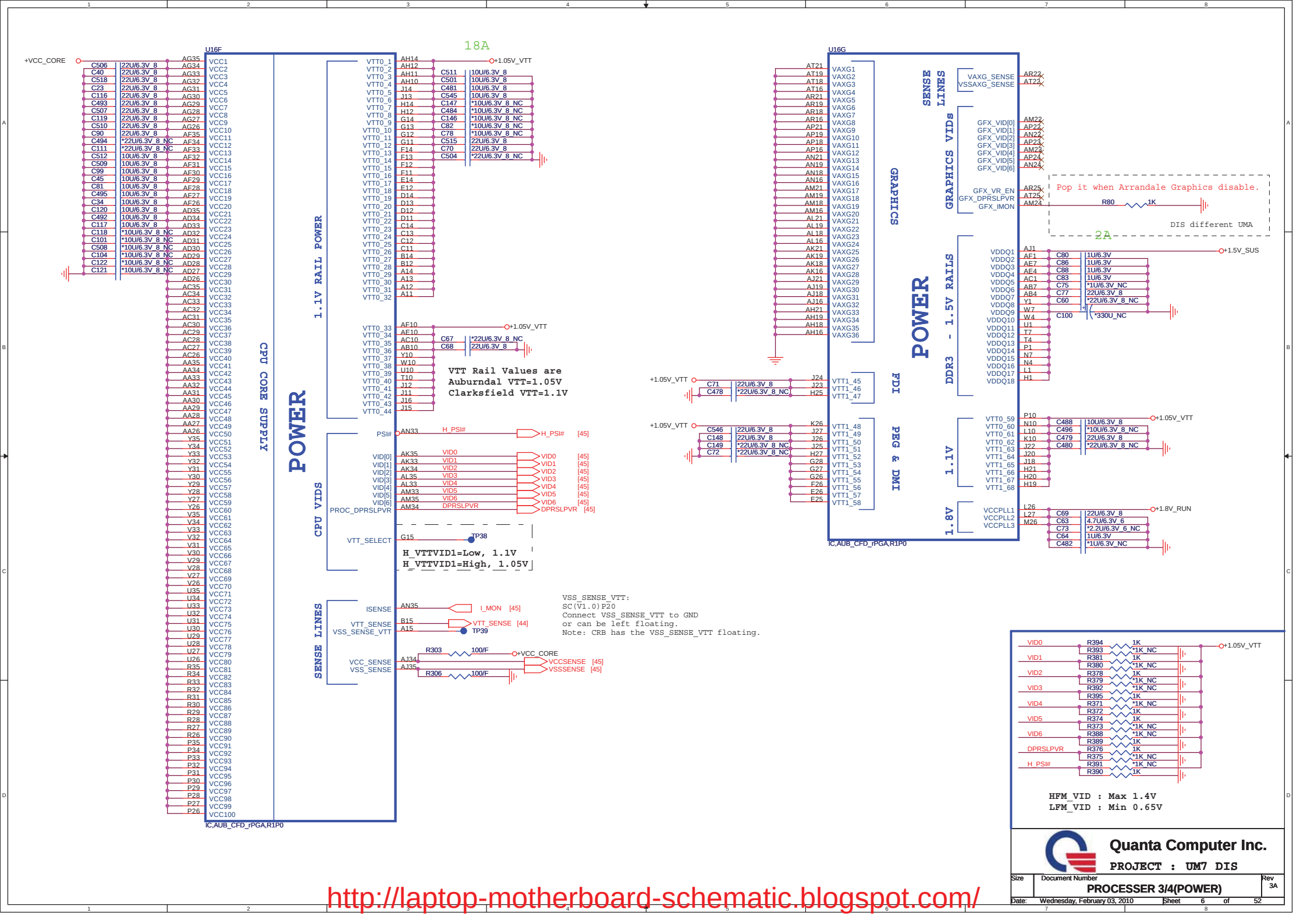
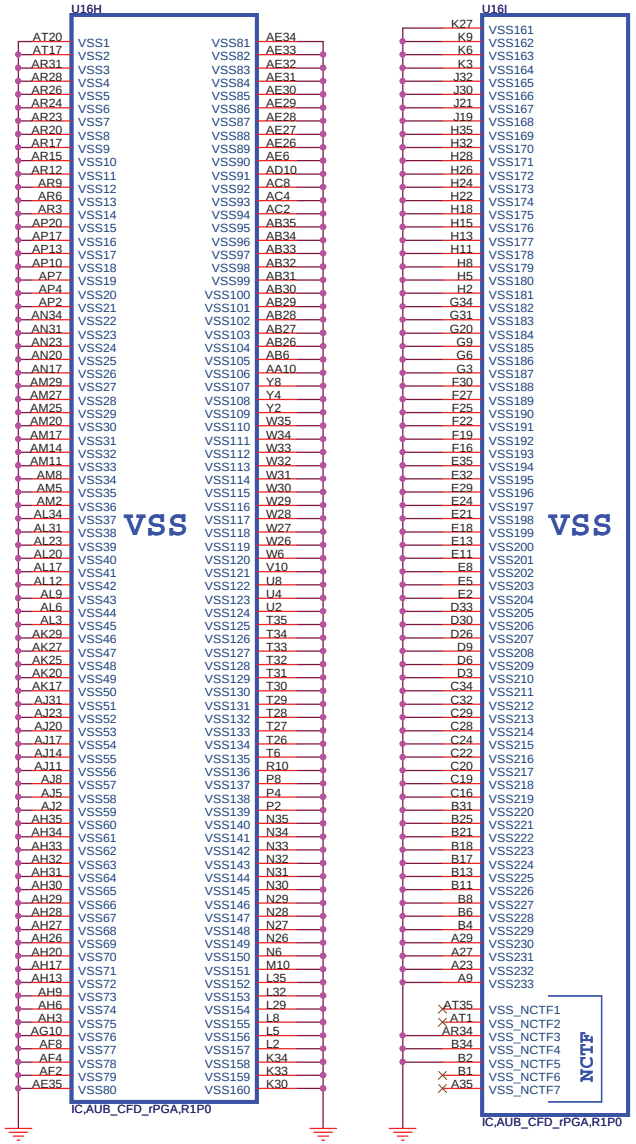
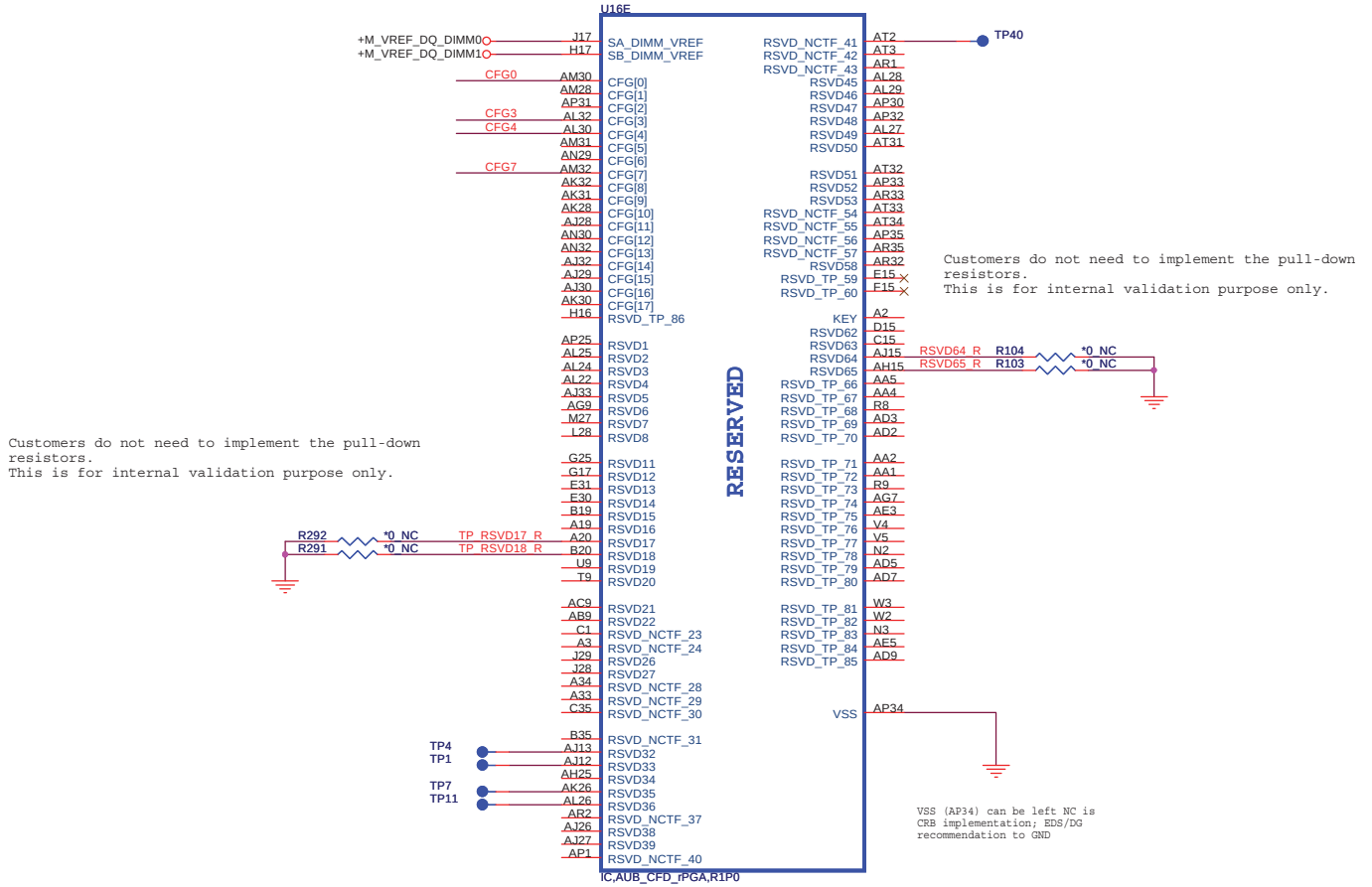
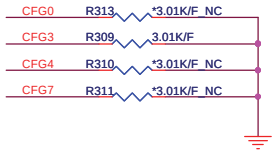


Arrandale PROCESSOR (GND)



Arrandale PROCESSOR(RESERVED, CFG)





The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

Quanta Computer Inc.
PROJECT : UM7 DIS

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	PROCESSER 4/4 (GND)	3A

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INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U23A

Ibex-M 1 OF 10

RTC
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN

IHDA
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN# / GPIO33 (+3V)
HDA_DOCK_RST# / GPIO13 (+3V_S5)

JTAG
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
TRST#

SPI
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO

LPC
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
FWH4 / LFRAME#
LDRQ0#
(+3V) LDRQ1# / GPIO23
SERIRQ

SATA
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATALED#
(+3V) SATA0GP / GPIO21
(+3V_S5) SATA1GP / GPIO19

HM57_MP

HDD
SATA_RXN0 [35]
SATA_RXP0 [35]
SATA_TXN0 [35]
SATA_TXP0 [35]

ESATA
SATA_RXN4 [33]
SATA_RXP4 [33]
SATA_TXN4 [33]
SATA_TXP4 [33]

UMA CRT,LVDS&HDMI signals
IBEX PEAK-M (LVDS,DDI)

U23D

Ibex-M 4 OF 10

LVDS--A
LVDS--B
CRT

Digital Display Interface
DISPLAY PORT B
DISPLAY PORT C
DISPLAY PORT D

SDVO
SDVO_TVCLKINN
SDVO_TVCLKINP
SDVO_STALLN
SDVO_STALLP
SDVO_INTN
SDVO_INTP
SDVO_CTRLCLK
SDVO_CTRLDATA

HM57_MP

iTPM ENABLE/DISABLE

+3.3V_RUN
R406 *1K_NC SPI_SI

TPM Function	
Enable	Mount
Disable	NC (Default)

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

For AUDIO

[26,29] ACZ_RST#_AUDIO R455 33 ACZ_RST#
[26] ACZ_SDOUT_AUDIO R450 33 ACZ_SDOUT
[26] ACZ_SYNC_AUDIO R452 33 ACZ_SYNC
[26] ACZ_BITCLK_AUDIO R205 33 ACZ_BITCLK, C324 10P/50V

+3.3V_RUN R397 *1K/F_NC ACZ_SPKR

No Reboot strap.	
SPKR	Low = Default. High = No Reboot

RTC 1mA

+RTC_CELL
R433 20K/F RTC_RST# C297 1U/6.3V
R439 20K/F SRTC_RST# C311 1U/6.3V
R434 1M SM_INTRUDER#

+3.3V_SUS Res. of TDI near PCH

R130 *200_NC, R131 *200_NC, R113 *200_NC, R111 *20K_NC
R123 *100_NC, R126 *100_NC, R382 *100_NC, R100 *10K_NC
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_RST#

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

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	PCH 1/5 (SATA,HDA,LPC)	3A
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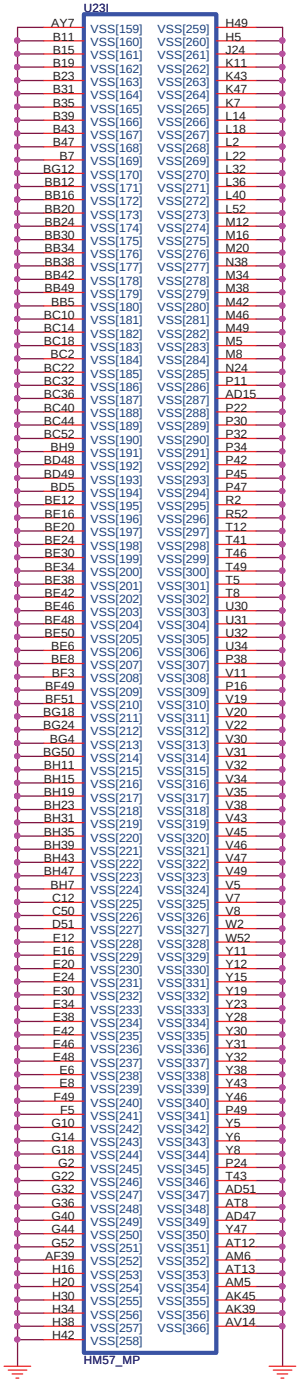
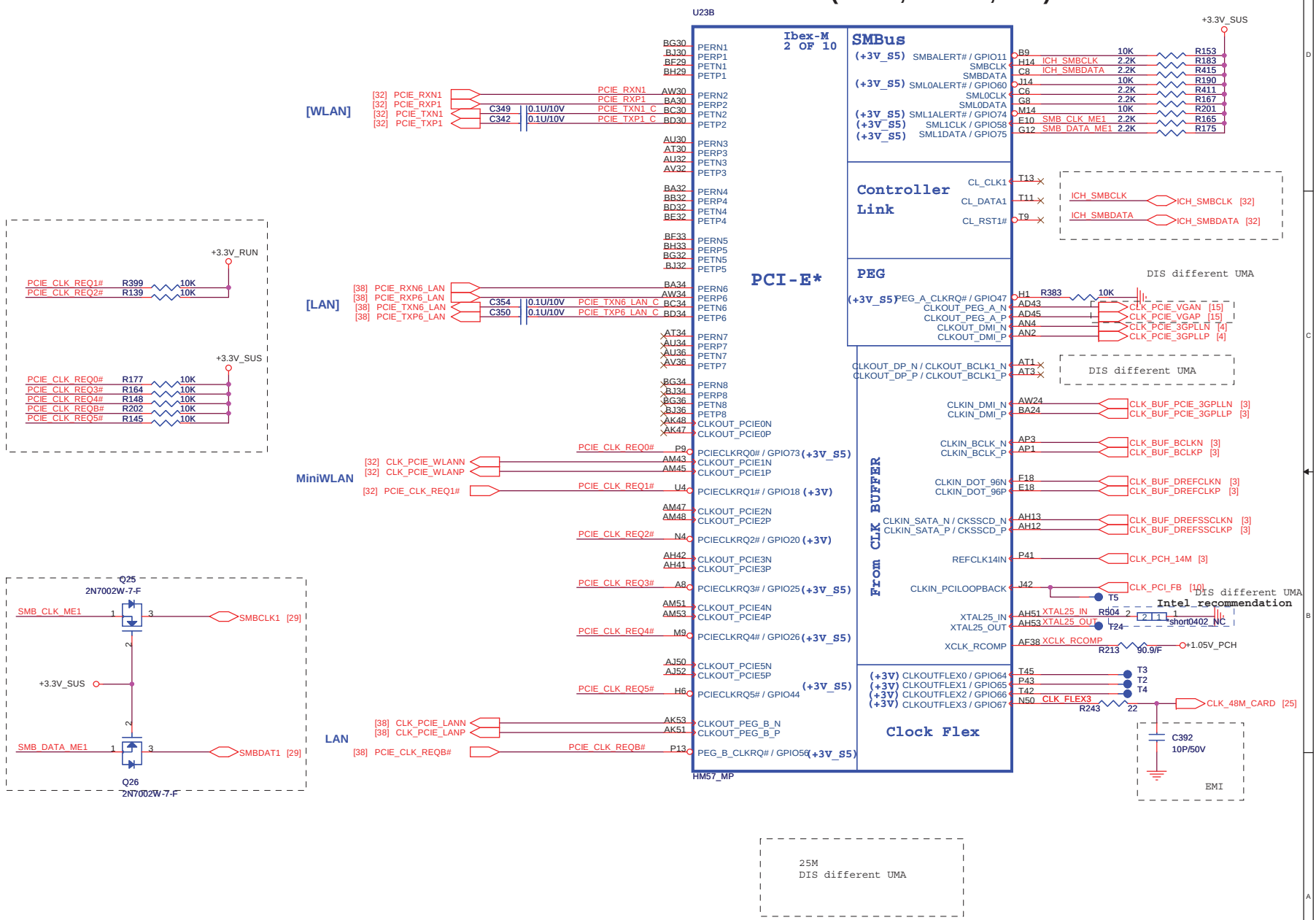
IBEX PEAK-M (GND)



IBEX PEAK-M (PCI-E,SMBUS,CLK)



Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: PCH 2/5 (PCIE, SMBUS, CK)	Rev 3A
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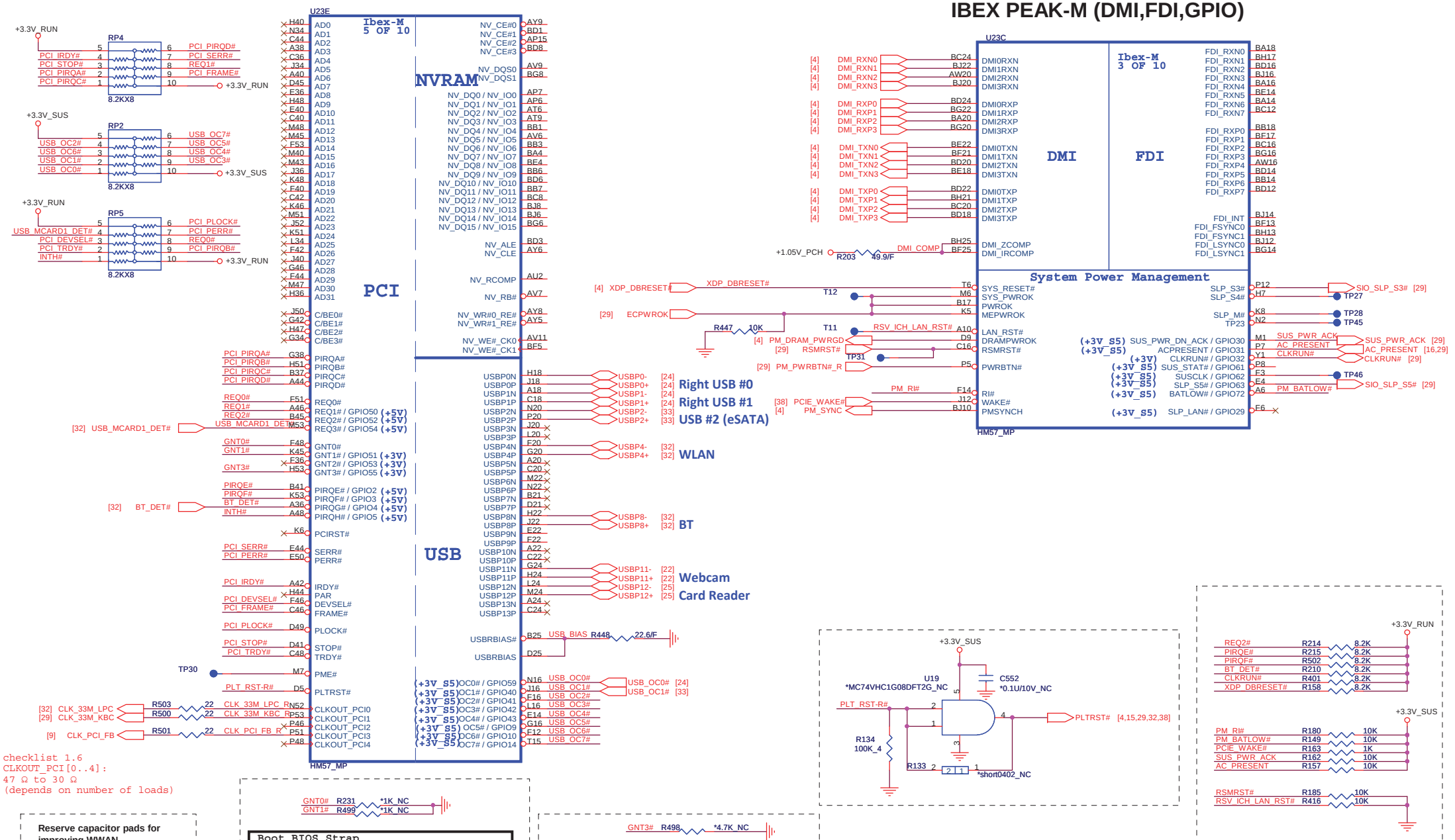
IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (DMI,FDI,GPIO)

Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	3A

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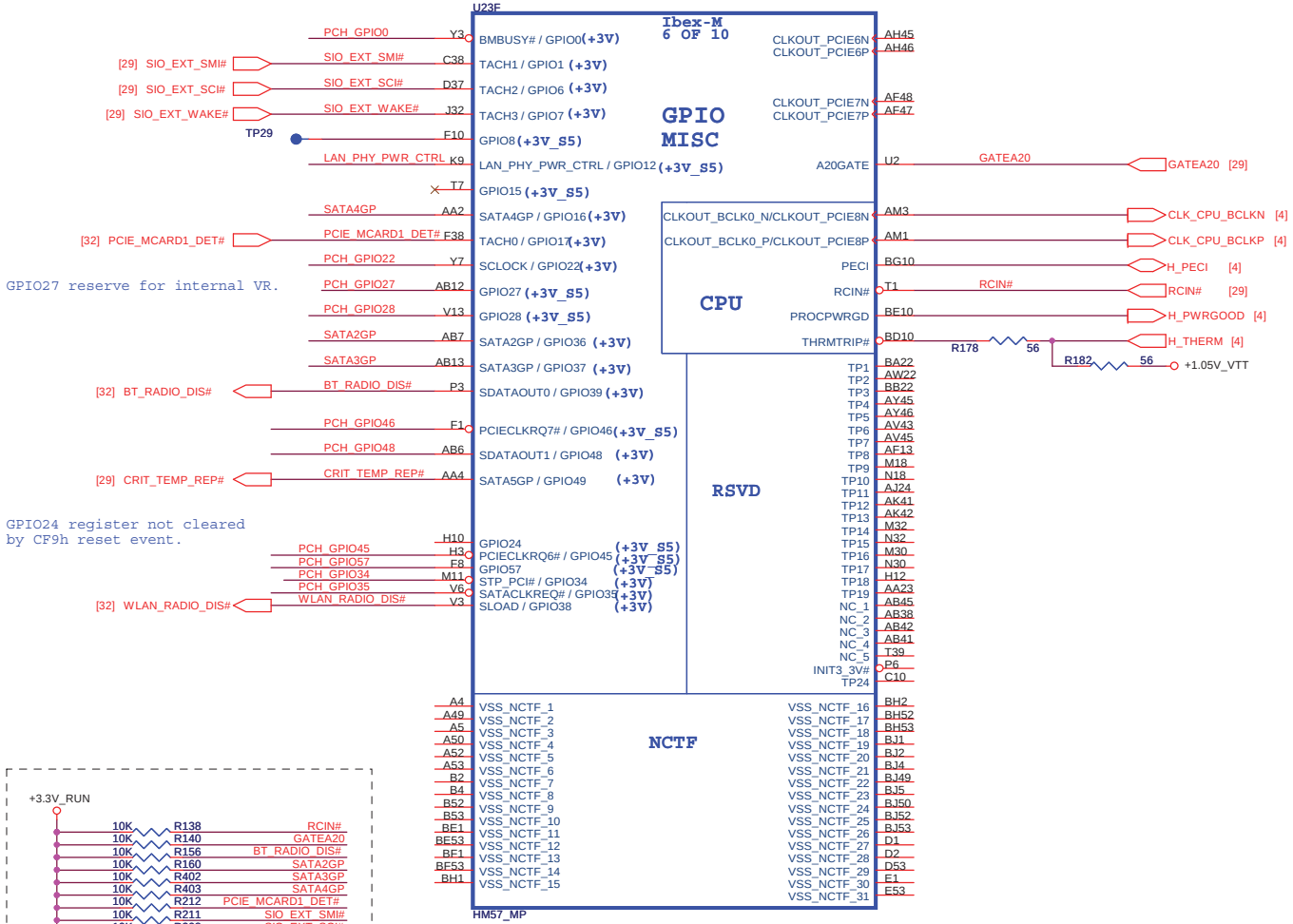
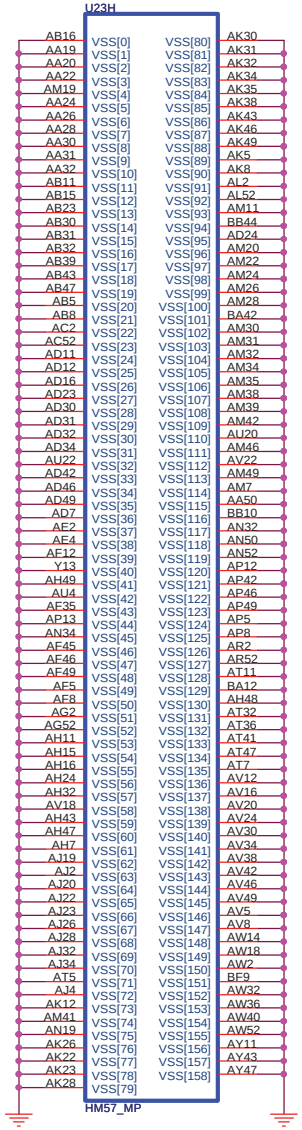
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	3A
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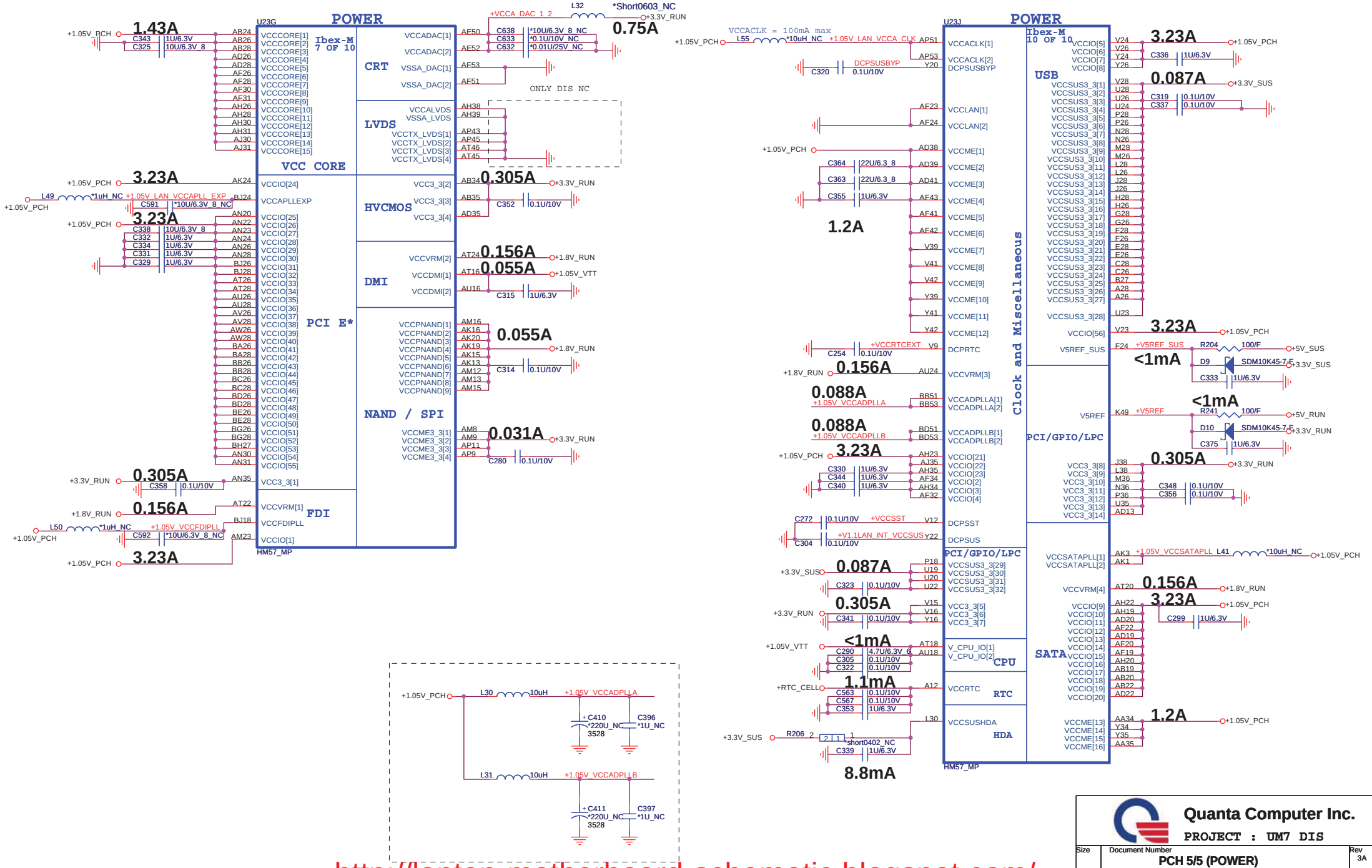
L32 UMA↓
EMI FILTER HCB1608KF-181T15(180,1.5A)
CX000181016

L32 DIS→SHORT



Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	PCH 5/5 (POWER)	3A
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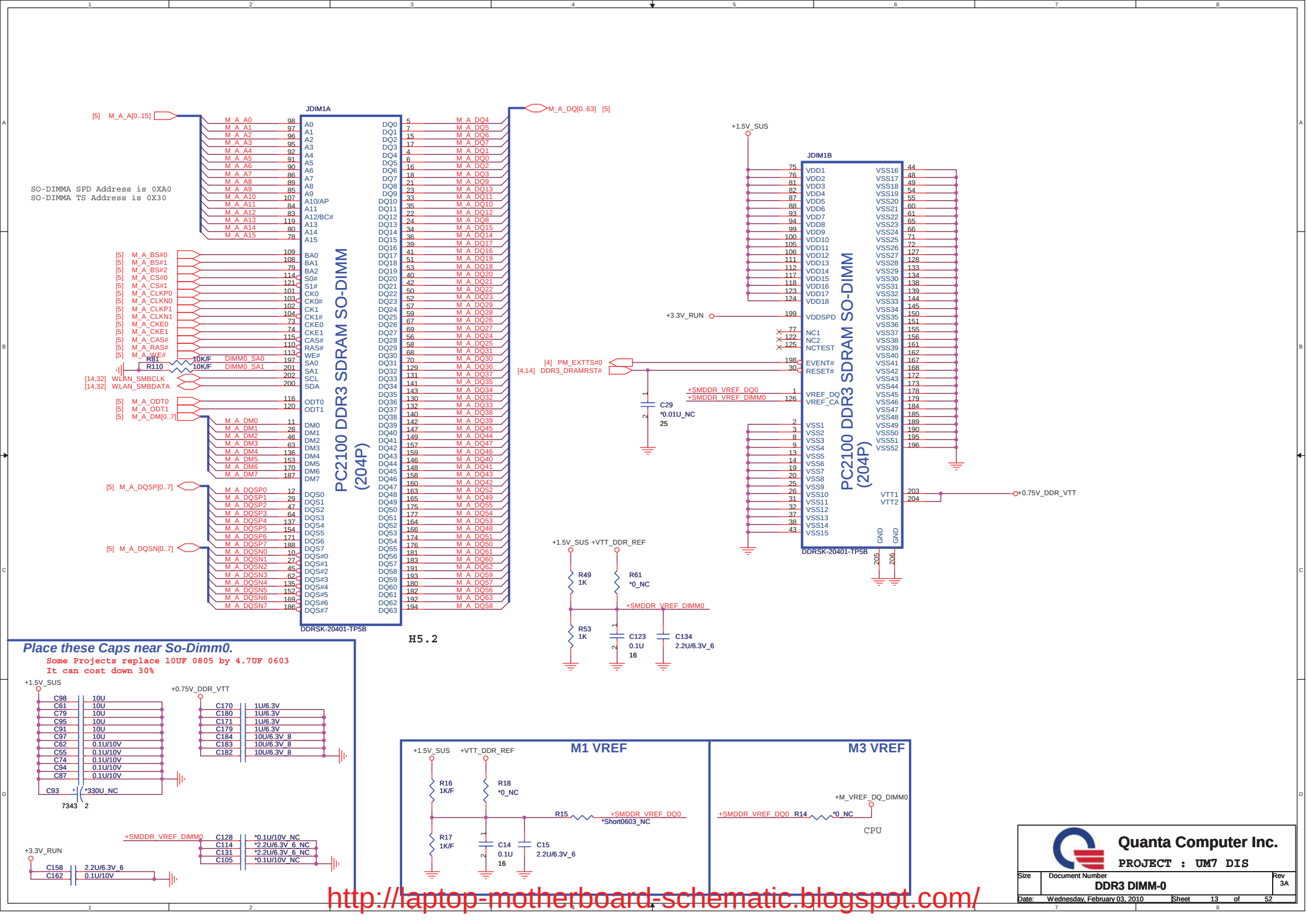

Quanta Computer Inc.

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Size	Document Number	Rev
	DDR3 DIMM-0	3A

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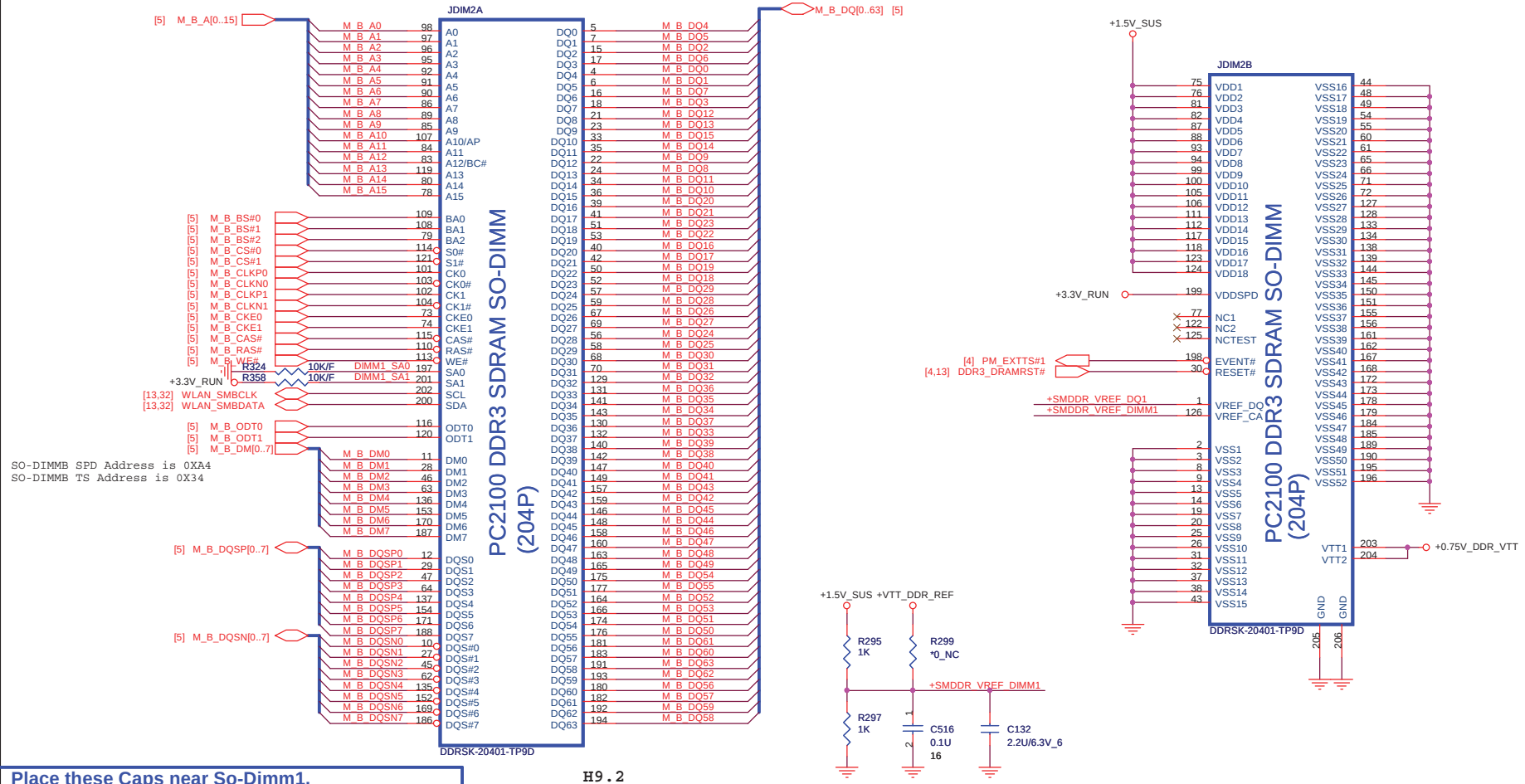
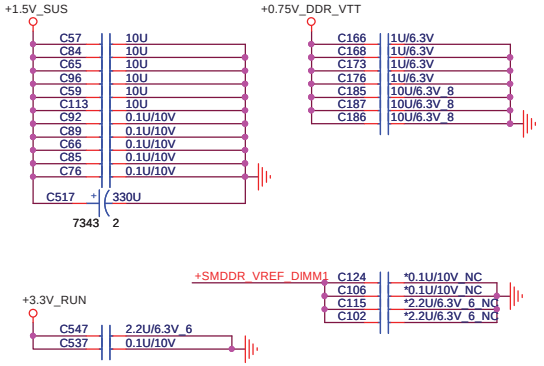


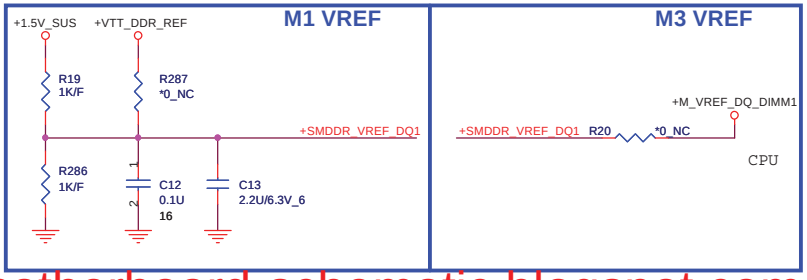
H9.2

Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603

It can cost down 30%





Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	DDR3 DIMM-1	3A

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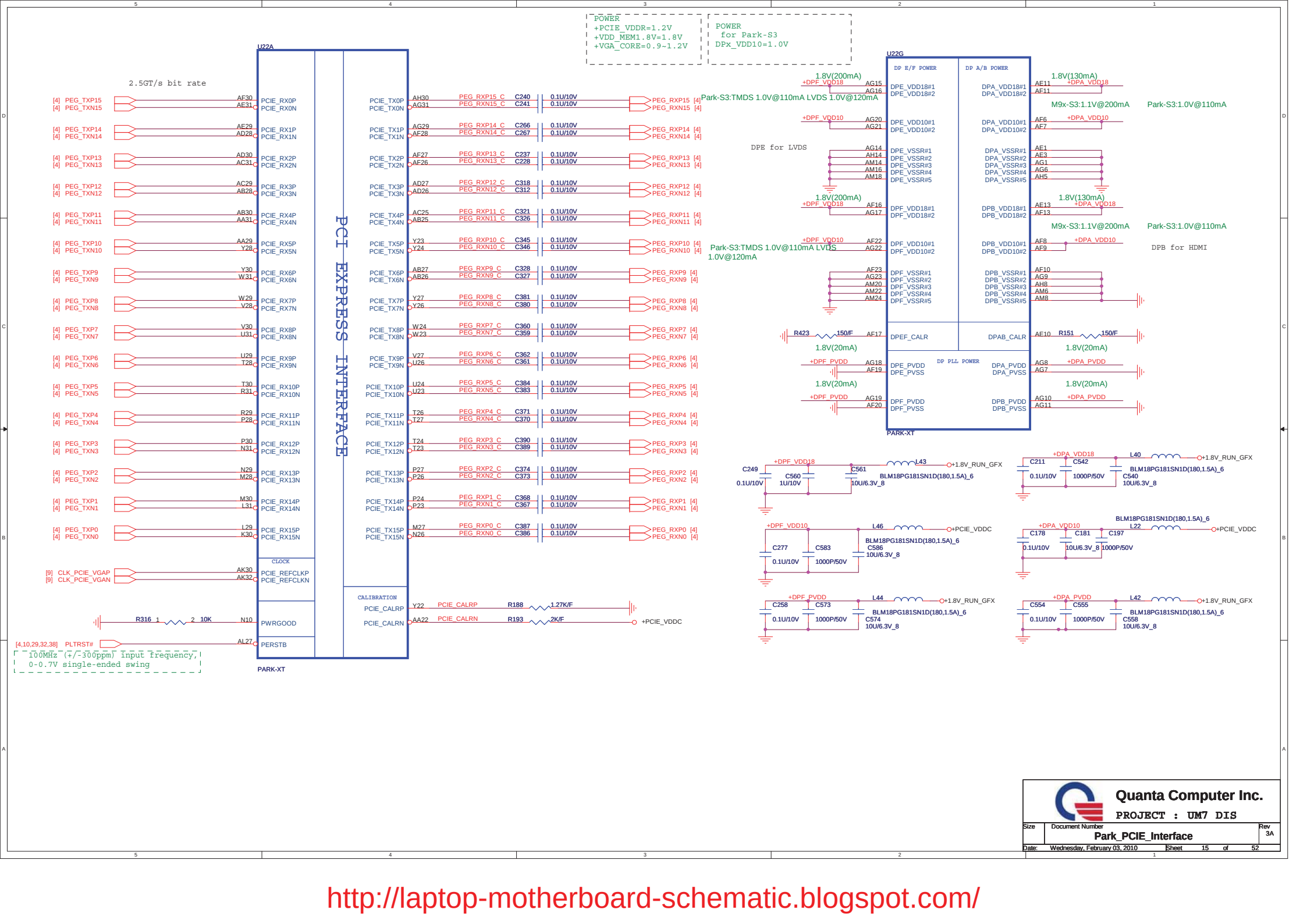

MEM_ID[3:0]	Vendor	Type	Vendor P/N	Quanta P/N
0000	Hynix Orion-die	64*16-800MHZ	H5TQ1G63BFR-12C	AKD5LZGTW00
0001	Samsung E-die	64*16-800MHZ	K4W1G1646E-HC12	AKD5LGGT502
0010	Samsung B-die	128*16-800MHZ	K4W2G1646B-HC12	AKD5MGGT501
0011			Reserved	
0100			Reserved	
0101			Reserved	
0110			Reserved	
0111			Reserved	
1000			Reserved	
1001			Reserved	
1010			Reserved	
1011			Reserved	
1100			Reserved	
1101			Reserved	
1110			Reserved	
1111			Reserved	

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

GPU Power-on sequence

Power-Up

- +3.3V_RUN → +VCC_GFX_CORE
- +PCIE_VDDC → +1.8V_RUN_GFX
- CLK_PCIE_VGAP/N → +1.8V_RUN_GFX
- +3.3V_RUN early +VCC_GFX_CORE /+1.8V_RUN_GFX or when +VCC_GFX_CORE /+1.8V_RUN_GFX up then +3.3V_RUN
- +VCC_GFX_CORE reach 90% and +1.8V_RUN_GFX

power-down

- +1.8V_RUN_GFX → +PCIE_VDDC

PCIe ref clock(CLK_PCIE_VGAA/B) early +1.8V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V

R475 =>
100/F for CLK_VGA_27M CLK Gen
0ohm for Crystal
CS11002FB22
RES CHIP 100 1/16W +-1%(0402)

THERMAL MONITOR

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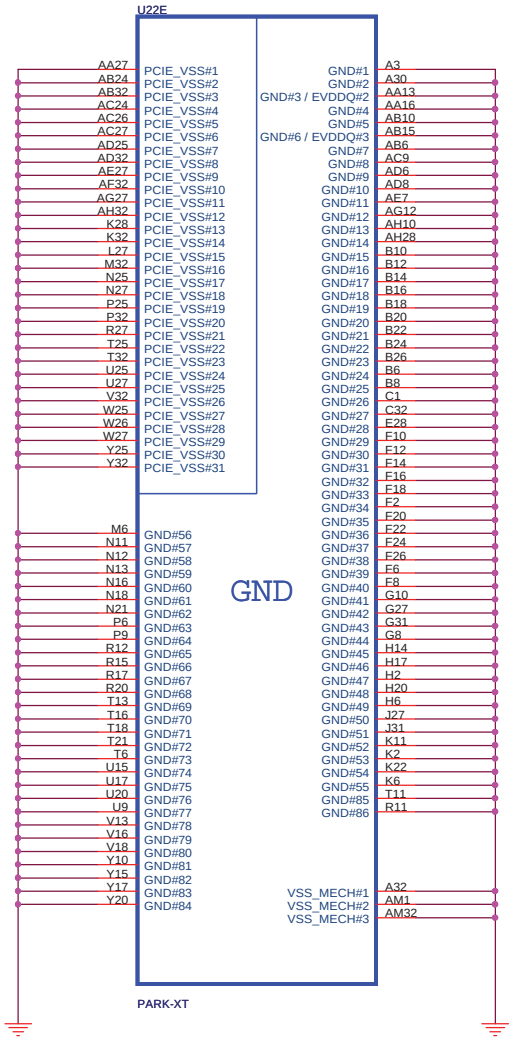

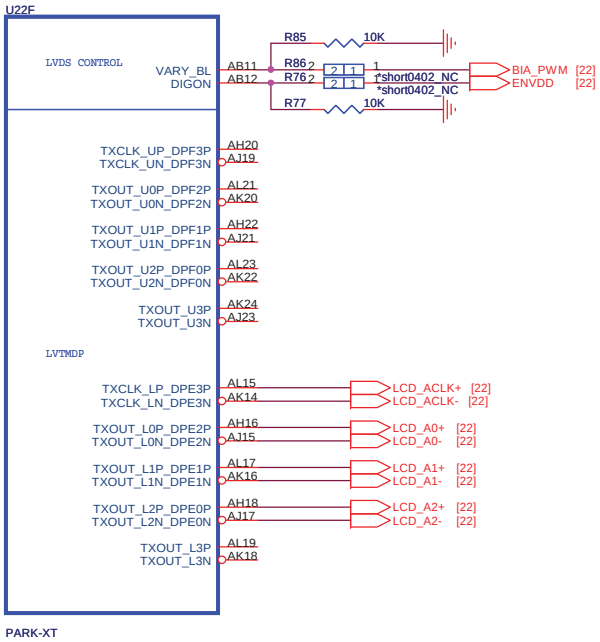

Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	**PCI Express Full TX Output Swing** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	**Enable CLKREQ# Power Management** 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0 0 0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
AUD[0] AUD(1)	VSYNC HSYNC	**AUD[1] AUD[0]** 00 No Audio function 01 Audio for DisplayPort and HDMI if dongle is detected 10 Audio for DisplayPort only 11 Audio for both DisplayPort and HDMI	1 1
VIP_DEVICE_STRAP_ENA	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
RSVD	GENERICC		0

Quanta Computer Inc.
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Size	Document Number	Rev
	Park_GND / LVDS/ Straps	3A
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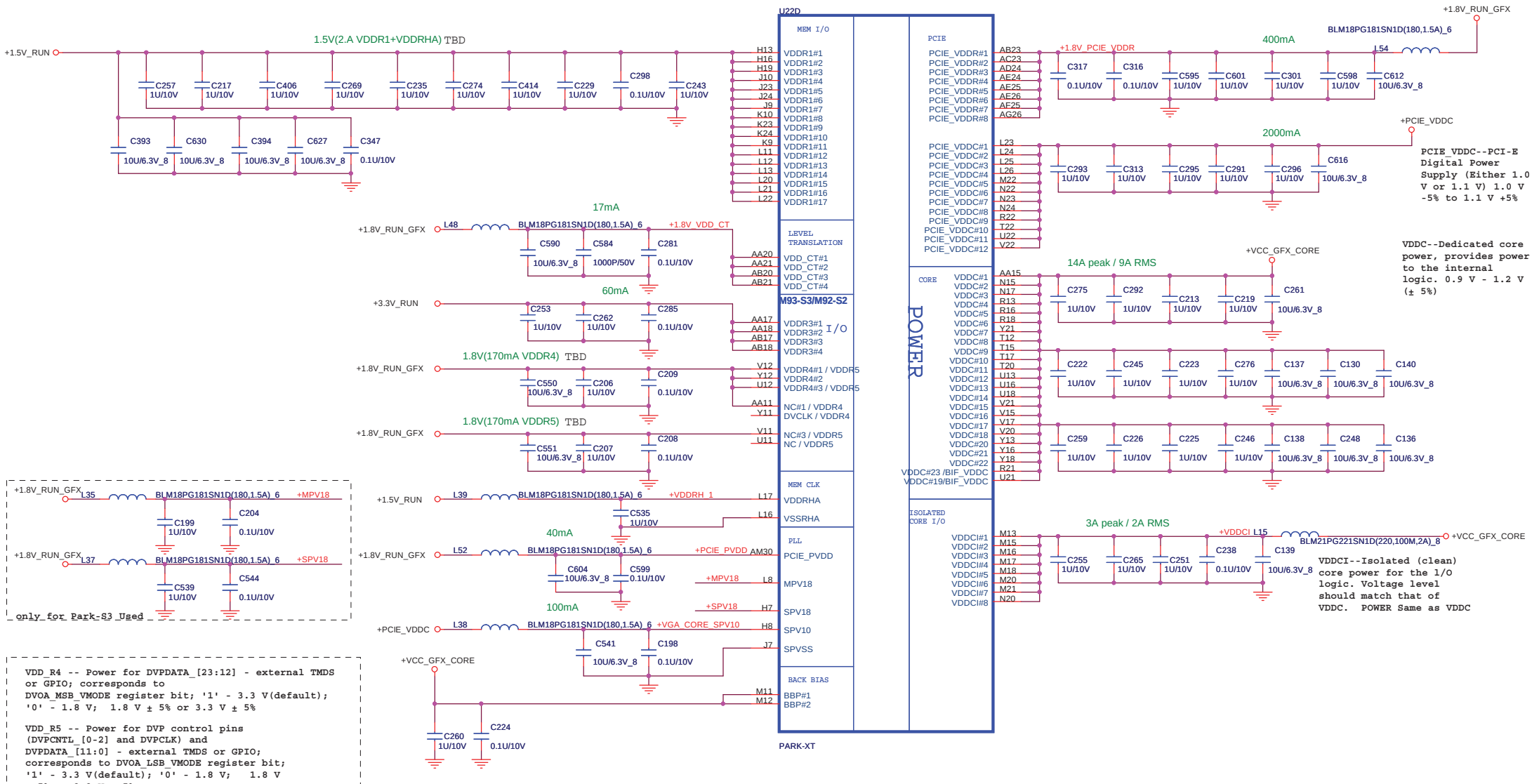
PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%



Quanta Computer Inc.

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Size	Document Number	Rev
	Park_Power_and_NC	3A
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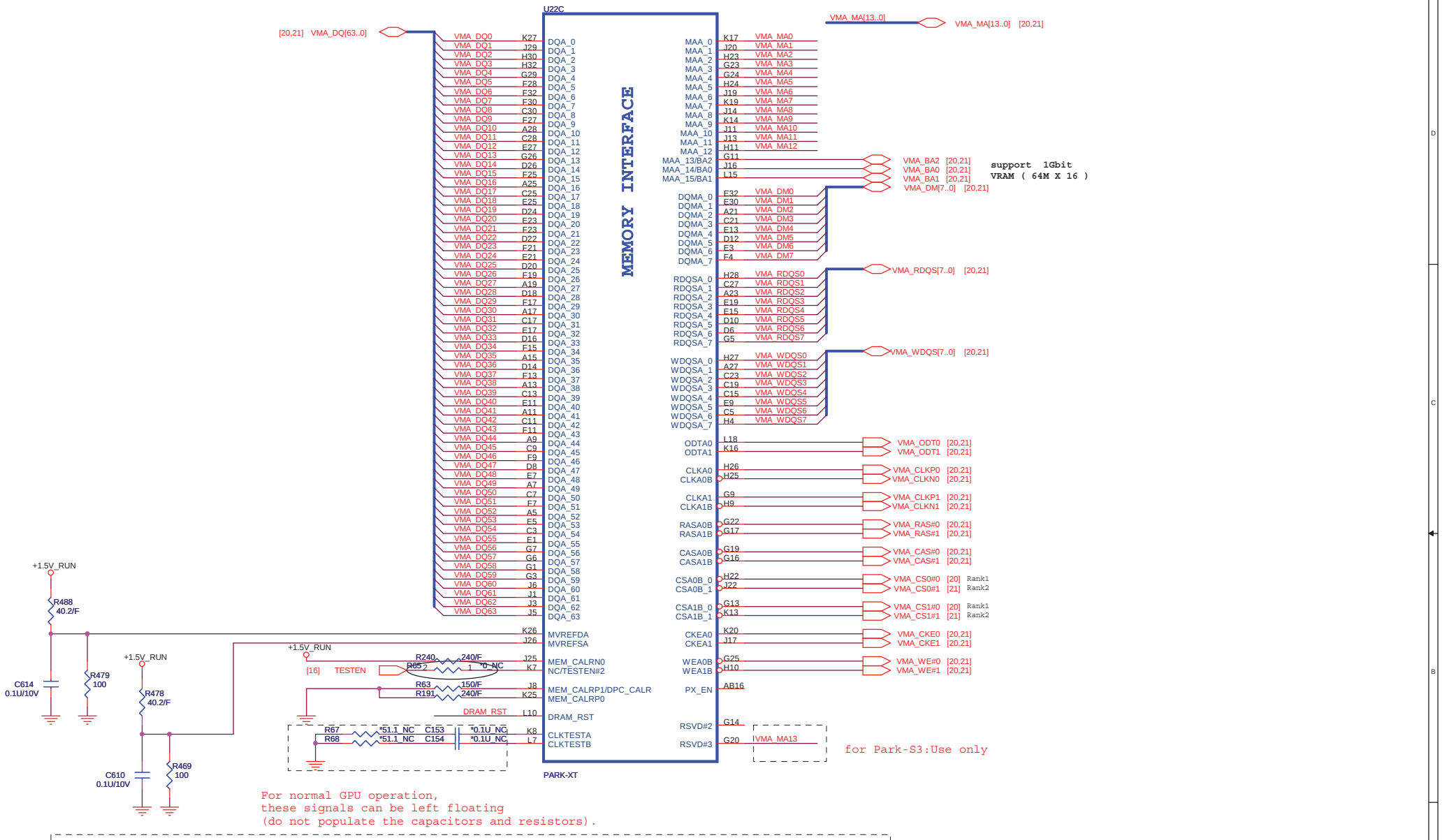
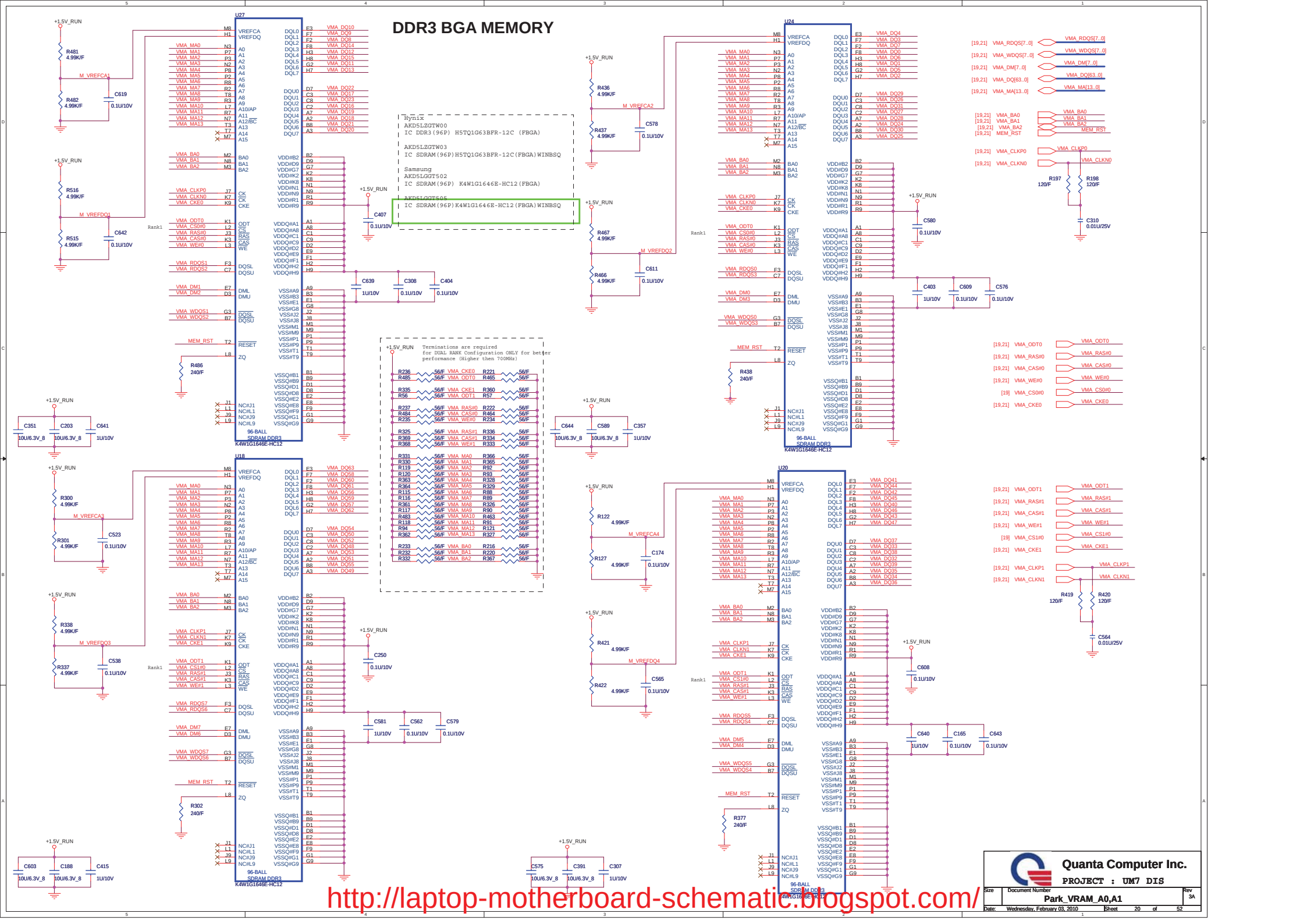


	M9x-S2/S3	Park-S3
MEM_CALRN0(J25) MEM_CALRP0(K25)	NC	240R
MEM_CALRP1(J8)	240R	150R
TESTEN2#2(K7)	NC	0R
R1	NC	10K
R2	0R	51R
R3	2.2K	NC
C1	2.2nF	68pF

Quanta Computer Inc.
PROJECT : UM7 DIS

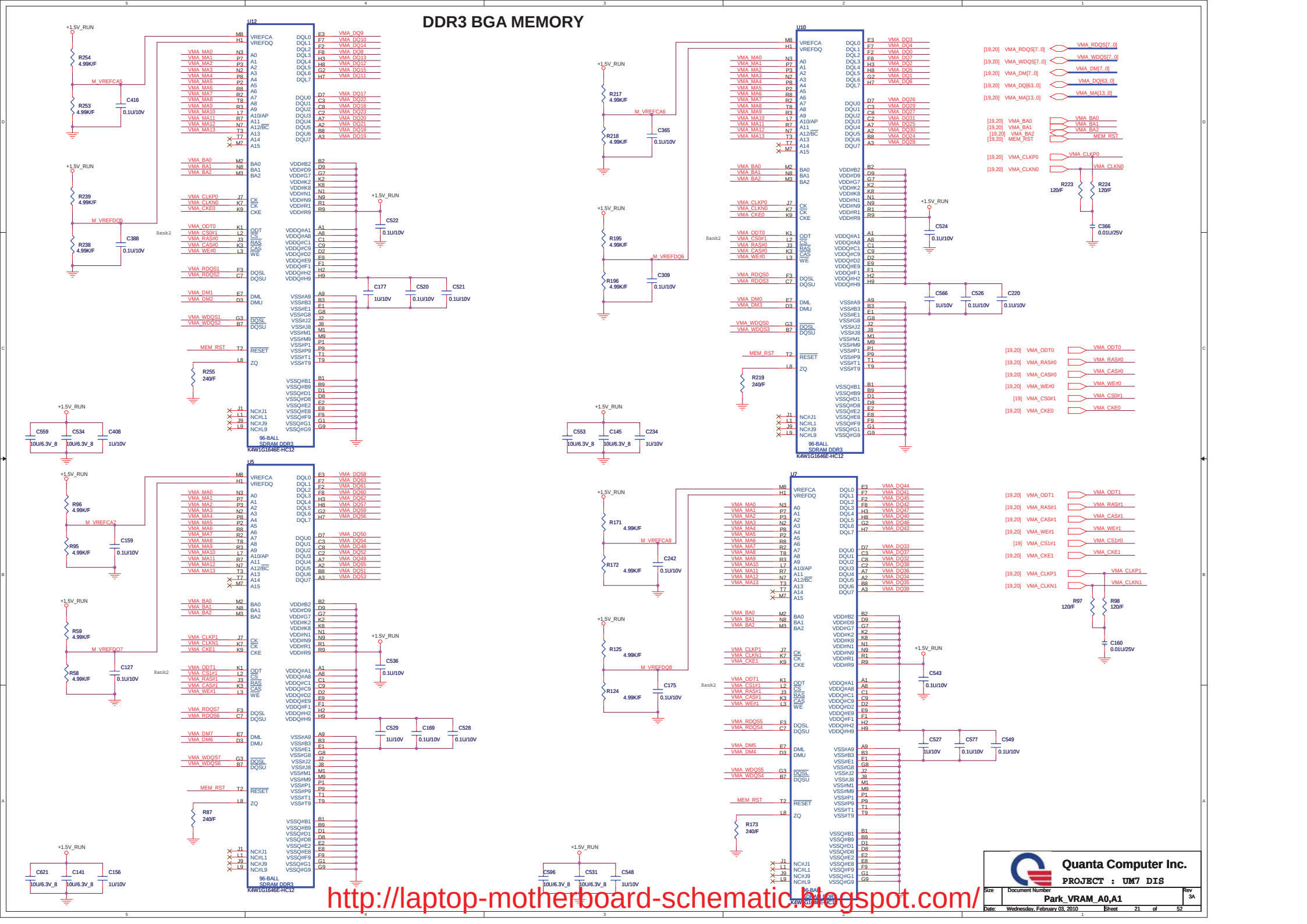
Size	Document Number	Rev
	Park_MEM_Interface	3A
Date: Wednesday, February 03, 2010	Sheet 19 of 52	

DDR3 BGA MEMORY



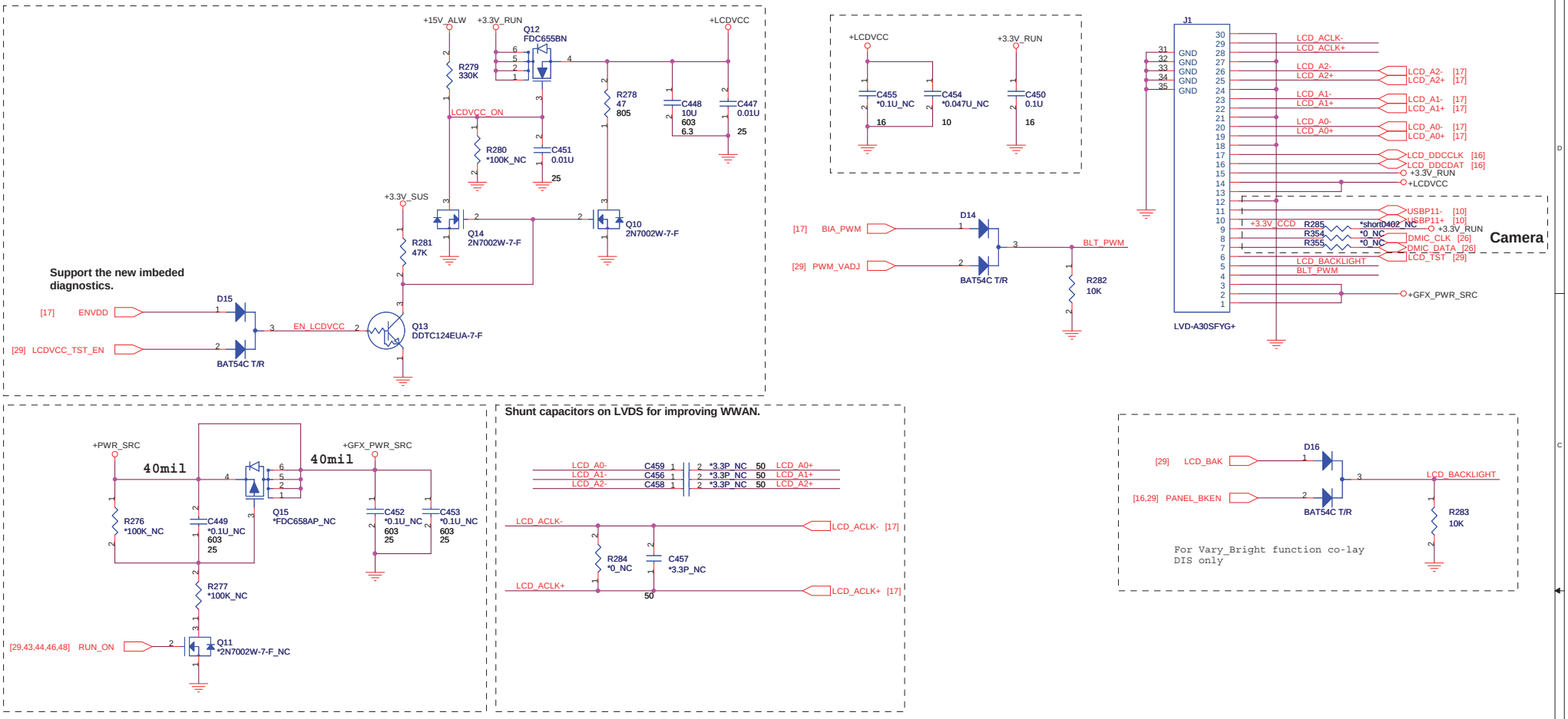
Quanta Computer Inc.			
PROJECT : UM7 DIS			
Size	Document Number		Rev
	Park_VRAM_A0,A1		3A
Date: Wednesday, February 03, 2010	Sheet 20 of 52		

DDR3 BGA MEMORY



Quanta Computer Inc.
PROJECT : UM7 DIS

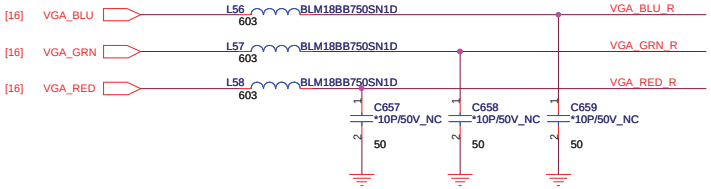
Size	Document Number	Rev
	Park_VRAM_A0,A1	3A
Date: Wednesday, February 03, 2010	Sheet 21 of 52	

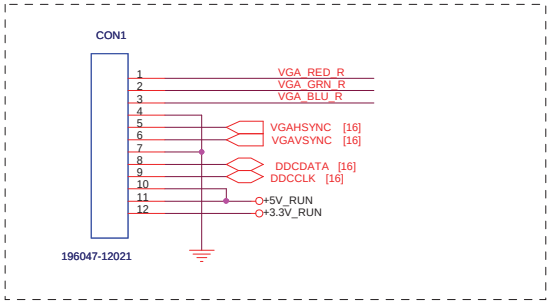


Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	LCD CONN / HDMI CONN	3A
Date: Wednesday, February 03, 2010	Sheet 22 of 52	



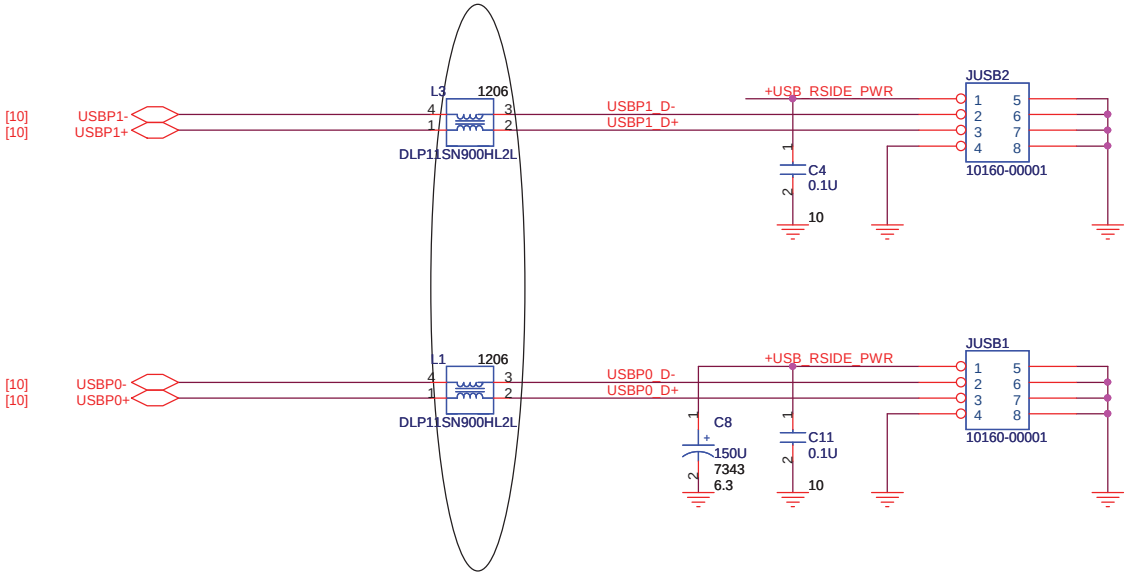


Quanta Computer Inc.

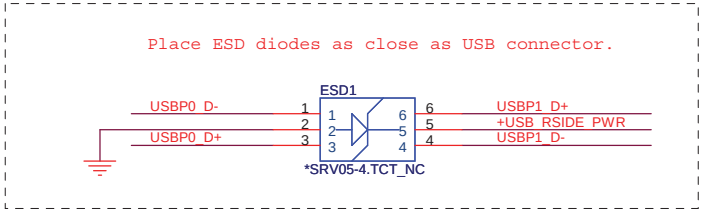
PROJECT : UM7 DIS

Size	Document Number	Rev
	CRT CONN	3A

Date: Wednesday, February 03, 2010 Sheet 23 of 52

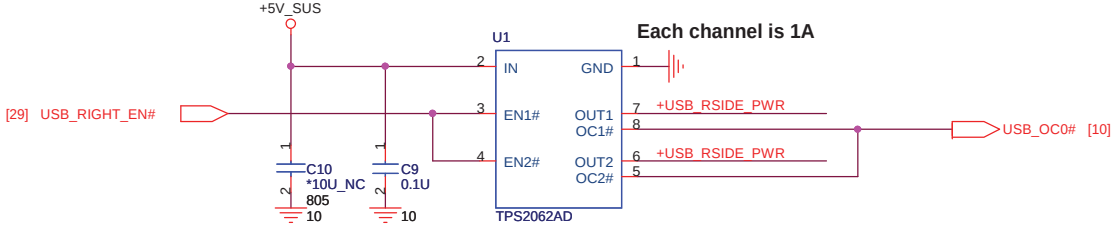


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

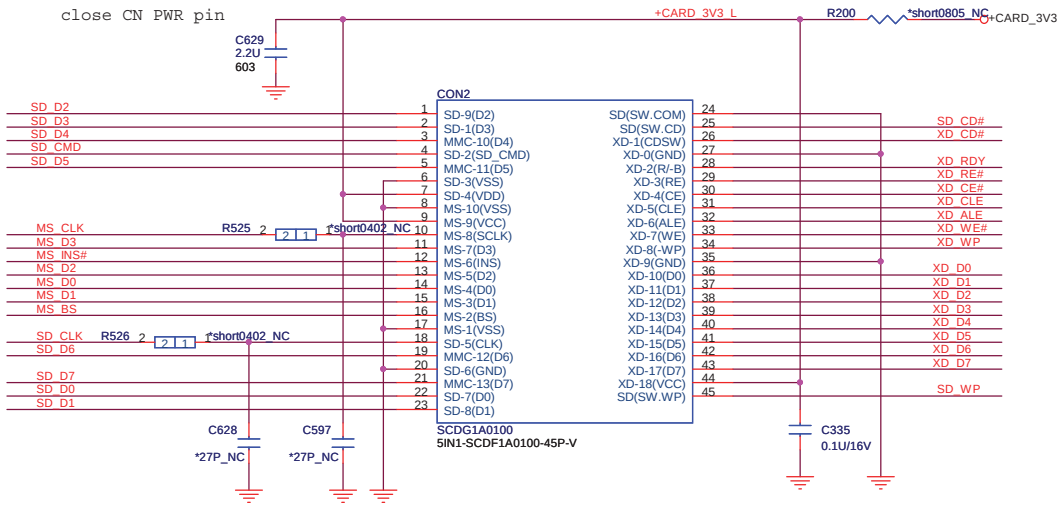


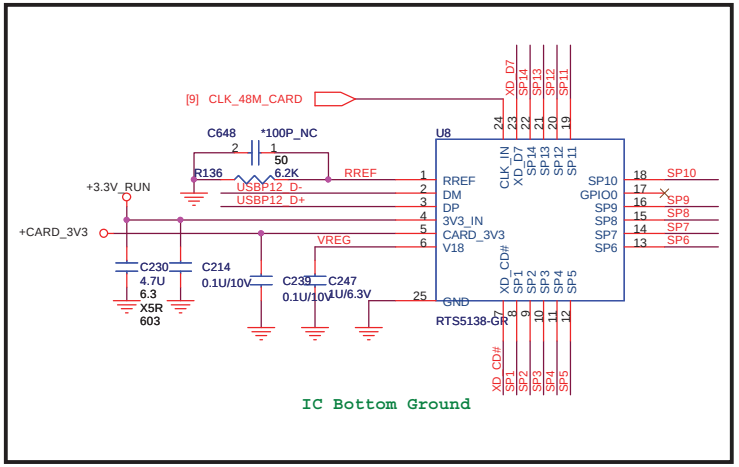
Place one 150uF cap by each USB connector.

Each channel is 1A

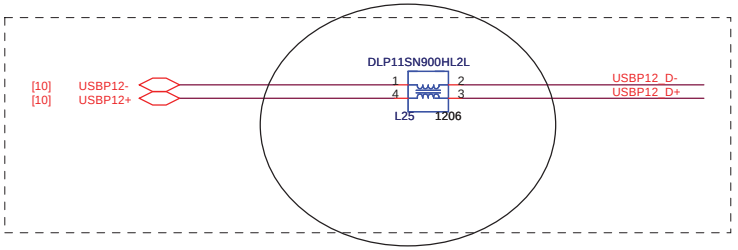


Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number	Rev
	Right USB	3A
Date: Wednesday, February 03, 2010	Sheet 24 of 52	





RTS5138-QFN24

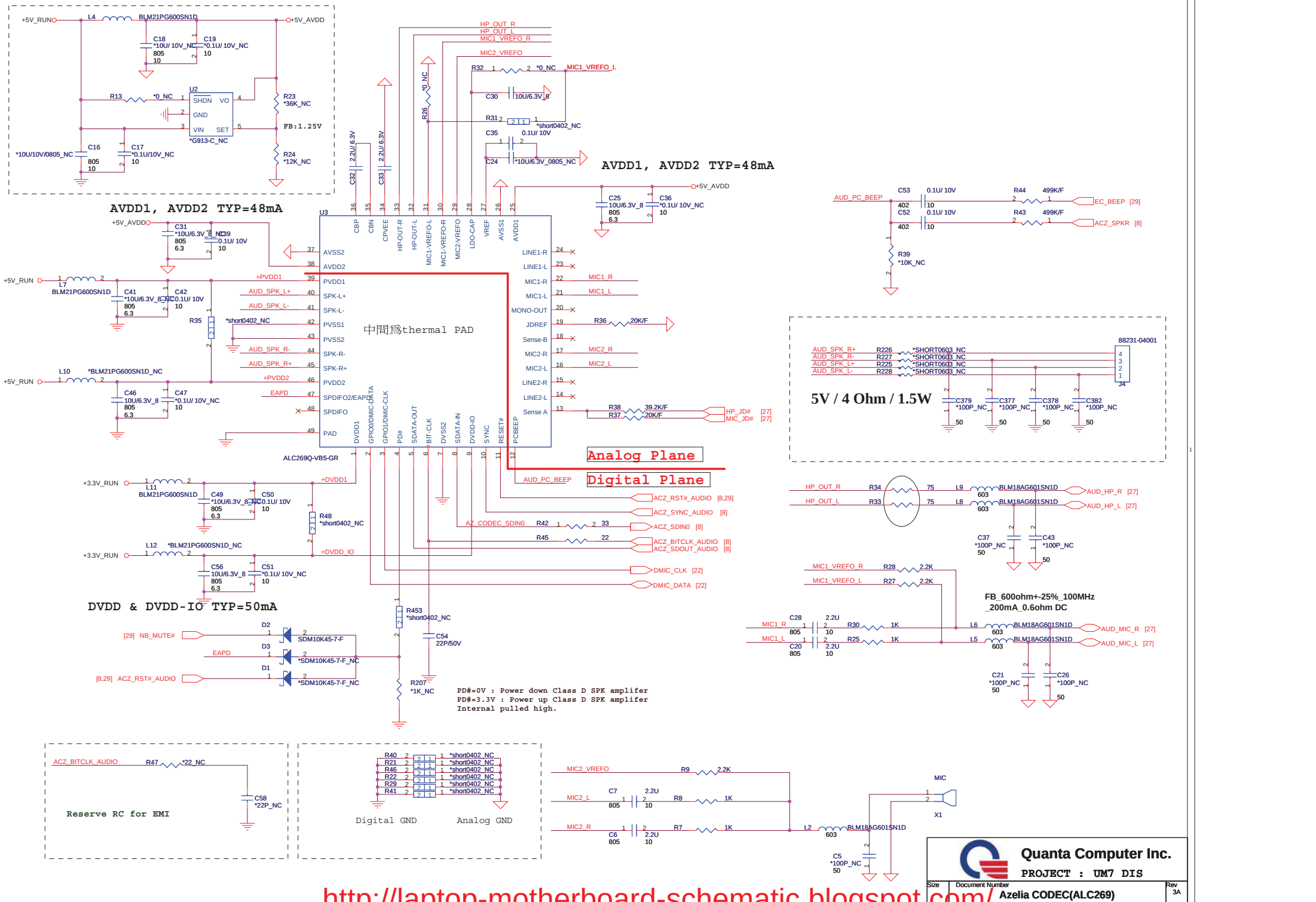


SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

Share Pin

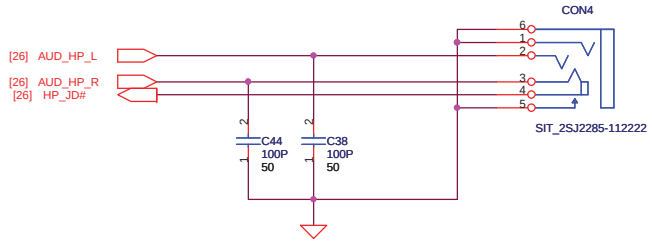
Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	Card Reader(RST5138)	3A
Date: Wednesday, February 03, 2010	Sheet 25 of 52	



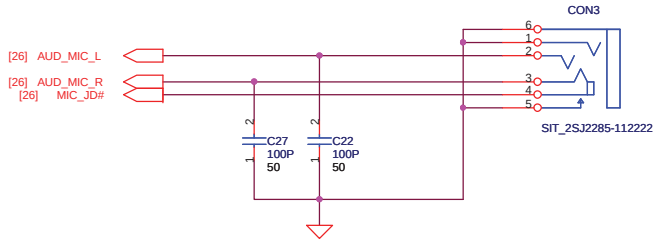
HP JACKN

SUYIN NORMAL OPEN



MIC JACK

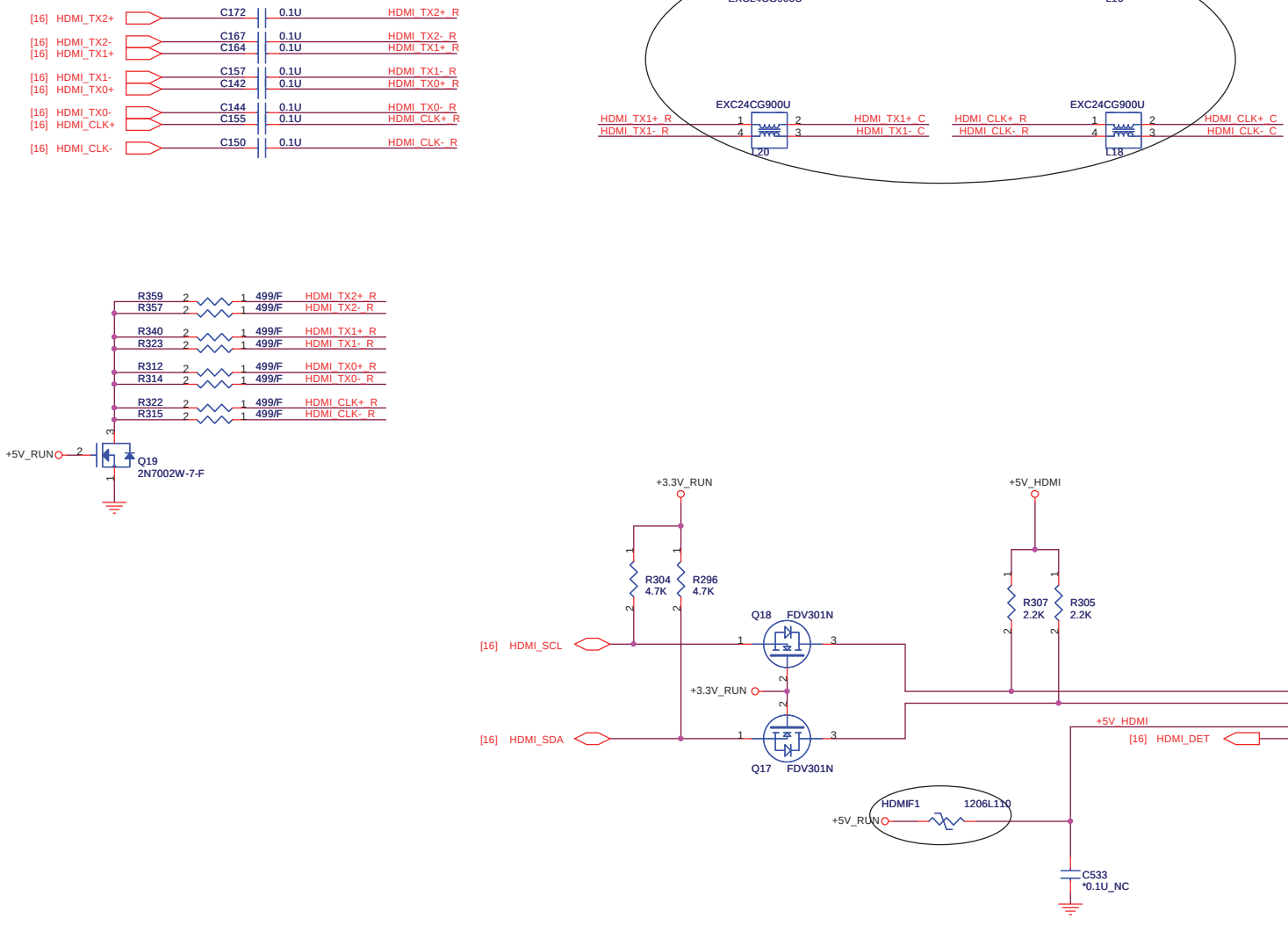
SUYIN NORMAL OPEN



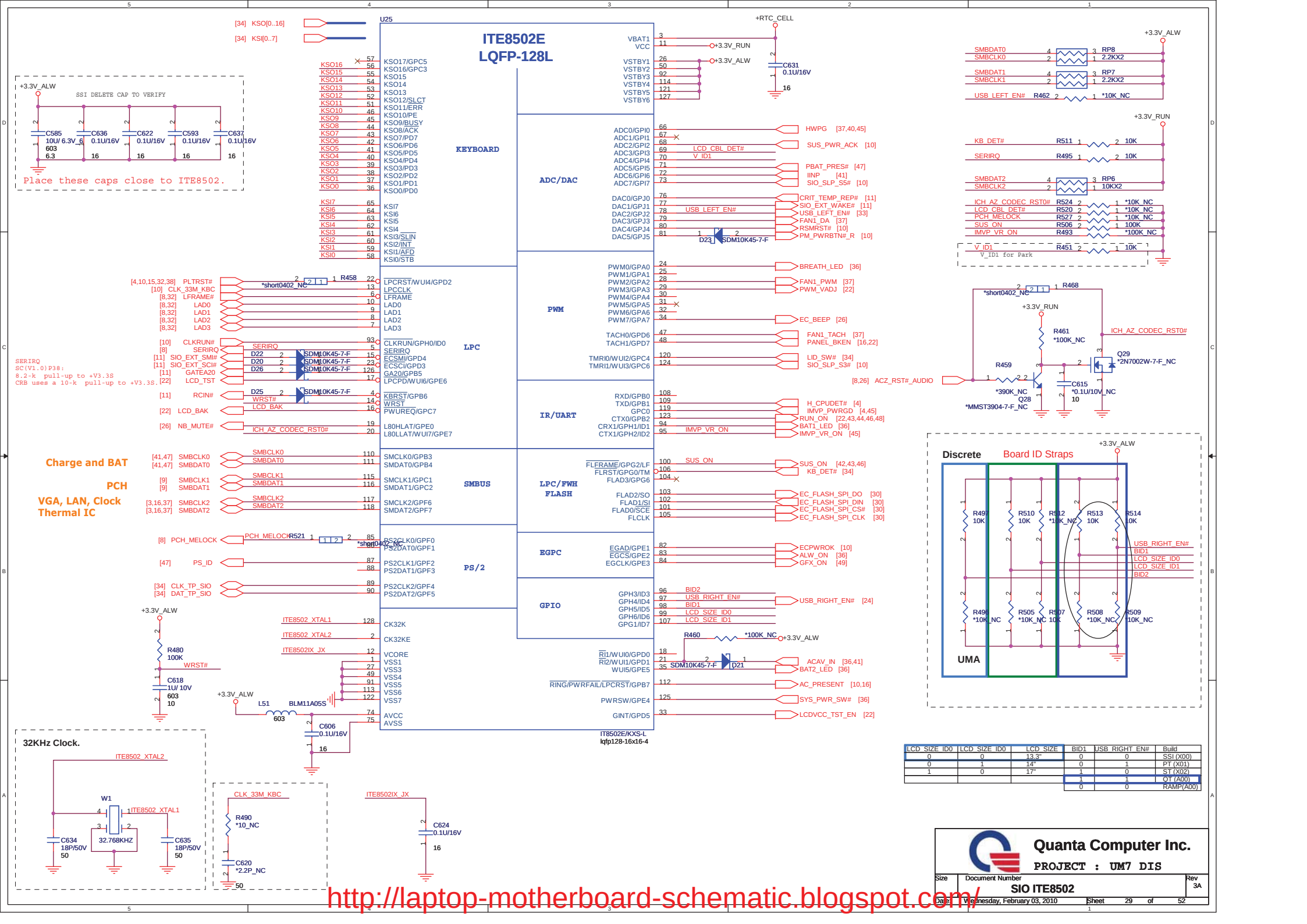
Quanta Computer Inc.

PROJECT : UM7 DIS

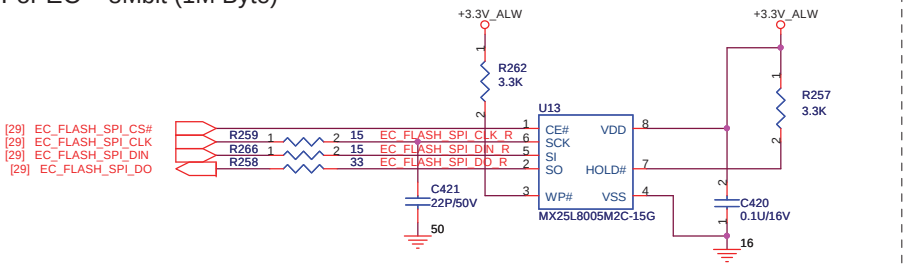
Size	Document Number	Rev
	AUDIO CONN	3A
Date:	Wednesday, February 03, 2010	Sheet 27 of 52



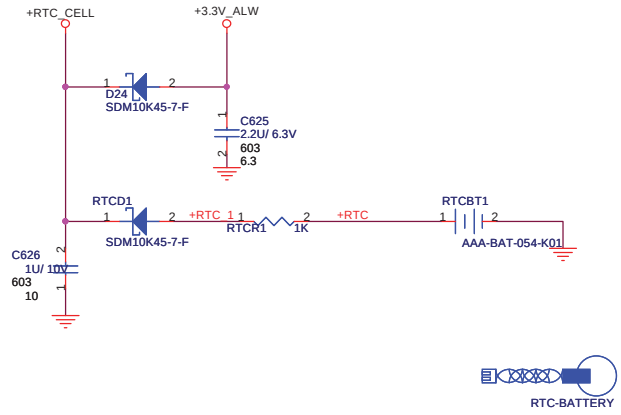
Quanta Computer Inc.			
PROJECT : UM7 DIS			
Size	Document Number		Rev
	Blank		3A
Date:	Wednesday, February 03, 2010	Sheet 28 of 52	


ITE8502E
LQFP-128L
U25
KEYBOARD
ADC/DAC
PWM
LPC
IR/UART
SMBUS
LPC/FWH
FLASH
EGPC
PS/2
GPIO
Place these caps close to ITE8502.
SSI DELETE CAP TO VERIFY
Charge and BAT
PCH
VGA, LAN, Clock
Thermal IC
32KHz Clock.
Discrete
Board ID Straps
UMA
Quanta Computer Inc.
PROJECT : UM7 DIS
SIO ITE8502
Wednesday, February 03, 2010
http://laptop-motherboard-schematic.blogspot.com/

For EC 8Mbit (1M Byte)



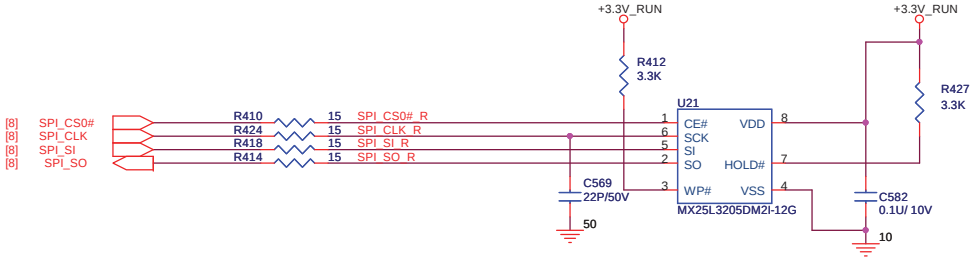
RTC BATTERY



For PCH

32Mbit (4M Byte)

2nd source:AKE39ZP0N00



Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	FLASH/RTC	3A
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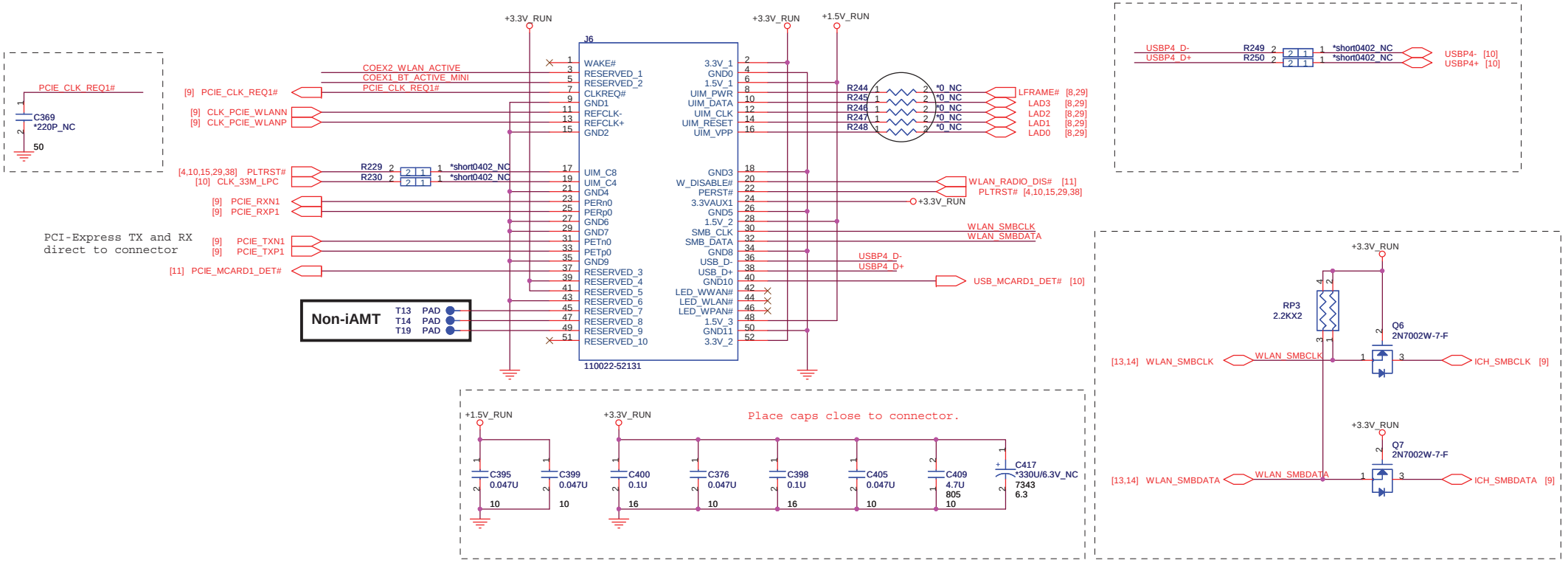
Quanta Computer Inc.

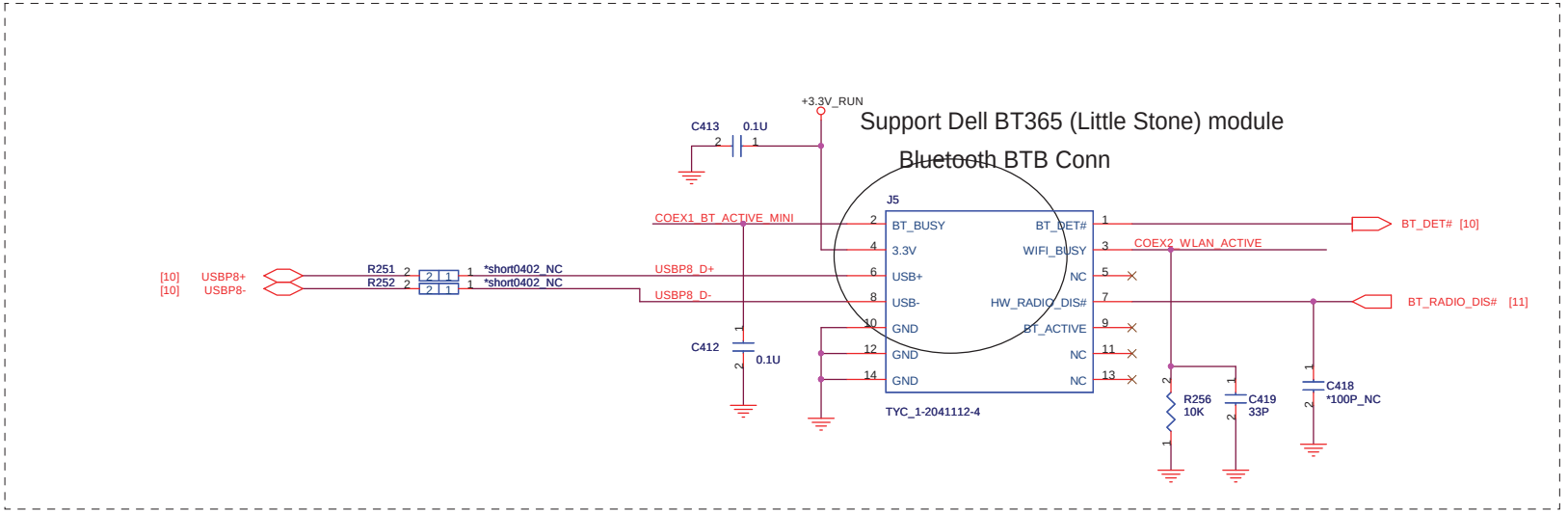
PROJECT : UM7 DIS

Size	Document Number	Rev
	MINI-Card WWAN	3A

Date: Wednesday, February 03, 2010 Sheet 31 of 52

MiniCard WLAN connector



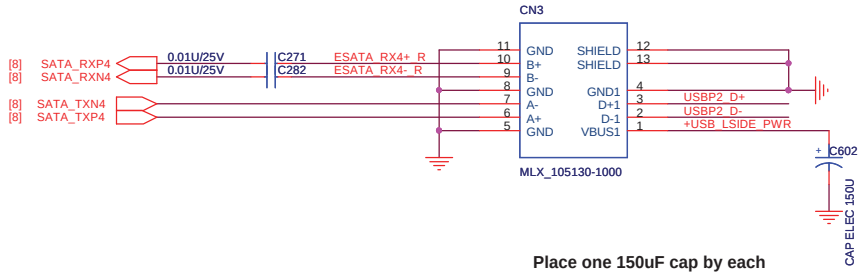


Quanta Computer Inc.

PROJECT : UM7 DIS

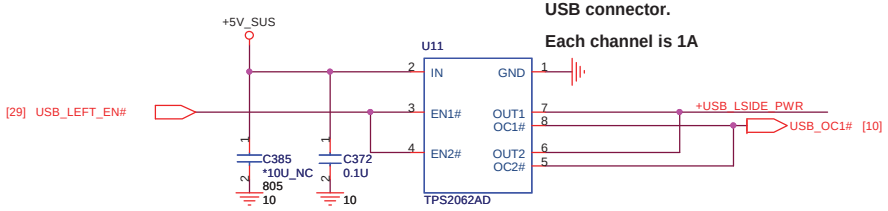
Size	Document Number	Rev
	MINI-Card WLAN / BT	3A
Date: Wednesday, February 03, 2010	Sheet 32 of 52	

USB and eSATA Conn.

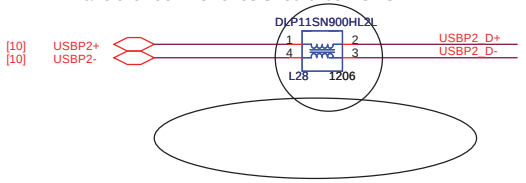


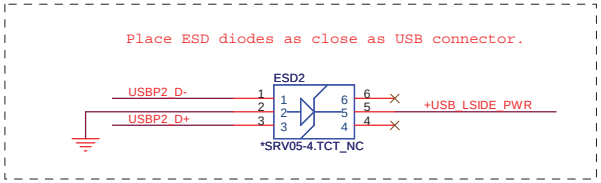
Place one 150uF cap by each USB connector.

Each channel is 1A



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

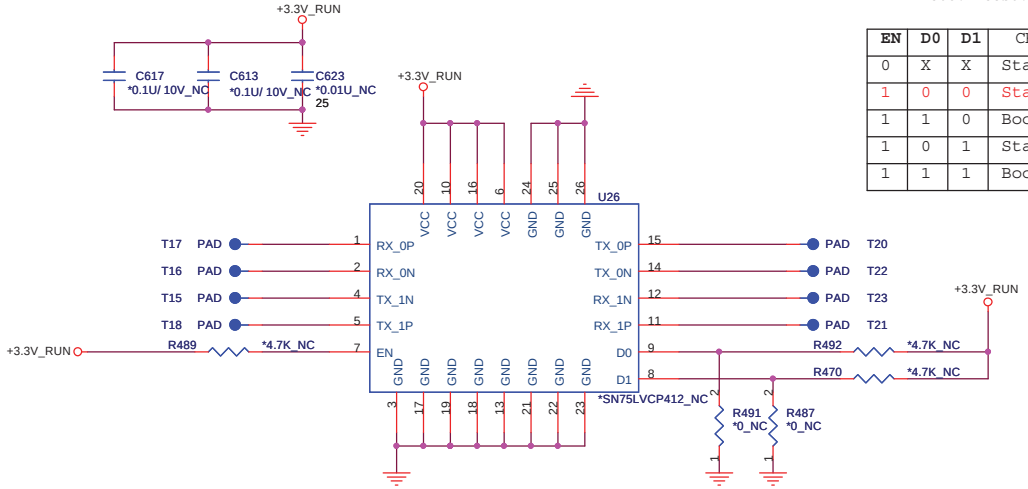




E-SATA Re-driver

Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost



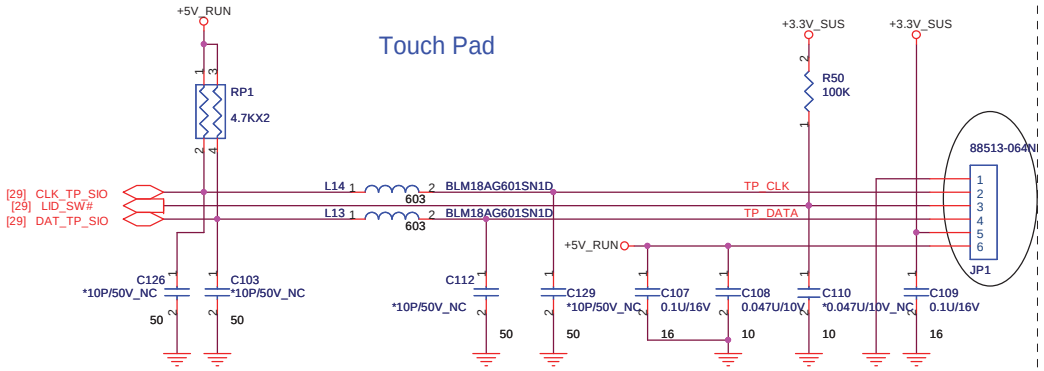
Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	eSATA & Right USB	3A

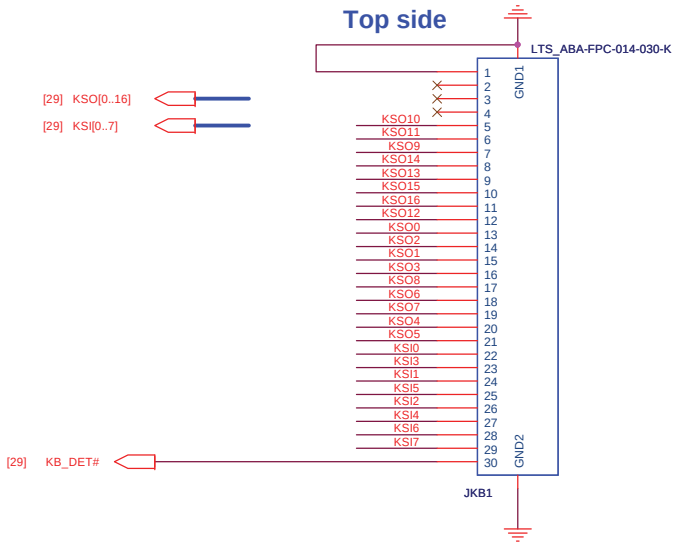
Date: Wednesday, February 03, 2010 Sheet 33 of 52

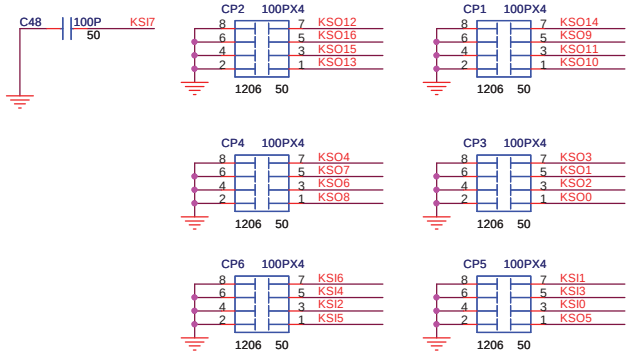
Touch Pad



KEYBOARD CONNECTOR

Top side

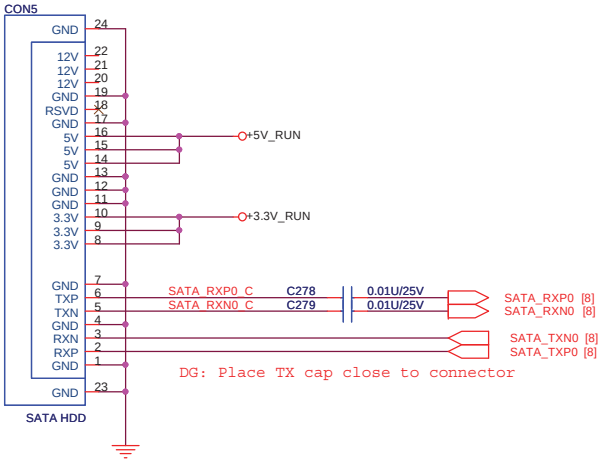


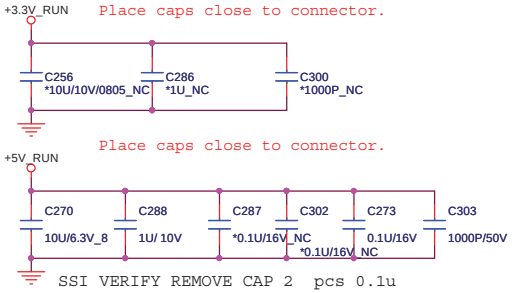


100P CAPS CLOSE TO JKB1

Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: TOUCH PAD, KB	Rev: 3A
Date: Wednesday, February 03, 2010	Sheet 34 of 52	

SATA Connector.



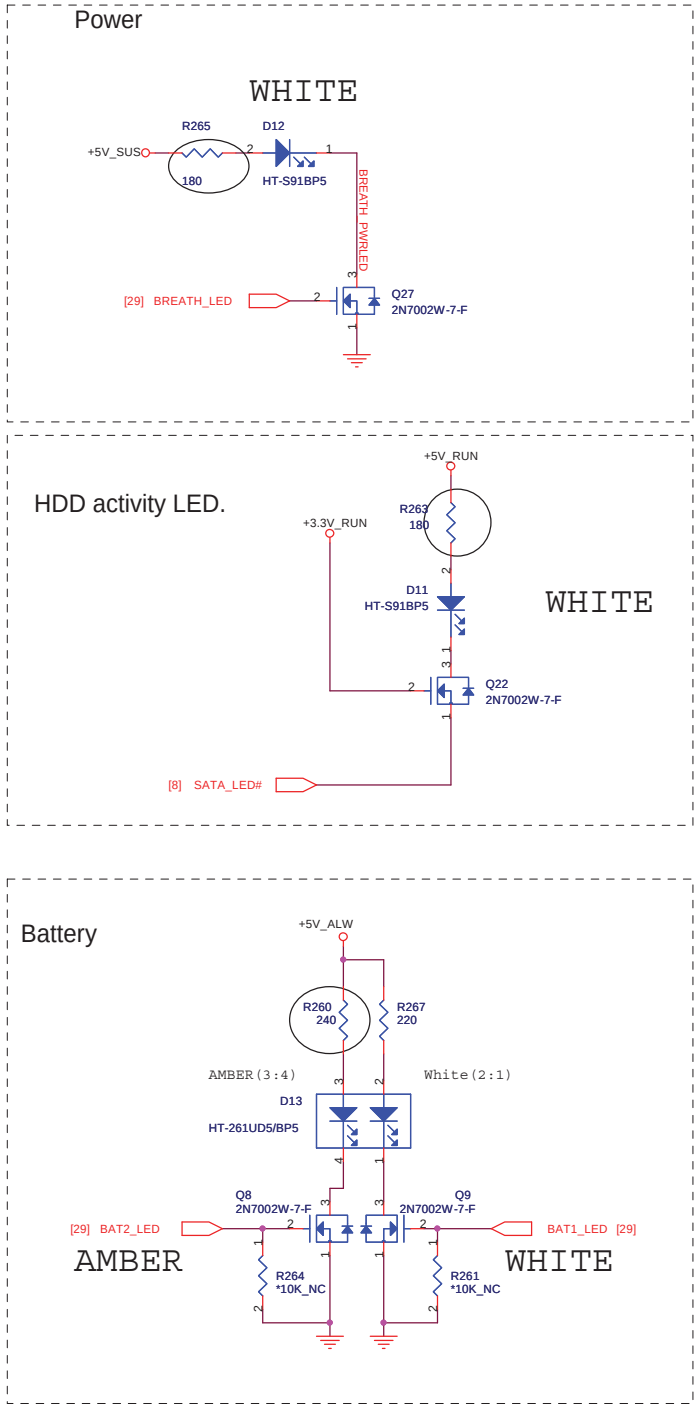


Quanta Computer Inc.

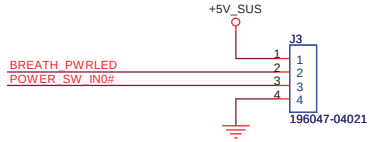
PROJECT : UM7 DIS

Size	Document Number	Rev
	SATA (HDD&CD_ROM)	3A

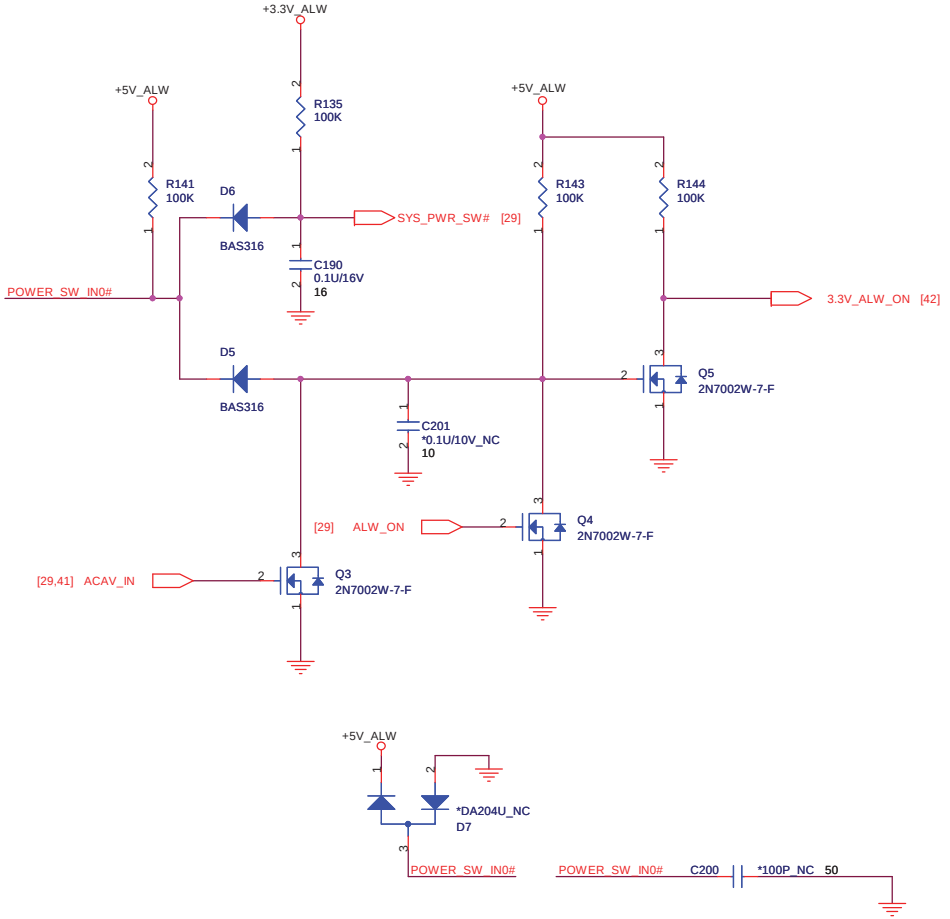
Date: Wednesday, February 03, 2010 Sheet 35 of 52



Power button Cable

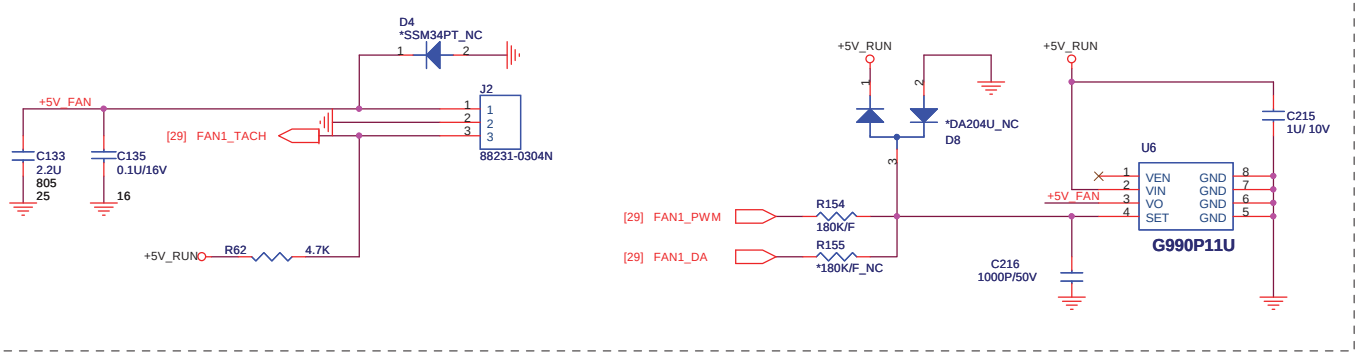


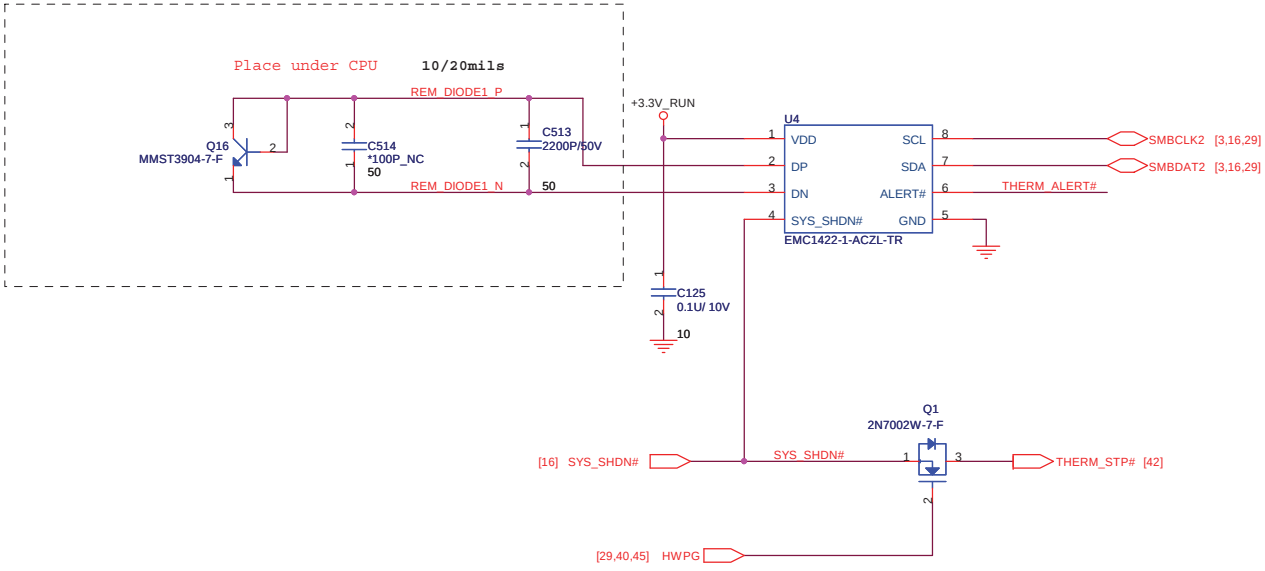
3VALW ON POWER LOGIC

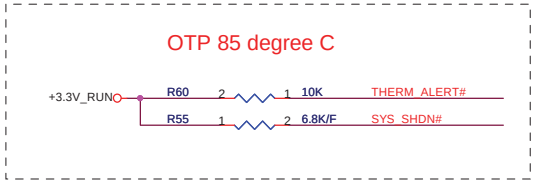


Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: SWITCH, LED	Rev: 3A
Date: Wednesday, February 03, 2010	Sheet 36 of 52	

FAN CONTROL





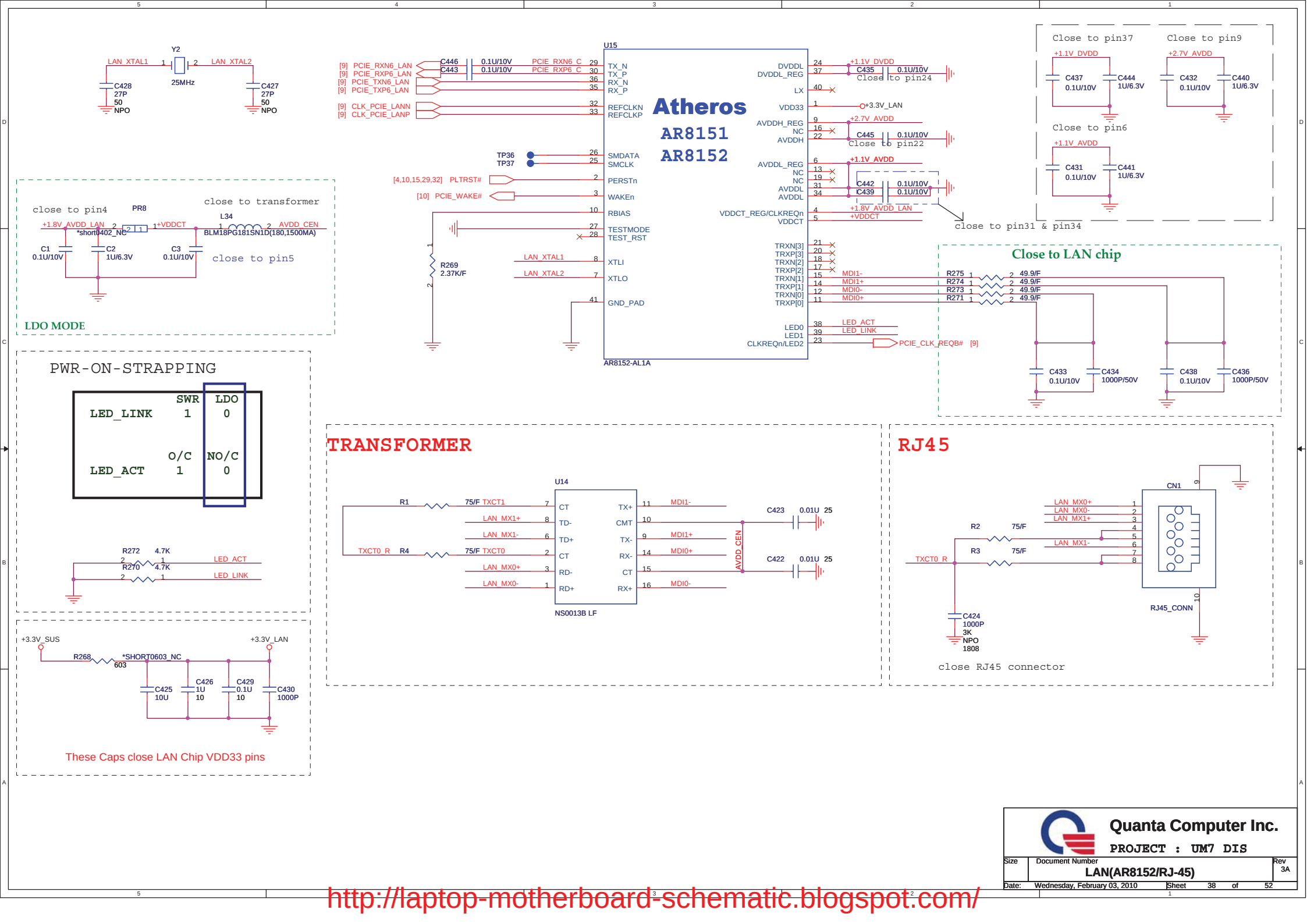


Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	FAN & THERMAL	3A

Date: Wednesday, February 03, 2010 Sheet 37 of 52

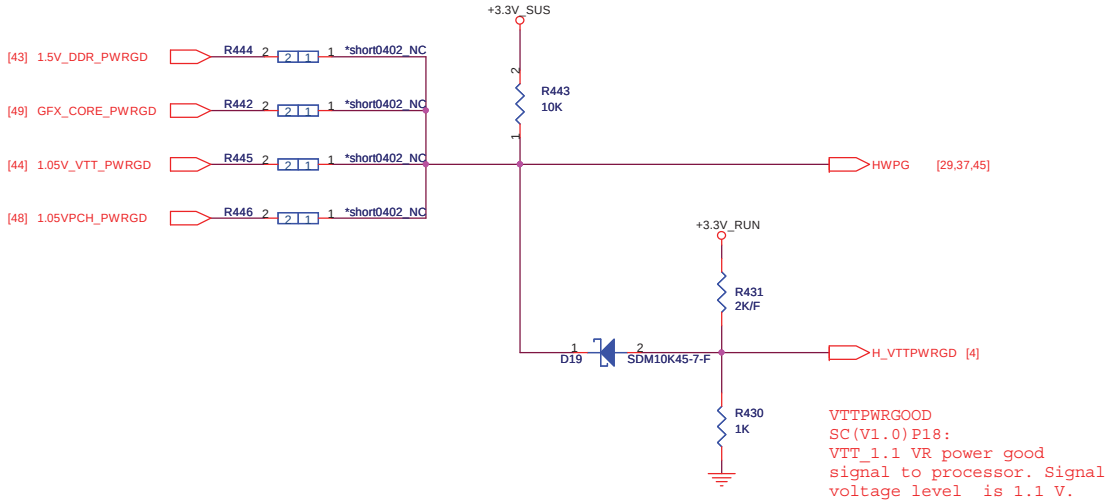


Quanta Computer Inc.	PROJECT : UM7 DIS
Size	Document Number: LAN(AR8152/RJ-45) — Rev 3A
Date: Wednesday, February 03, 2010	Sheet 38 of 52

Quanta Computer Inc.

PROJECT : UM7 DIS

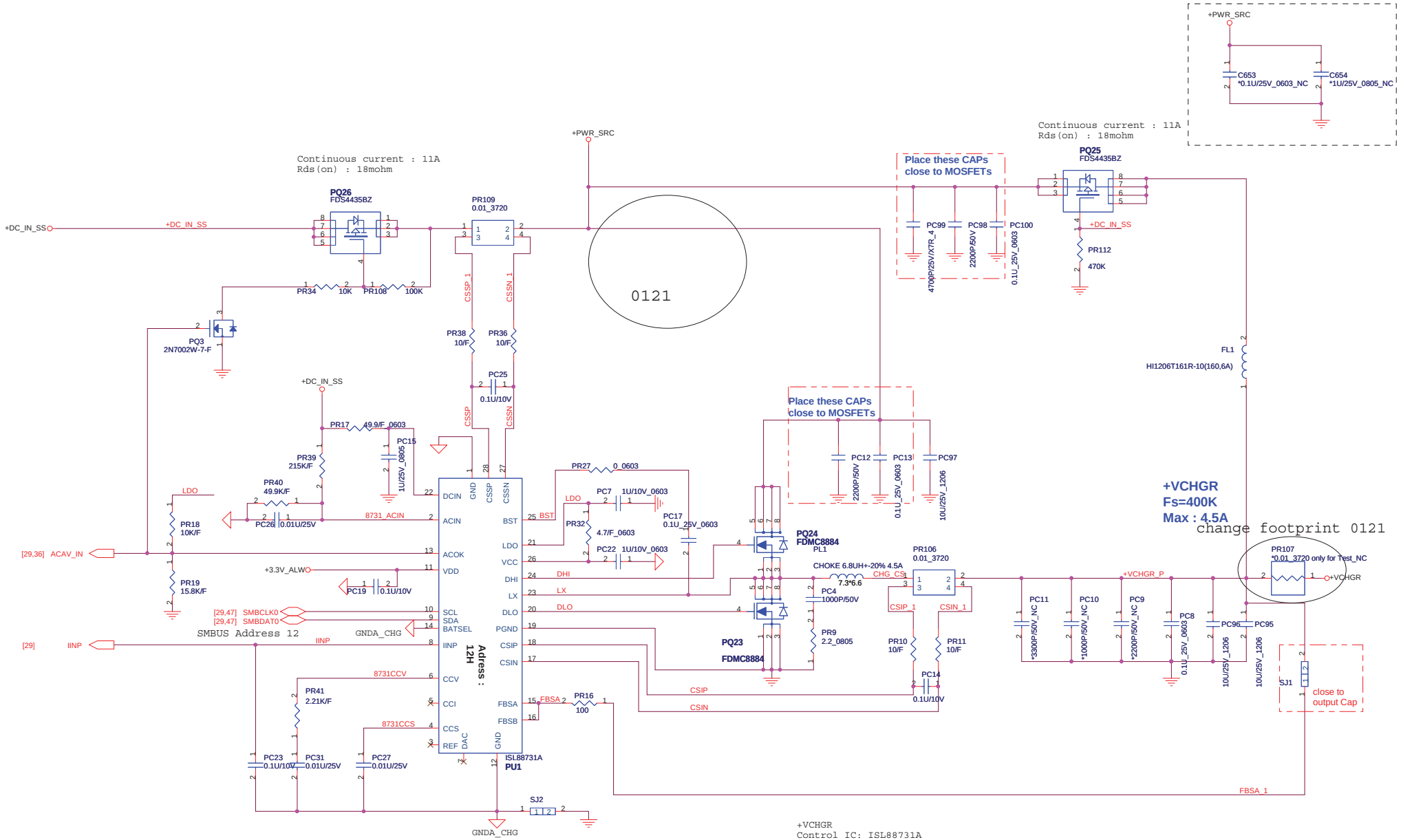
Size	Document Number	Rev
	BTB CONN	3A
Date: Wednesday, February 03, 2010	Sheet 39 of 52	



VTTPWRGOOD
SC(V1.0)P18:
VTT_1.1 VR power good
signal to processor. Signal
voltage level is 1.1 V.

Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	System Reset Circuit	3A
Date: Wednesday, February 03, 2010	Sheet 40 of 52	



+5V_SUS
Fs=200K
TDC : 4.915A
OCP : 6.881A

+3.3V_ALW
Fs=250K
TDC : 4.477A
OCP : 6.268A

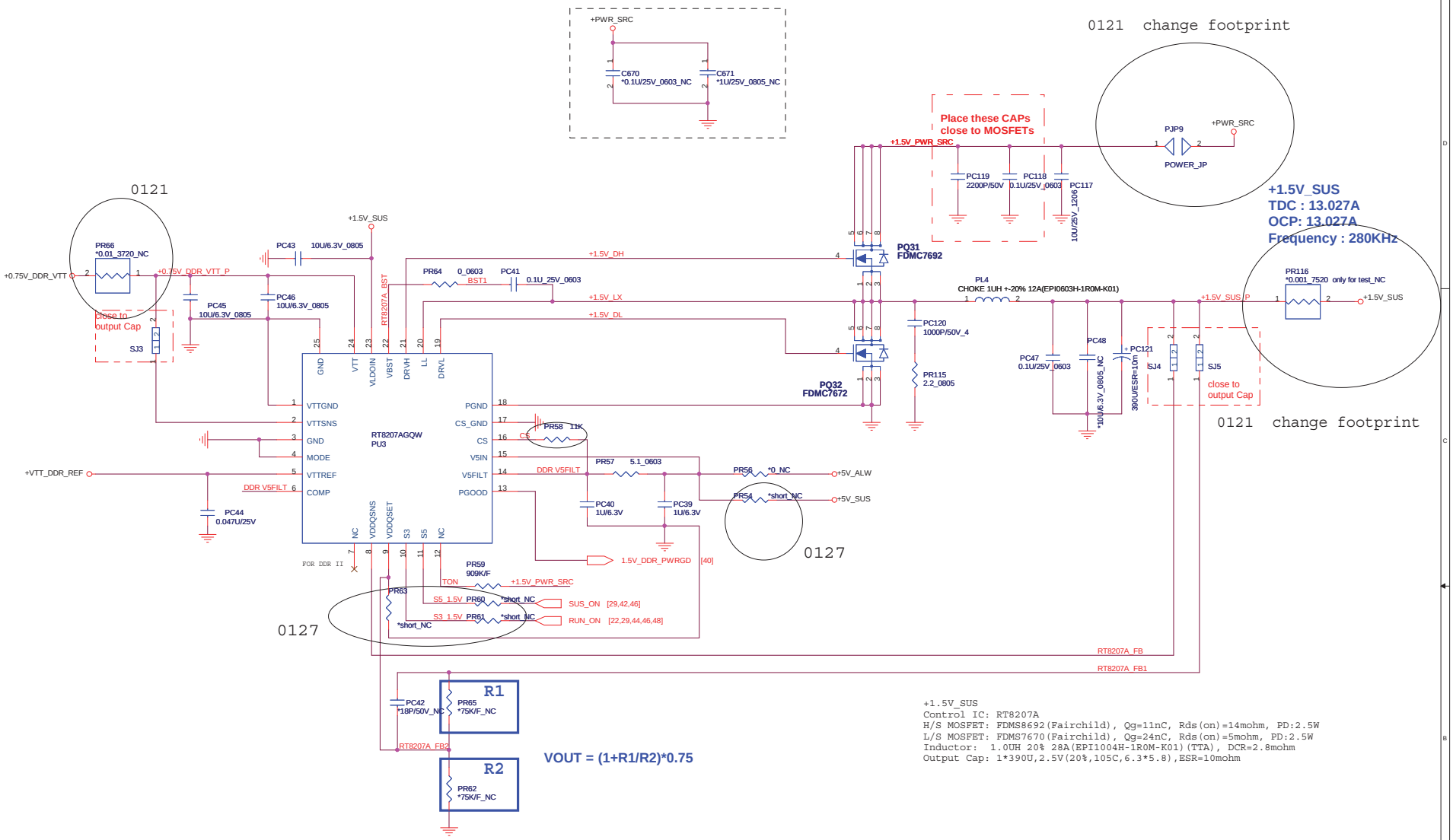
+5V_ALW
Control IC: RT8206B
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
Inductor: 3.8UH,30%8A(TPRH10D45F-3R8Y-F02)(TTA), DCR=21mohm
Output Cap: 1*330U,6.3V(20%ESR17,6.3*5.8)

+3.3V_ALW
Control IC: RT8206B
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
Inductor: 3 3.8UH,30%8A(TPRH10D45F-3R8Y-F02)(TTA), DCR=21mohm
Output Cap: 1*330U,6.3V(20%ESR17,6.3*5.8)

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

QUANTA COMPUTER

Title	3.3V_ALW / 5V_ALW(RT8206B)	
Size	Document Number UM7 Dis	Rev 3A
Date: Wednesday, February 03, 2010	Sheet 42 of 52	



VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Title: DDR3 +1.5V_SUS(RT8207AGQW)
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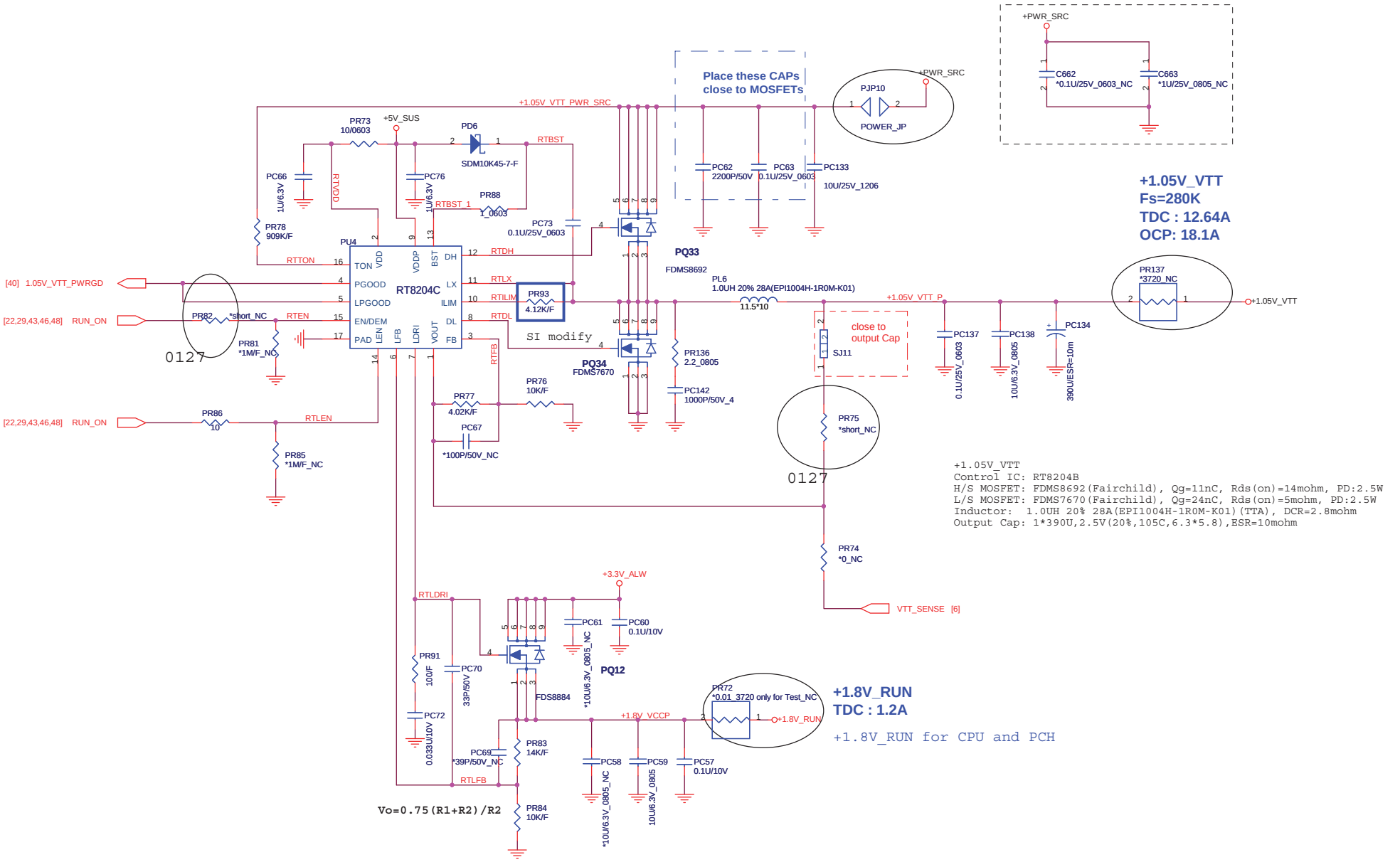
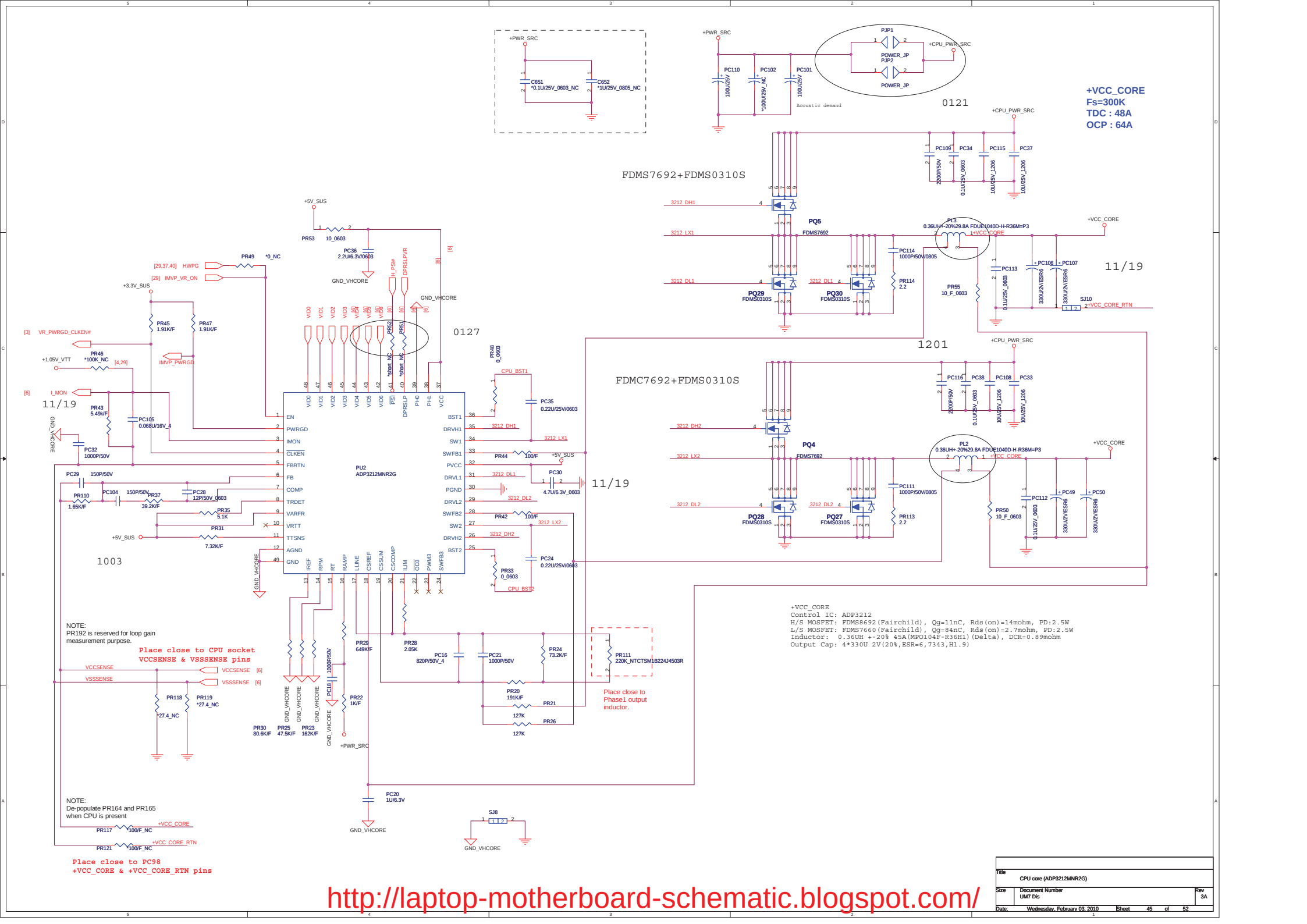
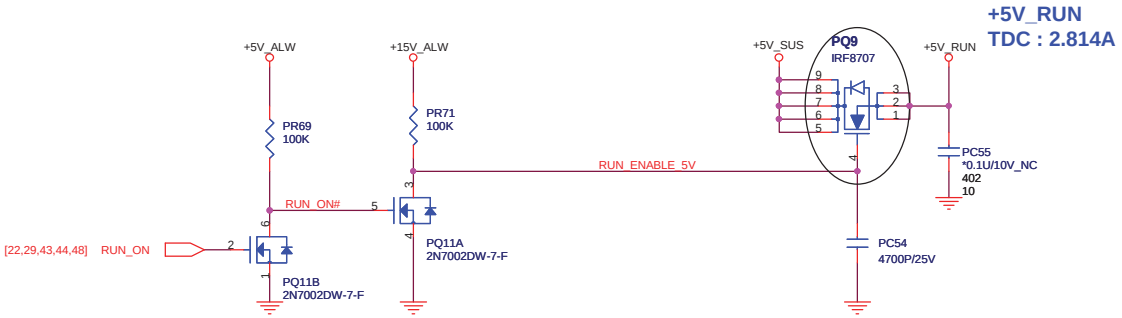
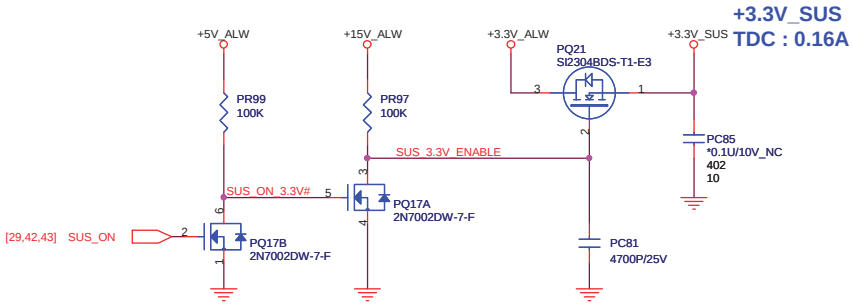
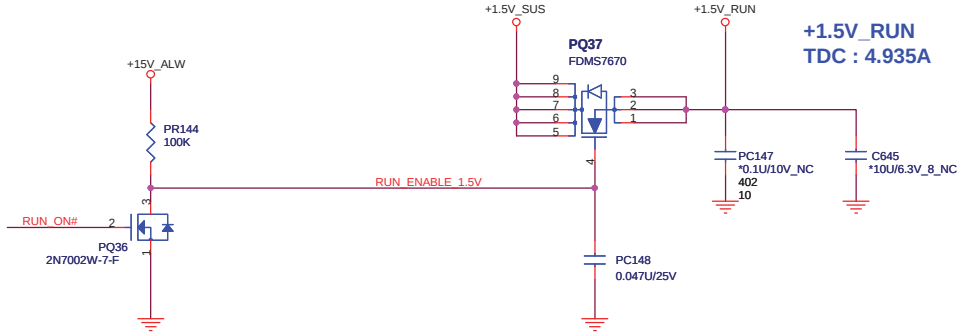
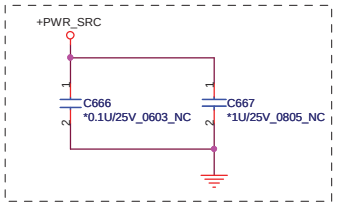


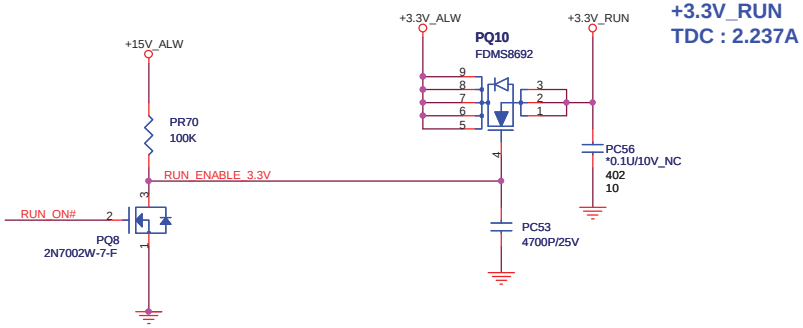




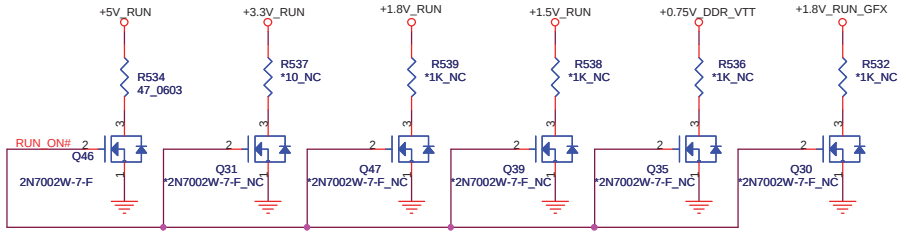


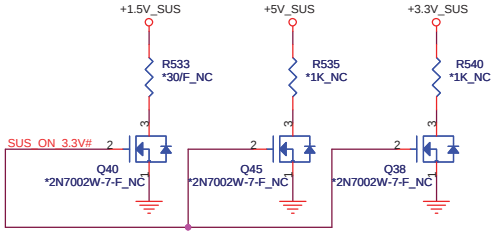






Reserve discharge path





QUANTA COMPUTER

Title	RUN / SUS POWER SW	
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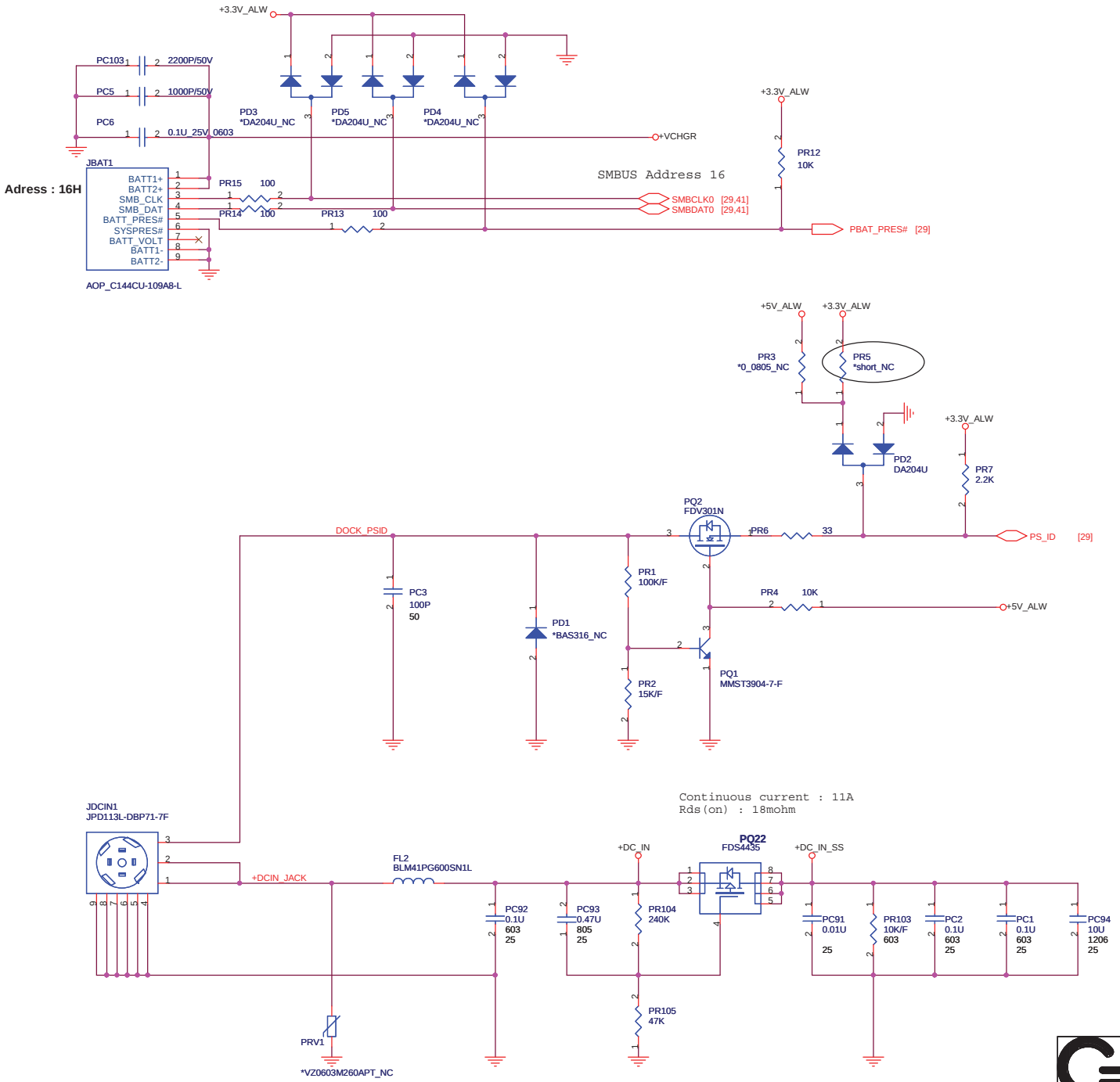

QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
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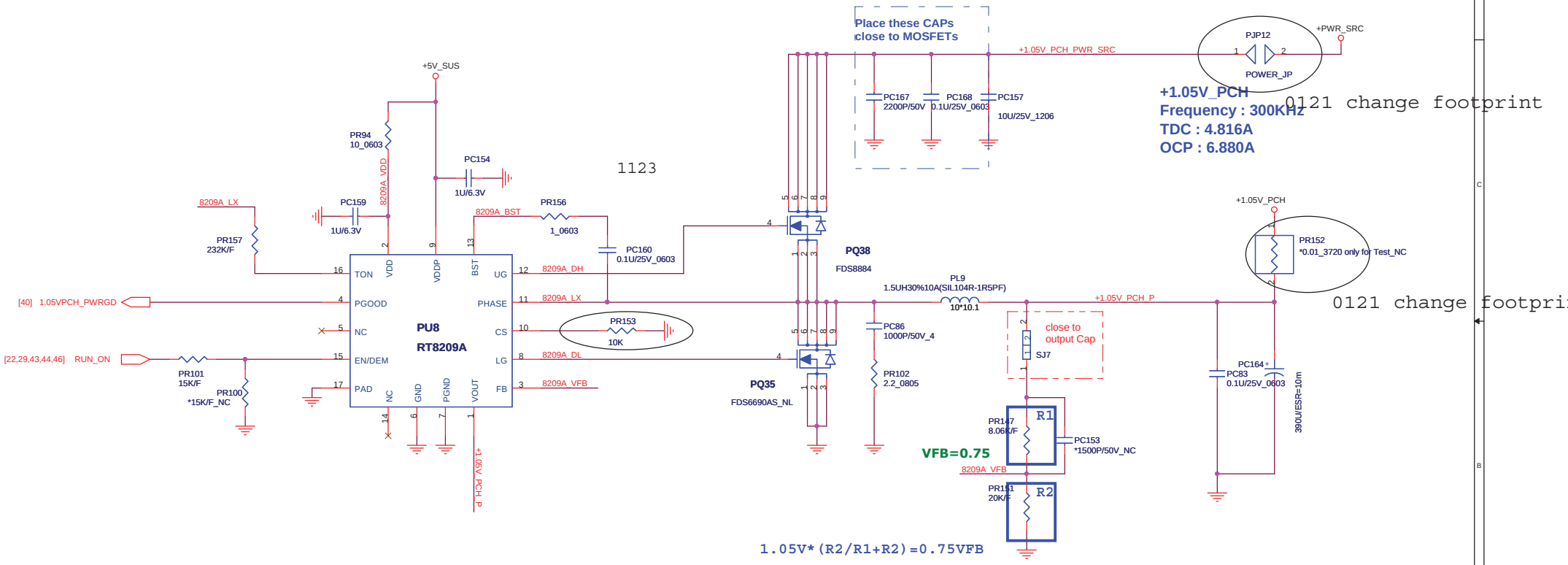

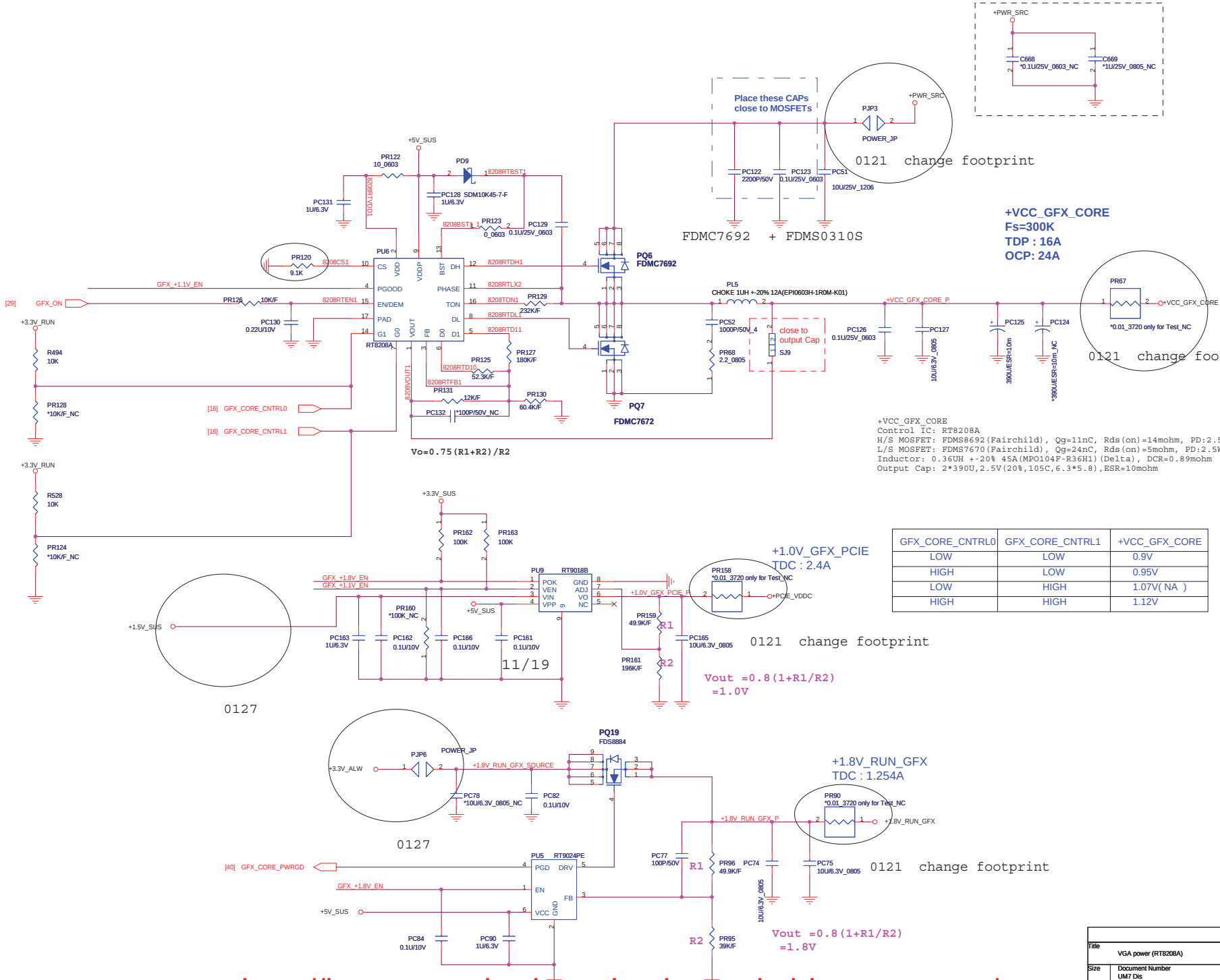

Title	VGA power (RT8208A)
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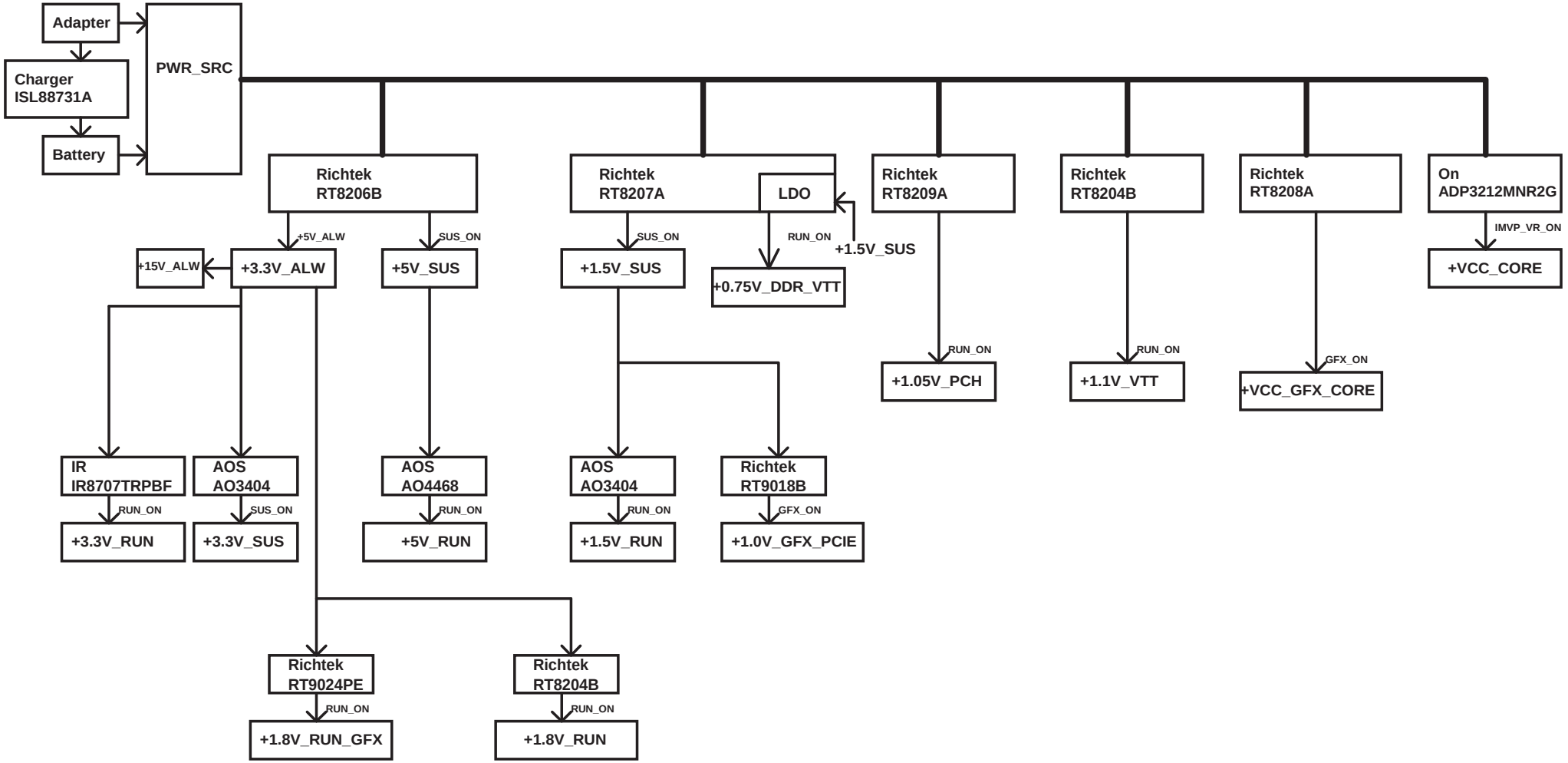

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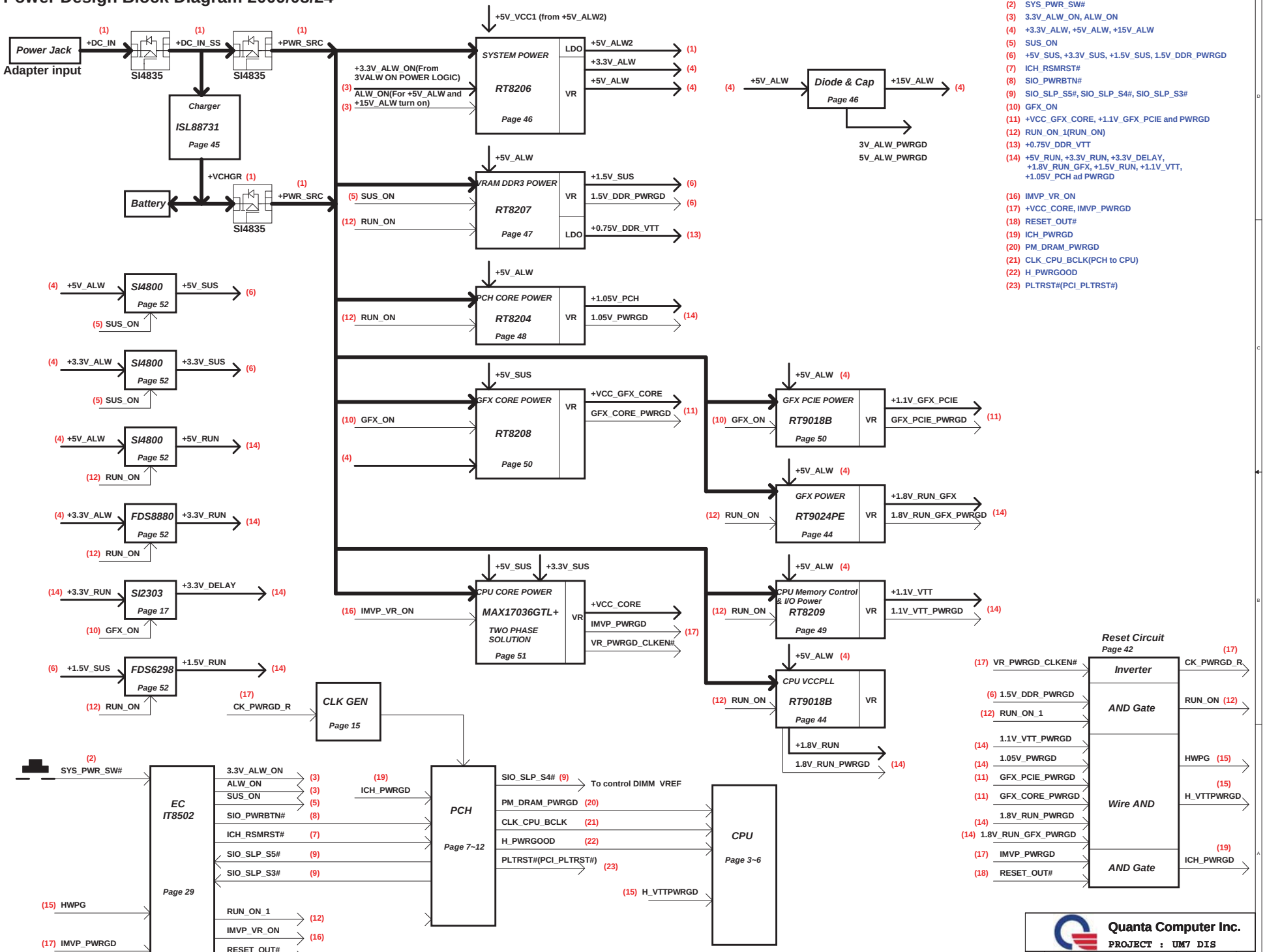
Power Design Block Diagram 2009/08/24



(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2) SYS_PWR_SW#
(3) 3.3V_ALW_ON, ALW_ON
(4) +3.3V_ALW, +5V_ALW, +15V_ALW
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
(7) ICH_RSMRST#
(8) SIO_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFX_ON
(11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
(12) RUN_ON_1(RUN_ON)
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD
(18) RESET_OUT#
(19) ICH_PWRGD
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

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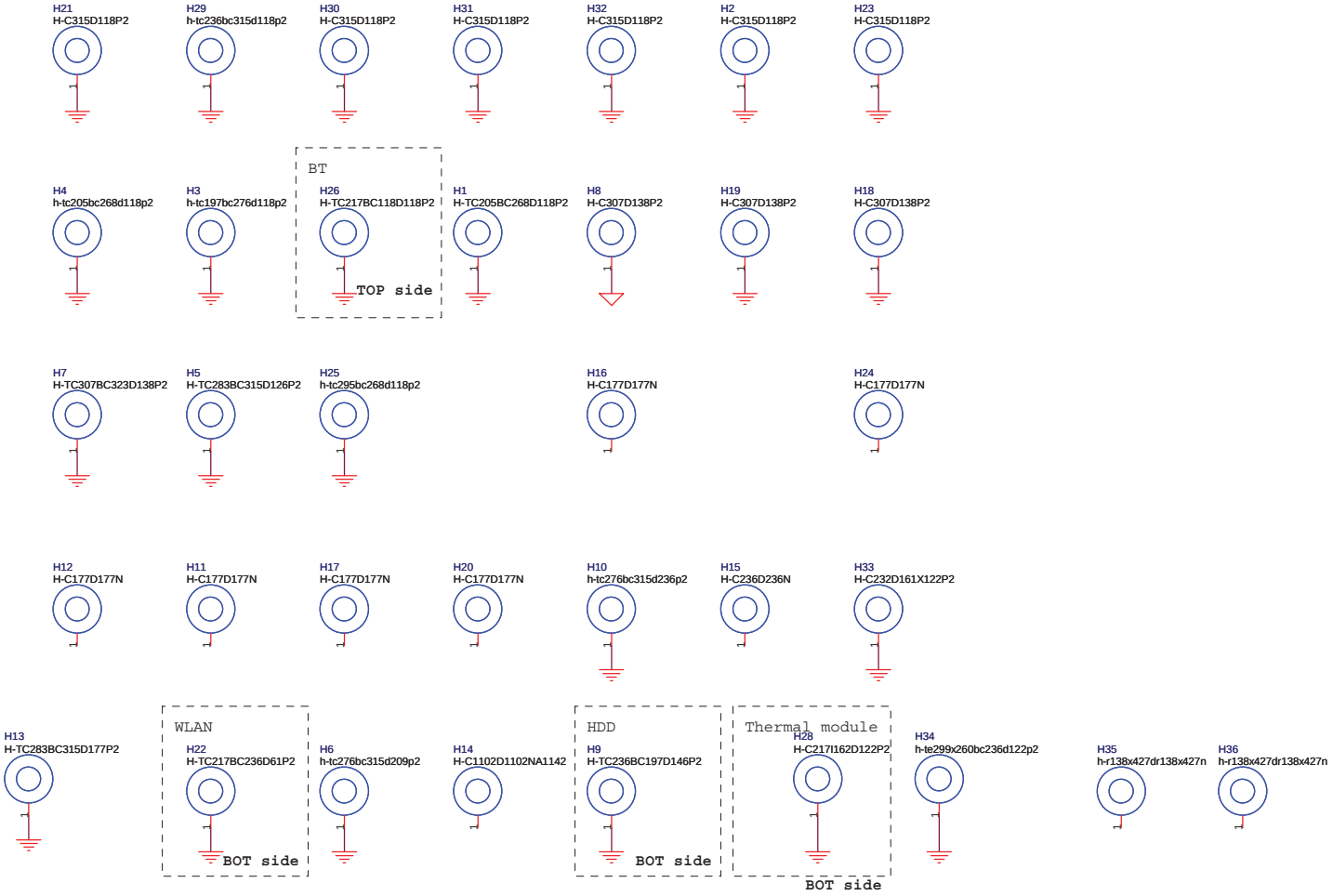

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