

UM7B DISCRETE SYSTEM DIAGRAM

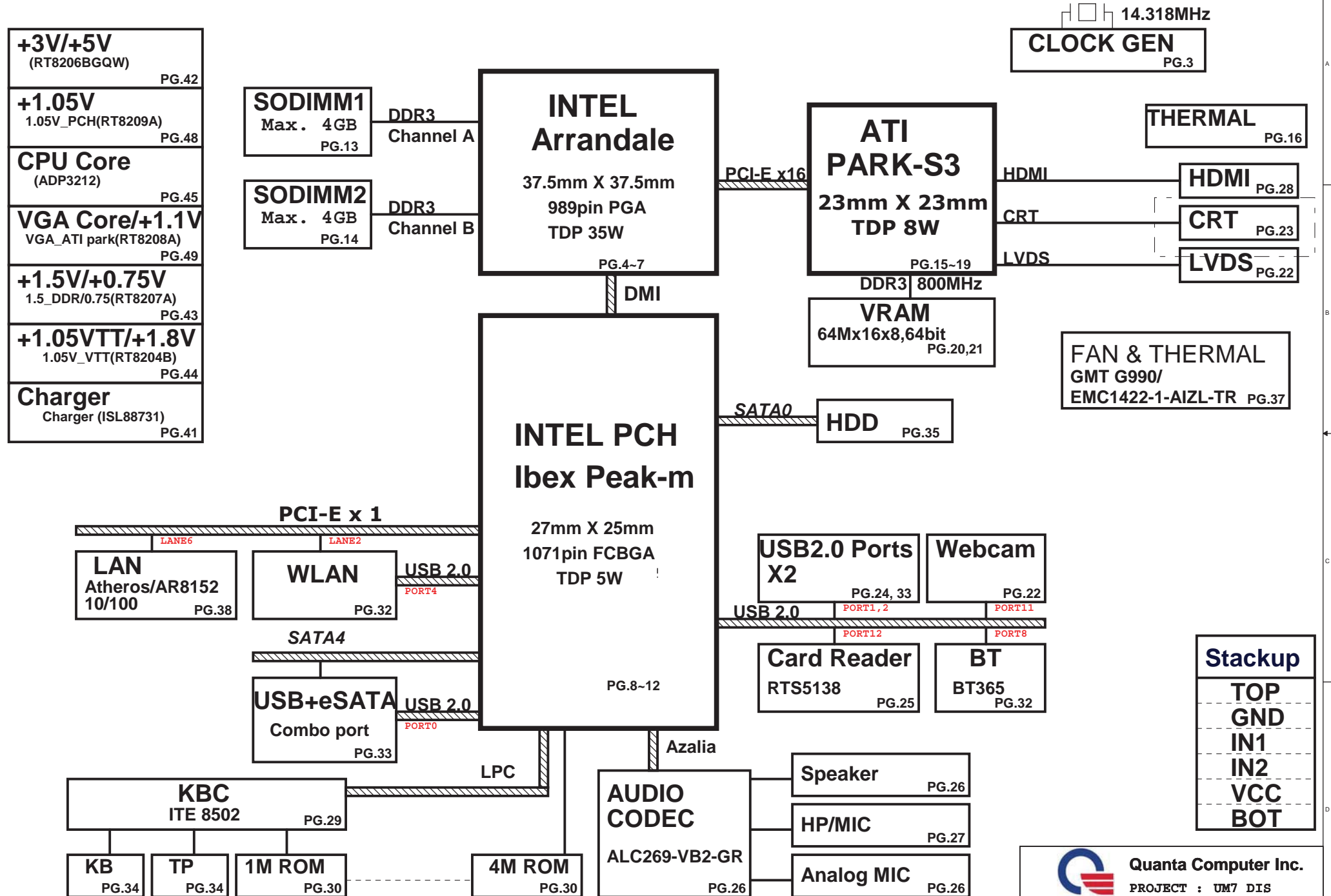



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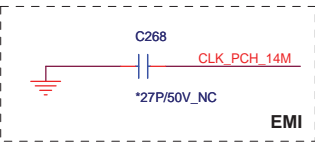
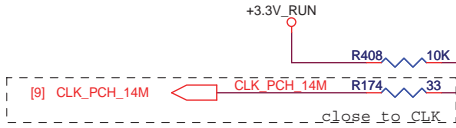
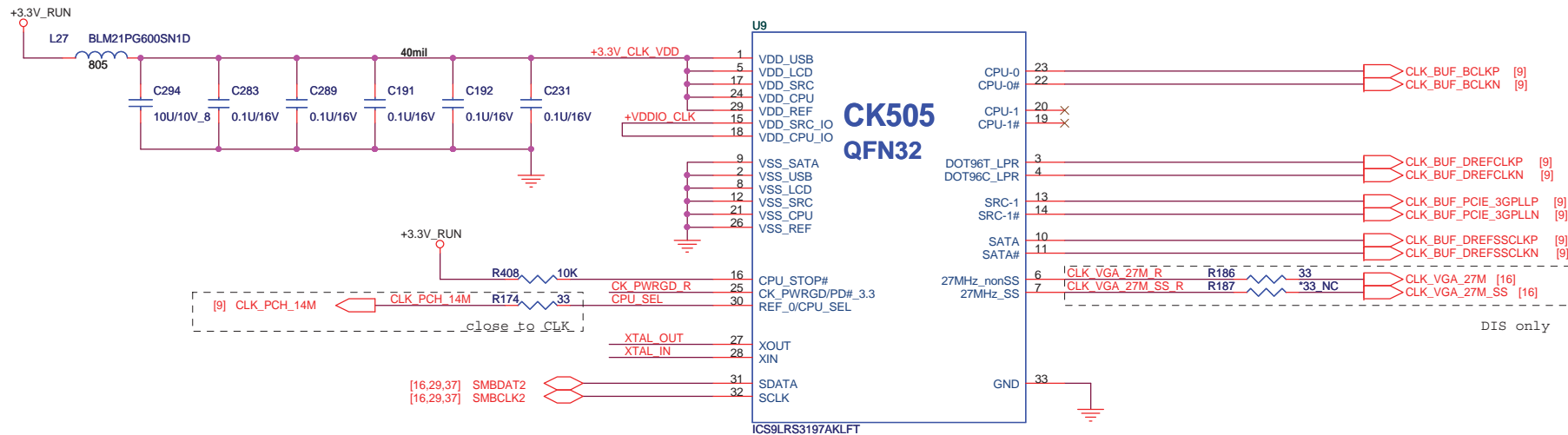
PAGE	DESCRIPTION
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23	CRT CONN
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47	DCin & Batt
48	1.05V_PCH(RT8209A)
49	GFX_VCORE (ADP3211)
50	Power Block Diagram
51	Power sequence Block

Power States

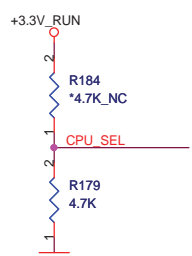
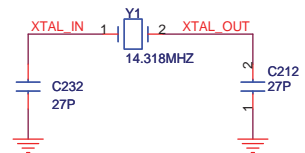
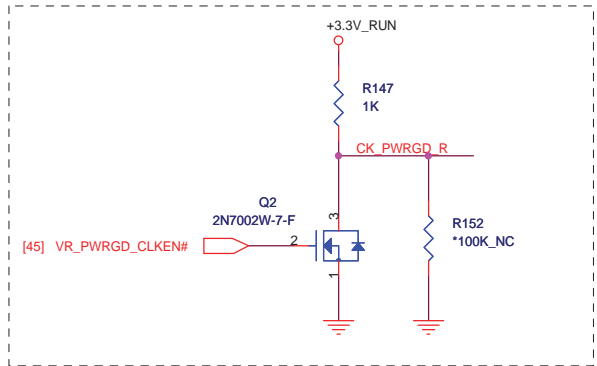
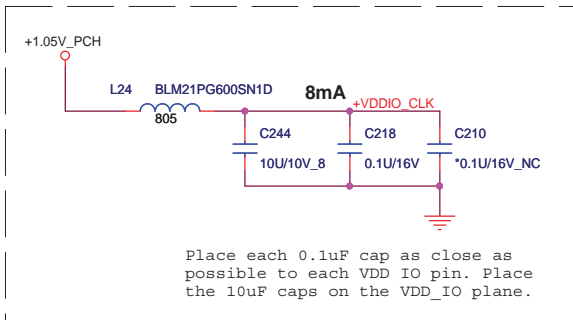
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	23,42,43,44,45,46,49,50	MAIN POWER		S0-S5
+RTC_CELL	+3.0V~+3.3V	09,12,30,31	RTC		S0-S5
					S0-S5
+5V_ALW	+5V	37,43,44,47,48	LARGE POWER	ALW_ON	S0-S5
+3.3V_ALW	+3.3V	30,31,37,42,43,45,47,48	8051 POWER	3.3V_ALW_ON	S0-S5
+5V_SUS	+5V	12,25,34,37,43,44,45,46,47,49,50	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	03,08,09,10,11,12,23,35,37,39,41,46,47,50	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	04,06,14,15,44,47	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	14,15,44	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	08,12,23,24,27,28,29,35,36,37,38,47	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,4,8,9,10,11,12,14,15,23,24,26,27,28,29,30,31,33,34,36,37,38,39,41,47	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	6,12,45	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	4,6,11,12,45,46	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	12,33,47	PCH/Min Card	RUN_ON	
+1.05V_PCH	+1.05V	3,8,9,10,12,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	6,46	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	23	LCD Power	LCDVCC_TST_EN & ENVDD	

GND PLANE	PAGE	DESCRIPTION
⏏ GND	ALL	


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 PROJECT : UM7 DIS
 BLOCK DIAGRAM
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AL003197000IC OTHER (32P) ICS9LRS3197AKLFT (QFN)
 AL8SP585000IC OTHER (32P) SLG8SP585VTR (QFN)
 AL8SP590000IC OTHER (32P) SLG8SP590VTR (QFN)



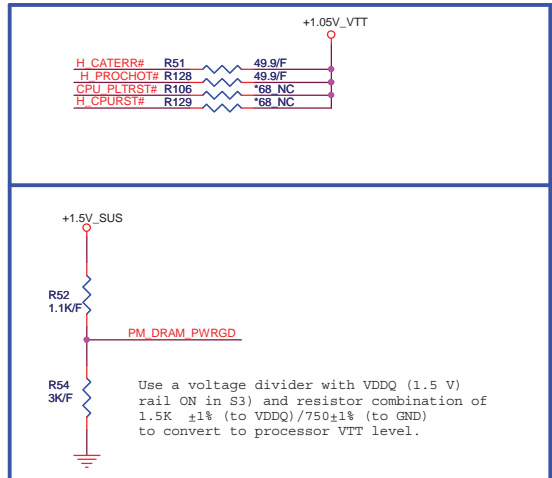
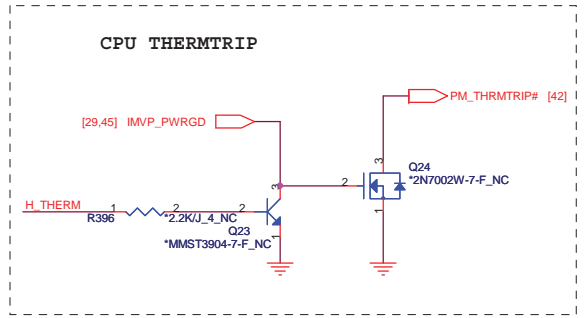
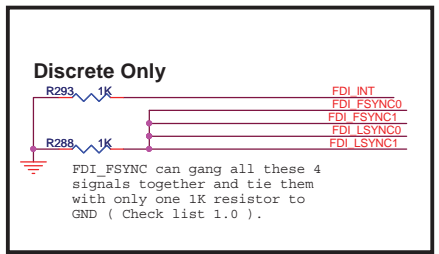
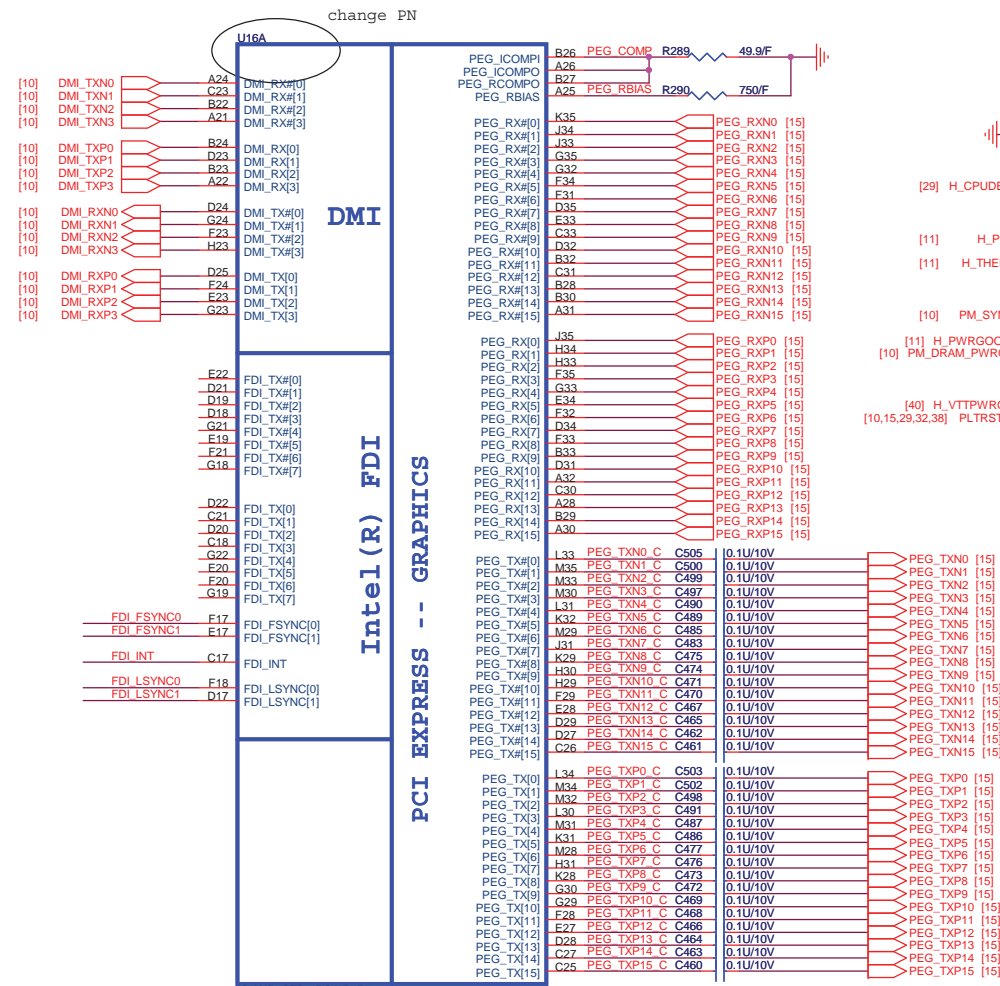
PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz

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Clock Generator

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JTAG

XDP_TDO_M

XDP_TDI_M

XDP_TRST#

R83 *short0402_NC

R101 51

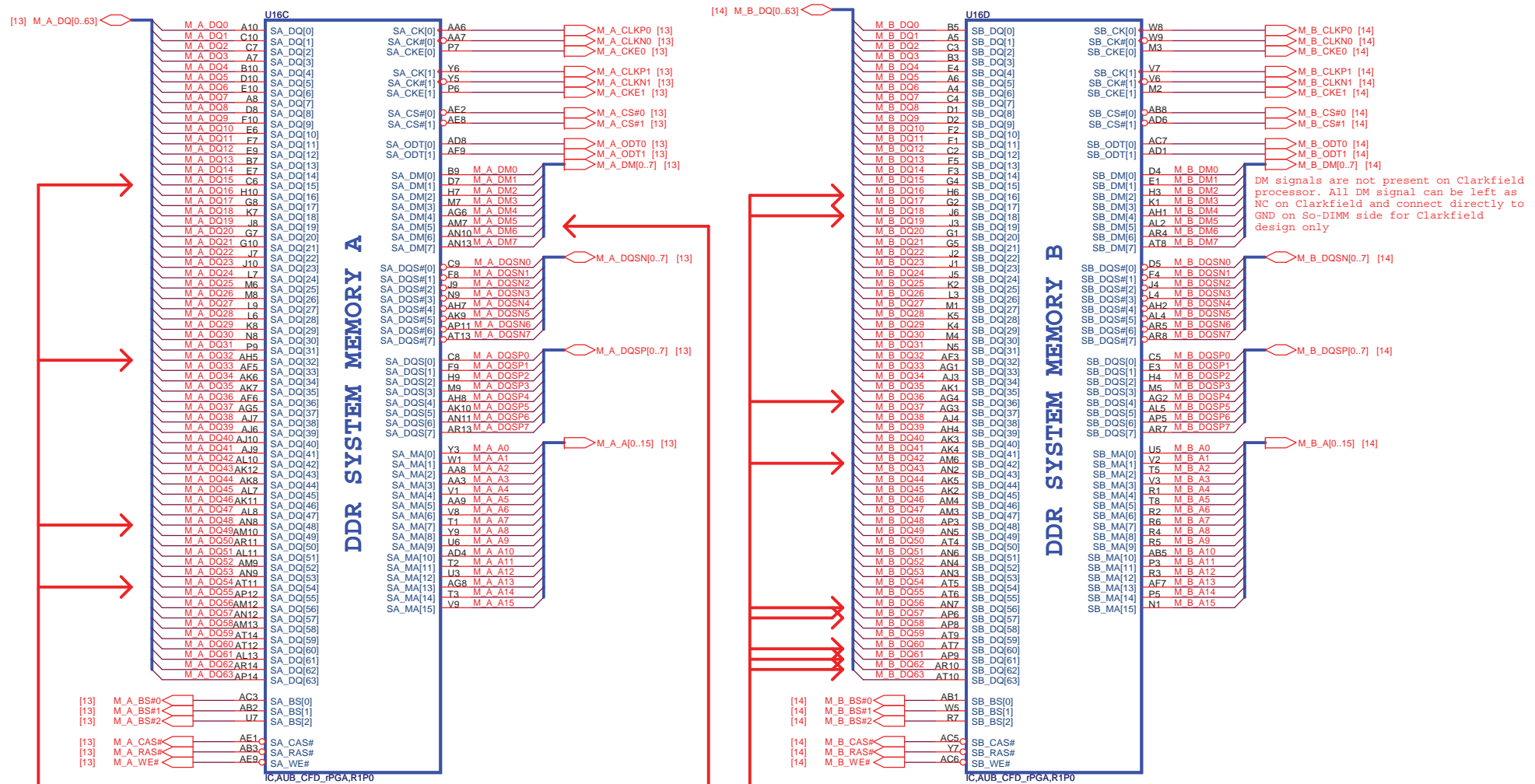
Intel Suggest to reserve 0.ohm below for CPU AP29 and AR29 pins.

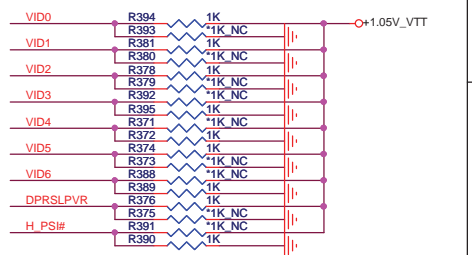
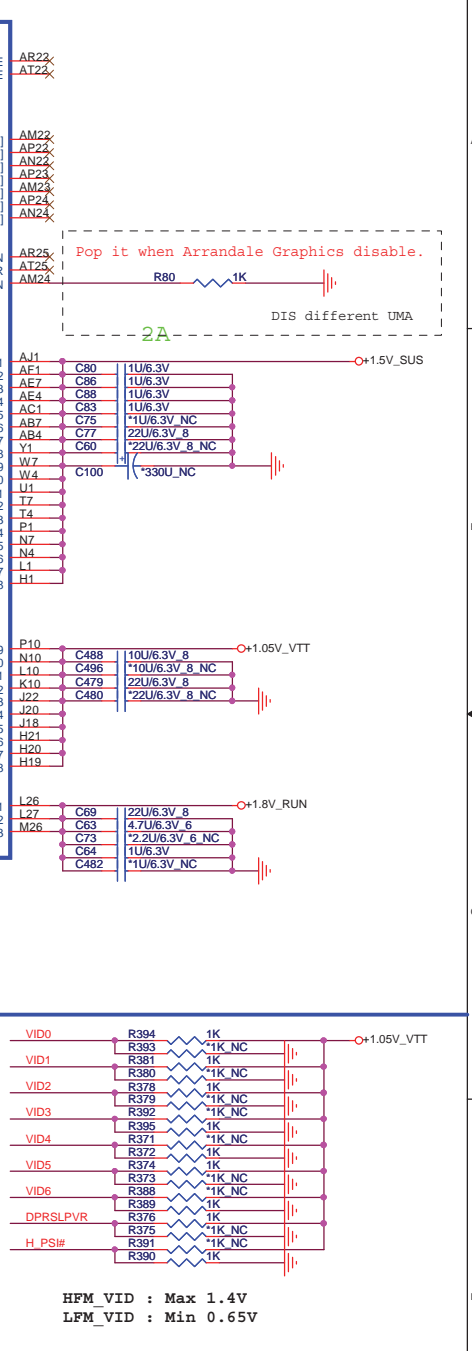
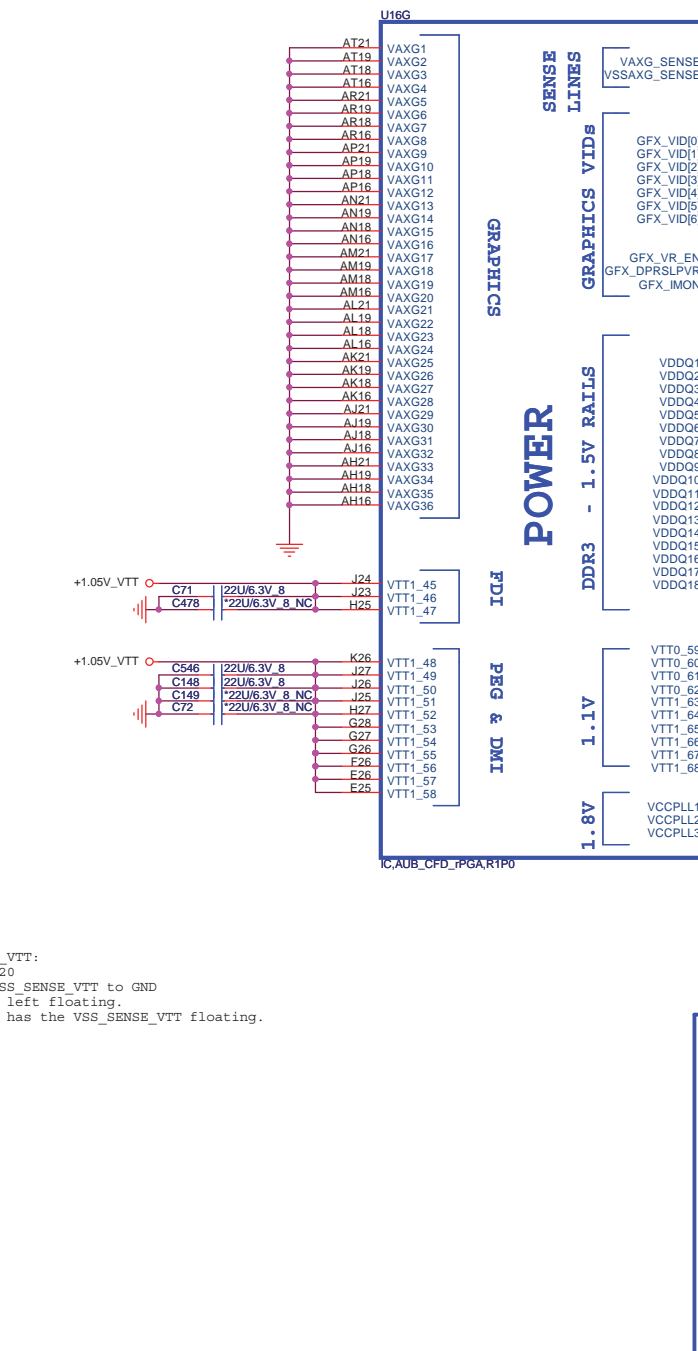
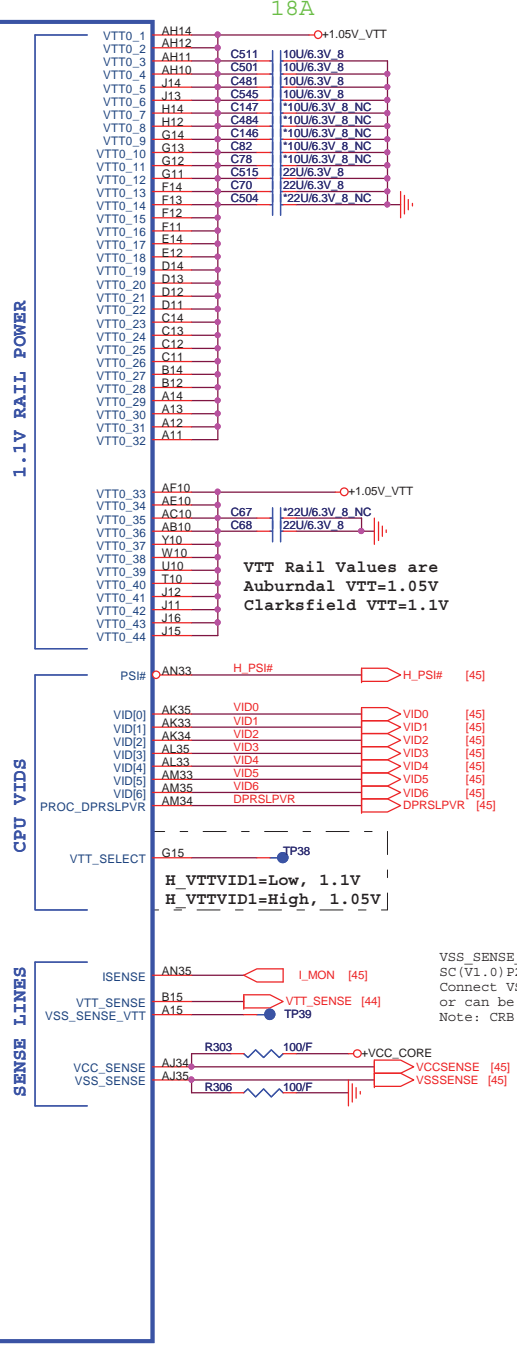
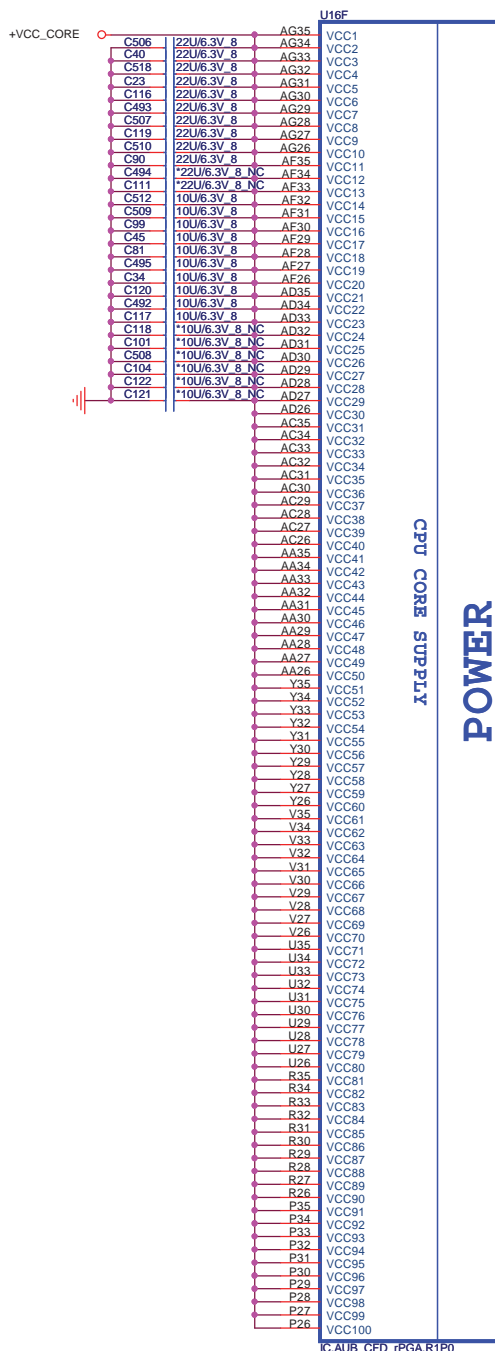
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	PROCESSOR 1/4(HOST&PEX)	3A
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AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



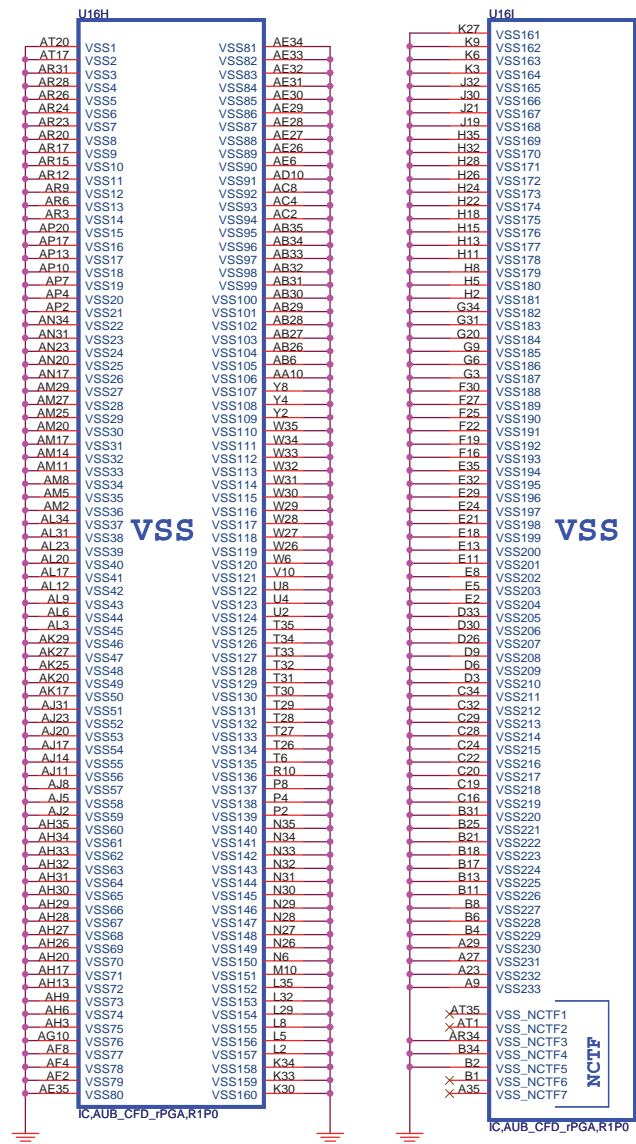


HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

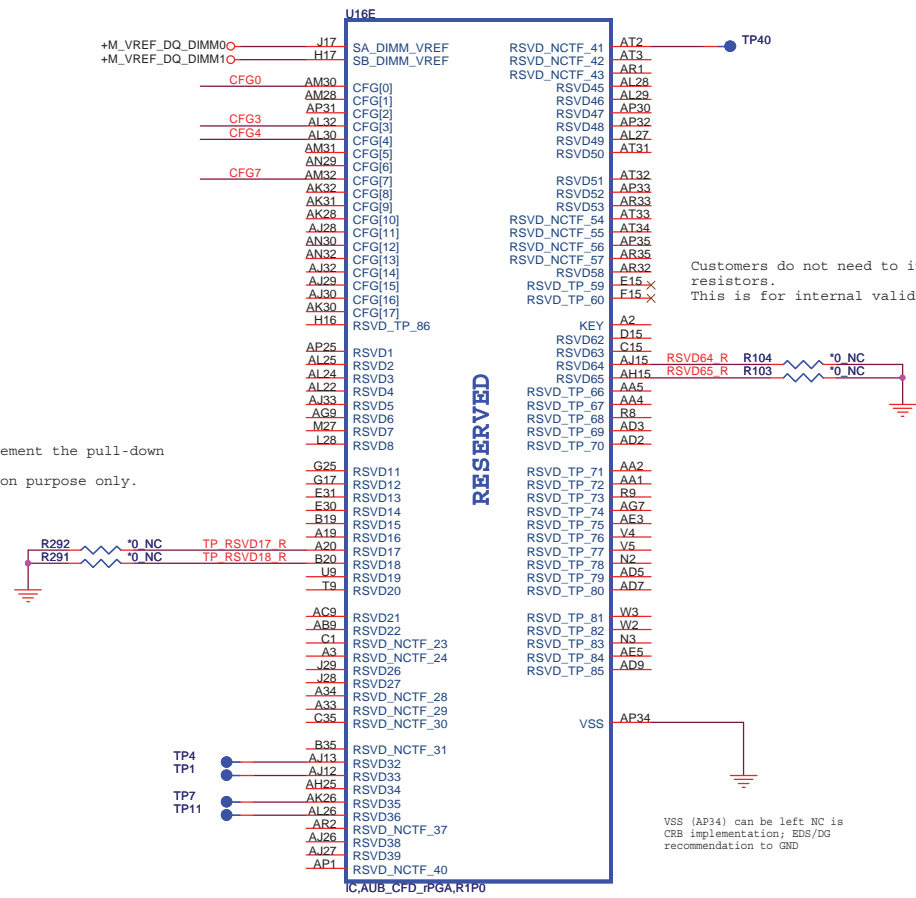


Arrandale PROCESSOR (GND)

Arrandale PROCESSOR(RESERVED, CFG)

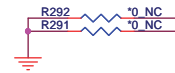


Customers do not need to implement the pull-down resistors.
This is for internal validation purpose only.



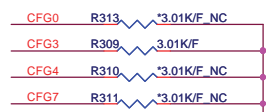
Customers do not need to implement the pull-down resistors.
This is for internal validation purpose only.

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

The Clarkfield processor's PCI Express 2.0 jitter specifications may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

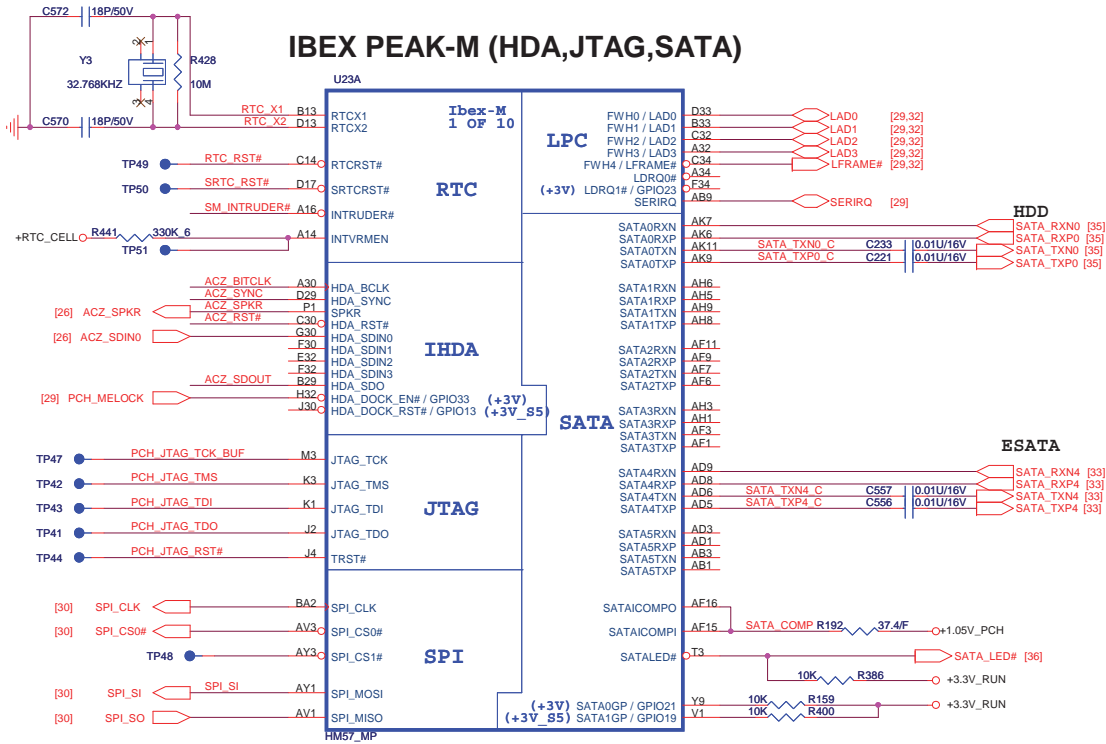


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	PROCESSOR 4/4 (GND)	3A
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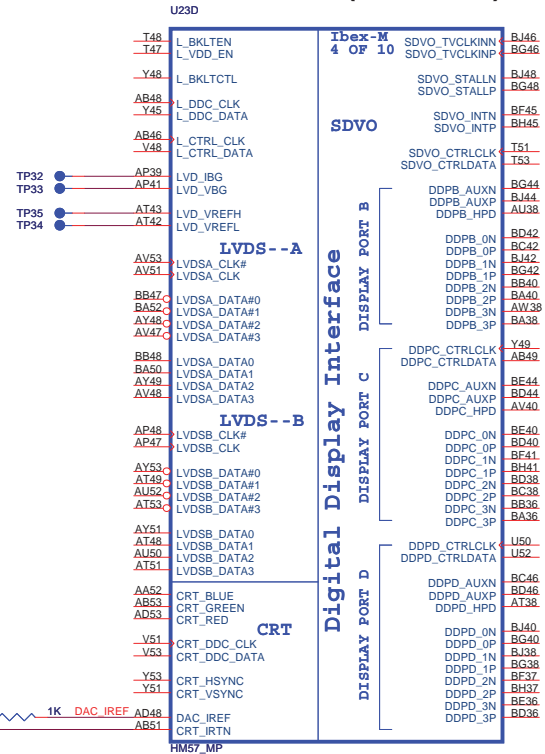
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)



UMA CRT, LVDS&HDMI signals

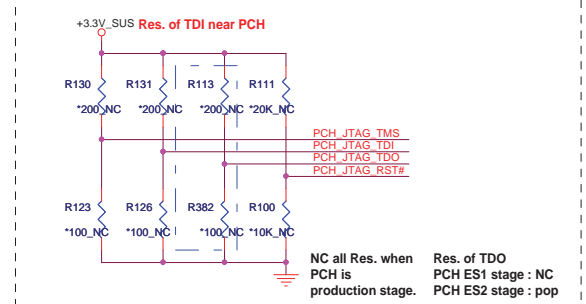
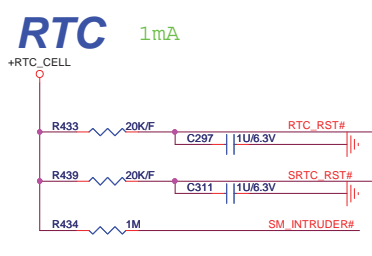
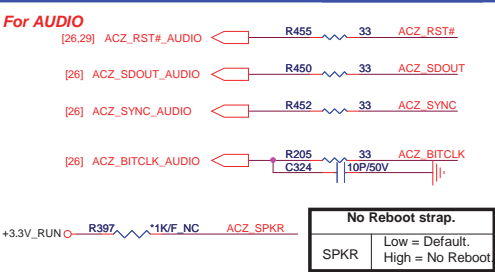
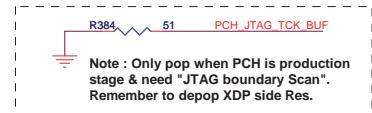
IBEX PEAK-M (LVDS,DDI)



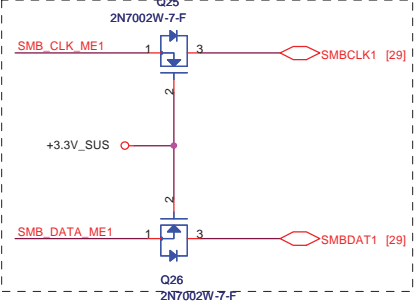
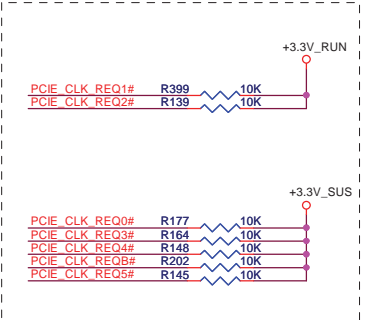
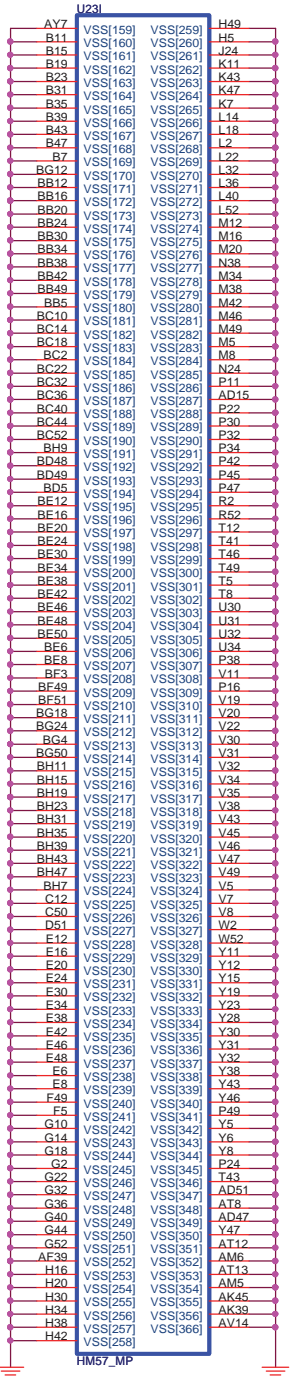
iTPM ENABLE/DISABLE



TPM Function	
Enable	Mount
Disable	NC (Default)



IBEX PEAK-M (GND)



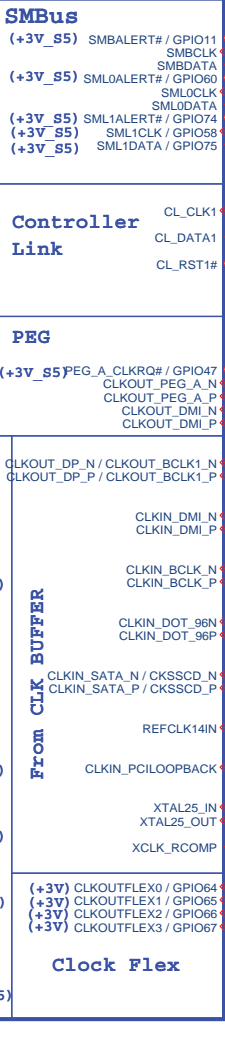
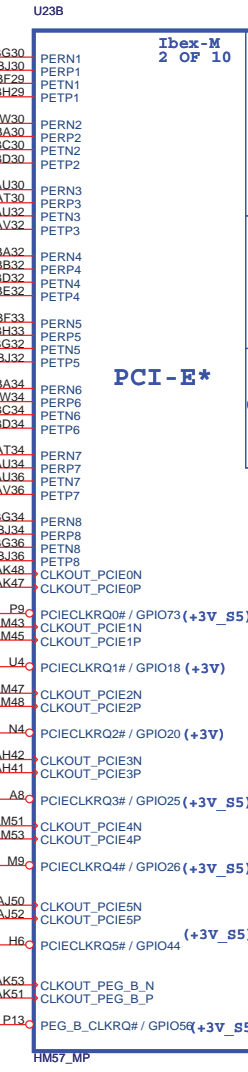
IBEX PEAK-M (PCI-E, SMBUS, CLK)

[WLAN]

[LAN]

MiniWLAN

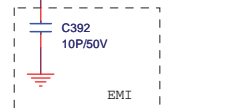
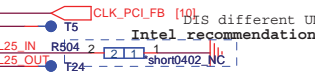
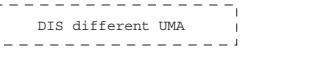
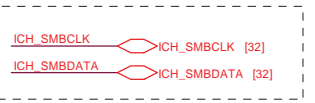
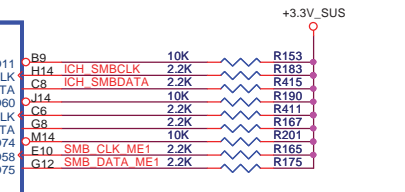
LAN



From CLK BUFFER

Clock Flex

25M
DIS different UMA

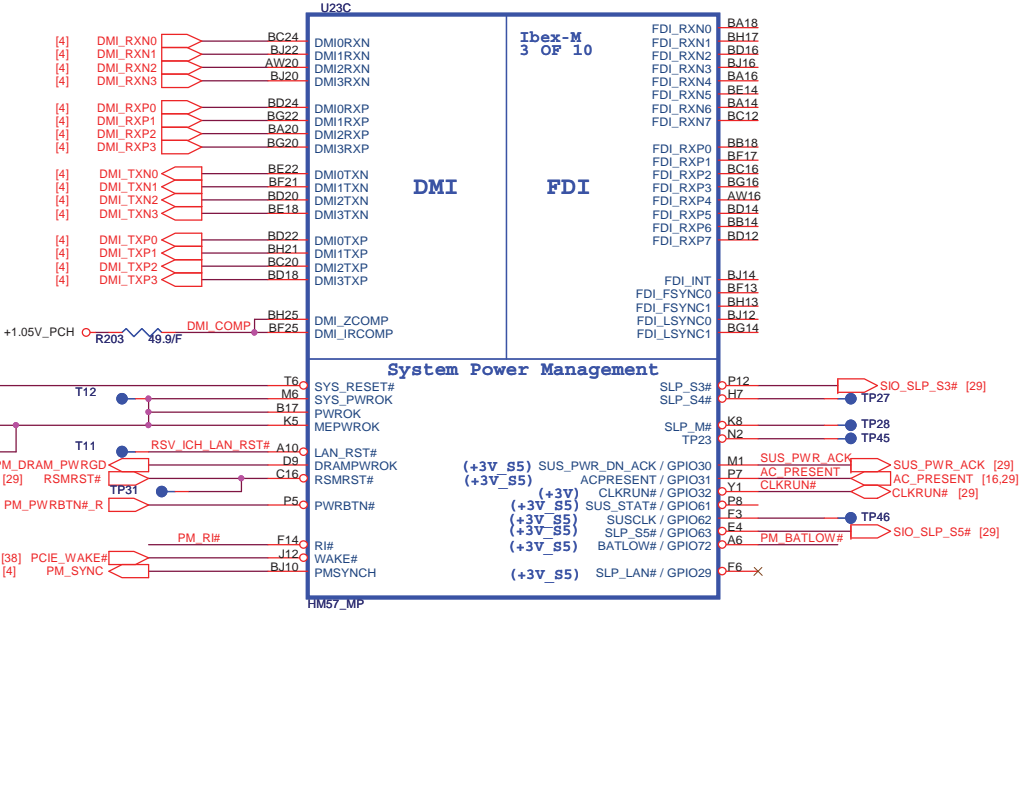
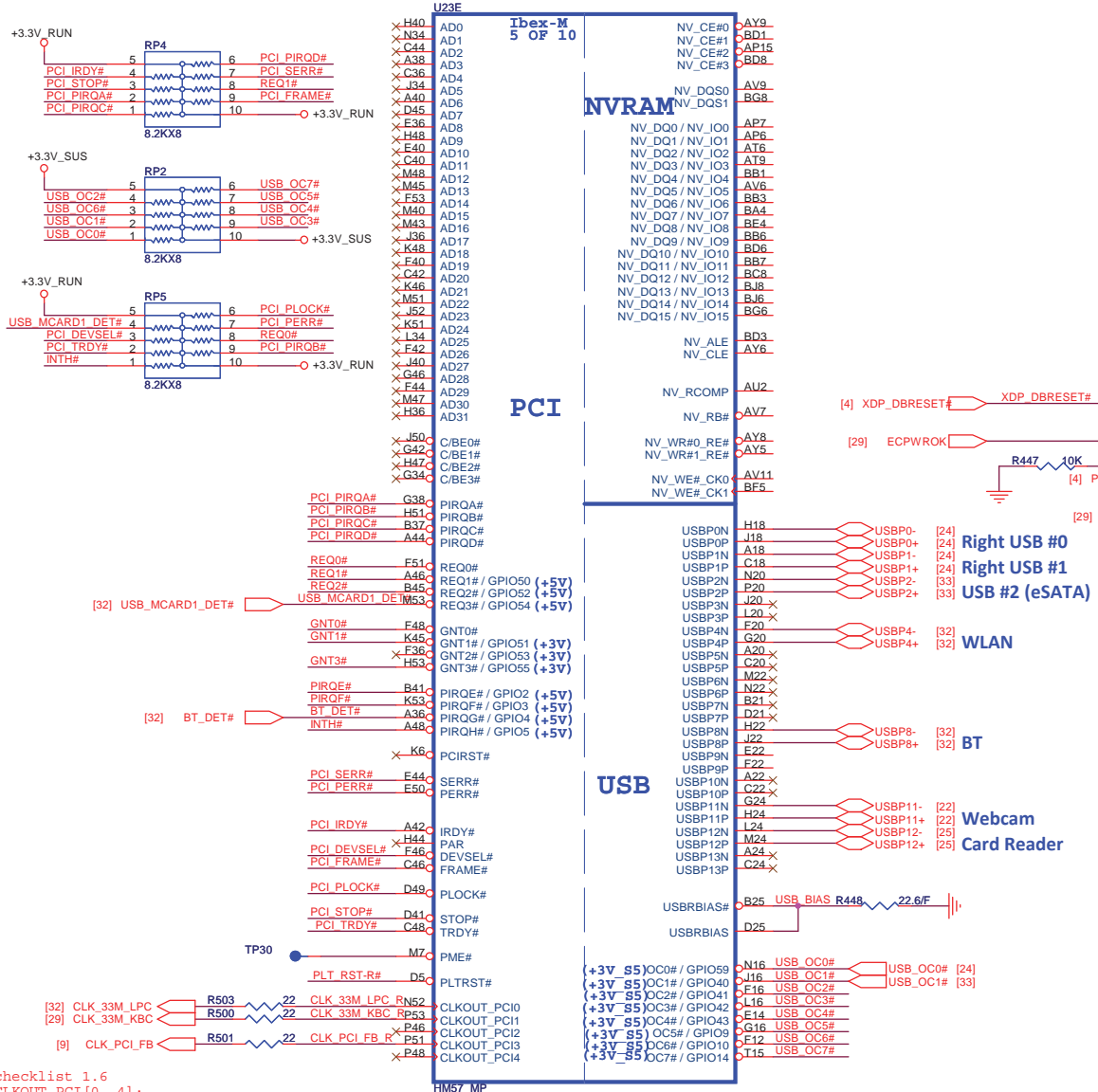


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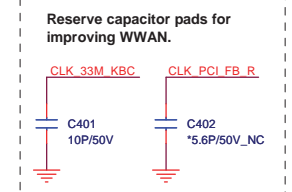
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	PCH 2/5 (PCI-E, SMBUS, CK)	3A
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IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)

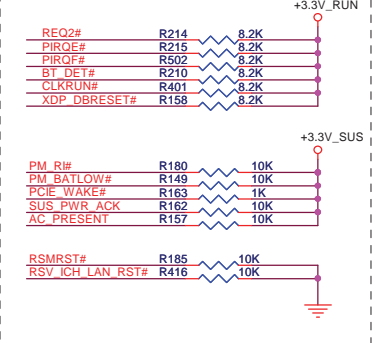
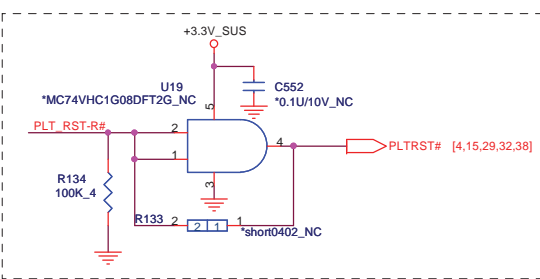
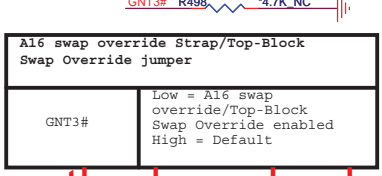


checklist 1.6
 CLKOUT_PCI[0..4]:
 47 Ω to 30 Ω
 (depends on number of loads)



Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

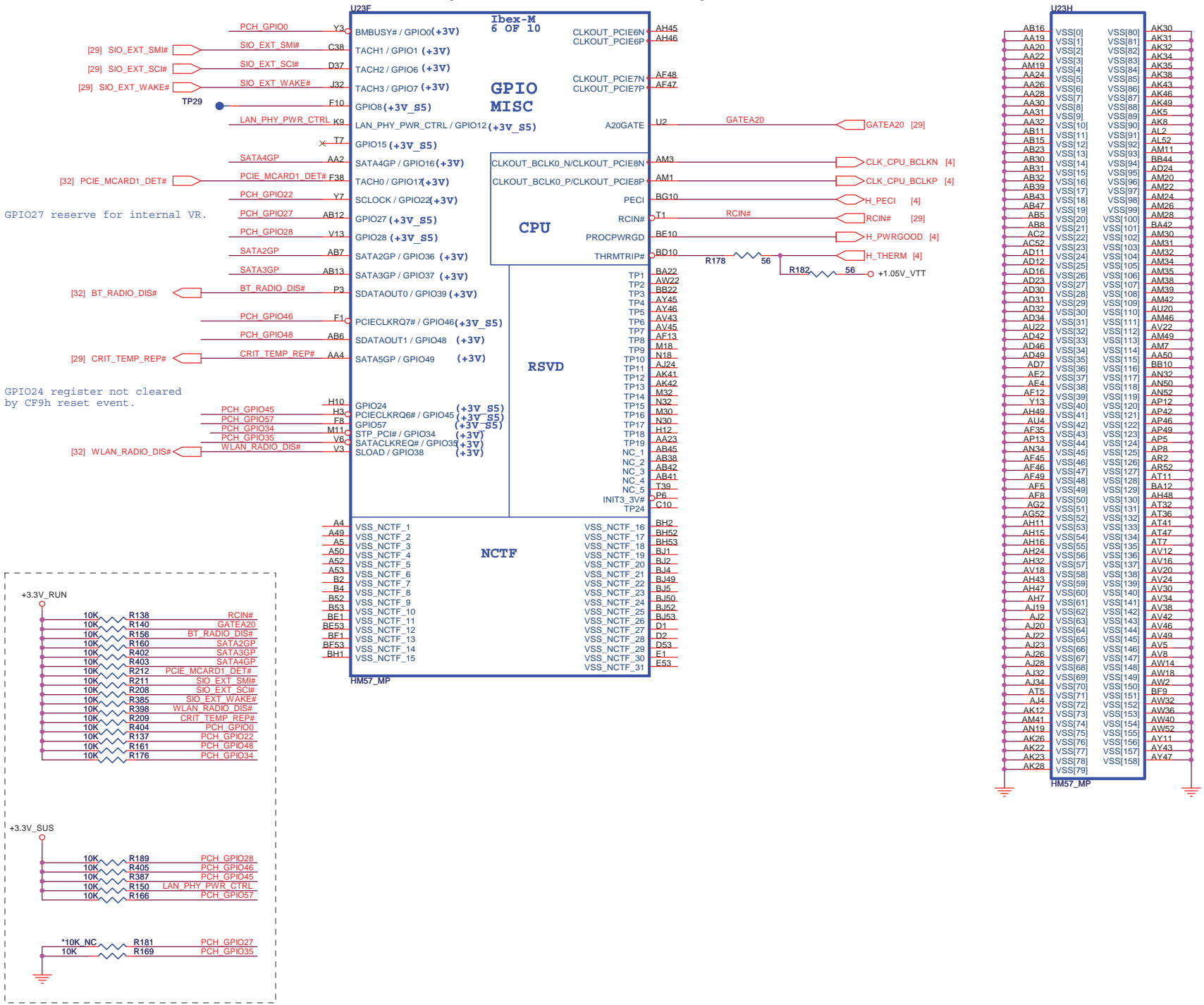


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	PCH 3/5 (PCI,ONFI,USB,DMI)	3A
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IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)



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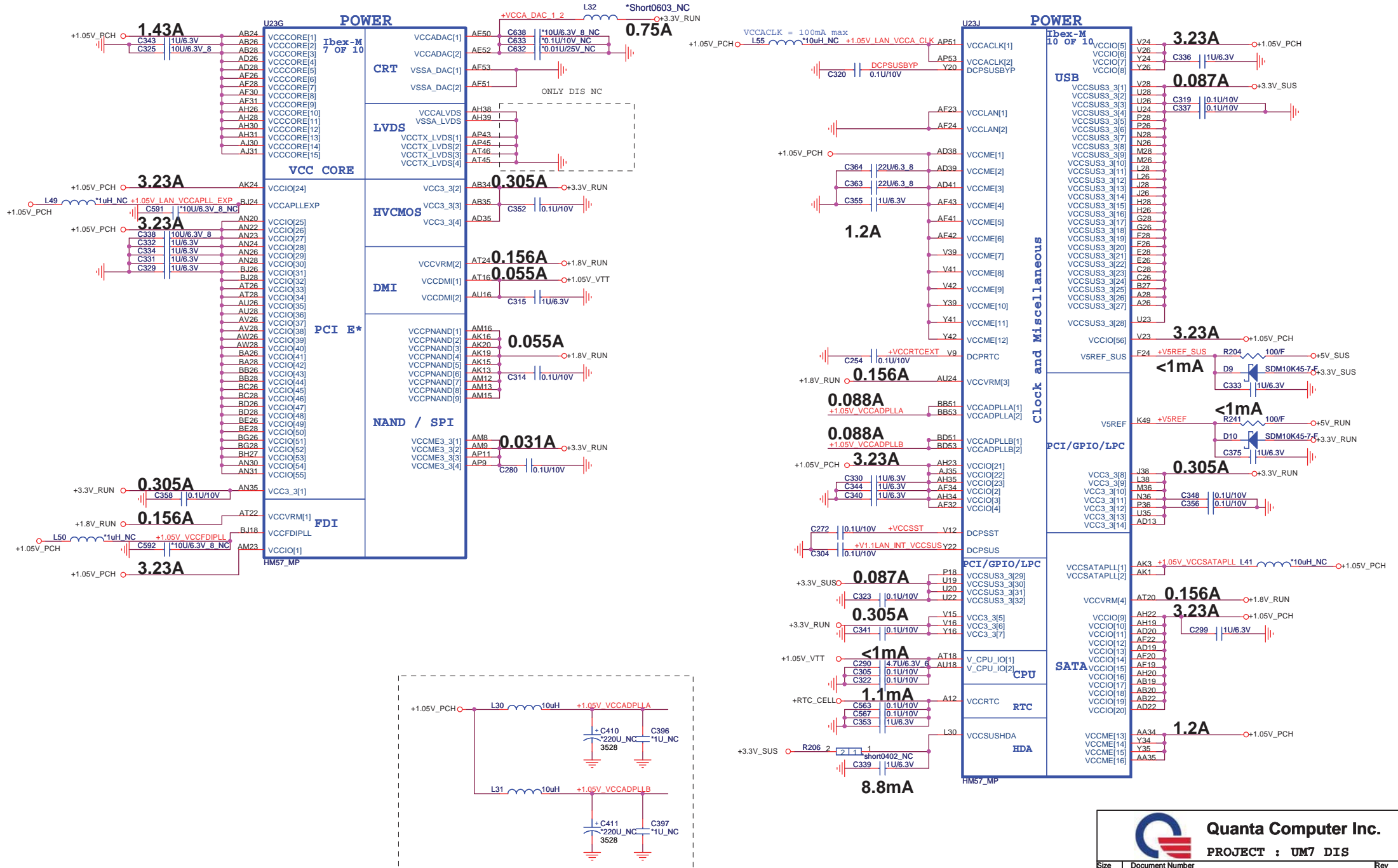


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	PCH 4/5 (GPIO & Strap)	3A
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L32 UMA
EMI FILTER HCBL608KF-181T15 (180, 1.5A)
CX000181016

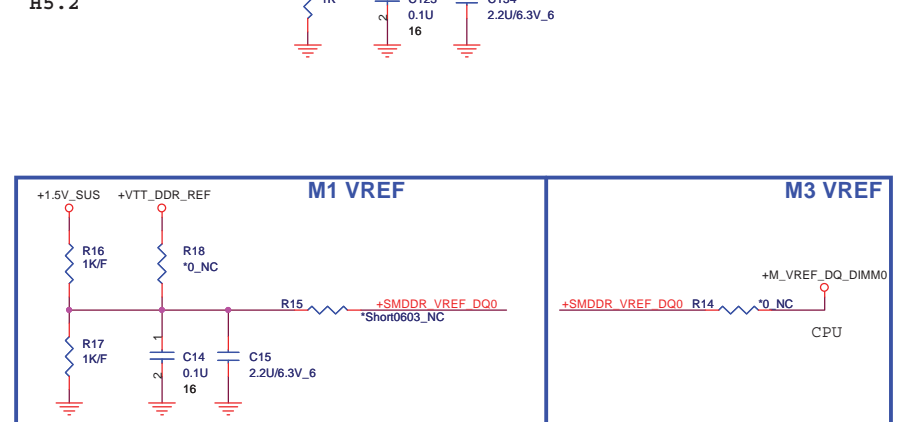
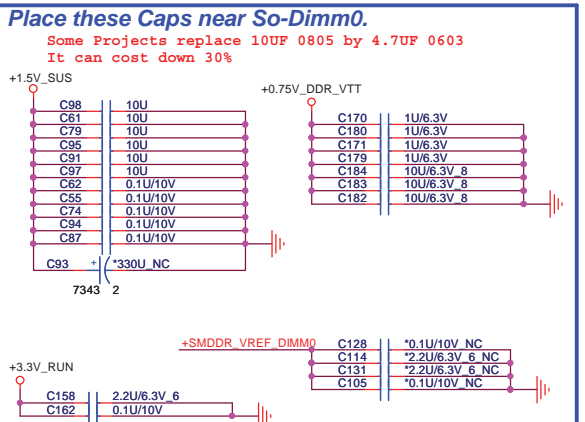
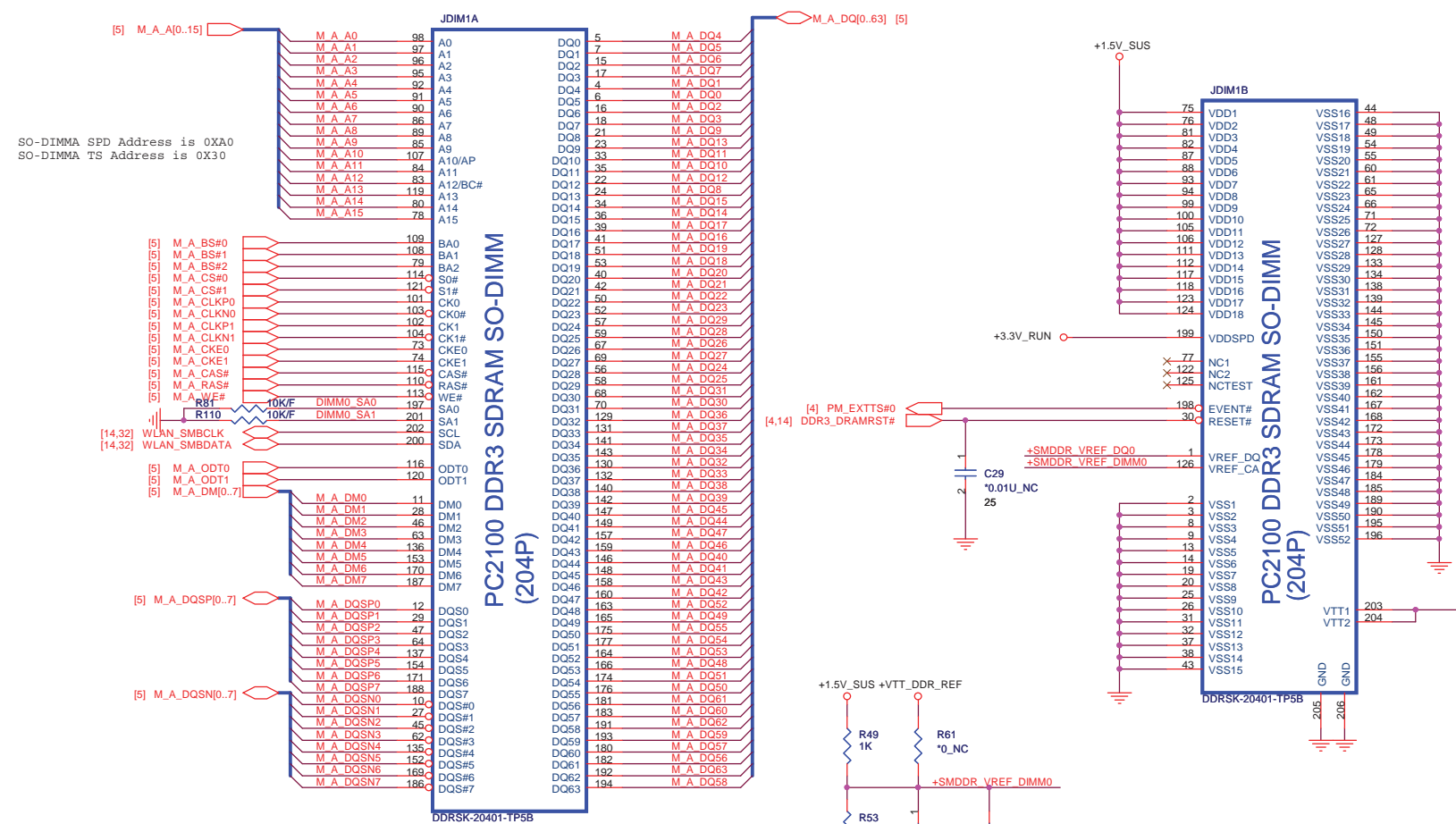
L32 DIS-SHORT



<http://laptop-motherboard-schematic.blogspot.com/>

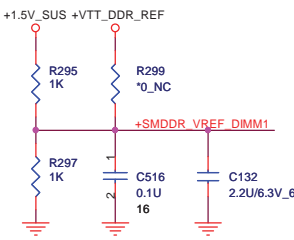
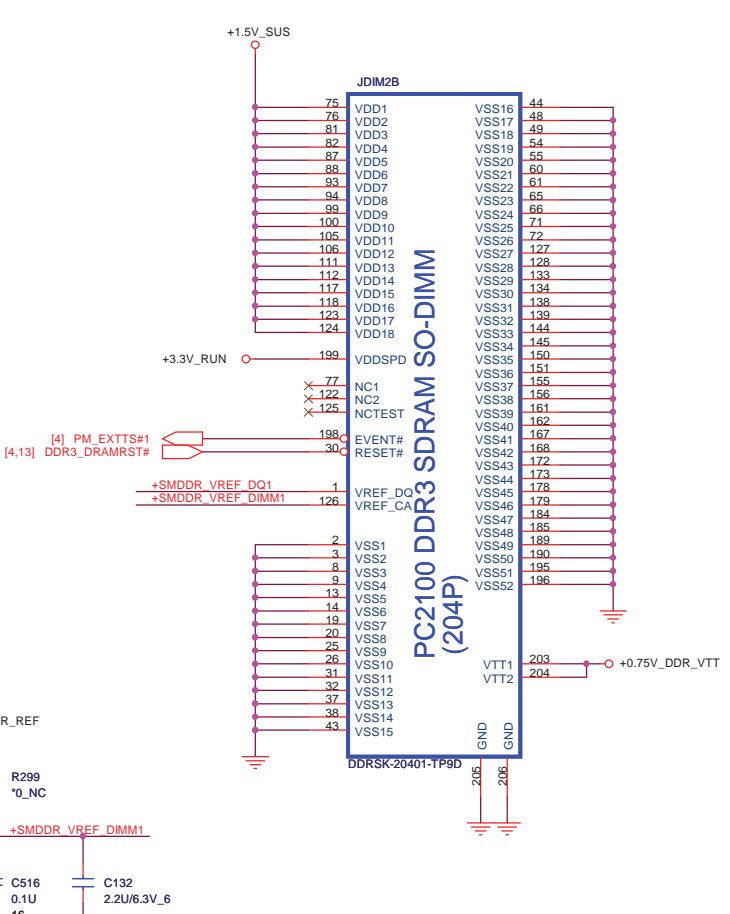
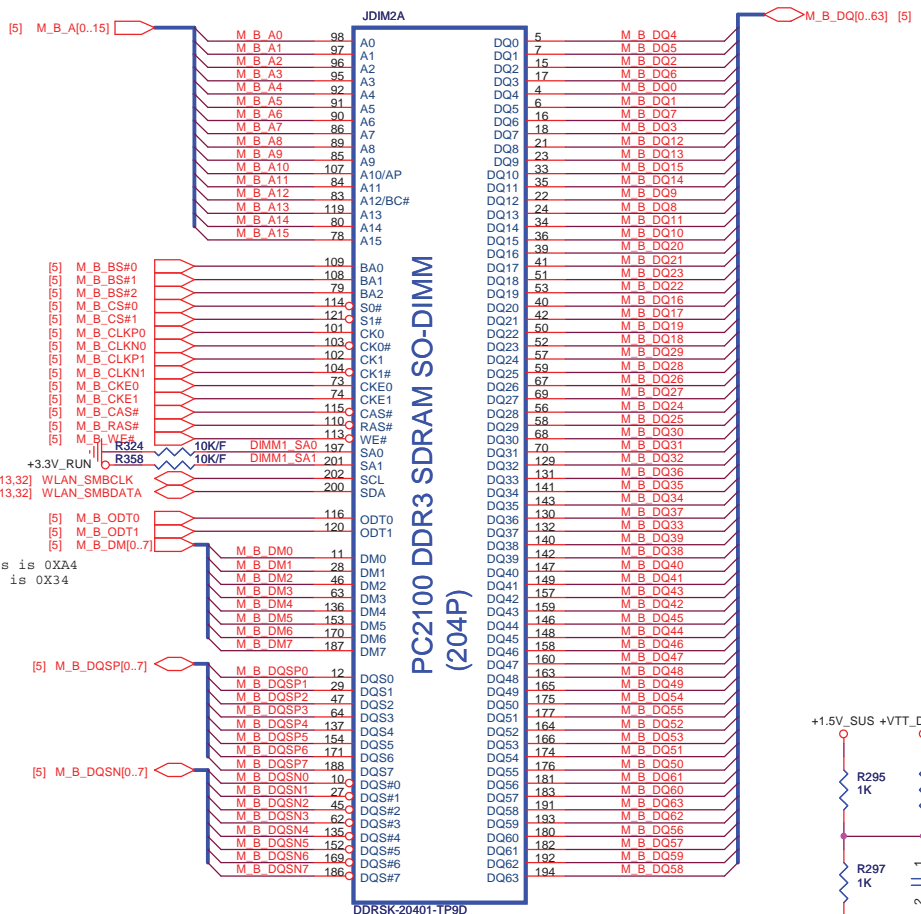
 **Quanta Computer Inc.**
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Size	Document Number	PCH 5/5 (POWER)	Rev	3A
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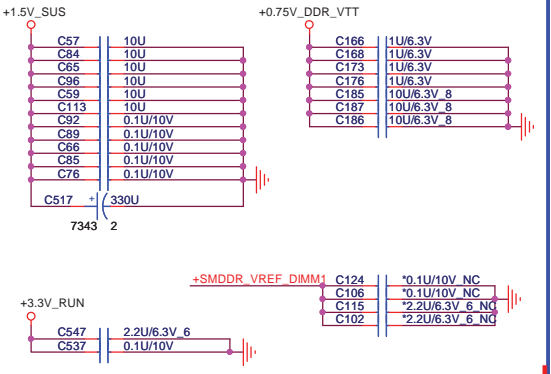


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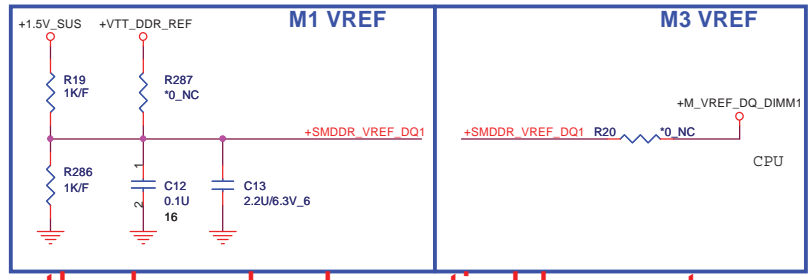
Size	Document Number	Rev
	DDR3 DIMM-0	3A
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Place these Caps near So-Dimm1.
 Some Projects replace 10UF 0805 by 4.7UF 0603
 It can cost down 30%



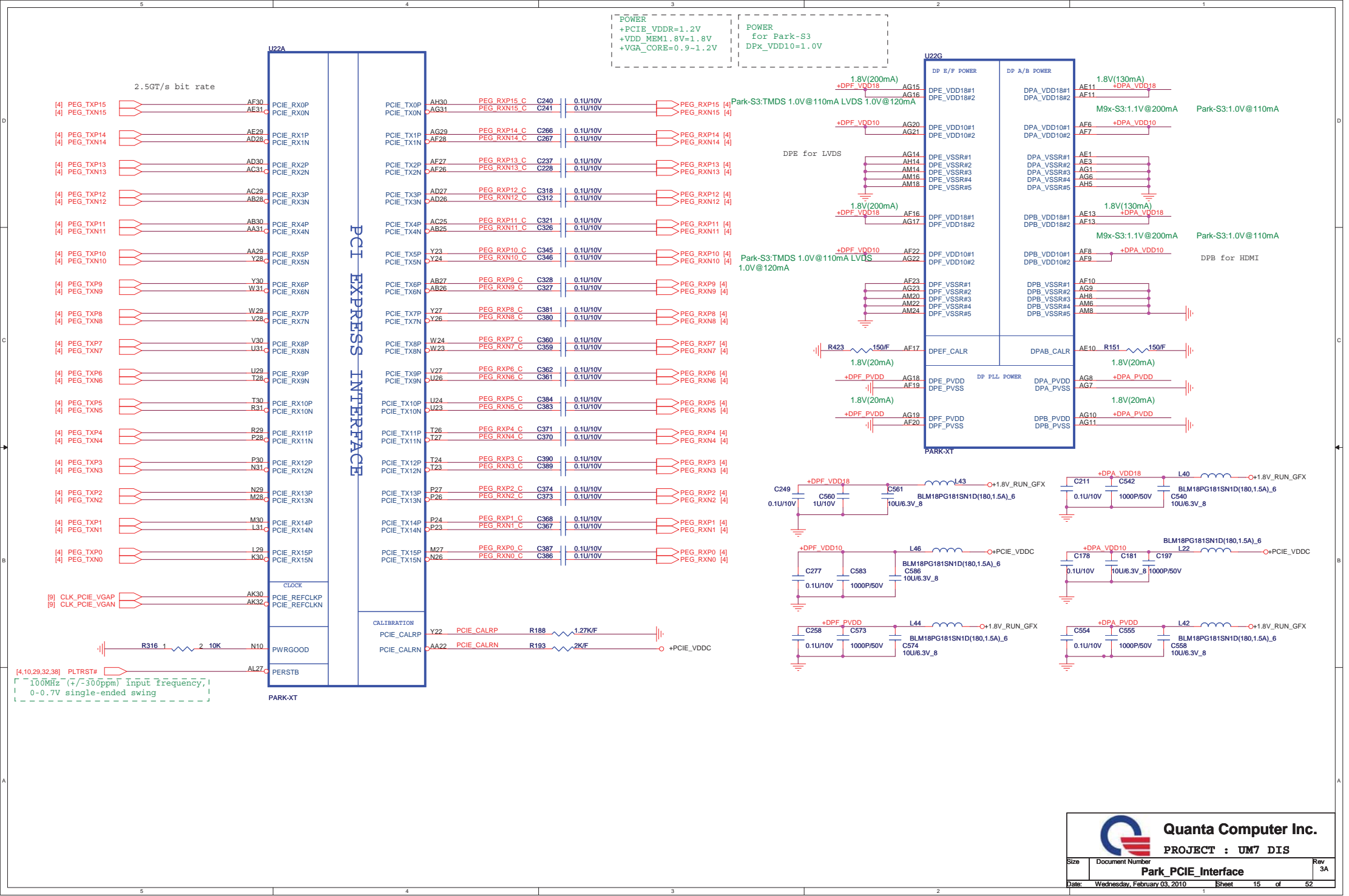
H9.2



<http://laptop-motherboard-schematic.blogspot.com/>

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	DDR3 DIMM-1	3A
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POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=0.9-1.2V
POWER for Park-S3
DPx_VDD10=1.0V

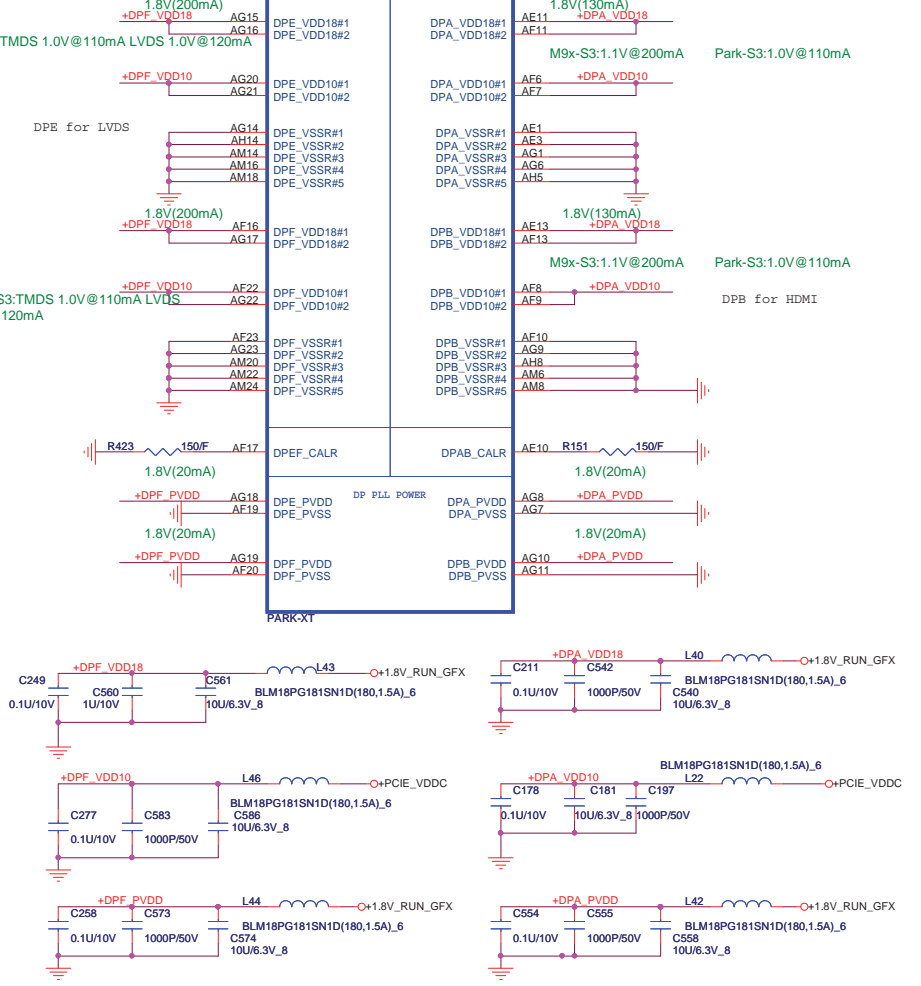
2.5GT/s bit rate

Source	Source Pin	U22A Pin	U22G Pin	Target Pin	Target Signal
PEG_TXP15	AF30	PCIE_RX0P	AH30	PEG_RXP15	PEG_RXP15 [4]
PEG_TXN15	AE31	PCIE_RX0N	AG31	PEG_RXN15	PEG_RXN15 [4]
PEG_TXP14	AE29	PCIE_RX1P	AG29	PEG_RXP14	PEG_RXP14 [4]
PEG_TXN14	AD28	PCIE_RX1N	AF28	PEG_RXN14	PEG_RXN14 [4]
PEG_TXP13	AD30	PCIE_RX2P	AF27	PEG_RXP13	PEG_RXP13 [4]
PEG_TXN13	AC31	PCIE_RX2N	AF26	PEG_RXN13	PEG_RXN13 [4]
PEG_TXP12	AC29	PCIE_RX3P	AD27	PEG_RXP12	PEG_RXP12 [4]
PEG_TXN12	AB28	PCIE_RX3N	AD26	PEG_RXN12	PEG_RXN12 [4]
PEG_TXP11	AB30	PCIE_RX4P	AC25	PEG_RXP11	PEG_RXP11 [4]
PEG_TXN11	AA29	PCIE_RX4N	AB25	PEG_RXN11	PEG_RXN11 [4]
PEG_TXP10	AA29	PCIE_RX5P	Y23	PEG_RXP10	PEG_RXP10 [4]
PEG_TXN10	Y28	PCIE_RX5N	Y24	PEG_RXN10	PEG_RXN10 [4]
PEG_TXP9	Y30	PCIE_RX6P	AB27	PEG_RXP9	PEG_RXP9 [4]
PEG_TXN9	W31	PCIE_RX6N	AB26	PEG_RXN9	PEG_RXN9 [4]
PEG_TXP8	W29	PCIE_RX7P	Y27	PEG_RXP8	PEG_RXP8 [4]
PEG_TXN8	W23	PCIE_RX7N	Y26	PEG_RXN8	PEG_RXN8 [4]
PEG_TXP7	V30	PCIE_RX8P	LW24	PEG_RXP7	PEG_RXP7 [4]
PEG_TXN7	U31	PCIE_RX8N	W23	PEG_RXN7	PEG_RXN7 [4]
PEG_TXP6	U29	PCIE_RX9P	LV27	PEG_RXP6	PEG_RXP6 [4]
PEG_TXN6	R31	PCIE_RX9N	U26	PEG_RXN6	PEG_RXN6 [4]
PEG_TXP5	T30	PCIE_RX10P	U24	PEG_RXP5	PEG_RXP5 [4]
PEG_TXN5	R31	PCIE_RX10N	U23	PEG_RXN5	PEG_RXN5 [4]
PEG_TXP4	R29	PCIE_RX11P	T26	PEG_RXP4	PEG_RXP4 [4]
PEG_TXN4	P28	PCIE_RX11N	T27	PEG_RXN4	PEG_RXN4 [4]
PEG_TXP3	P30	PCIE_RX12P	T24	PEG_RXP3	PEG_RXP3 [4]
PEG_TXN3	N31	PCIE_RX12N	T23	PEG_RXN3	PEG_RXN3 [4]
PEG_TXP2	N29	PCIE_RX13P	P27	PEG_RXP2	PEG_RXP2 [4]
PEG_TXN2	M28	PCIE_RX13N	P26	PEG_RXN2	PEG_RXN2 [4]
PEG_TXP1	M30	PCIE_RX14P	P24	PEG_RXP1	PEG_RXP1 [4]
PEG_TXN1	L31	PCIE_RX14N	P23	PEG_RXN1	PEG_RXN1 [4]
PEG_TXP0	L29	PCIE_RX15P	M27	PEG_RXP0	PEG_RXP0 [4]
PEG_TXN0	K30	PCIE_RX15N	N26	PEG_RXN0	PEG_RXN0 [4]

PCI EXPRESS INTERFACE

Signal	U22A Pin	U22G Pin	Component	Value	Target
PCI_CALRP	Y22	PCIE_CALRP	R188	1.27K/F	
PCI_CALRN	AA22	PCIE_CALRN	R193	2K/F	+PCIE_VDDC

[4,10,29,32,38] PLTRST#
100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing



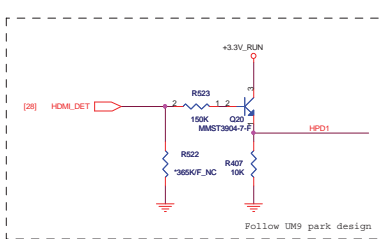
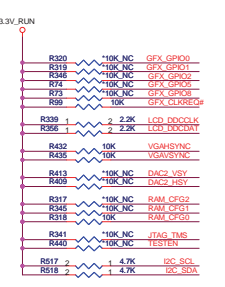
Quanta Computer Inc.
PROJECT : UM7 DIS
Park_PCIE_Interface
Date: Wednesday, February 03, 2010 15 of 52

MEM_ID[3:0]	Vendor	Type	Vendor P/N	Quanta P/N
0000	Hynix	Orion-die	H5701G38FR-17C	ADP572G1700
0001	Samsung	B-die	K4W111638HC12	ADP572G1702
0010	Samsung	B-die	K4W111638HC12	ADP572G1701
0011	Reserved			
0100	Reserved			
0101	Reserved			
0110	Reserved			
0111	Reserved			
1000	Reserved			
1001	Reserved			
1010	Reserved			
1011	Reserved			
1100	Reserved			
1101	Reserved			
1110	Reserved			
1111	Reserved			

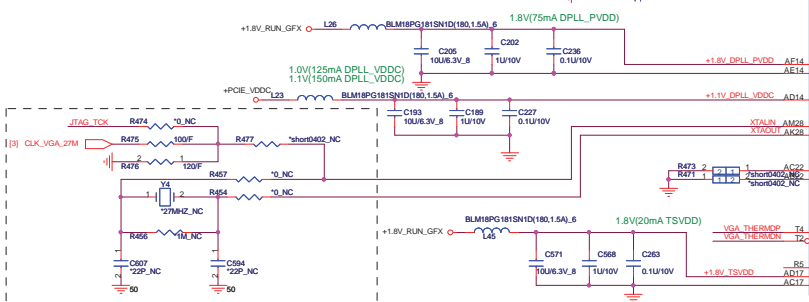
Memory Aperture size

GPIO9	GPIO13	GPIO12	GPIO11
BIOSROM	ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	1	0
0	32M	0	1
0	512M	1	0
0	1G	1	0
0	2G	1	0
0	4G	1	1

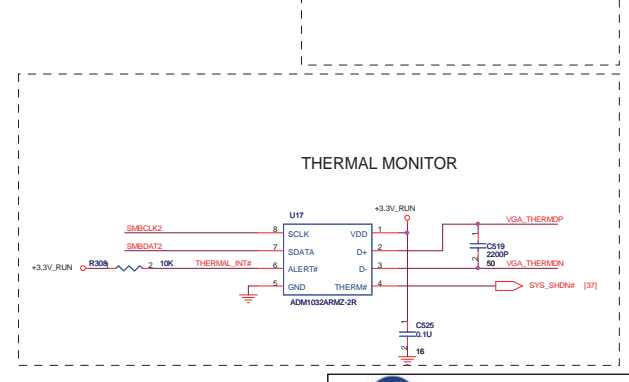
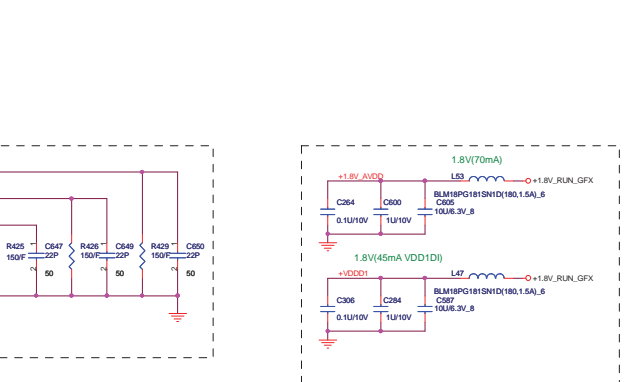
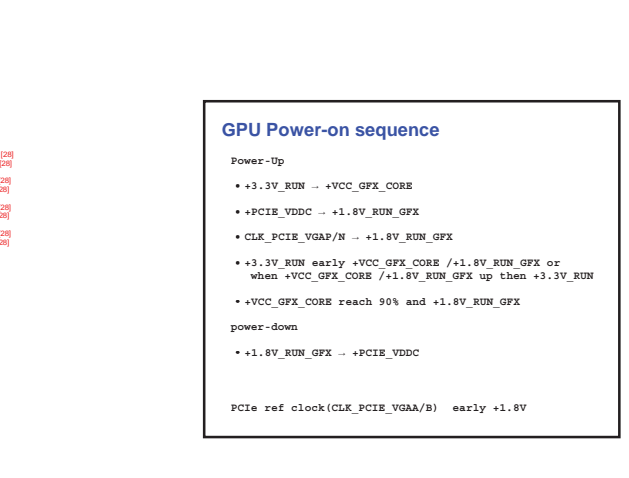
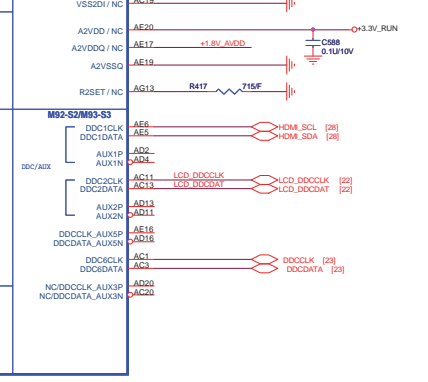
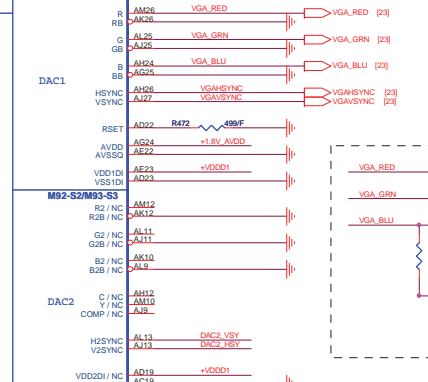
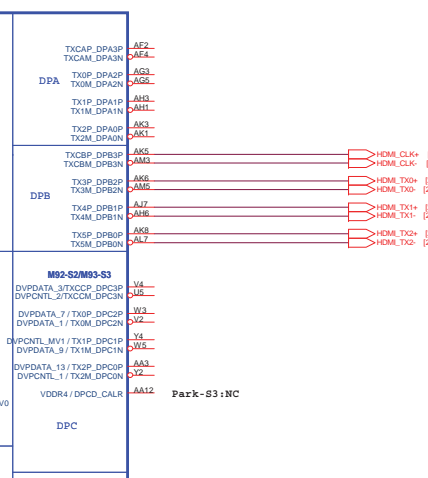
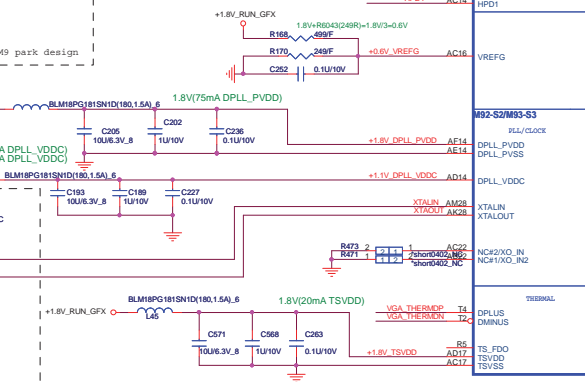
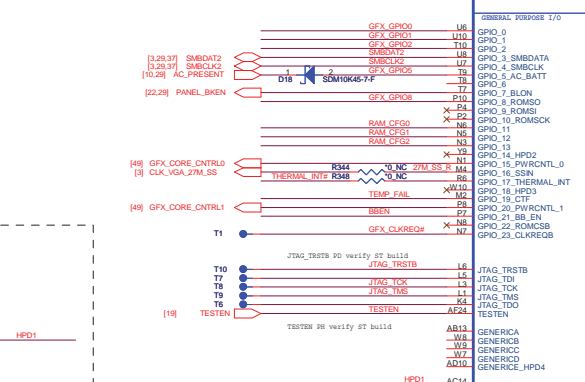
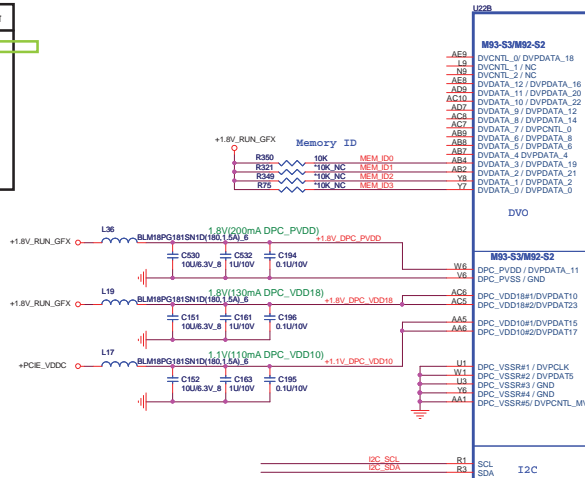
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

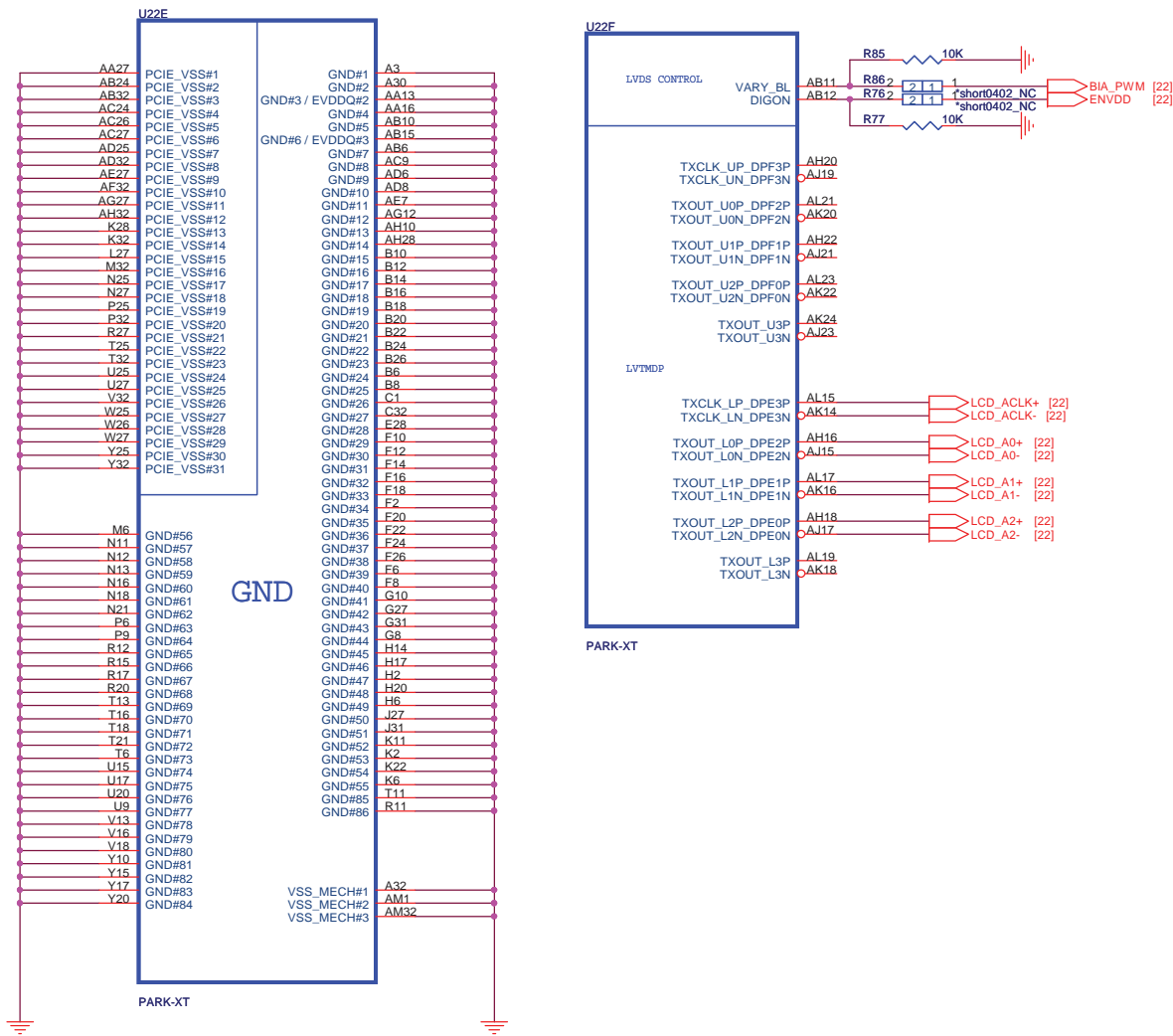


	BBEN	BBP
L	0	V-CORE
H	1	+1.8V



R475 --> 100pF for CLK_VGA_27M CLK Gen
0ohm for Crystal
CS11002P822
RHS CHIP 100 1/16W +-1% (0402)

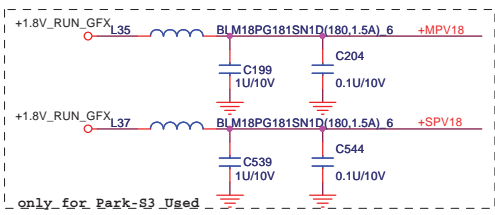
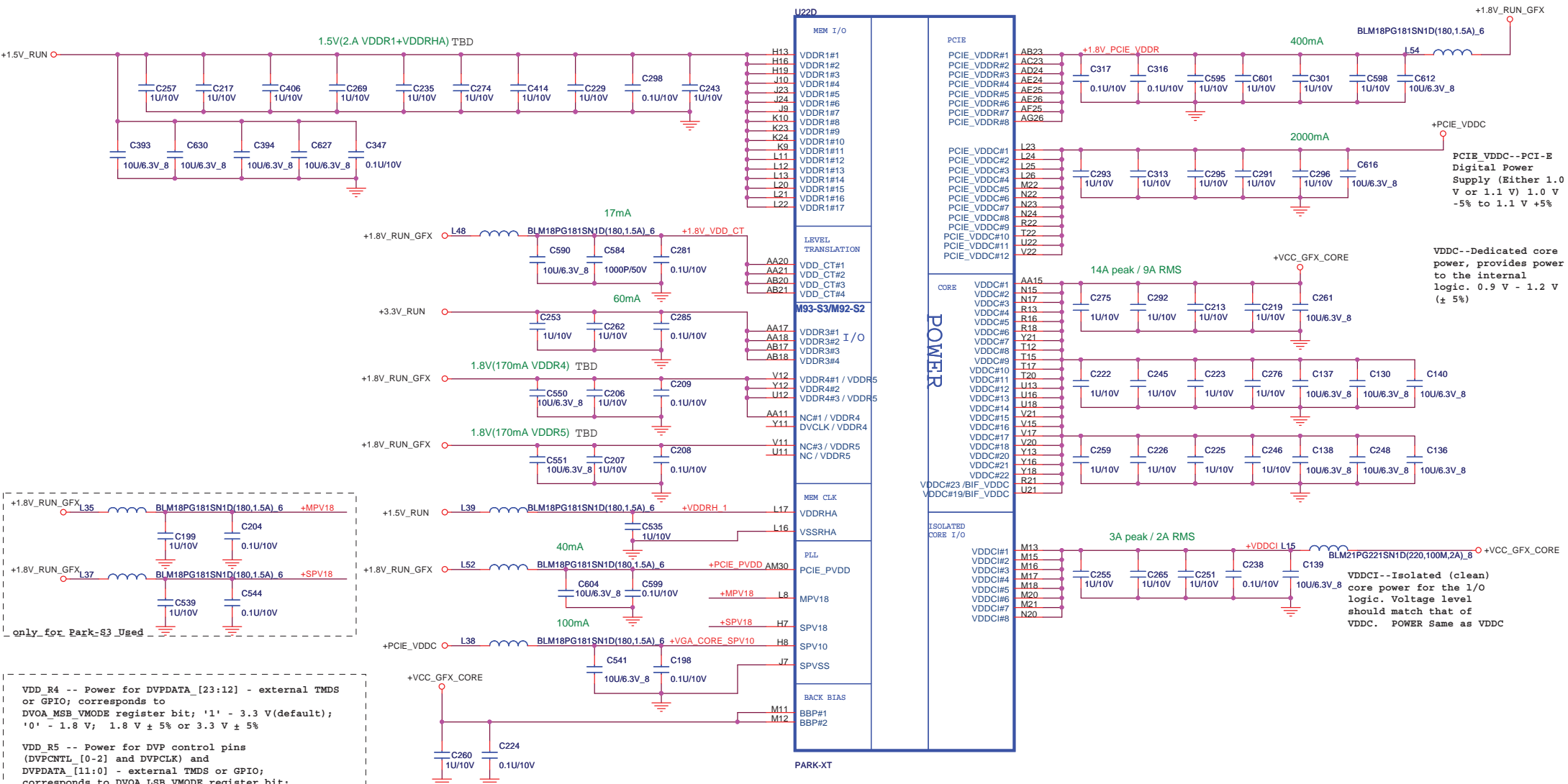




Strap Name	Pin	Straps description	Default Value
TX_PWRS_ENB	GPIO0	PCI Express Full TX Output Swing 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
RSVD	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
BIF_VGA_DIS	GPIO9		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
AUD [0]	VSYN	AUD[1] AUD[0] 00 No Audio function 01 Audio for DisplayPort and HDMI if dongle is detected	1
AUD (1)	HSYN	10 Audio for DisplayPort only 11 Audio for both DisplayPort and HDMI	1
VIP_DEVICE_STRAP_ENA	V2SYN	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
RSVD	GENERIC		0


Quanta Computer Inc.
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Park_GND / LVDS/ Straps		3A
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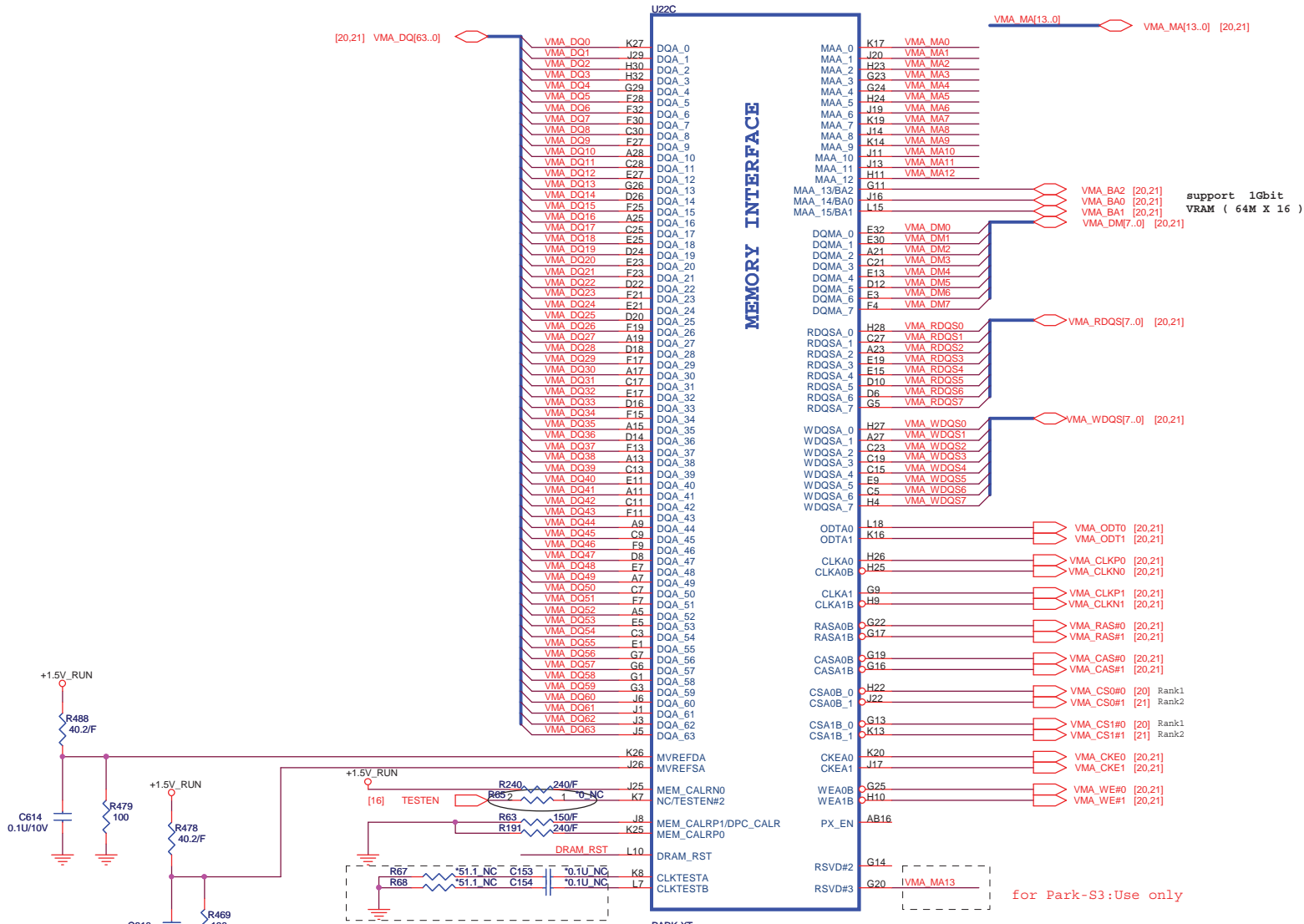
VDD_R4 -- Power for DVPDATA [23:12] - external TMSD or GPIO; corresponds to DVOA_MSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%

VDD_R5 -- Power for DVP control pins (DVPCNTL [0-2] and DVPCLK) and DVPDATA [11:0] - external TMSD or GPIO; corresponds to DVOA_LSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%



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Size	Document Number	Rev
	Park_Power_and_NC	3A
Date:	Wednesday, February 03, 2010	Sheet 18 of 52



For normal GPU operation, these signals can be left floating (do not populate the capacitors and resistors).

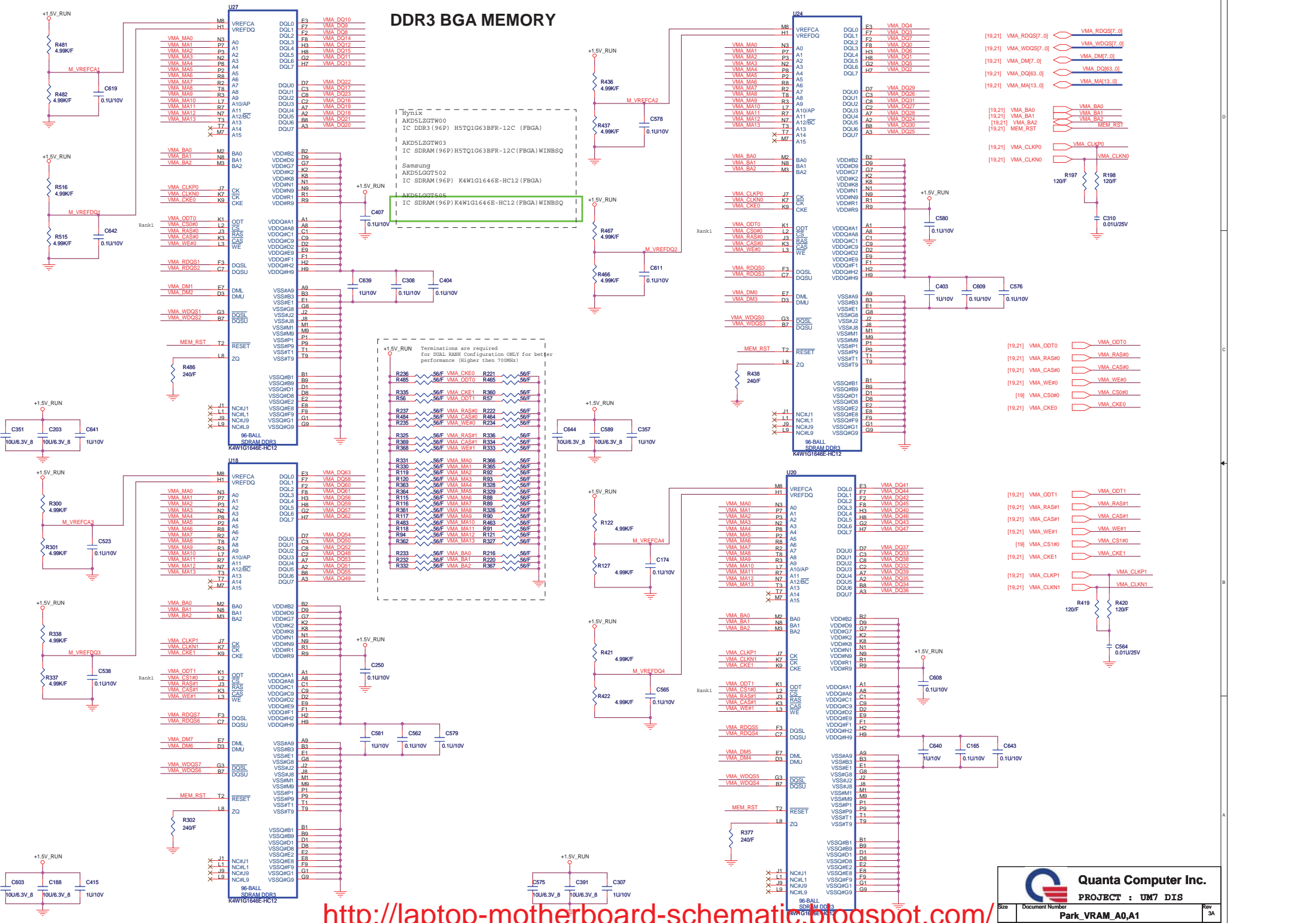
	M9x-S2/S3	Park-S3
MEM_CALRNO (J25)	NC	240R
MEM_CALRP0 (K25)	NC	240R
MEM_CALRP1 (J8)	240R	150R
TESTEN2#2 (K7)	NC	0R
R1	NC	10K
R2	0R	51R
R3	2.2K	NC
C1	2.2nF	68pF

240R: CS12402FB03
150R: CS11502FB21

0R: CS00002JB38
51R: CS05102JB35

2.2nF: CH22206KB16
68pF: CH06806JB01

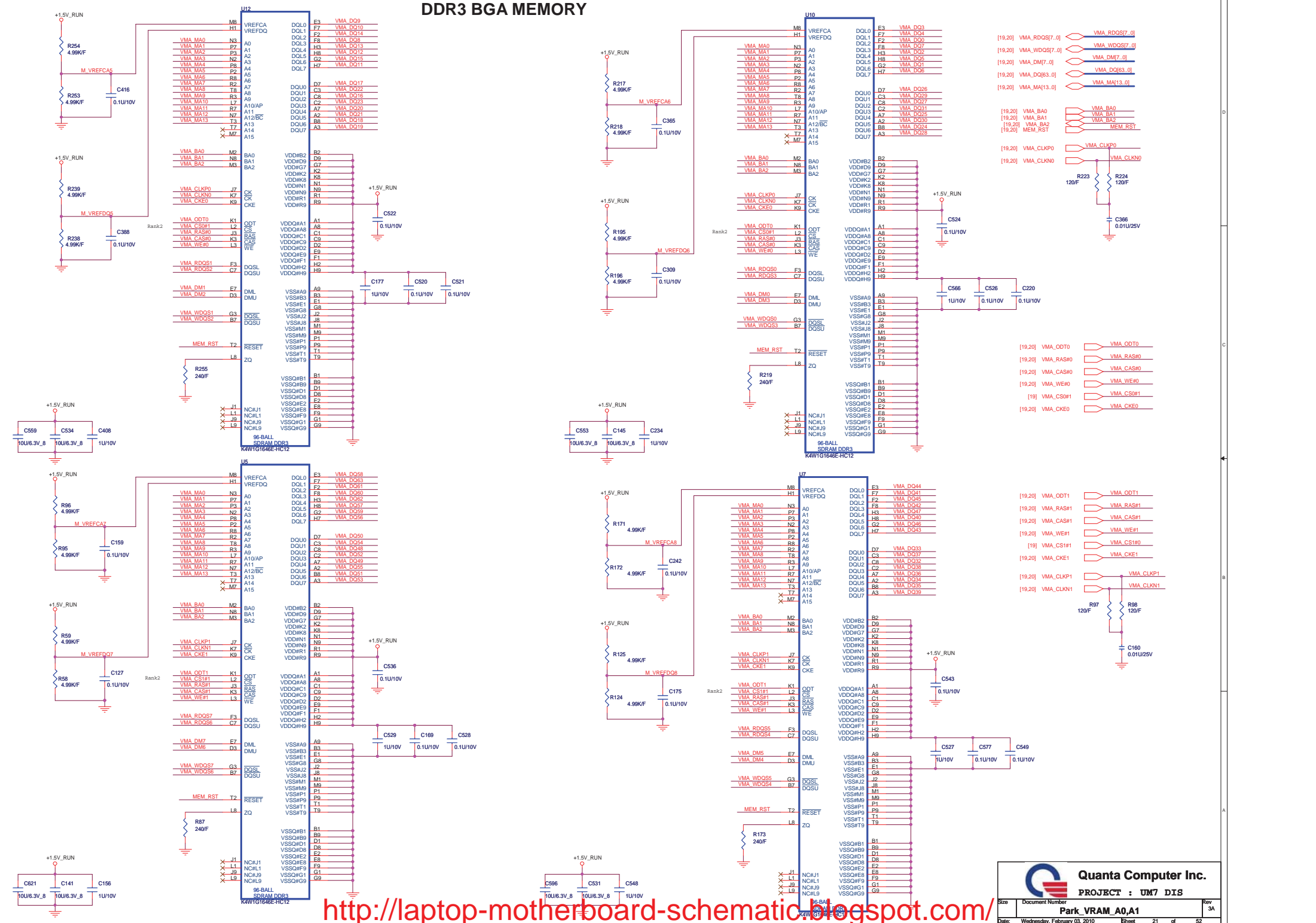
DDR3 BGA MEMORY



<http://laptop-motherboard-schematic.blogspot.com/>

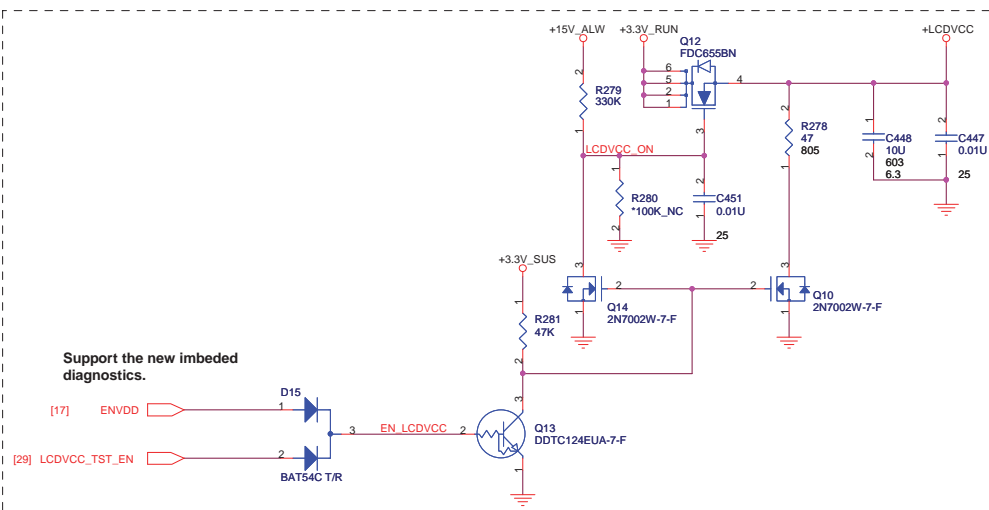
Quanta Computer Inc.
PROJECT : UM7 DIS
Park_VRAM_A0,A1
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DDR3 BGA MEMORY

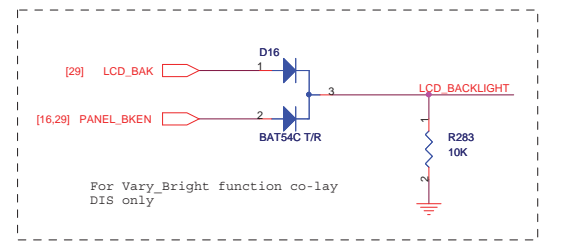
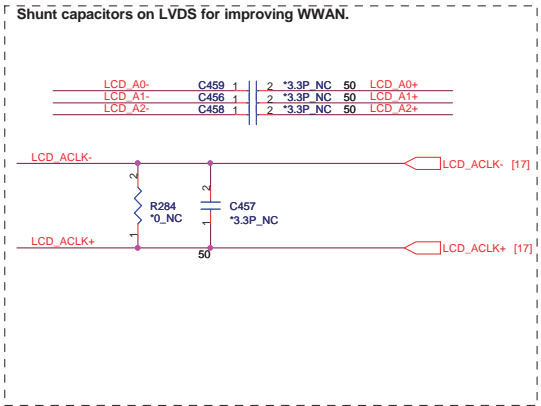
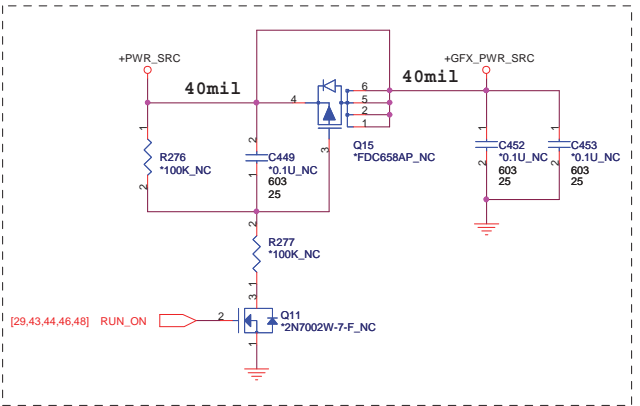
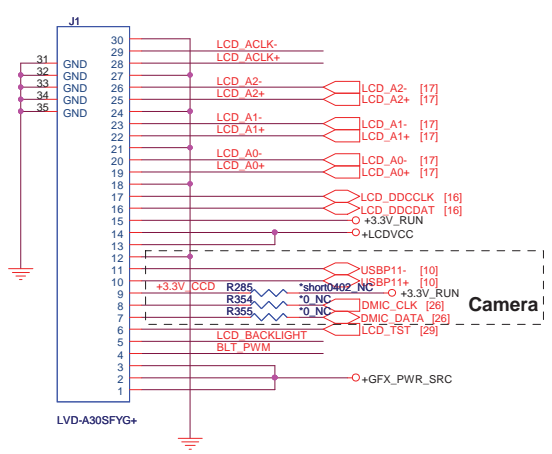
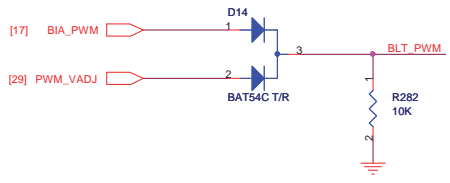
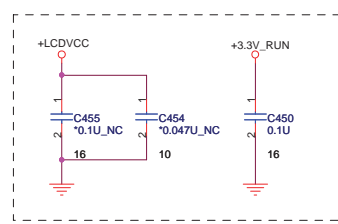
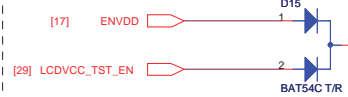


Quanta Computer Inc.
PROJECT : UM7 DIS
Park_VRAM_A0_A1
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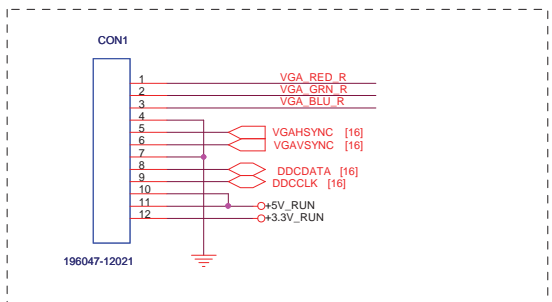
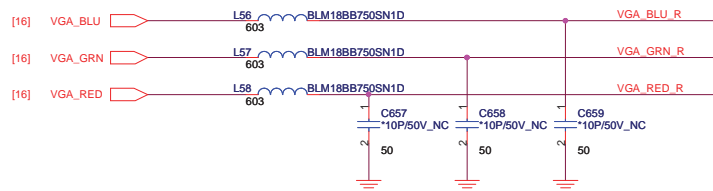
<http://laptop-motherboard-schematic.blogspot.com/>




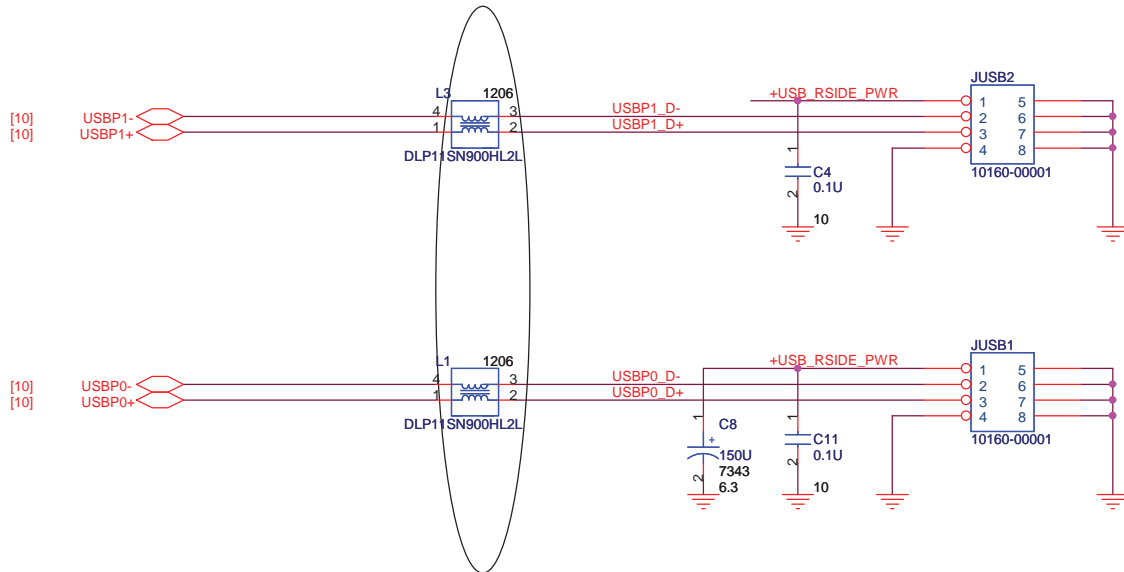
Support the new imbedded diagnostics.



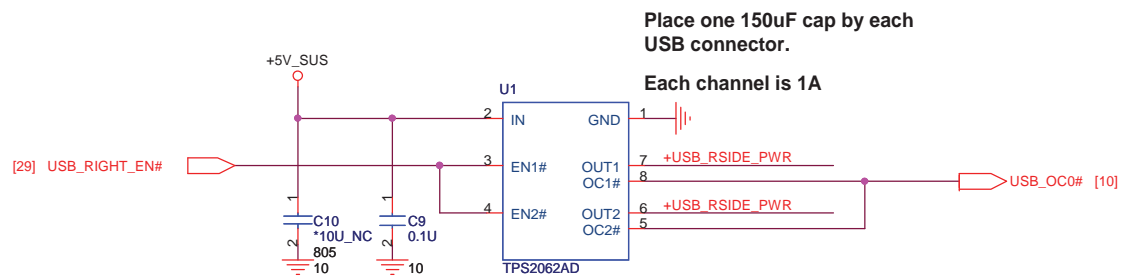
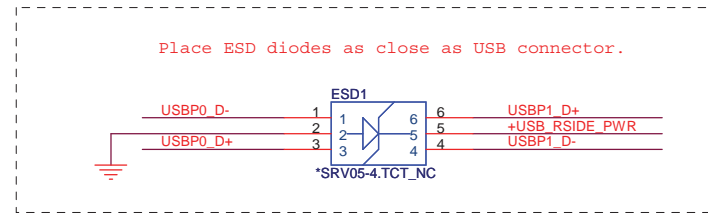
For Vary_Bright function co-lay DIS only



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		3A
Size	Document Number	
CRT CONN		
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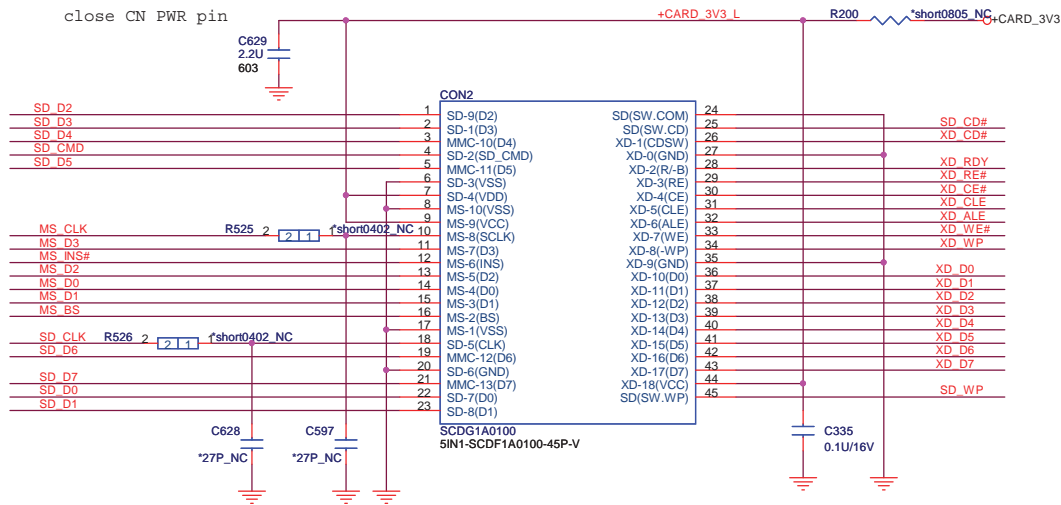


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



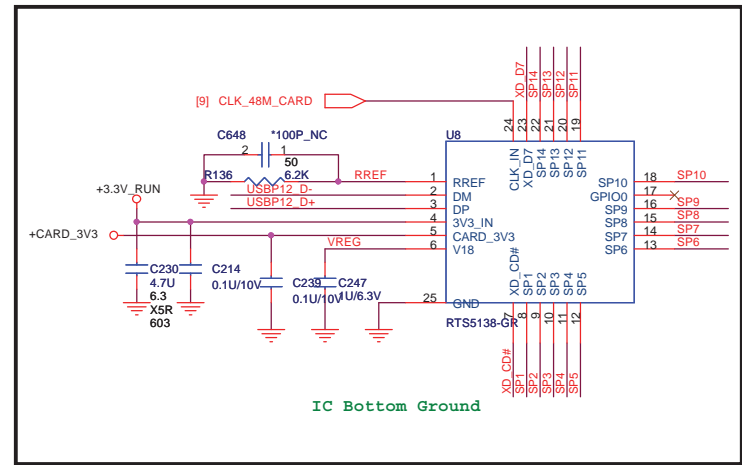
Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	Right USB	3A
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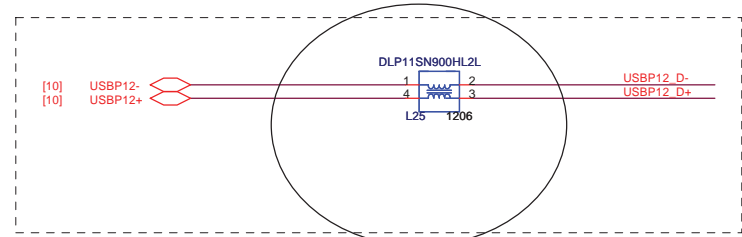


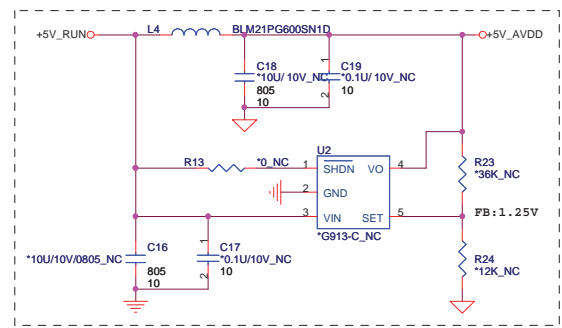
SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#		MS INS#
SP3	XD CE#	SD D1	
SP4	XD CLE	SD D0	MS D7
SP5	XD ALE	SD D7	MS D3
SP6	XD WE#	SD CD#	
SP7	XD WP	SD D6	MS D6
SP8	XD D0	SD CLK	MS D2
SP9	XD D1	SD D5	MS D0
SP10	XD D2	SD CMD	
SP11	XD D3	SD D4	MS D4
SP12	XD D4	SD D3	MS D1
SP13	XD D5	SD D2	MS D5
SP14	XD D6		MS BS

Share Pin

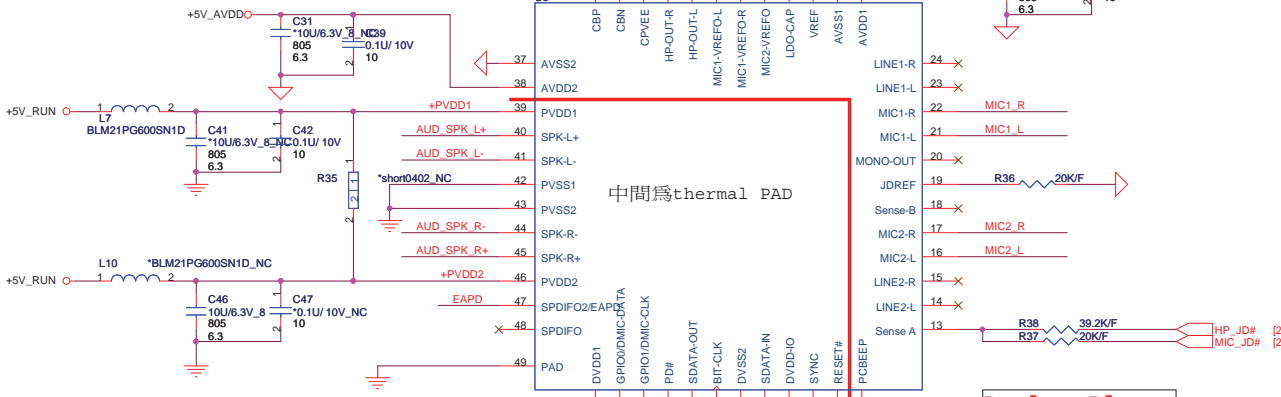


RTS5138 - QFN24





AVDD1, AVDD2 TYP=48mA

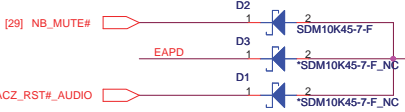
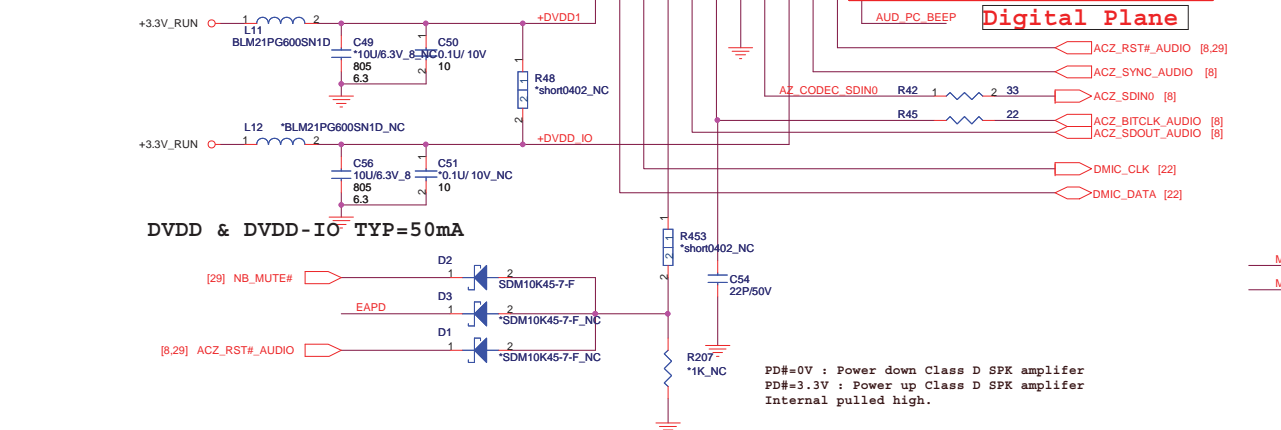


中間為thermal PAD

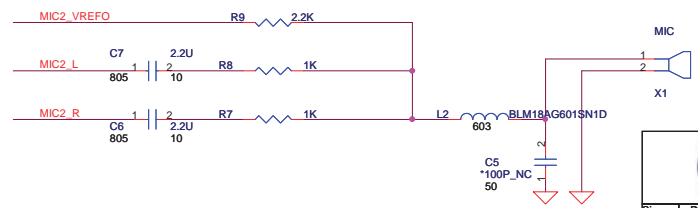
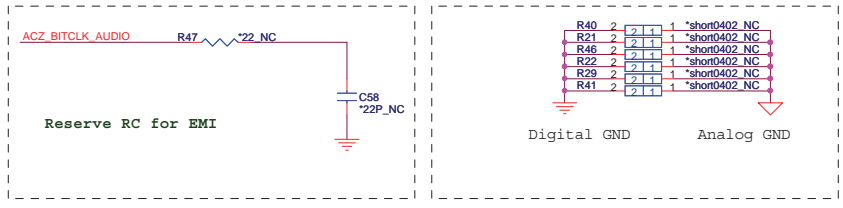
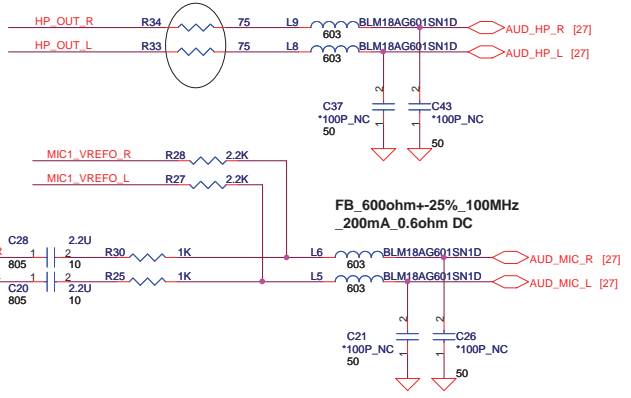
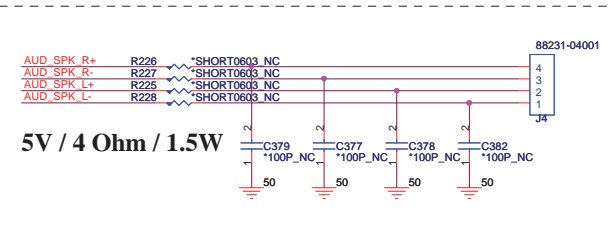
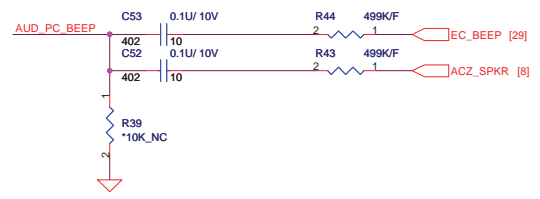
Analog Plane

Digital Plane

DVDD & DVDD-IO TYP=50mA



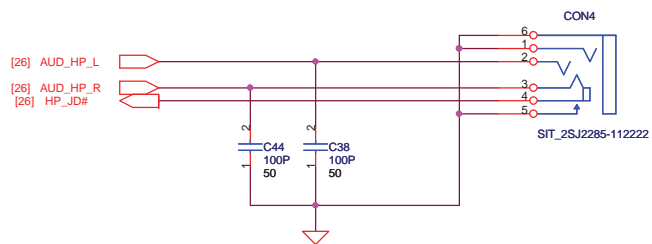
PD#=0V : Power down Class D SPK amplifier
 PD#=3.3V : Power up Class D SPK amplifier
 Internal pulled high.



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 Azelia CODEC(ALC269)
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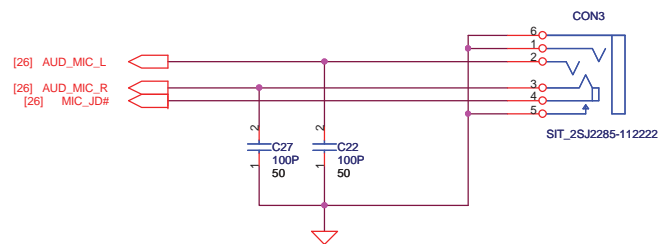
HP JACKN

SUYIN NORMAL OPEN



MIC JACK

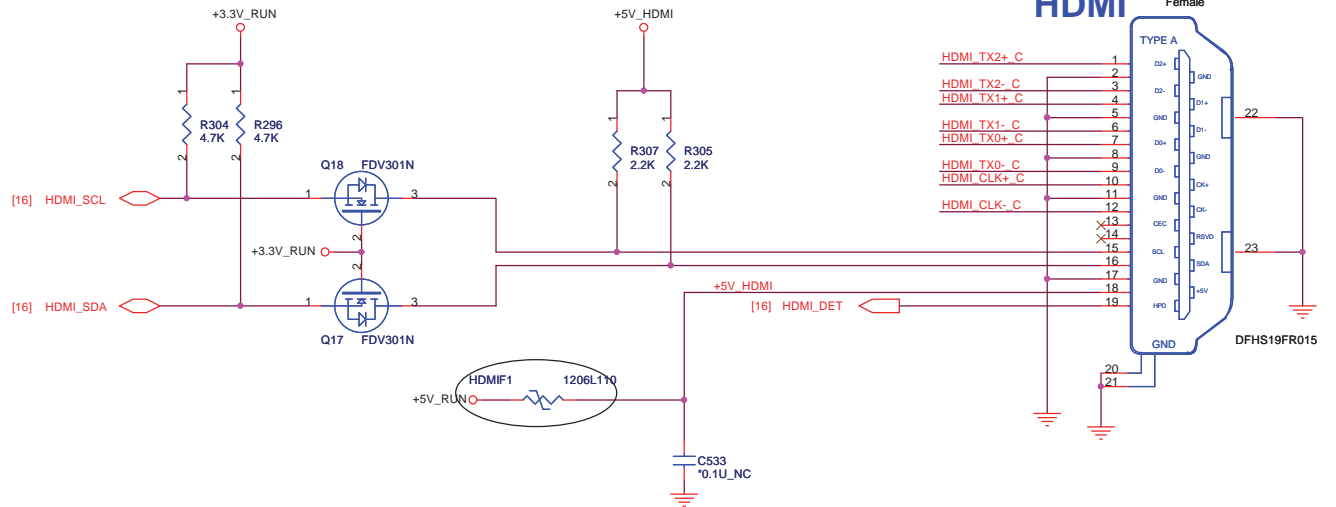
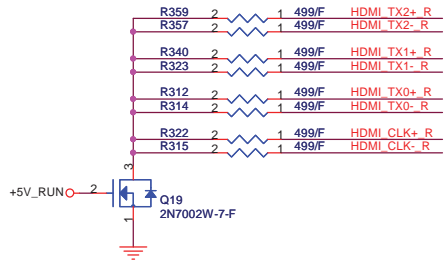
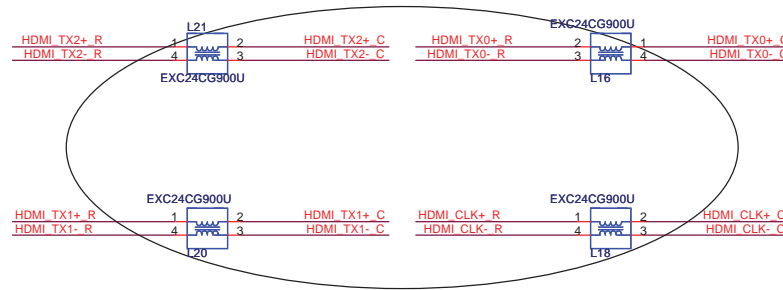
SUYIN NORMAL OPEN



Quanta Computer Inc.
PROJECT : UM7 DIS

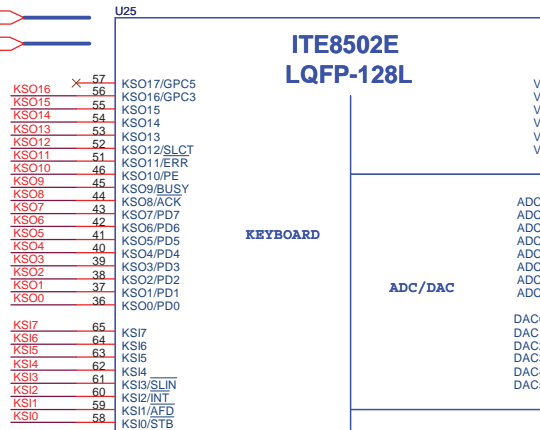
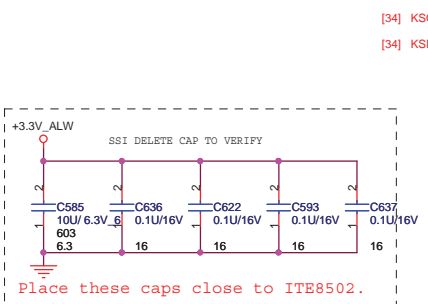
Size	Document Number	Rev
	AUDIO CONN	3A
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[16] HDMI_TX2+	C172	0.1U	HDMI TX2+ R
[16] HDMI_TX2-	C167	0.1U	HDMI TX2- R
[16] HDMI_TX1+	C164	0.1U	HDMI TX1+ R
[16] HDMI_TX1-	C157	0.1U	HDMI TX1- R
[16] HDMI_TX0+	C142	0.1U	HDMI TX0+ R
[16] HDMI_TX0-	C144	0.1U	HDMI TX0- R
[16] HDMI_CLK+	C155	0.1U	HDMI CLK+ R
[16] HDMI_CLK-	C150	0.1U	HDMI CLK- R

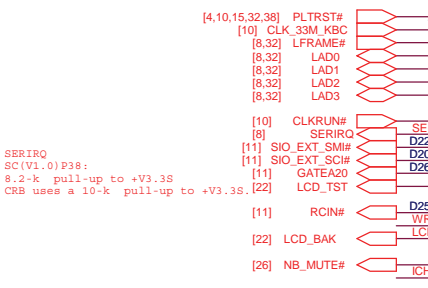


Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	Blank	3A
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**ITE8502E
LQFP-128L**



KEYBOARD

ADC/DAC

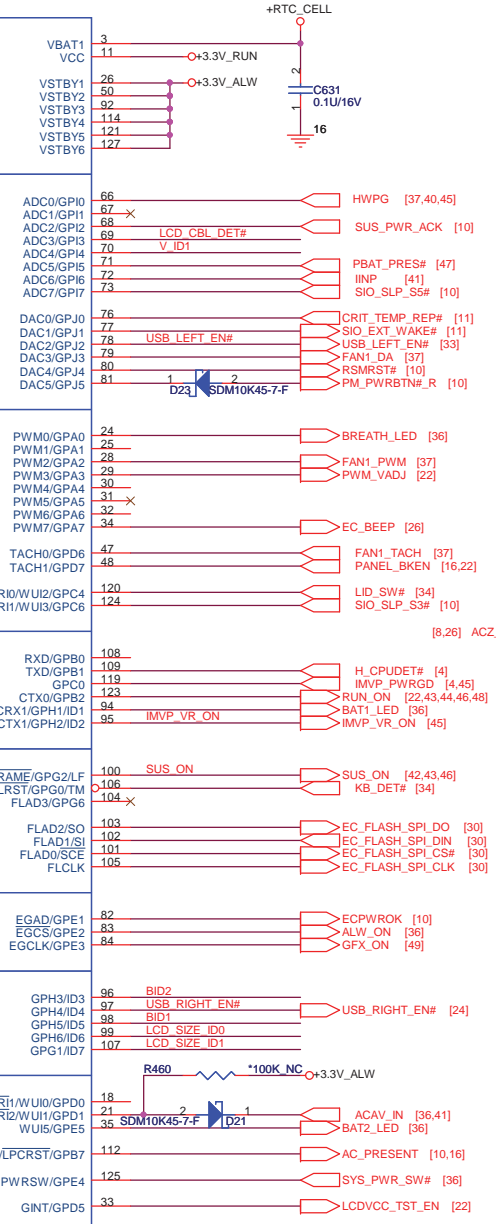
LPC

IR/UART

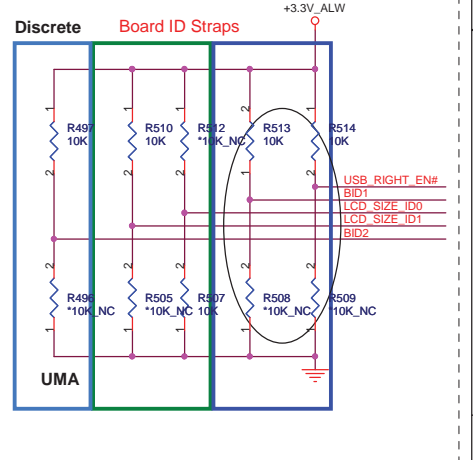
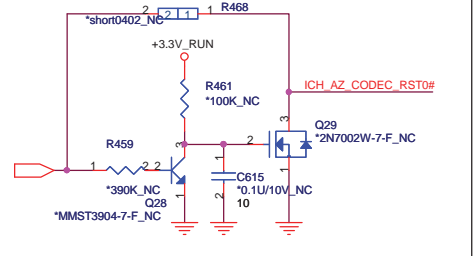
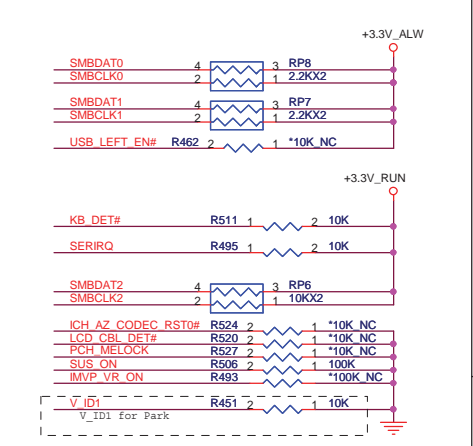
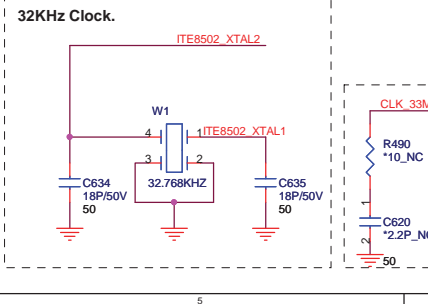
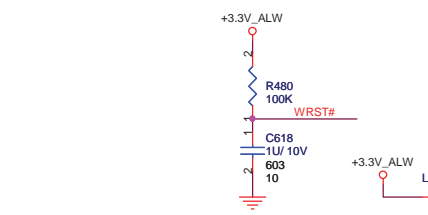
**LPC/FWH
FLASH**

EGPC

GPIO



**Charge and BAT
PCH
VGA, LAN, Clock
Thermal IC**



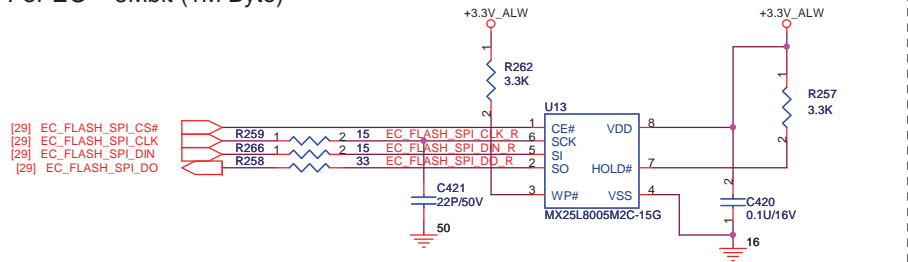
LCD SIZE ID0	LCD SIZE ID0	LCD SIZE	BID1	USB RIGHT EN#	Build
0	0	13.3"	0	0	SSI (X00)
0	1	14"	0	1	PT (X01)
1	0	17"	1	0	ST (X02)
			1	1	QT (A00)
			0	0	RAMP(A00)

Quanta Computer Inc.
PROJECT : UM7 DIS

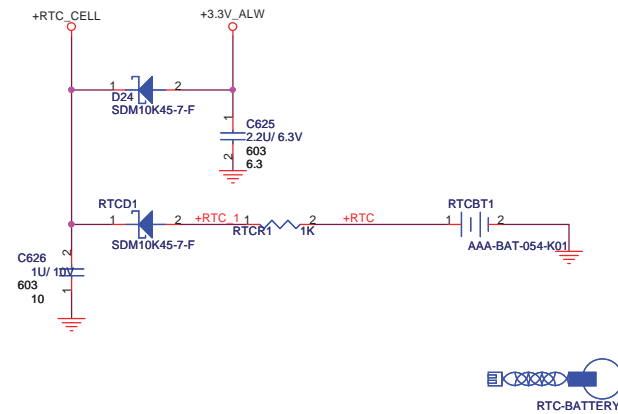
SIO ITE8502

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For EC 8Mbit (1M Byte)

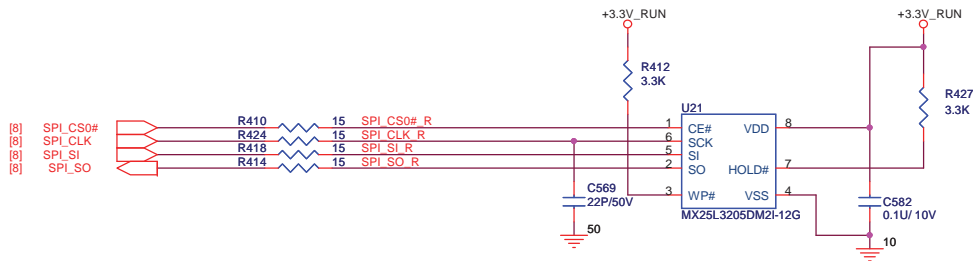


RTC BATTERY




For PCH
32Mbit (4M Byte)

2nd source:AKE39ZP0N00

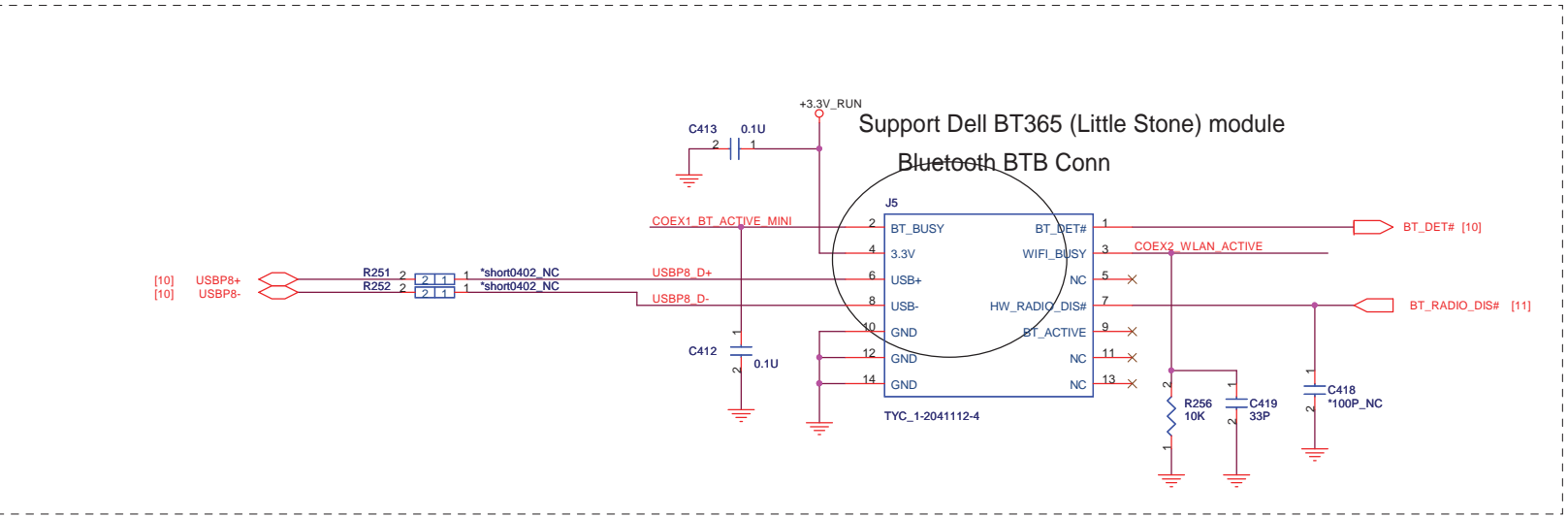
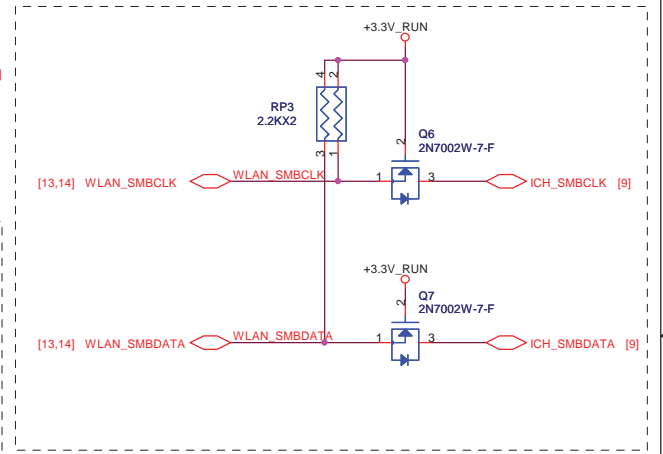
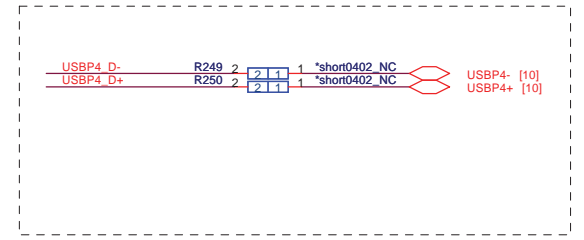
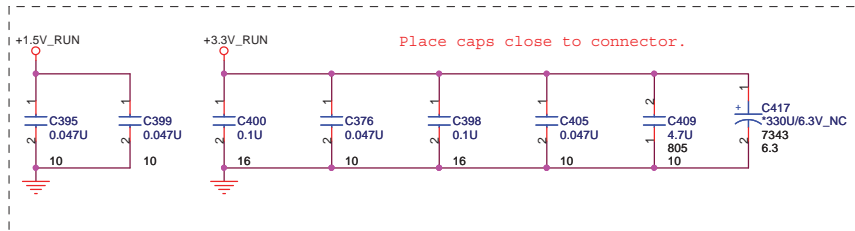
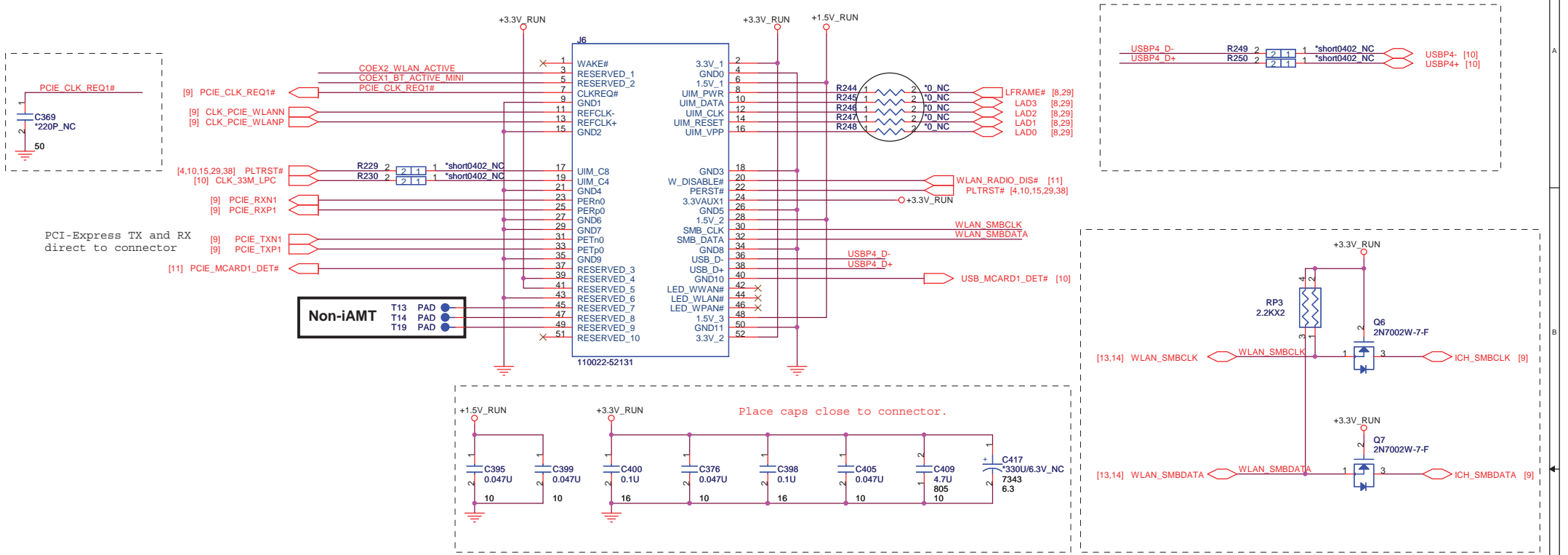




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		Quanta Computer Inc.
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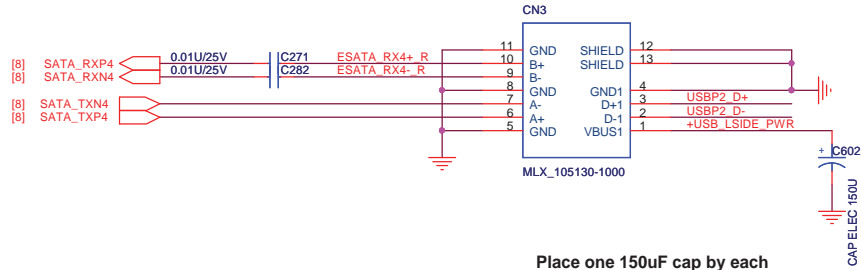
MiniCard WLAN connector



Quanta Computer Inc.
PROJECT : UM7 DIS

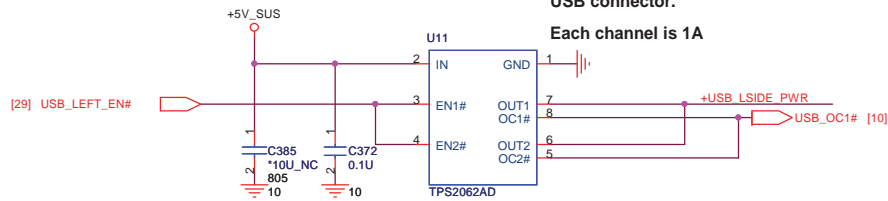
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	MINI-Card WLAN / BT	3A
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USB and eSATA Conn.

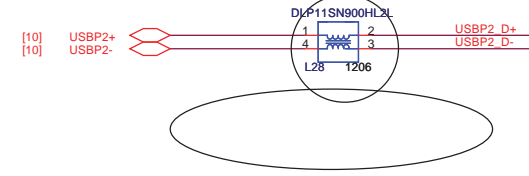


Place one 150uF cap by each USB connector.

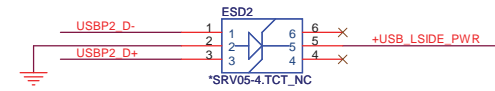
Each channel is 1A



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



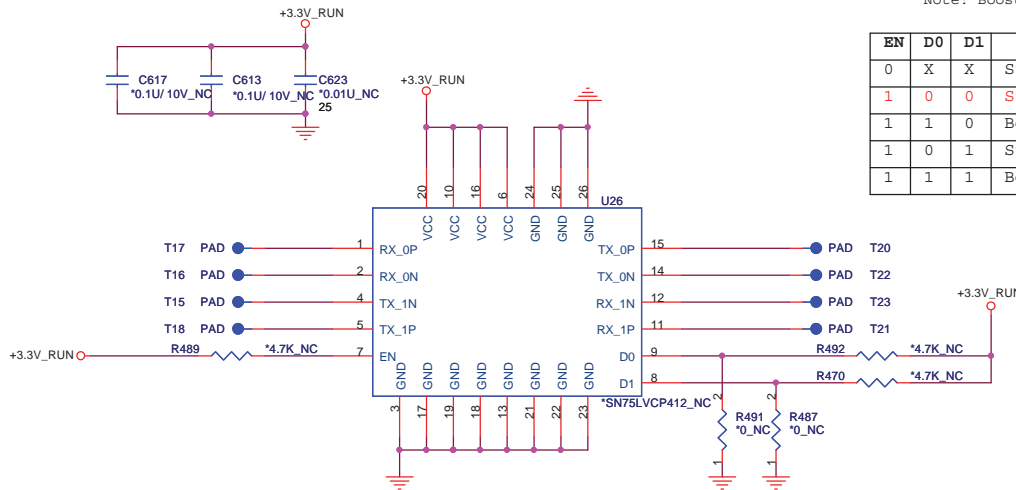
Place ESD diodes as close as USB connector.

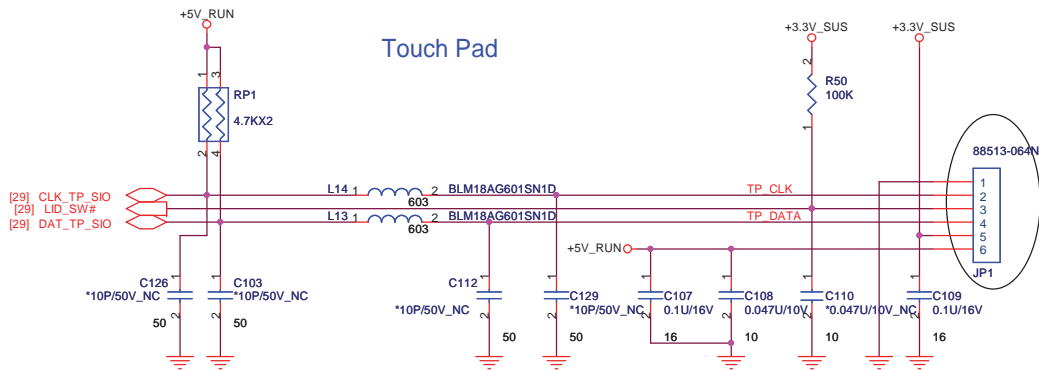


E-SATA Re-driver

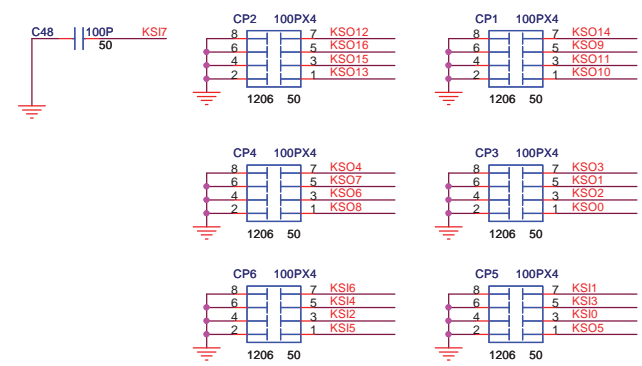
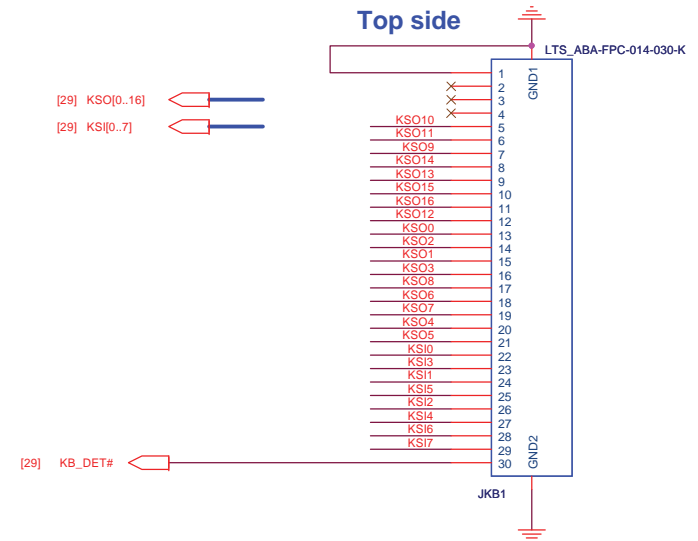
Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost



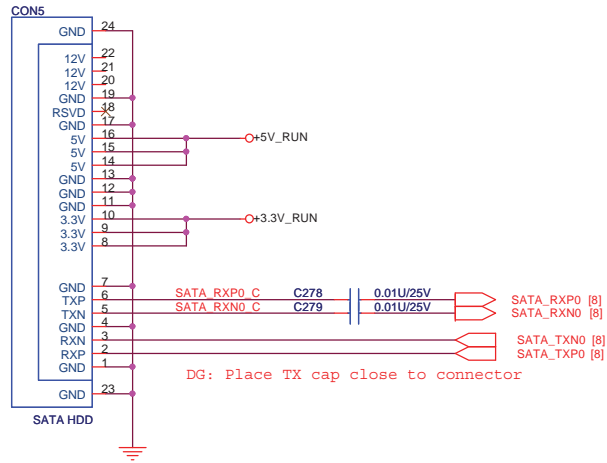


KEYBOARD CONNECTOR

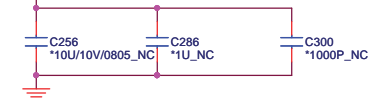


100P CAPS CLOSE TO JKB1

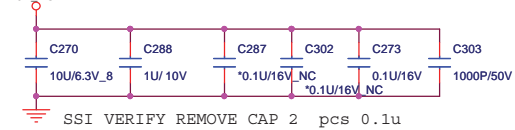
SATA Connector.



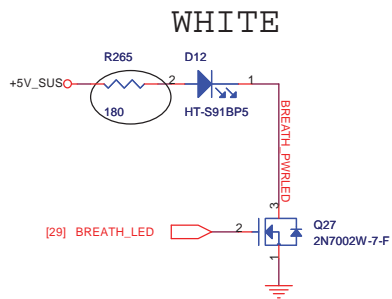
+3.3V_RUN Place caps close to connector.



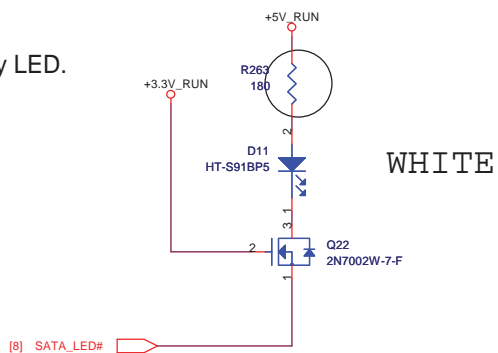
+5V_RUN Place caps close to connector.



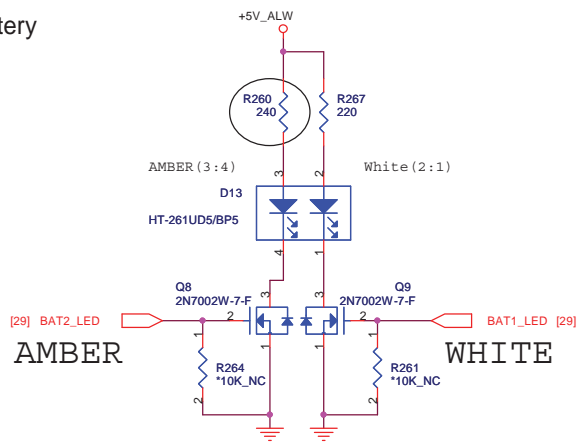
Power



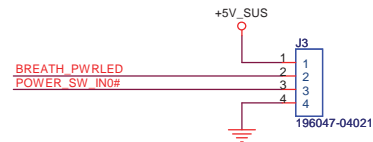
HDD activity LED.



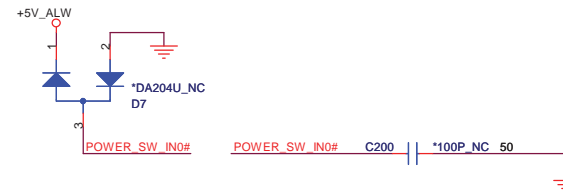
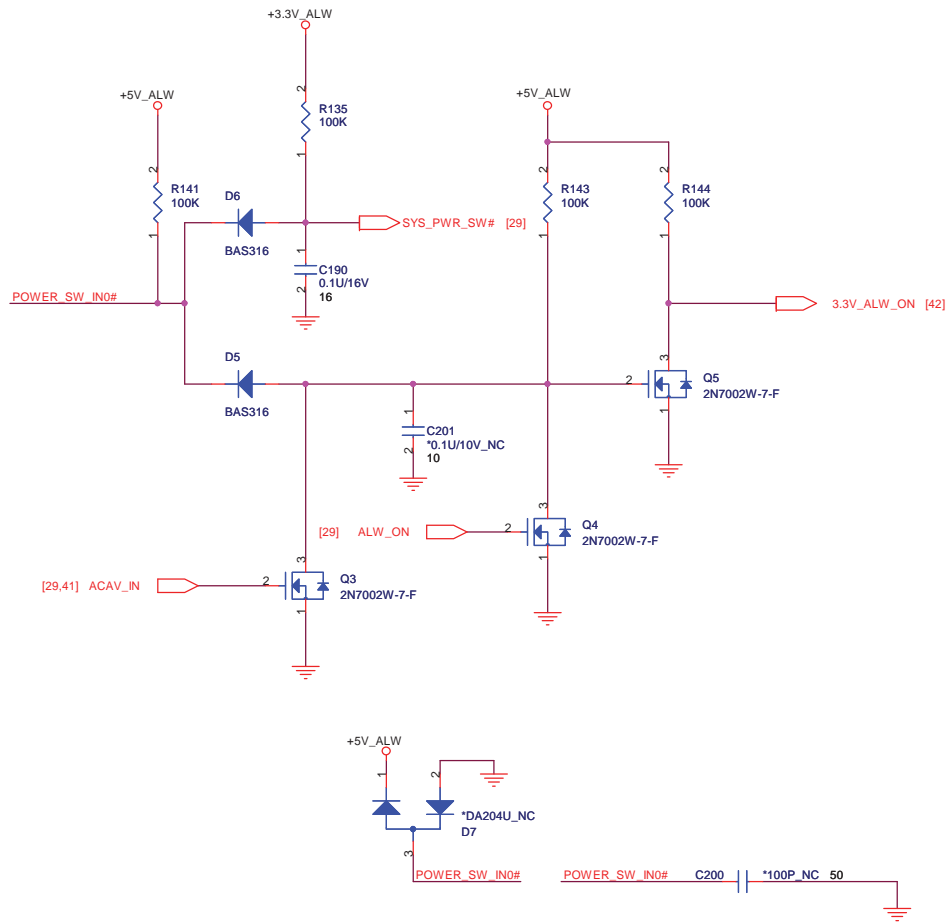
Battery



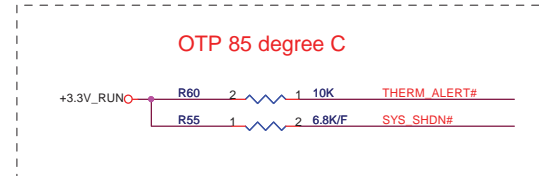
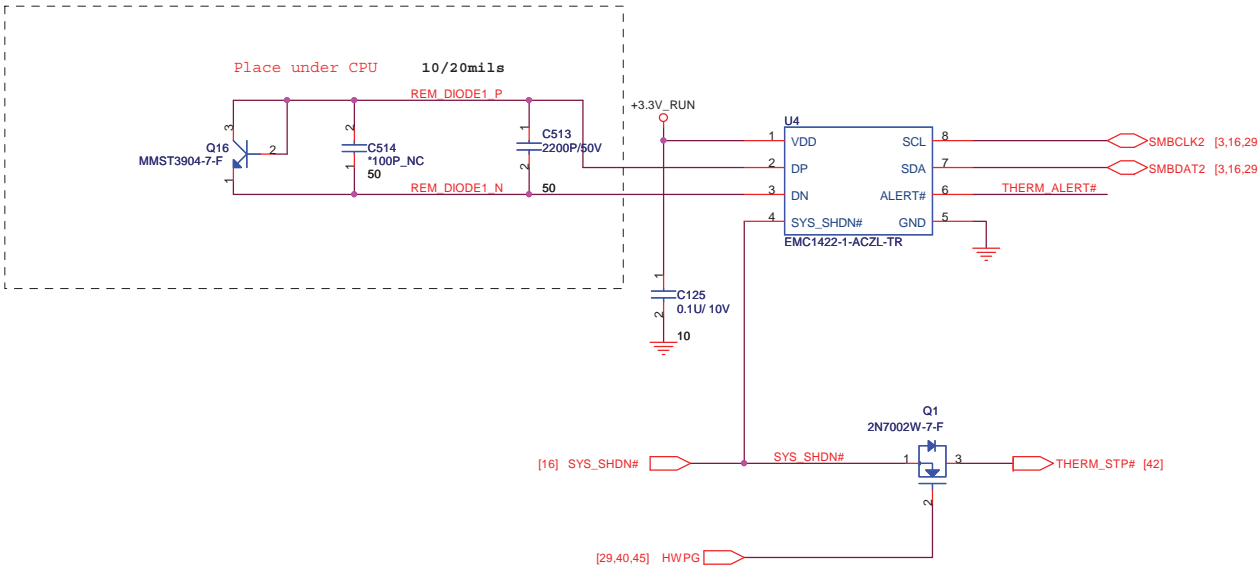
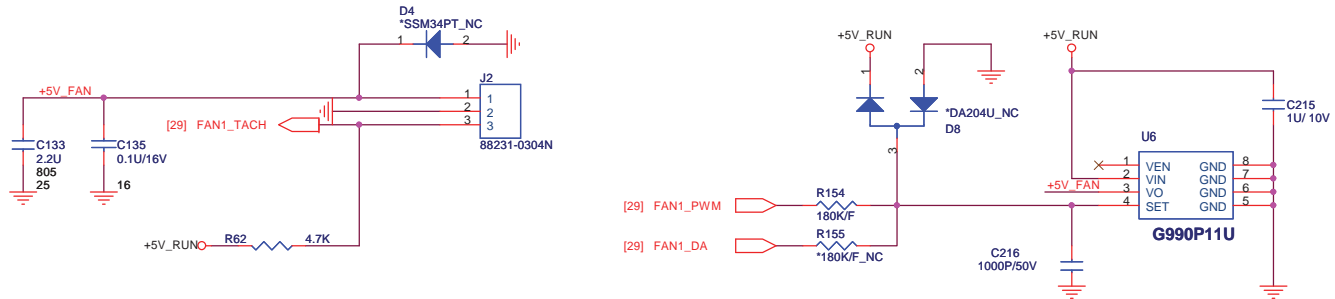
Power button Cable

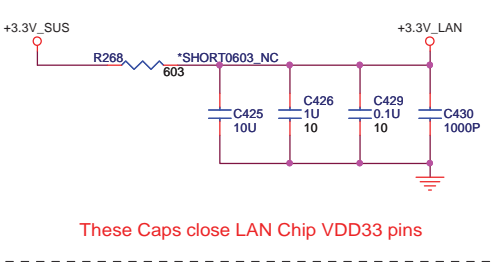
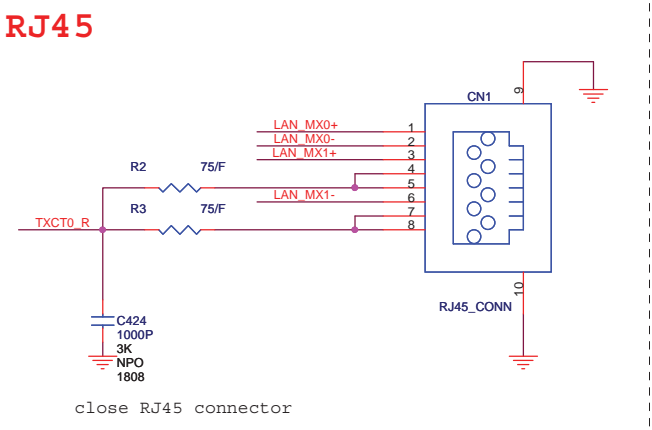
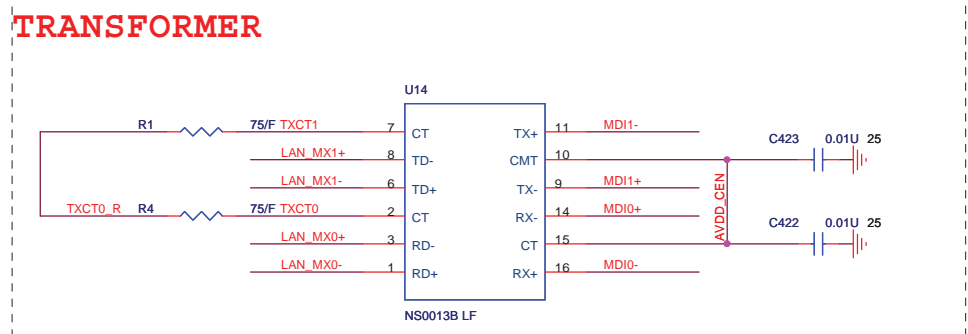
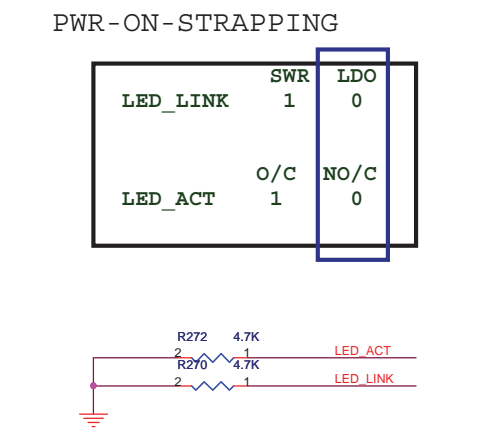
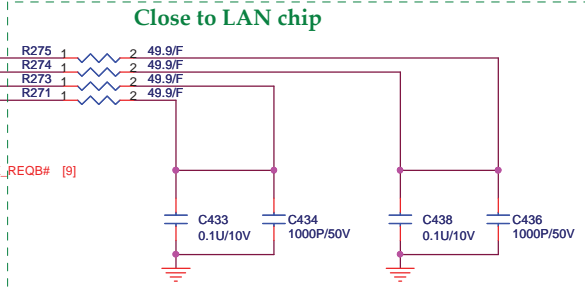
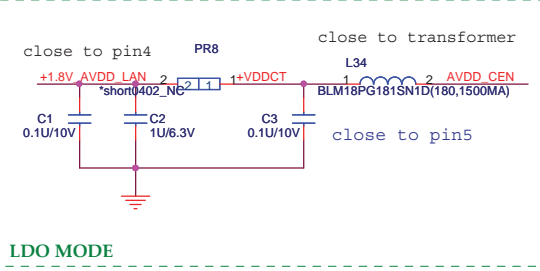
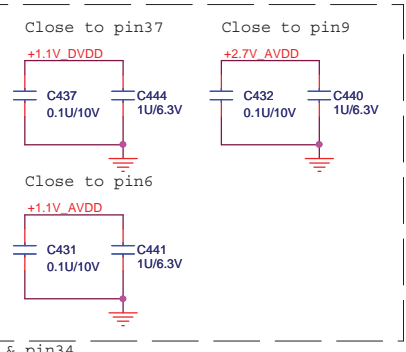
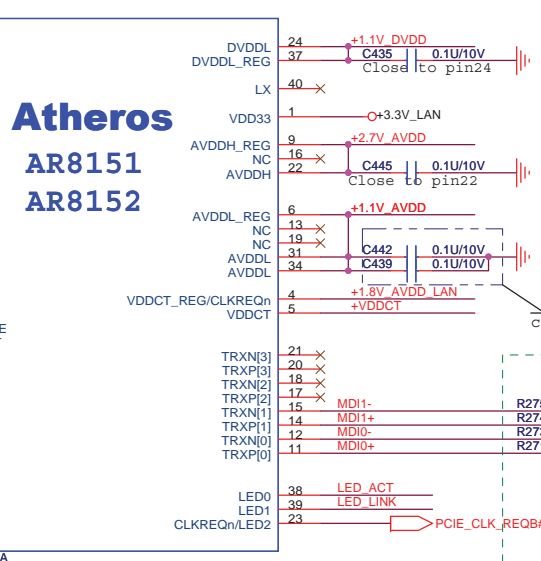
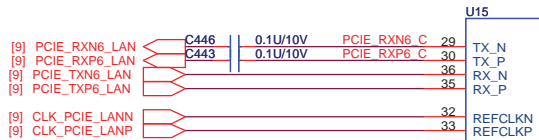
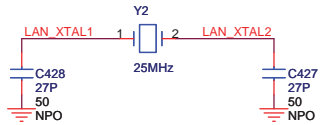


3VALW ON POWER LOGIC




FAN CONTROL

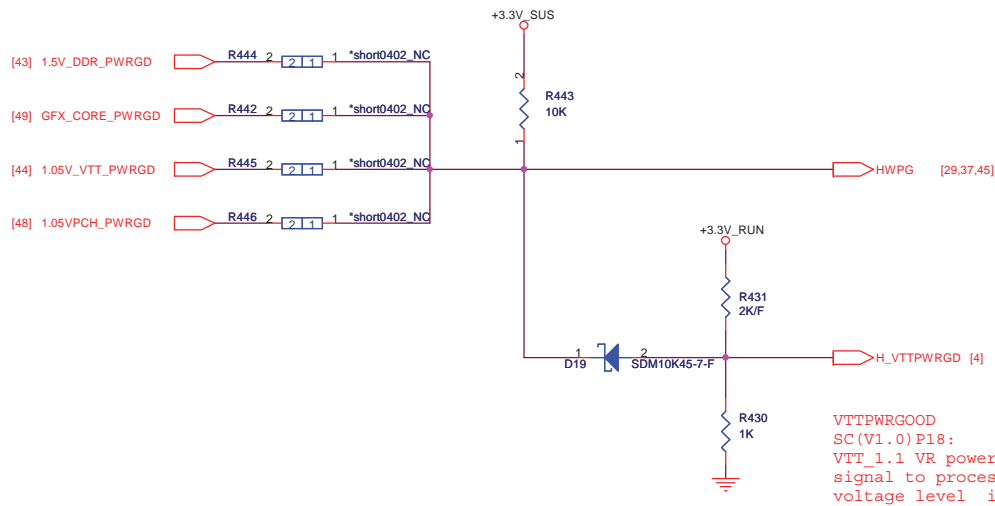






		Quanta Computer Inc.
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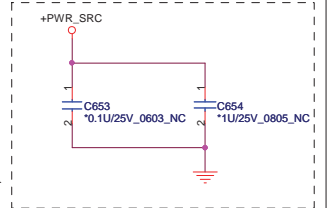
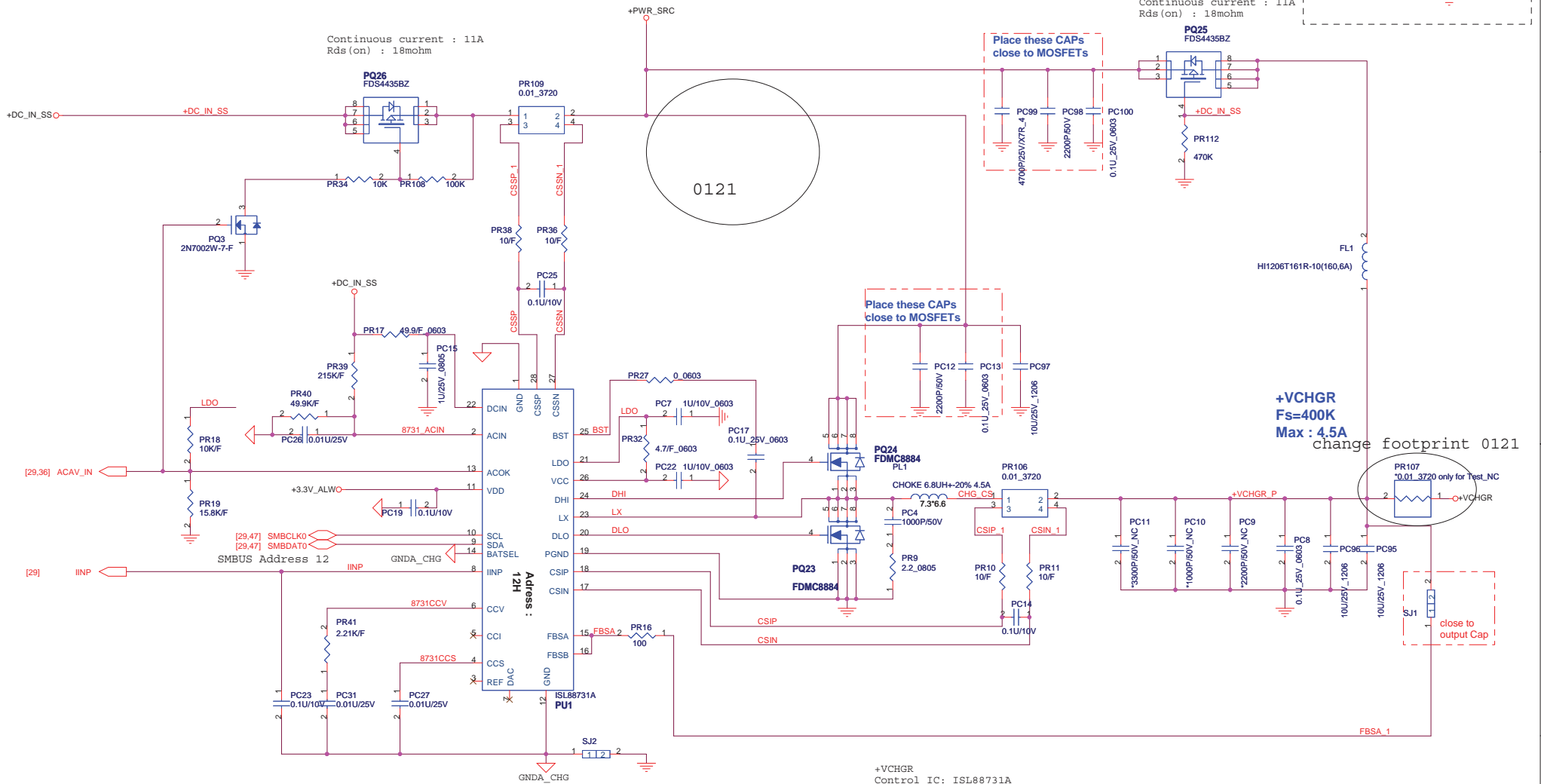
VTT_PWRGOOD
 SC (V1.0) P18:
 VTT_1.1 VR power good
 signal to processor. Signal
 voltage level is 1.1 V.



Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	System Reset Circuit	3A
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+VCHGR
 Control IC: ISL88731A
 H/S MOSFET: FDMC8884 (FAC), Qg=7nC, Rds(on)=30mohm, PD:2.3W
 L/S MOSFET: FDMC8884 (FAC), Qg=7nC, Rds(on)=30mohm, PD:2.3W
 Inductor: CHOKE 6.8UH+-20% 4.5A DCR=44mohm
 Output Cap: 2*10U 25V(+/-10%, X6S, 1206)

QUANTA COMPUTER

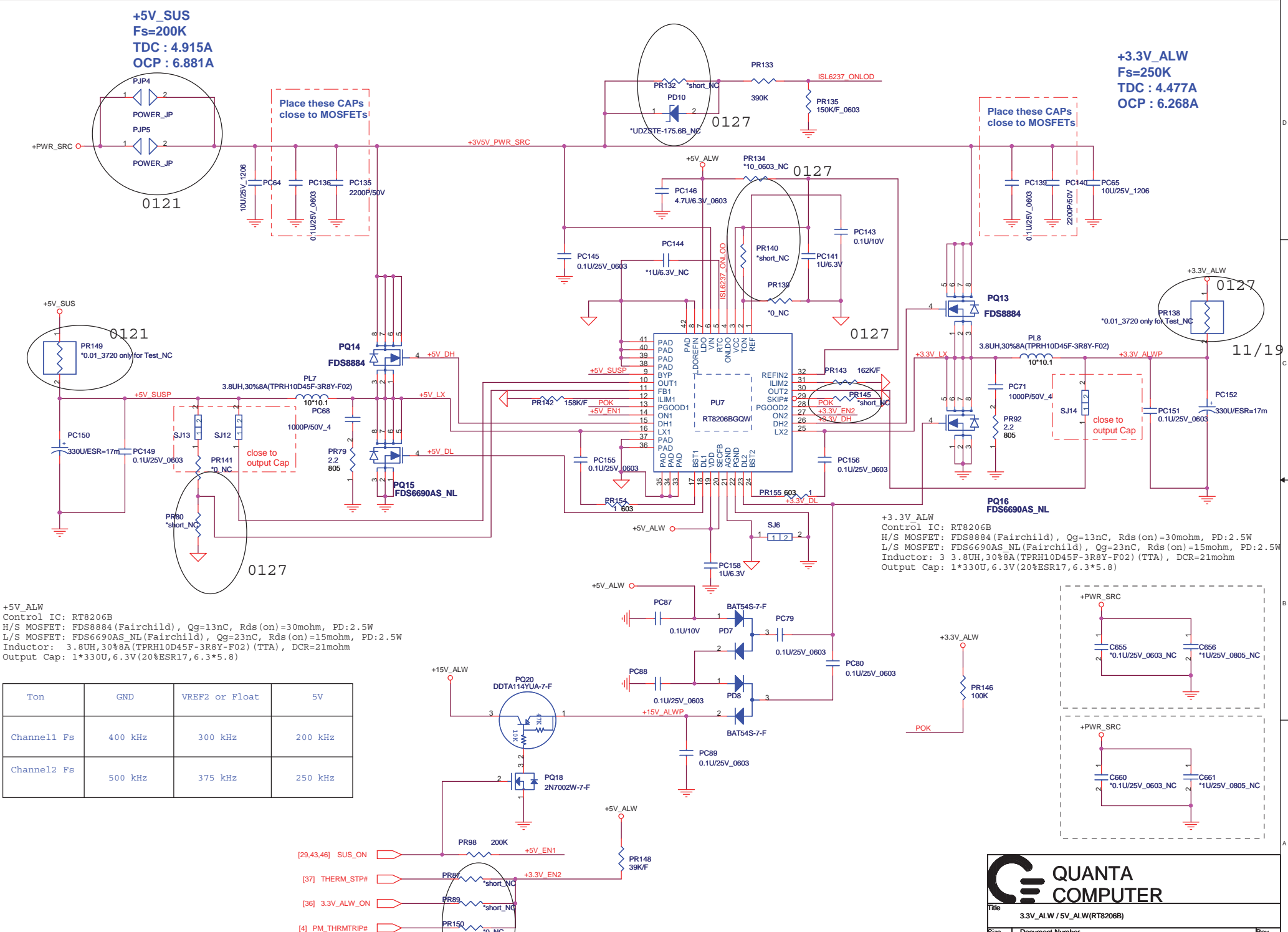
Title: Charger (ISL88731)

Size: UM7 Dis	Document Number: UM7 Dis	Rev: 3A
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+5V_SUS
Fs=200K
TDC : 4.915A
OCP : 6.881A

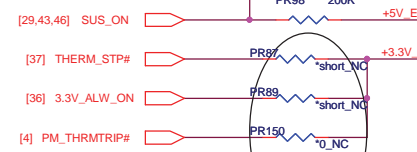
+3.3V_ALW
Fs=250K
TDC : 4.477A
OCP : 6.268A



+5V_ALW
 Control IC: RT8206B
 H/S MOSFET: FDS8884 (Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
 L/S MOSFET: FDS6690AS_NL (Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
 Inductor: 3.8UH, 30%8A (TPRH10D45F-3R8Y-F02) (TTA), DCR=21mohm
 Output Cap: 1*330U, 6.3V (20%ESR17, 6.3*5.8)

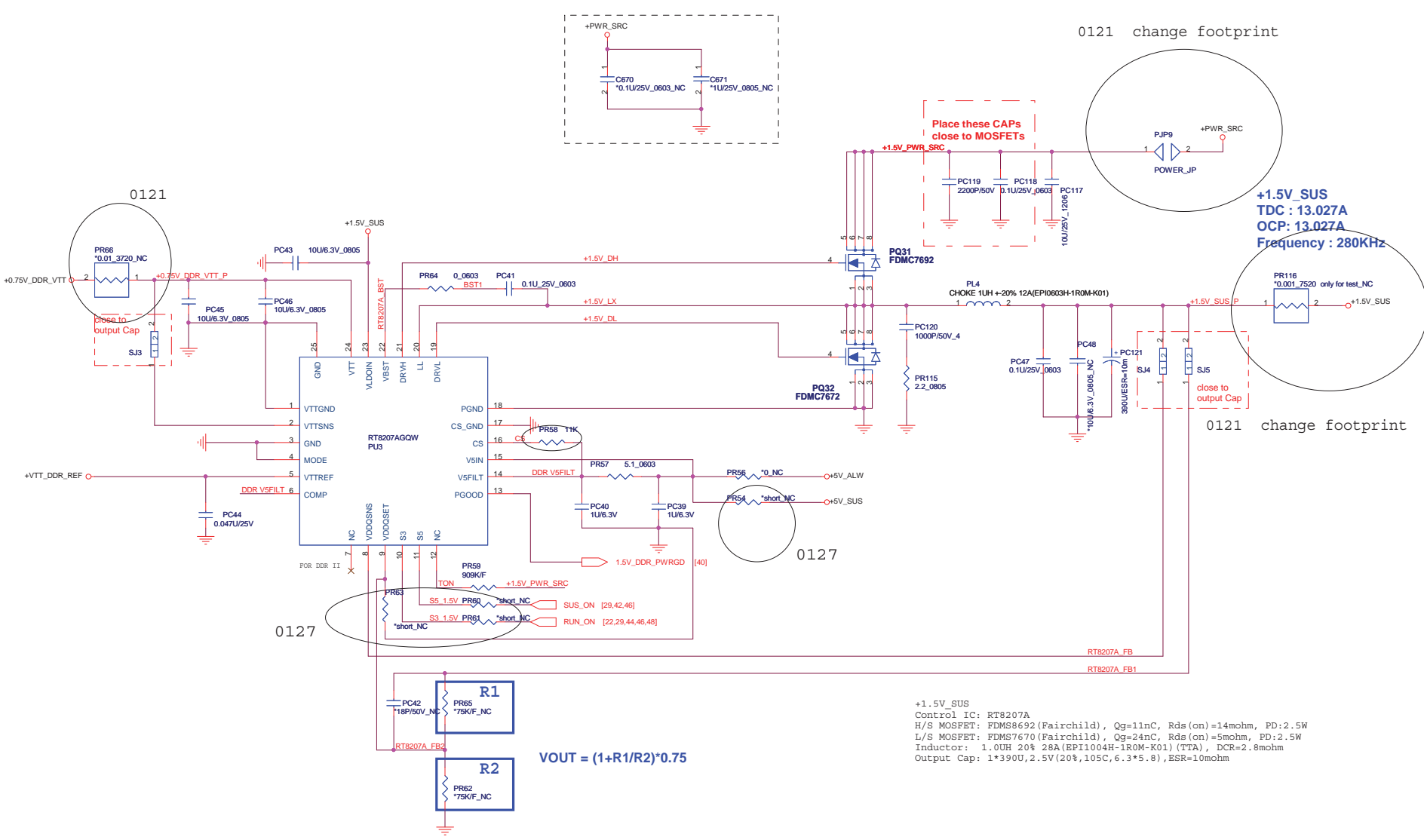
+3.3V_ALW
 Control IC: RT8206B
 H/S MOSFET: FDS8884 (Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
 L/S MOSFET: FDS6690AS_NL (Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
 Inductor: 3.8UH, 30%8A (TPRH10D45F-3R8Y-F02) (TTA), DCR=21mohm
 Output Cap: 1*330U, 6.3V (20%ESR17, 6.3*5.8)

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz



Title 3.3V_ALW / 5V_ALW(RT8206B)		
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+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDM8692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDM87670 (Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 1.0UH 20% 28A (EPI1004H-1ROM-K01) (TTA), DCR=2.8mohm
Output Cap: 1*390U, 2.5V (20%, 105C, 6.3*5.8), ESR=10mohm

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

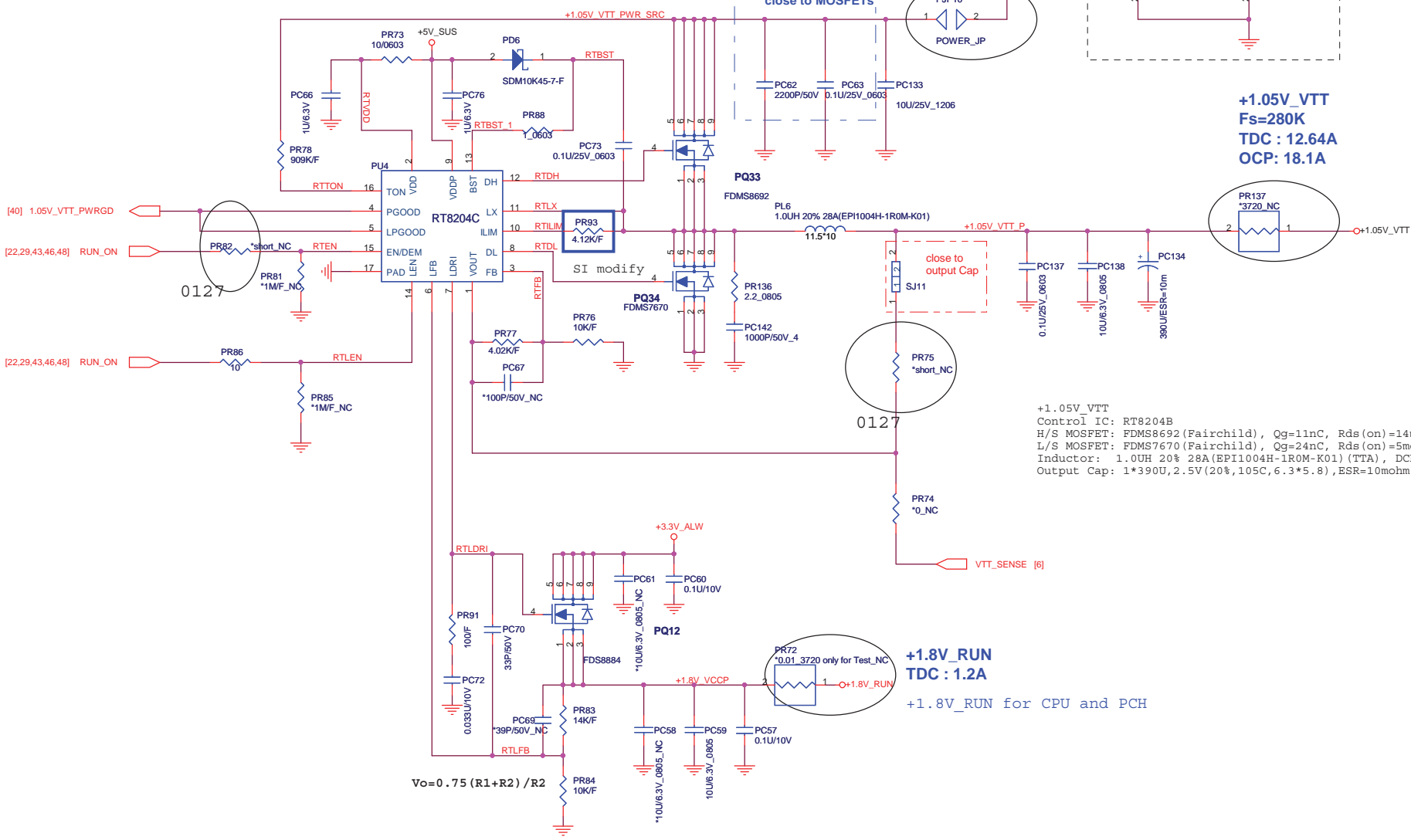
VDDQ output voltage selection

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQNS/2	DDR3
V5IN	1.8V	VDDQNS/2	DDR2
FB Resistors	Adjusting	VDDQNS/2	1.5V < VVDDQ < 3V

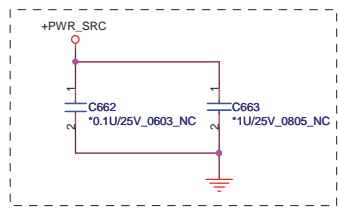
Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

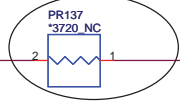
[40] 1.05V_VTT_PWRGD
 [22,29,43,46,48] RUN_ON
 [22,29,43,46,48] RUN_ON



Place these CAPs close to MOSFETS



+1.05V_VTT
Fs=280K
TDC : 12.64A
OCP: 18.1A

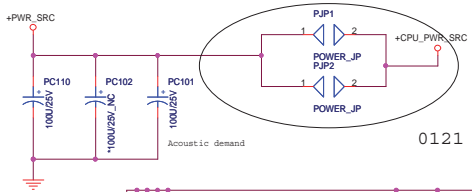
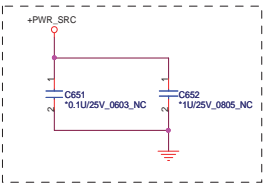
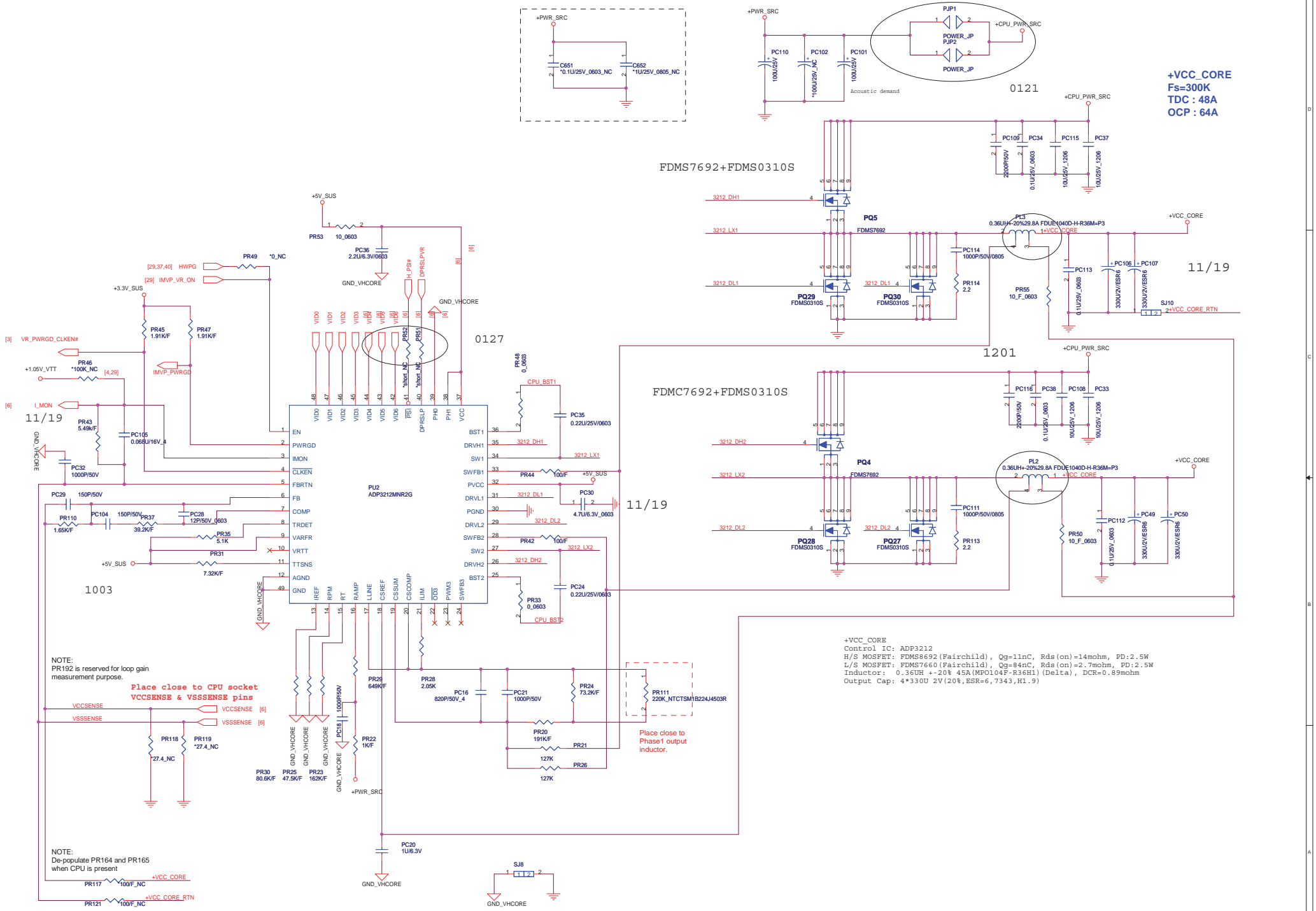


+1.05V_VTT
 Control IC: RT8204B
 H/S MOSFET: FDS8692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
 L/S MOSFET: FDS7670 (Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
 Inductor: 1.0UH 20% 28A(EPI1004H-1R0M-K01) (TTA), DCR=2.8mohm
 Output Cap: 1*390U, 2.5V (20%, 105C, 6.3*5.8), ESR=10mohm

+1.8V_RUN
TDC : 1.2A
+1.8V_RUN for CPU and PCH

$V_o = 0.75 (R1 + R2) / R2$

Title		
+1.05V_VTT(RT8204B)		
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+VCC_CORE
Fs=300K
TDC : 48A
OCP : 64A

FDMS7692+FDMS0310S

FDMS7692+FDMS0310S

1003

0127

1201

NOTE:
PR192 is reserved for loop gain measurement purpose.

Place close to CPU socket
VCCSENSE & VSSSENSE pins

NOTE:
De-populate PR164 and PR165 when CPU is present

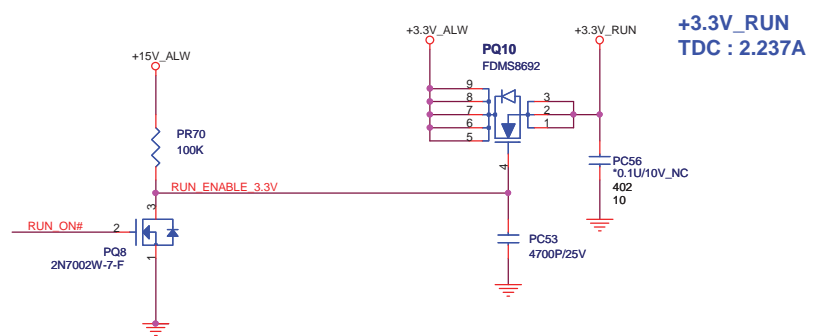
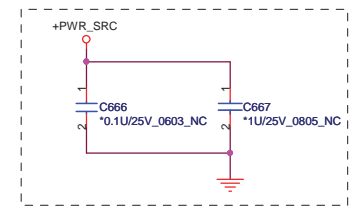
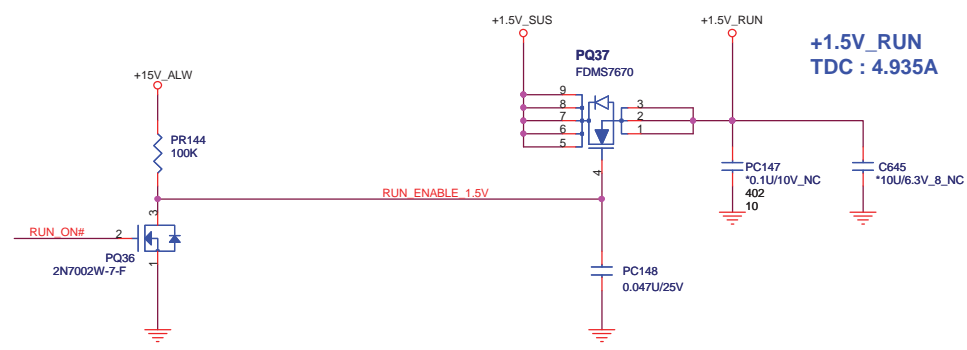
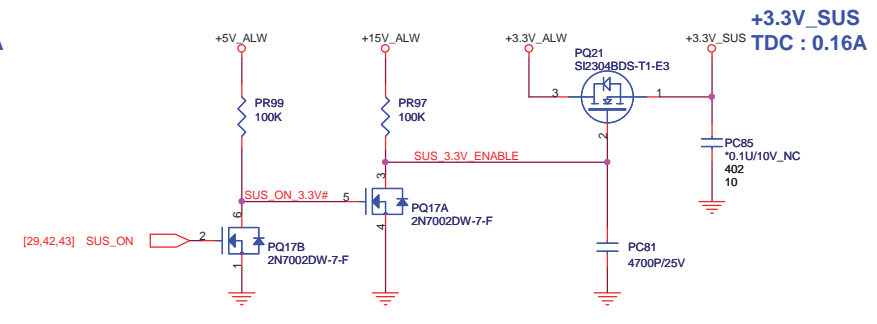
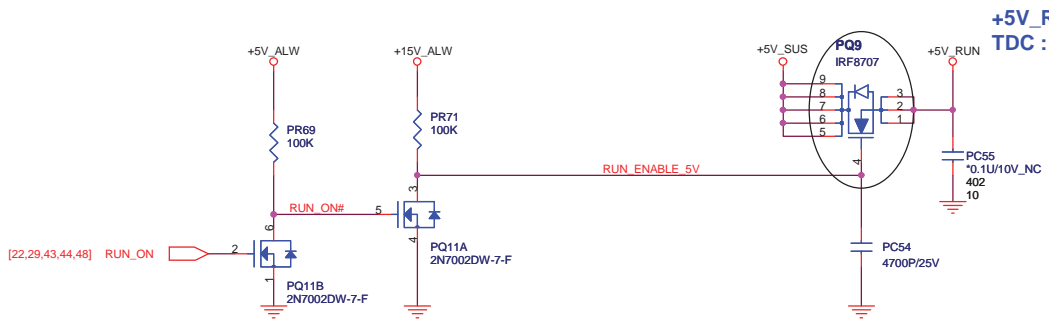
Place close to PC98
+VCC_CORE & +VCC_CORE_RTIN pins

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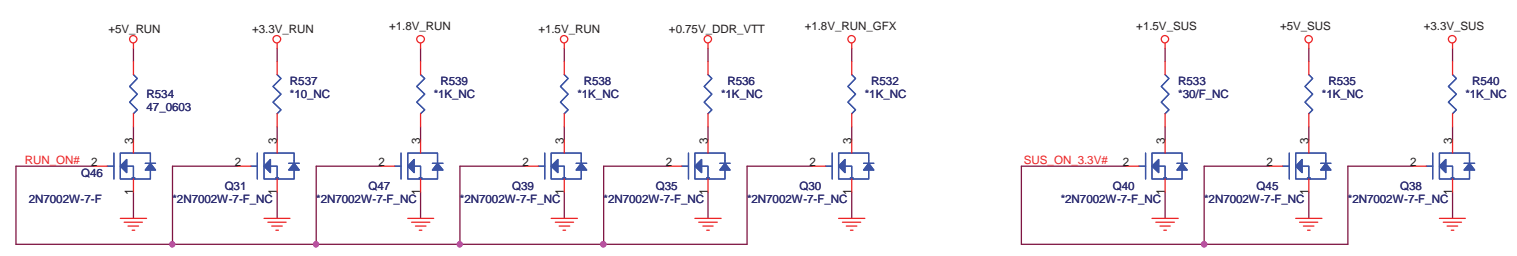
11/19

+VCC_CORE
Control IC: ADP3212
H/S MOSFET: FDMS8692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7660 (Fairchild), Qg=84nC, Rds(on)=2.7mohm, PD:2.5W
Inductor: 0.35uH +/-20% 45A (MPO104F-R36H) (Delta), DCR=0.89mohm
Output Cap: 4*330U 2V(20%, ESR=6, 7343, H1.9)

Title			CPU core (ADP3212MNR2G)		
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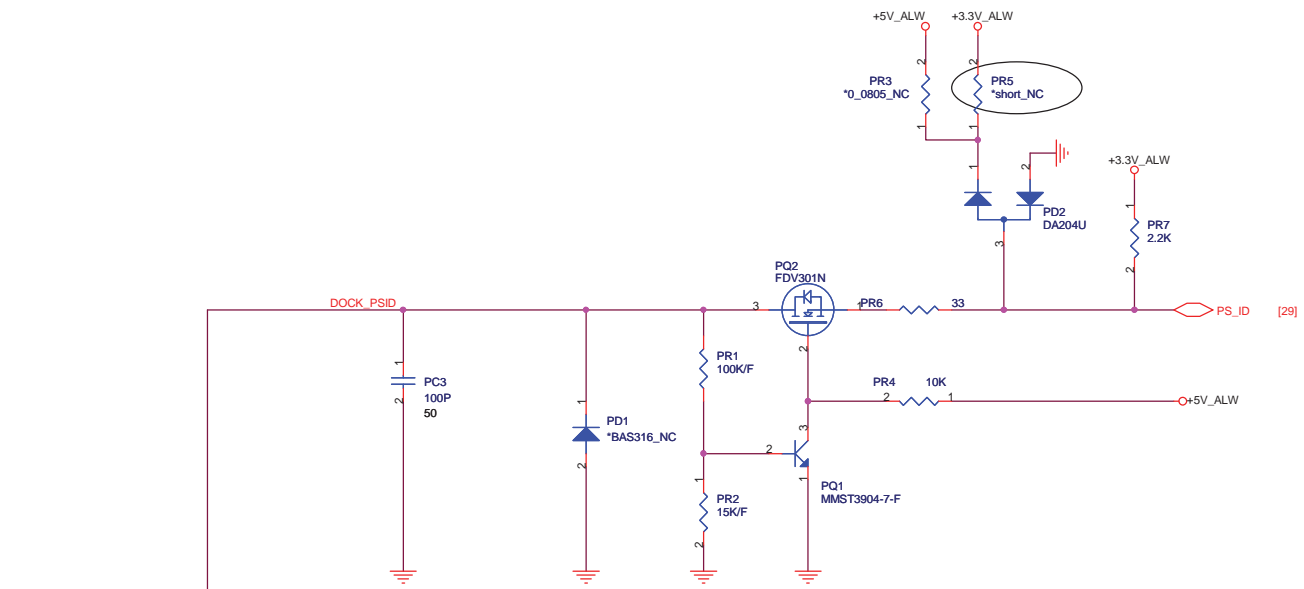
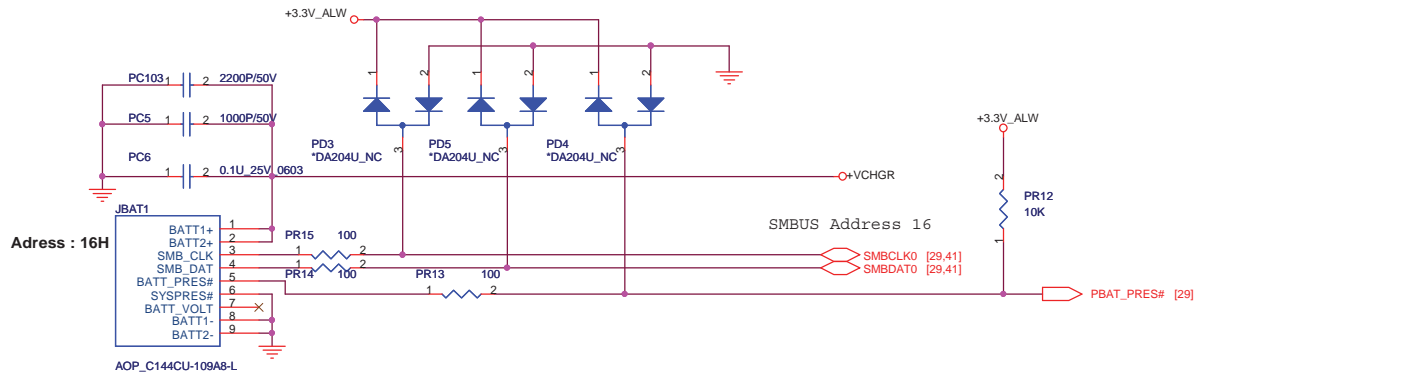
Reserve discharge path



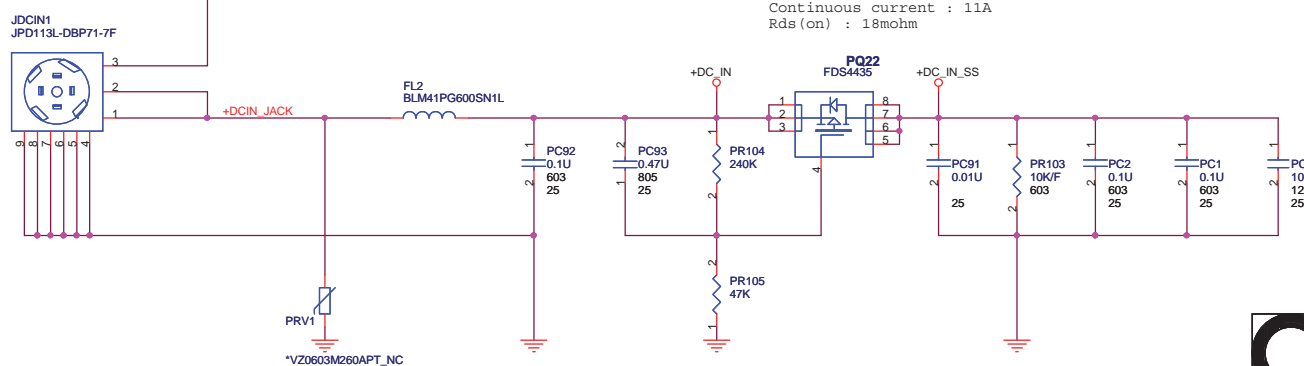
QUANTA COMPUTER

Title: RUN / SUS POWER SW

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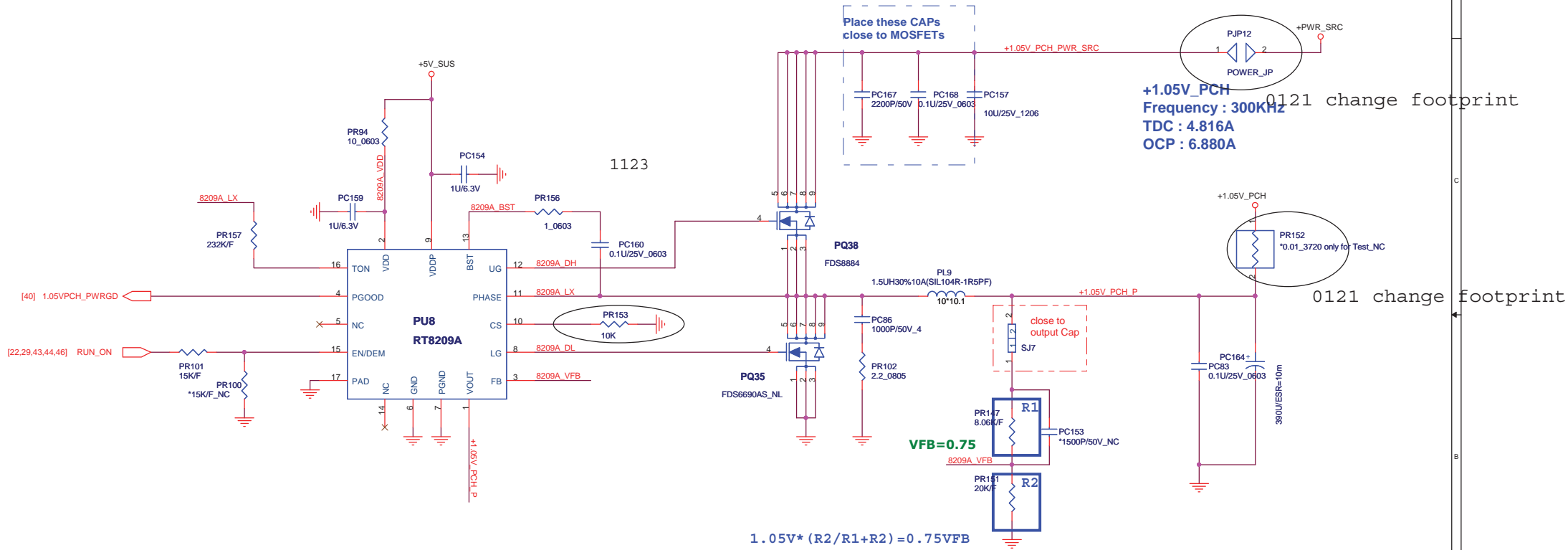
Continuous current : 11A
Rds (on) : 18mohm



QUANTA COMPUTER

Title: DCIN,BATT CONNECTOR

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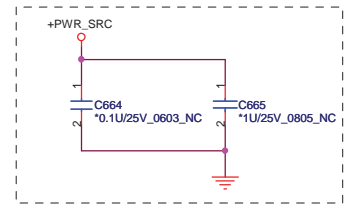


0121 change footprint
+1.05V_PCH
Frequency : 300KHz
TDC : 4.816A
OCP : 6.880A

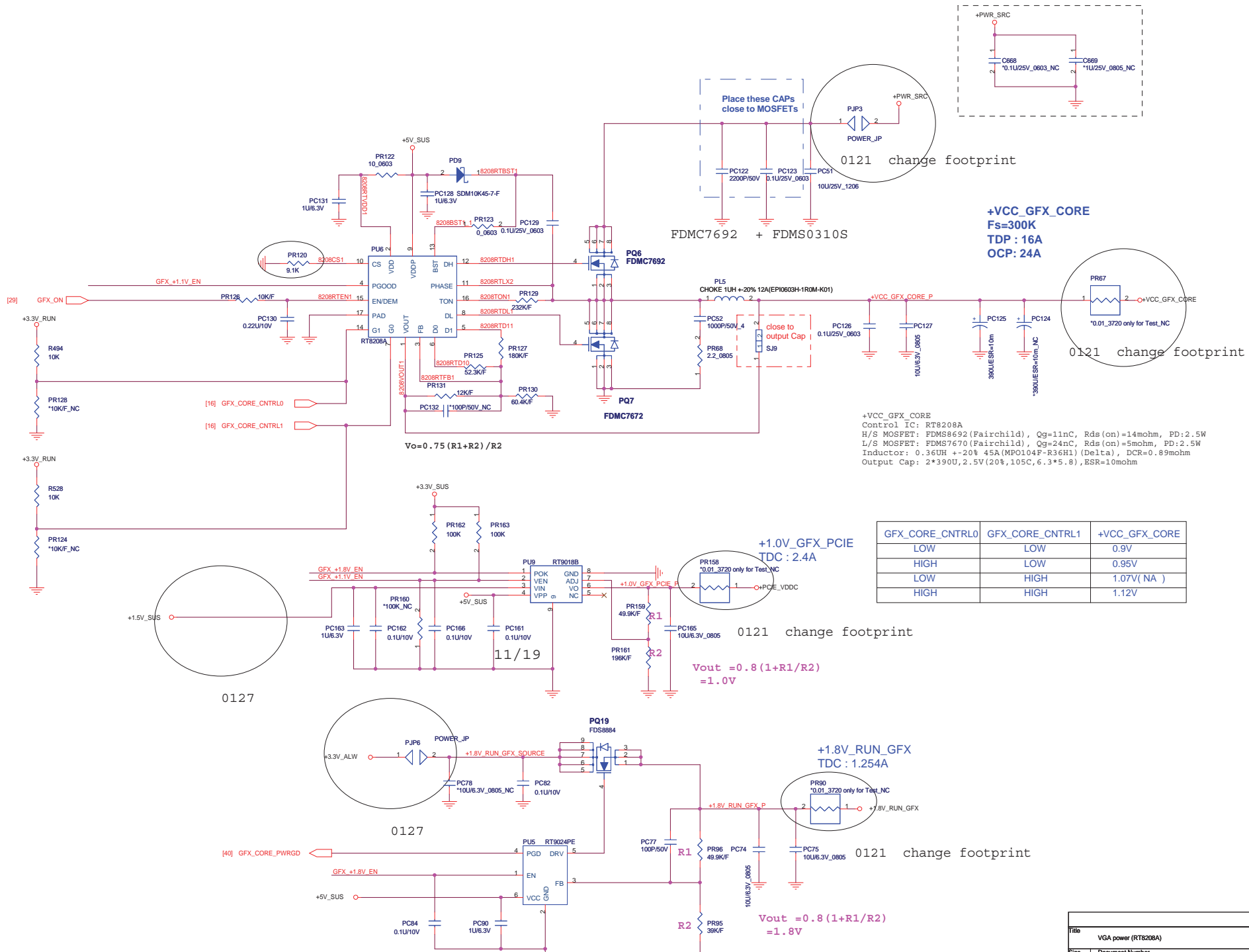
0121 change footprint

$$1.05V * (R2 / (R1 + R2)) = 0.75V_{FB}$$

+1.05V_PCH
 Control IC: RT8209A
 H/S MOSFET: AO4496 (AOS), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
 L/S MOSFET: AO4468 (AOS), Qg=12nC, Rds(on)=22mohm, PD:3.1W
 Inductor: 1.5UH+20% 9A (10D40F-1R5M) (TTA), DCR=10.5mohm
 Output Cap: 1*390U, 2.5V (20%, 105C, 6.3*5.8), ESR=10mohm



Title		
+1.05V_PCH(RT8209A)		
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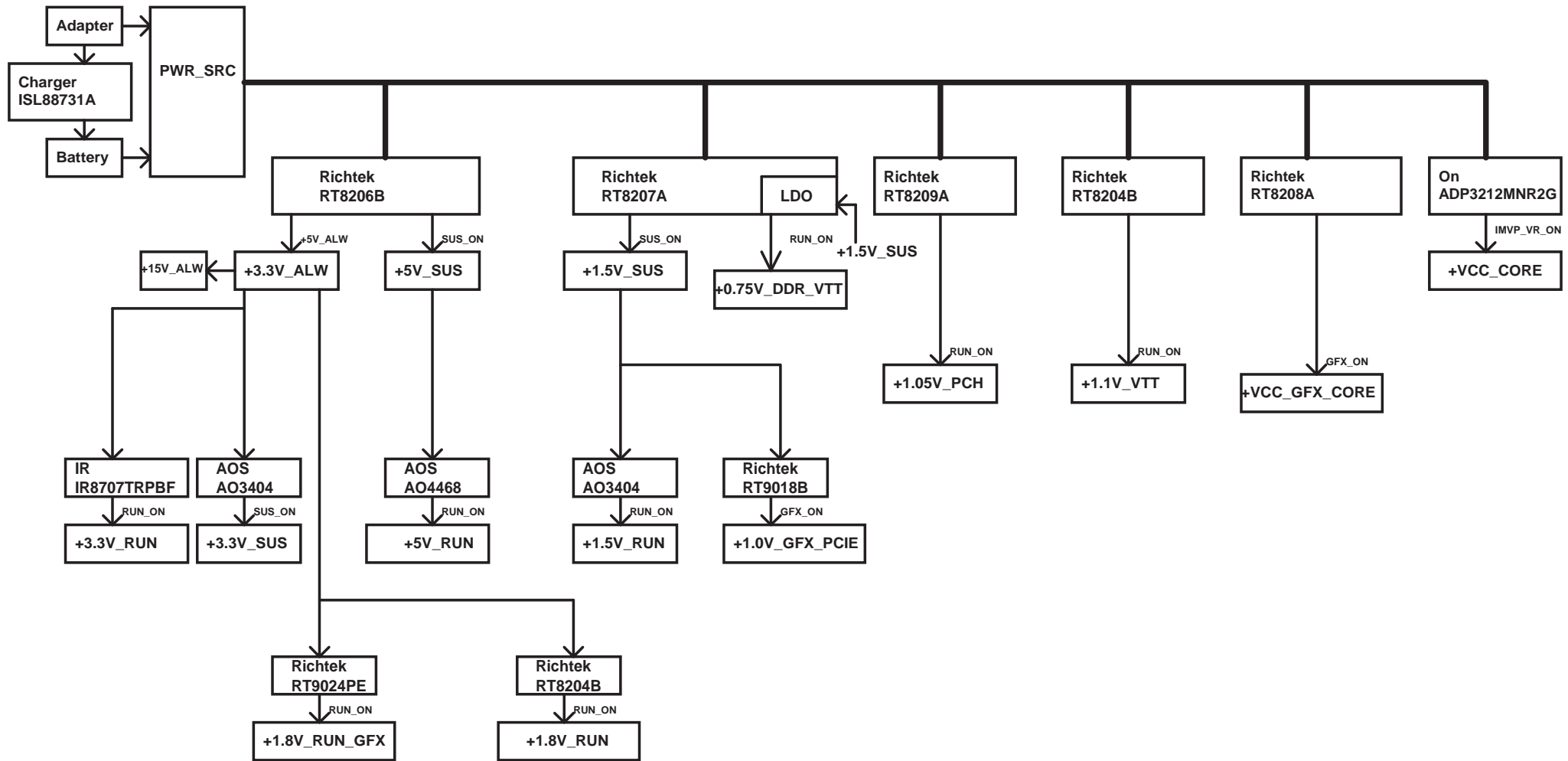



+VCC_GFX_CORE
 Control IC: RT8208A
 H/S MOSFET: FDMC7692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
 L/S MOSFET: FDMC7670 (Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
 Inductor: 0.36UH +/-20% 45A (MPO104F-R36H1) (Delta), DCR=0.89mohm
 Output Cap: 2*390U, 2.5V (20%, 105C, 6.3*5.8), ESR=10mohm

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
LOW	HIGH	1.07V(NA)
HIGH	HIGH	1.12V

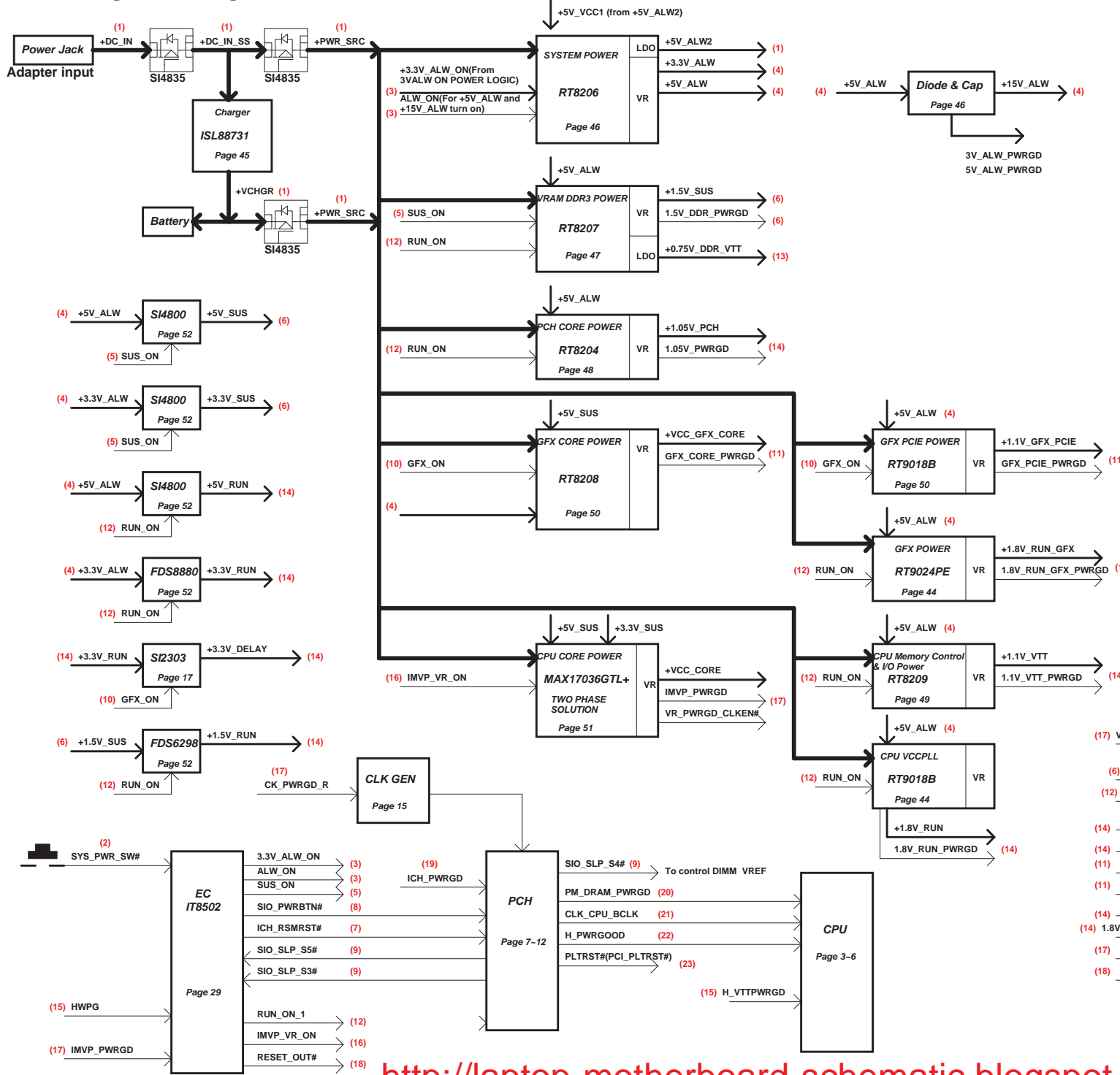
$V_{out} = 0.8 (1 + R1/R2) = 1.0V$

$V_{out} = 0.8 (1 + R1/R2) = 1.8V$



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Power Design Block Diagram 2009/08/24



- (1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC, +5V_ALW2,
- (2) SYS_PWR_SW#
- (3) 3.3V_ALW_ON, ALW_ON
- (4) +3.3V_ALW, +5V_ALW, +15V_ALW
- (5) SUS_ON
- (6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
- (7) ICH_RSMRST#
- (8) SIO_PWRBTN#
- (9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
- (10) GFX_ON
- (11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
- (12) RUN_ON_1(RUN_ON)
- (13) +0.75V_DDR_VTT
- (14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
- (16) IMVP_VR_ON
- (17) +VCC_CORE, IMVP_PWRGD
- (18) RESET_OUT#
- (19) ICH_PWRGD
- (20) PM_DRAM_PWRGD
- (21) CLK_CPU_BCLK(PCH to CPU)
- (22) H_PWRGOOD
- (23) PLTRST#(PCI_PLTRST#)

