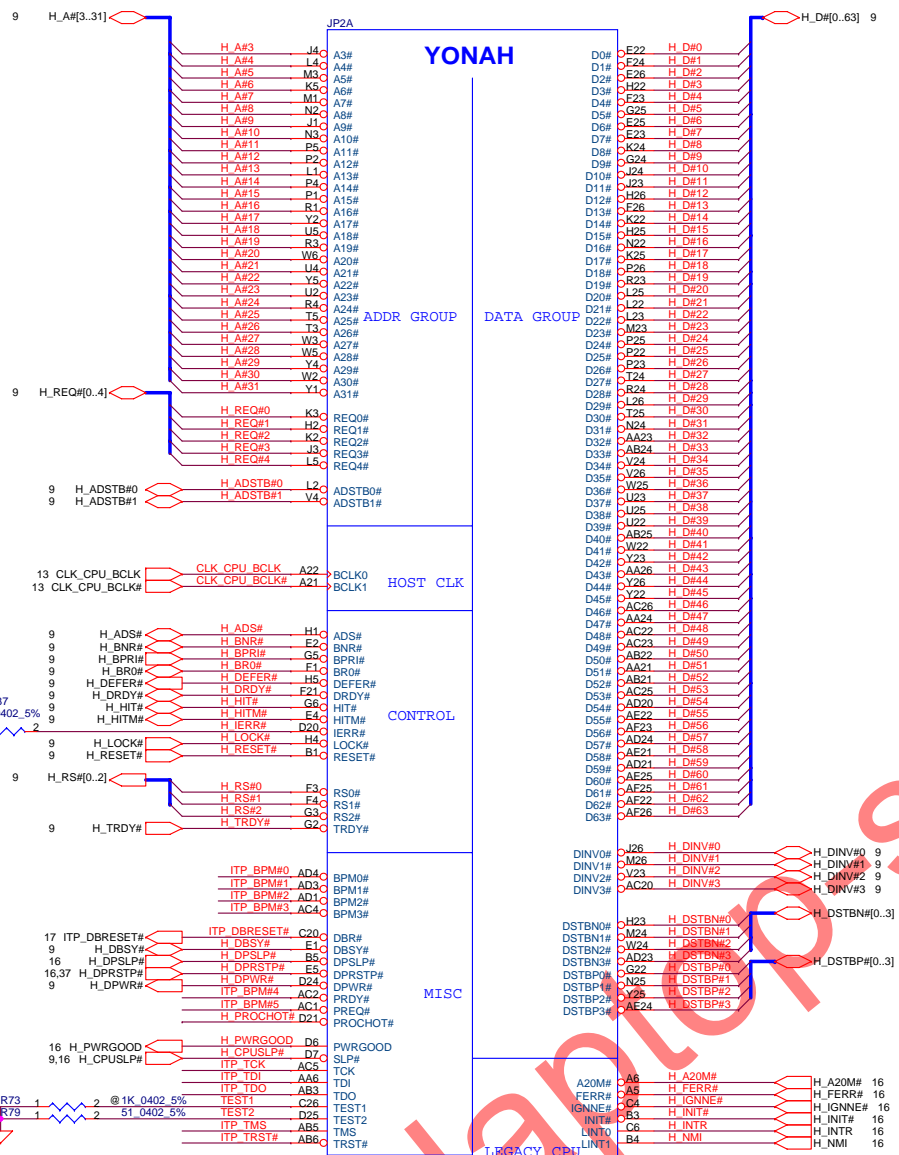
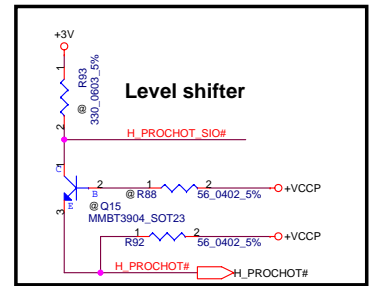
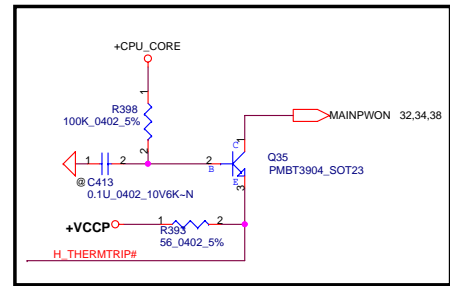
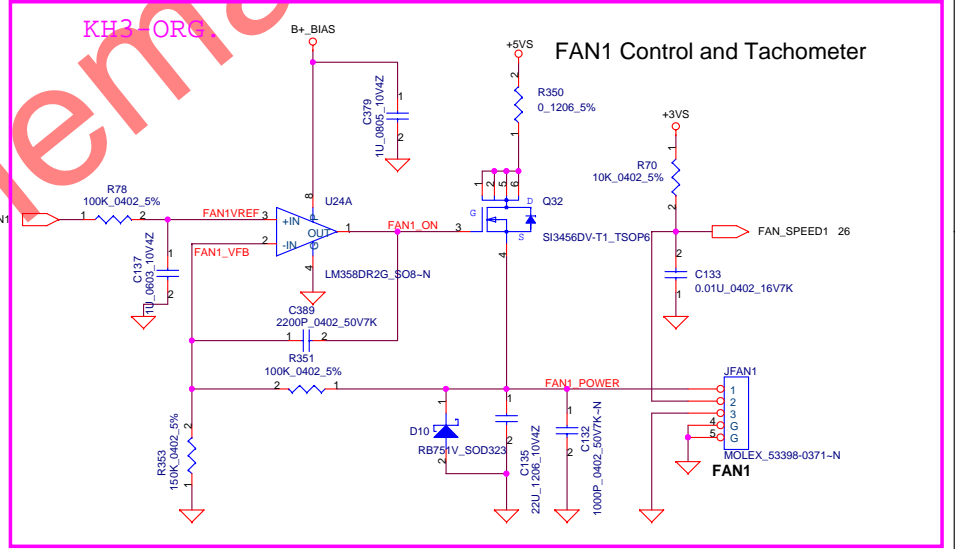
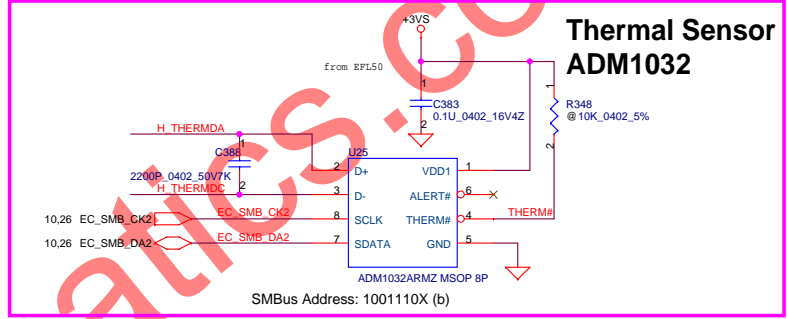
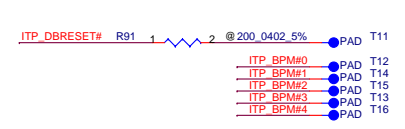
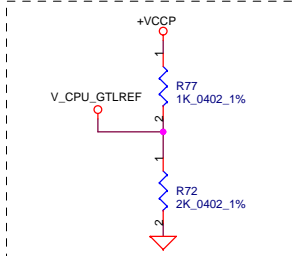


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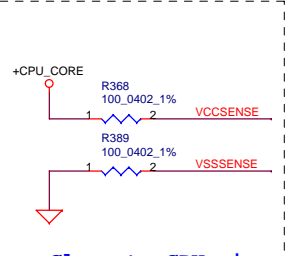


H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil





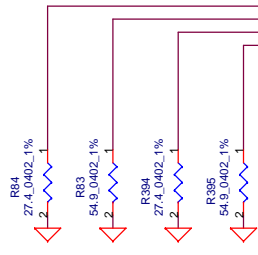
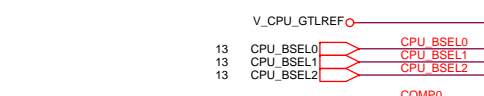
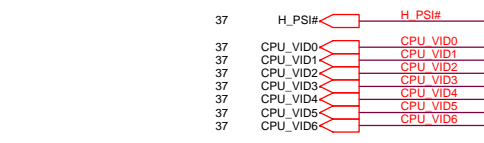
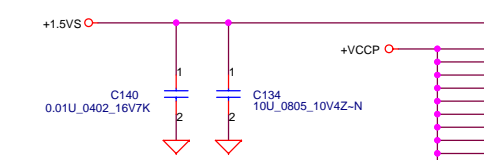
Close to CPU pin AD26 within 0.5 inch



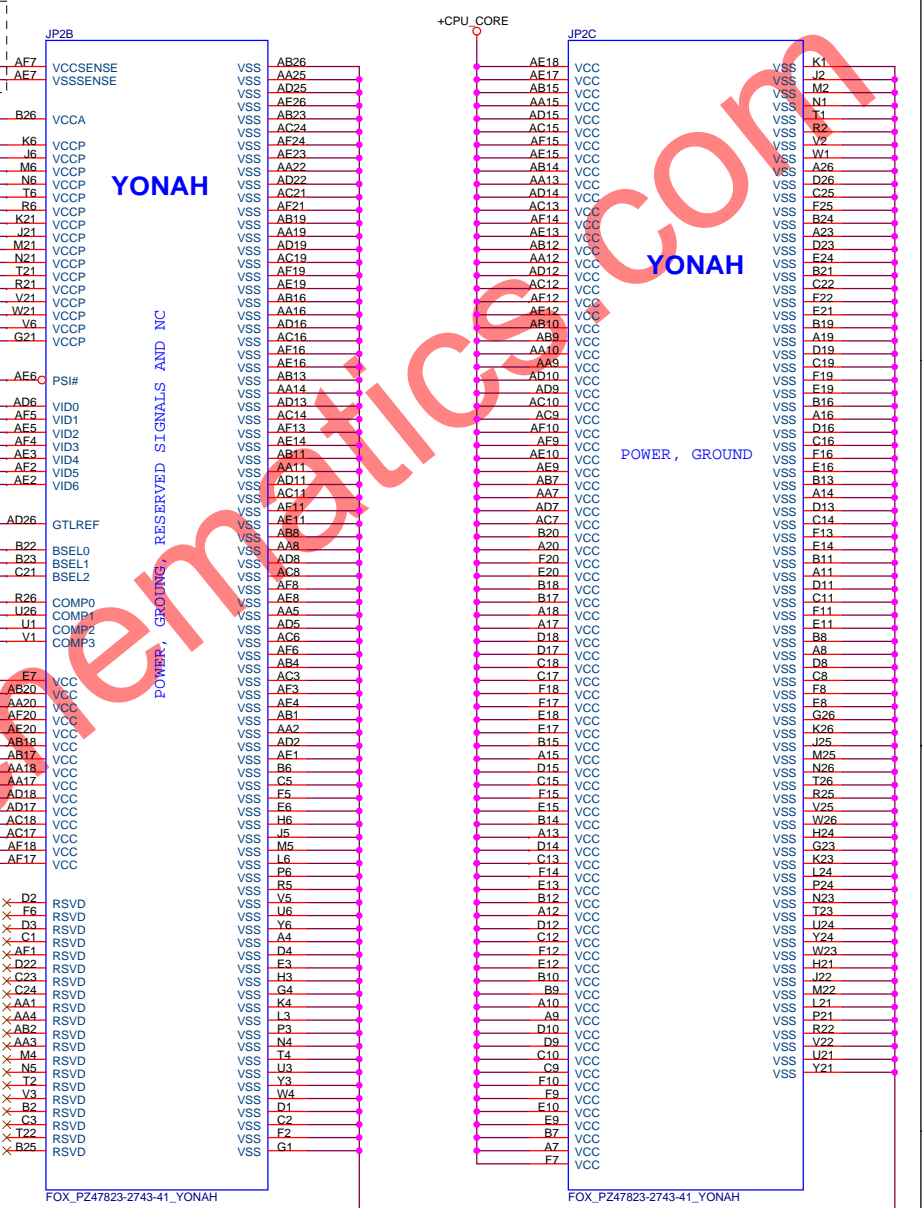
Close to CPU pin within 500mils.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

Length match within 25 mils
The trace width 18 mils space
7 mils



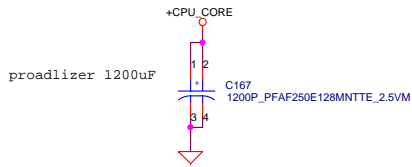
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.



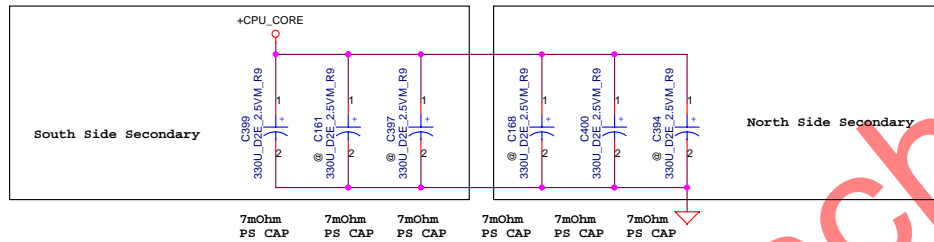
FOX_PZ47823-2743-41_YONAH

FOX_PZ47823-2743-41_YONAH

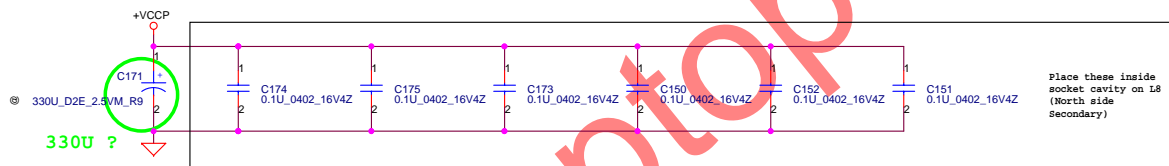
www.laptop-schematics.com



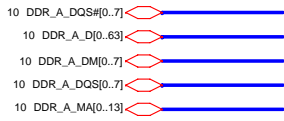
Mid Frequency Decoupling



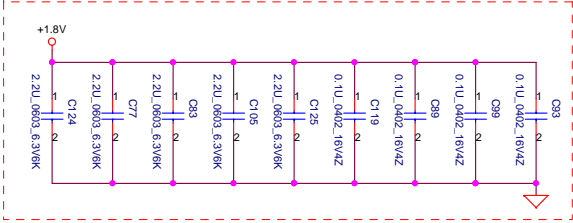
ESR <= 1.5m ohm
Capacitor > 1980uF



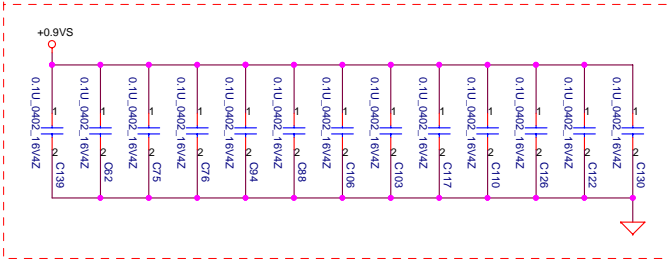
www.laptop-schematics.com



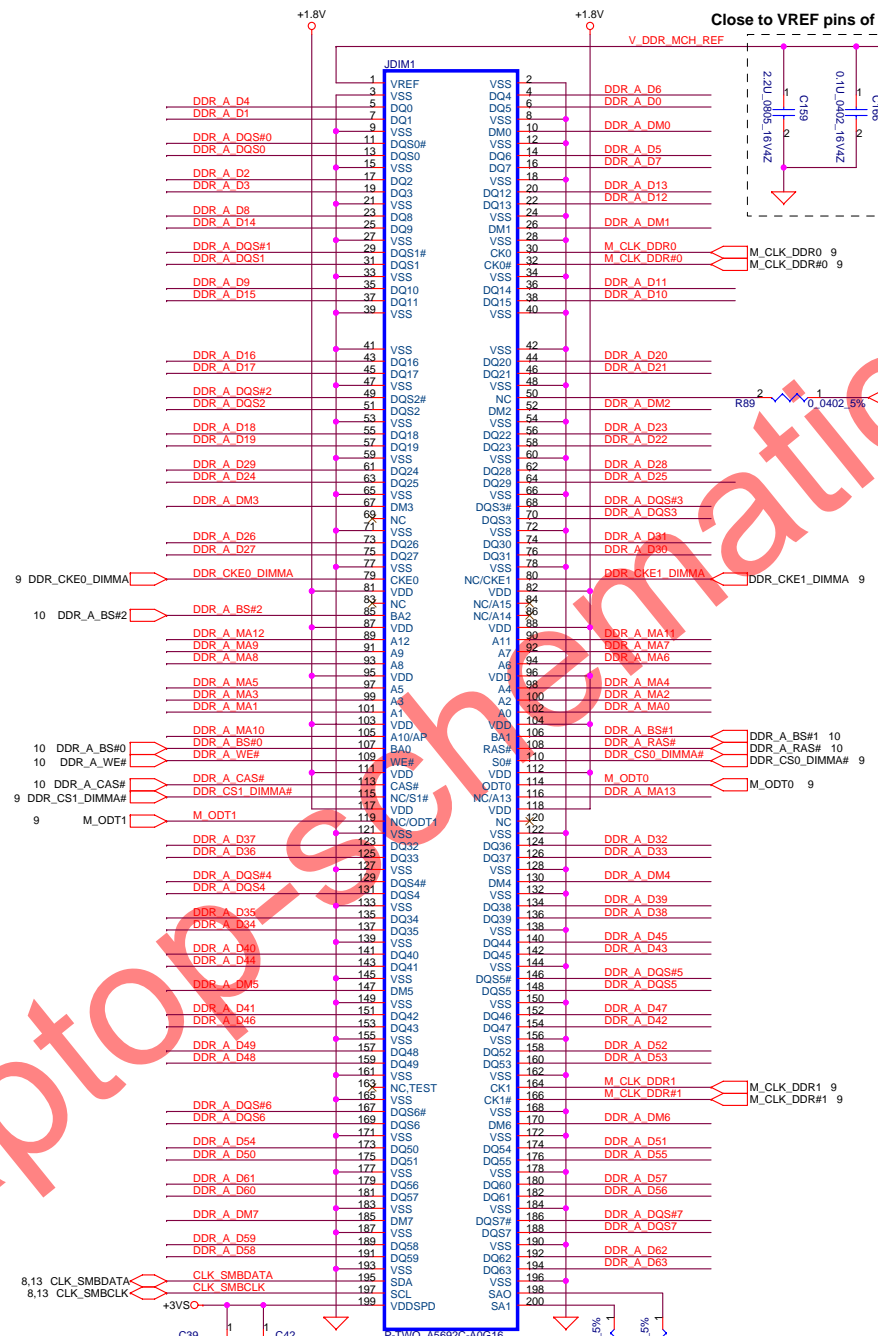
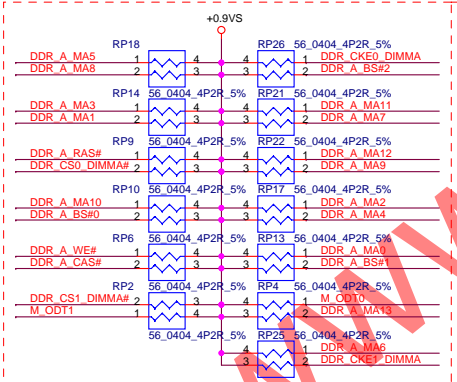
Layout Note:
Place near JP41



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

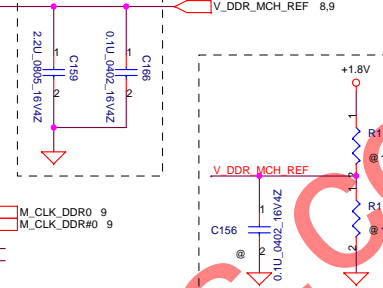


Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"

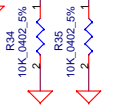
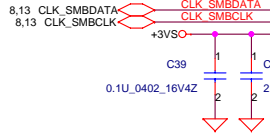


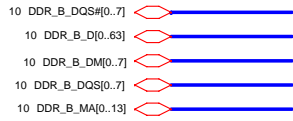
SO-DIMM A REVERSE
Top side

Close to VREF pins of SO-DIMM

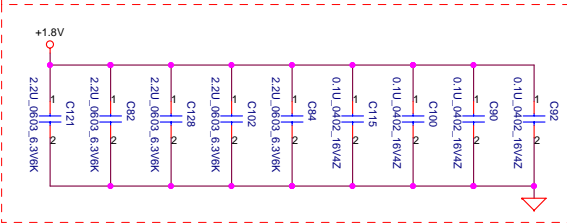


Close to connect

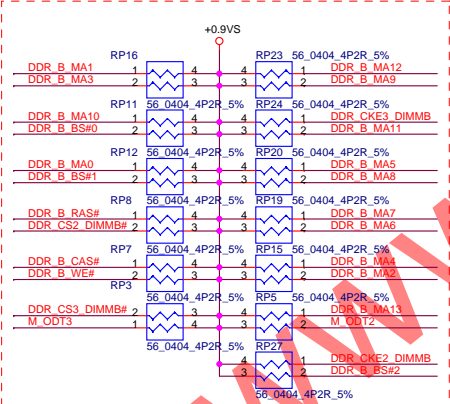
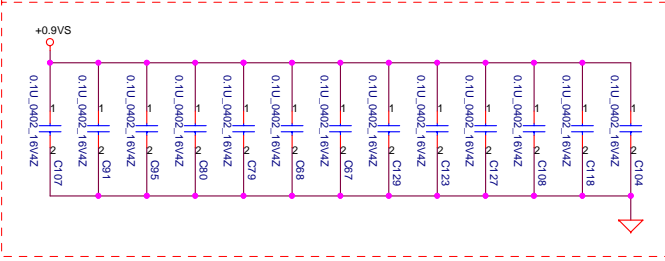




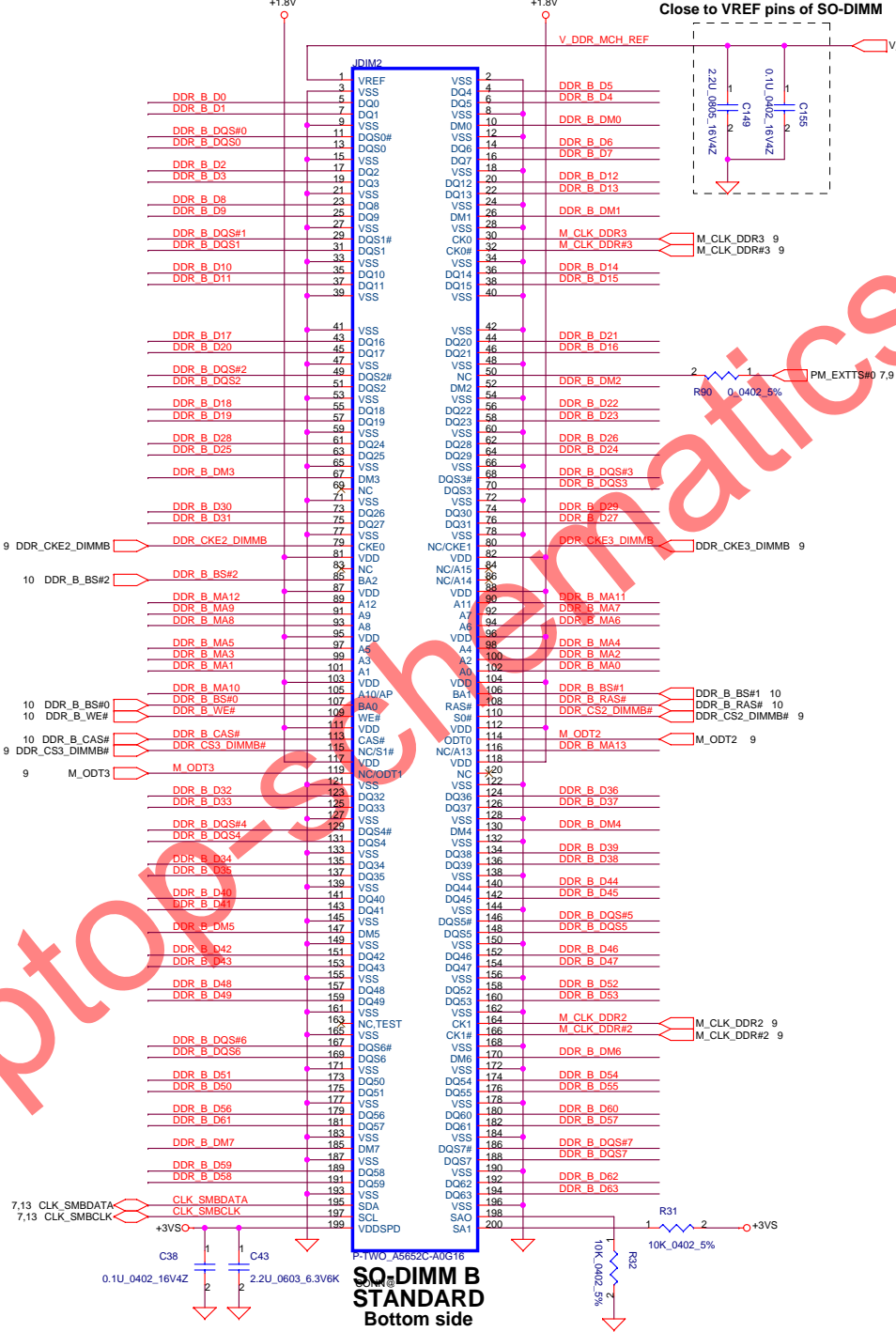
Layout Note:
Place near JP42



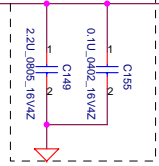
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



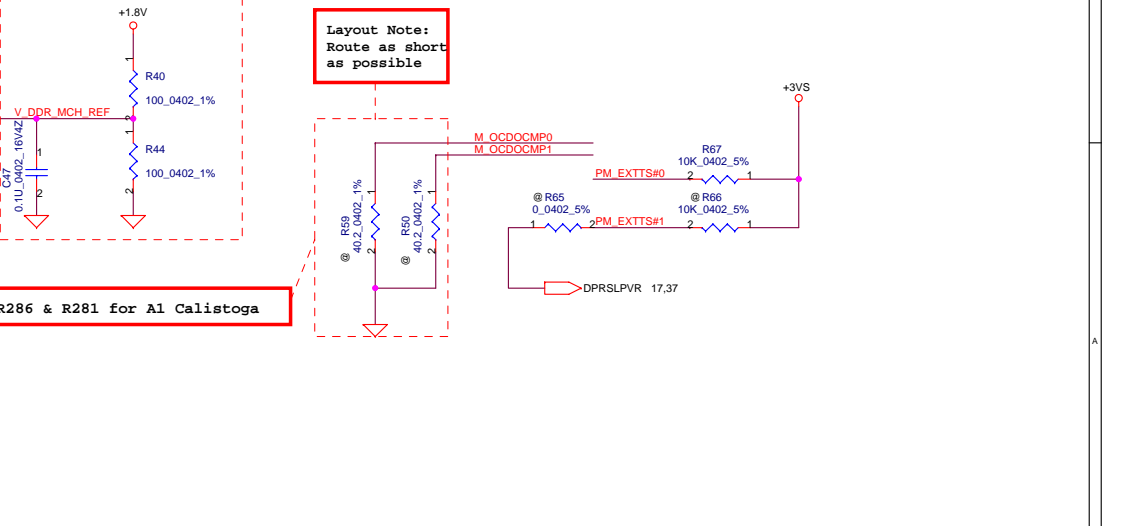
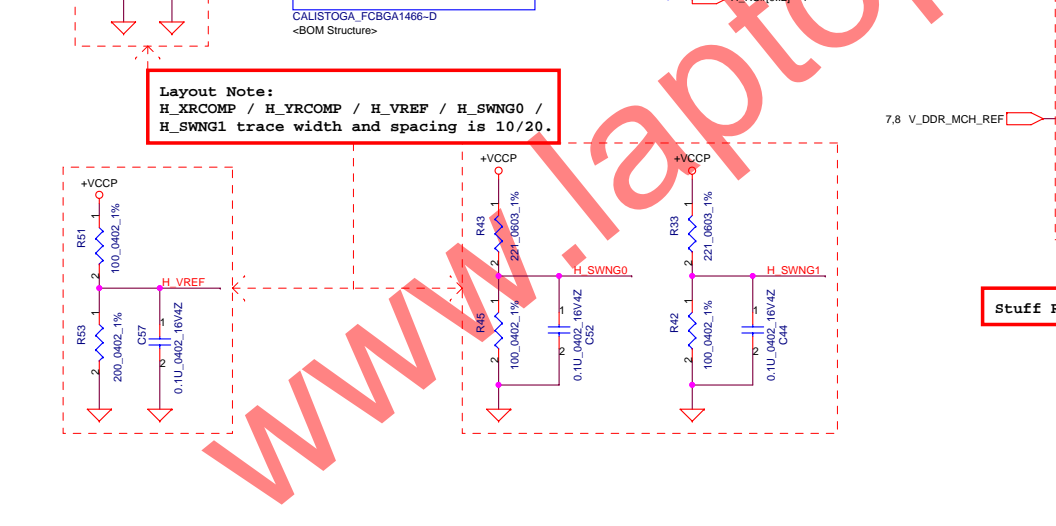
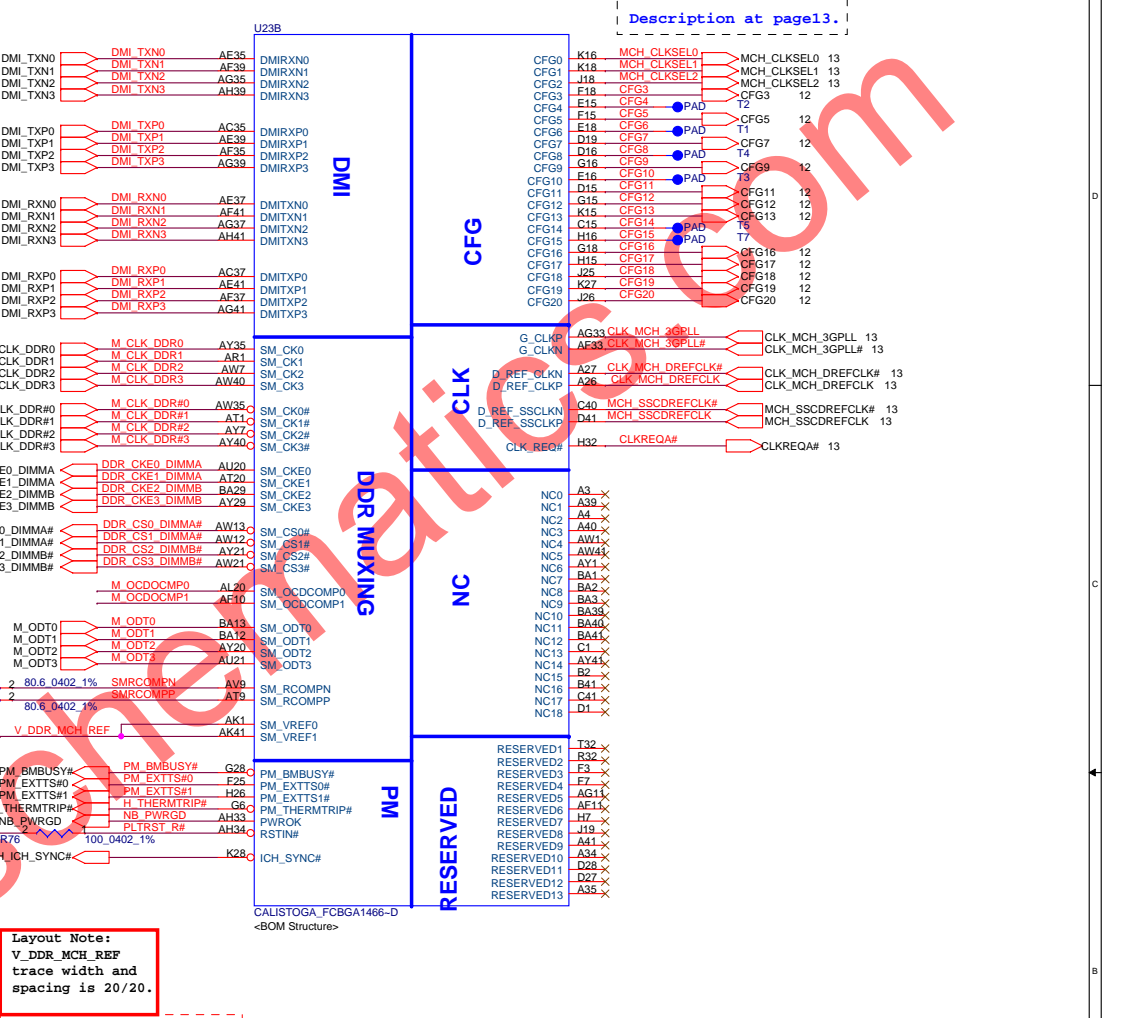
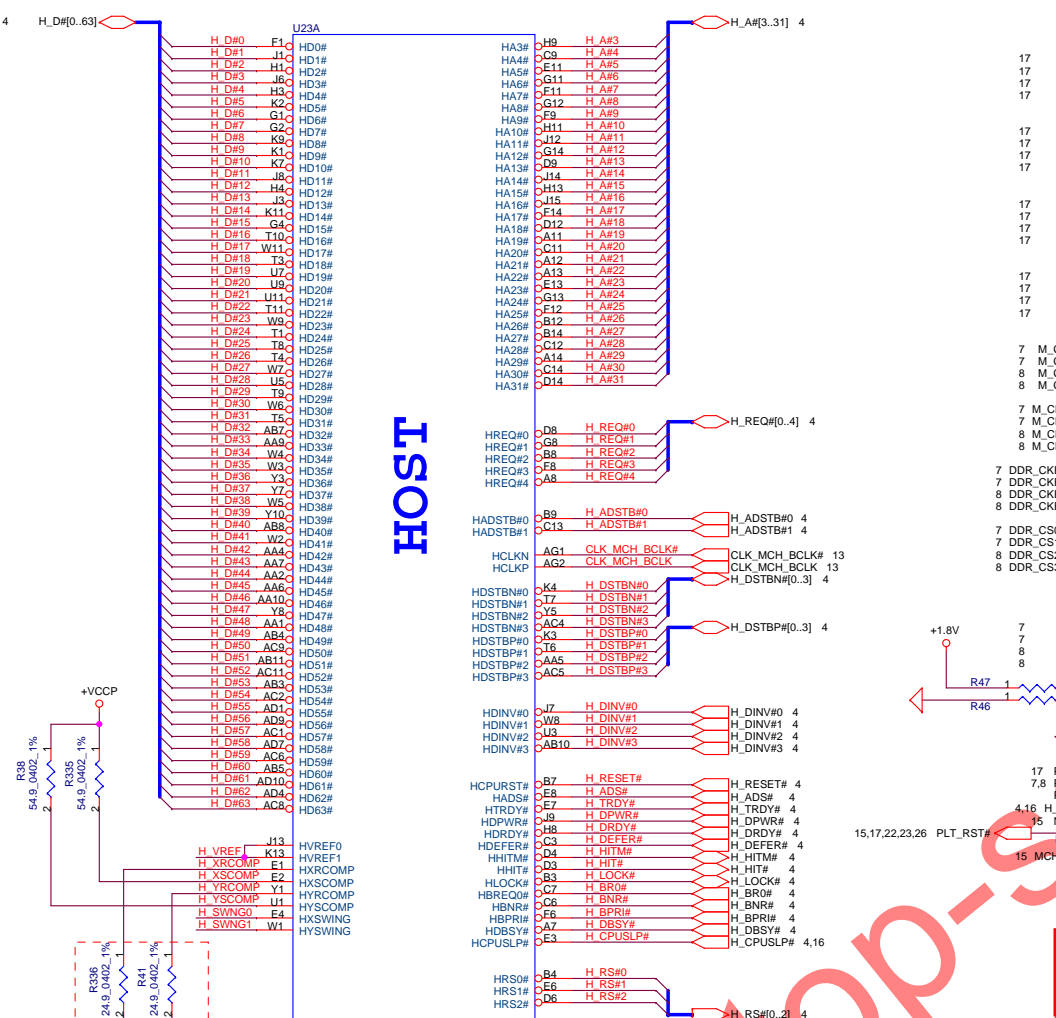
Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"



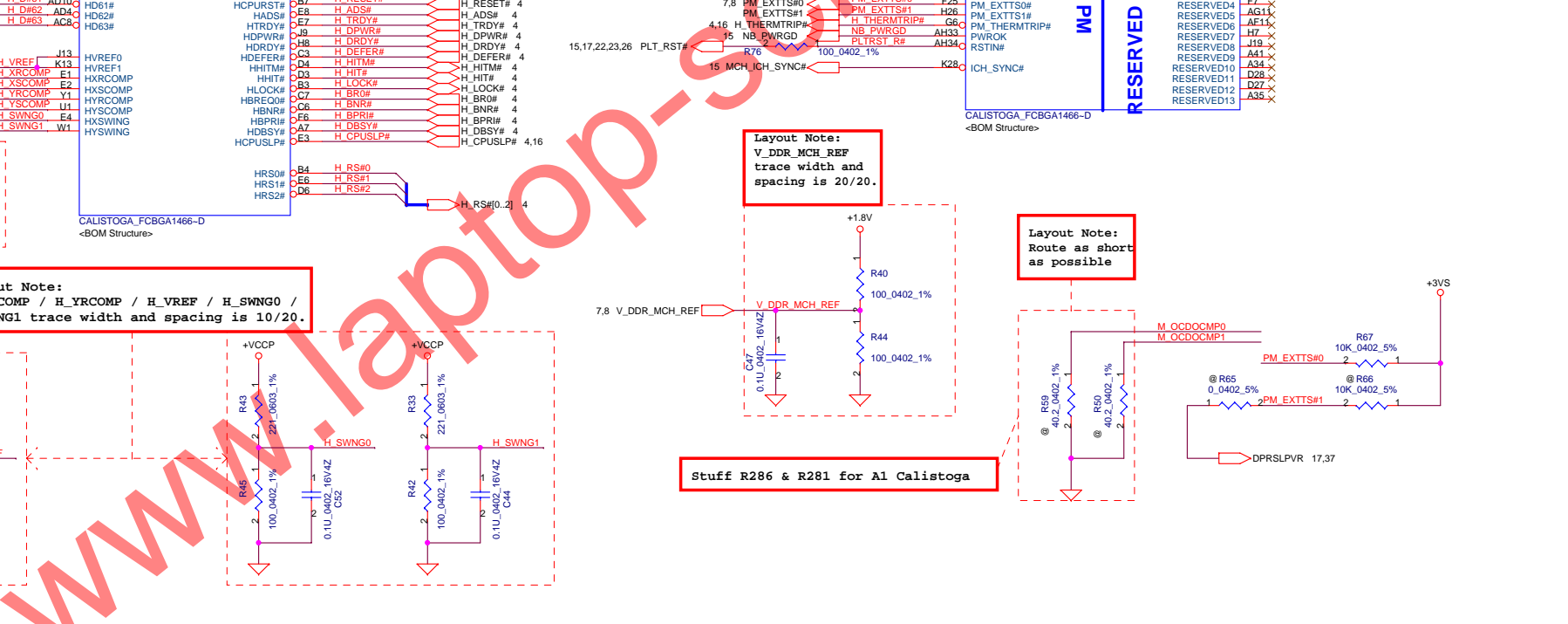
Close to VREF pins of SO-DIMM

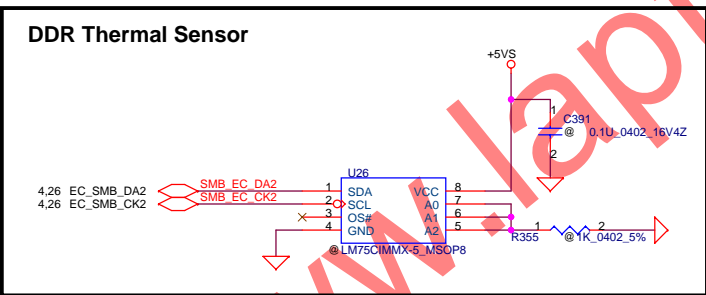


**SO-DIMM B
STANDARD
Bottom side**

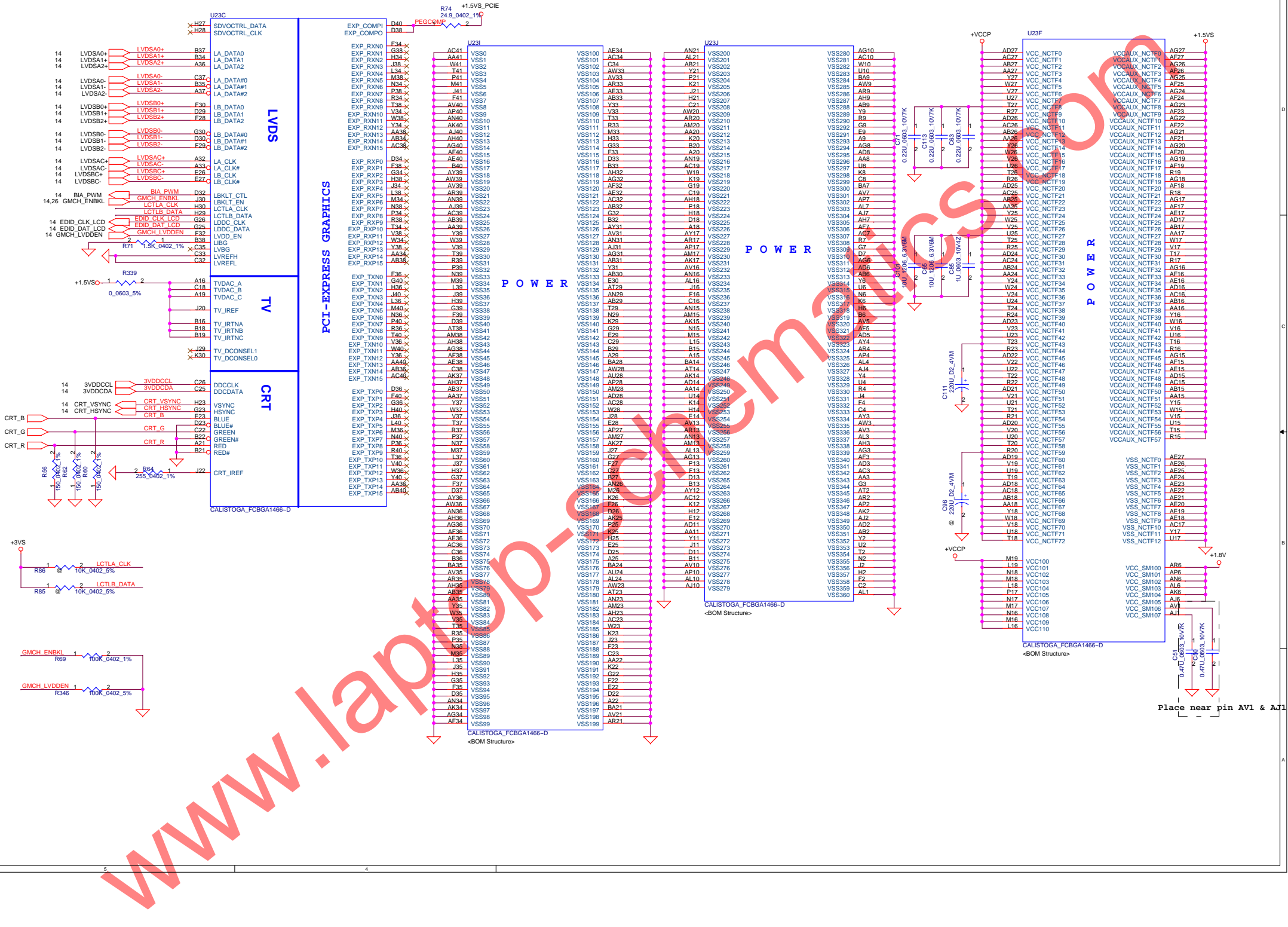


Description at pagel3.





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R74 24.9_0402_1%
+1.5VS_PCIE
PEGCQMR

U23C
SDVCTRL_DATA
SDVCTRL_CLK

EXP_COMP1
EXP_COMP0

U23I

U23J

U23F

+1.5VS

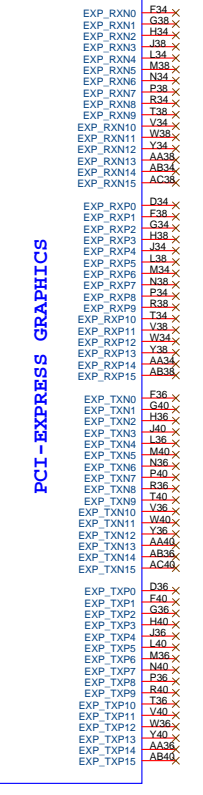
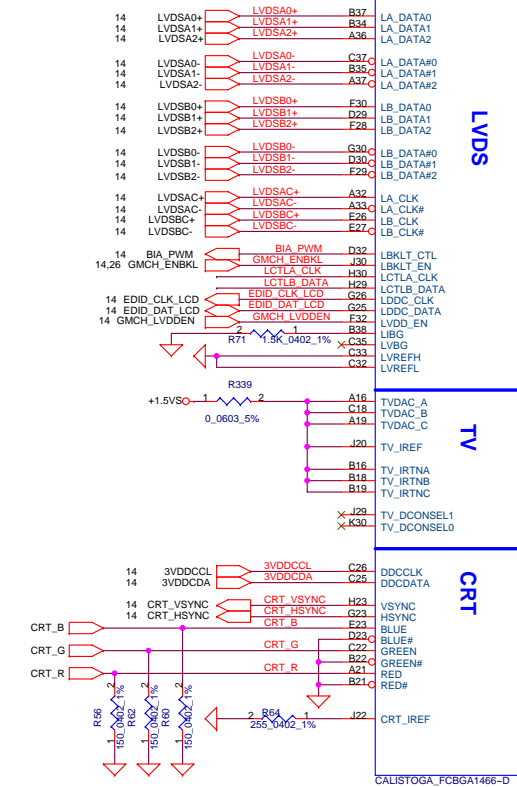
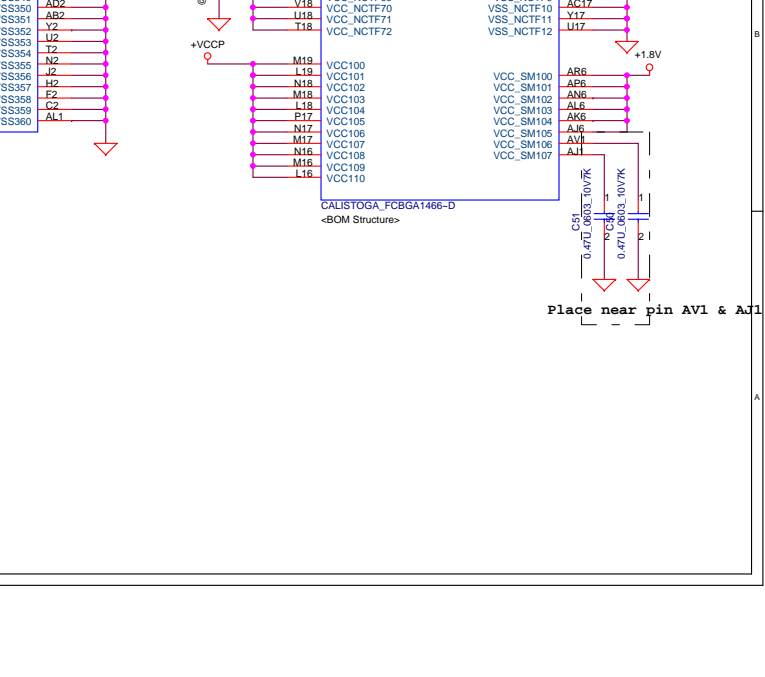
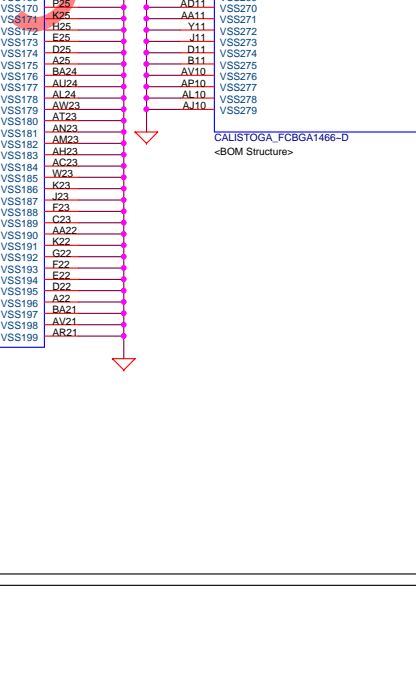
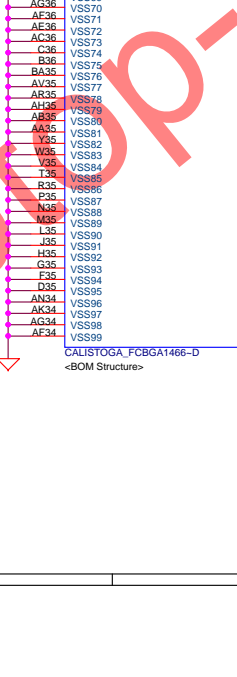
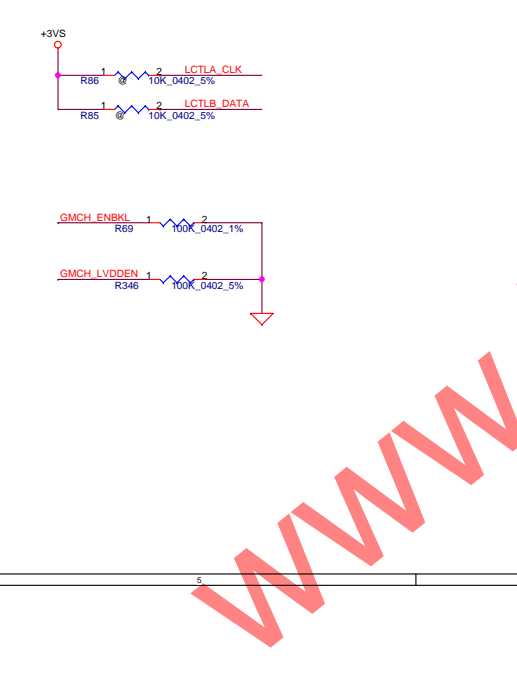
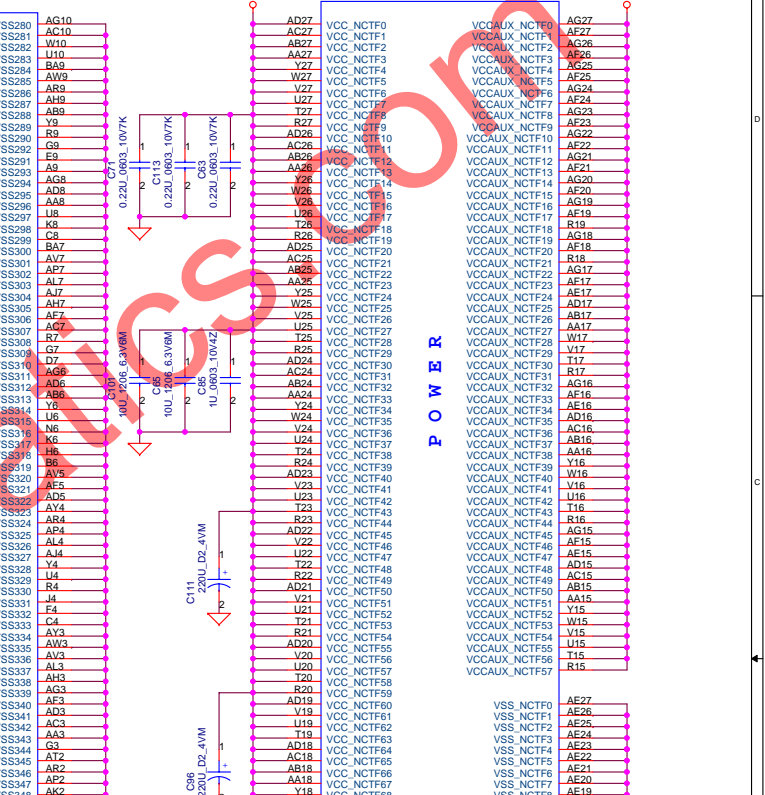
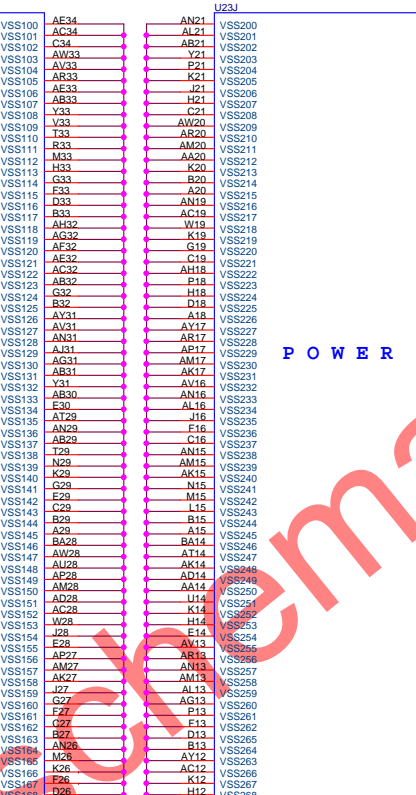
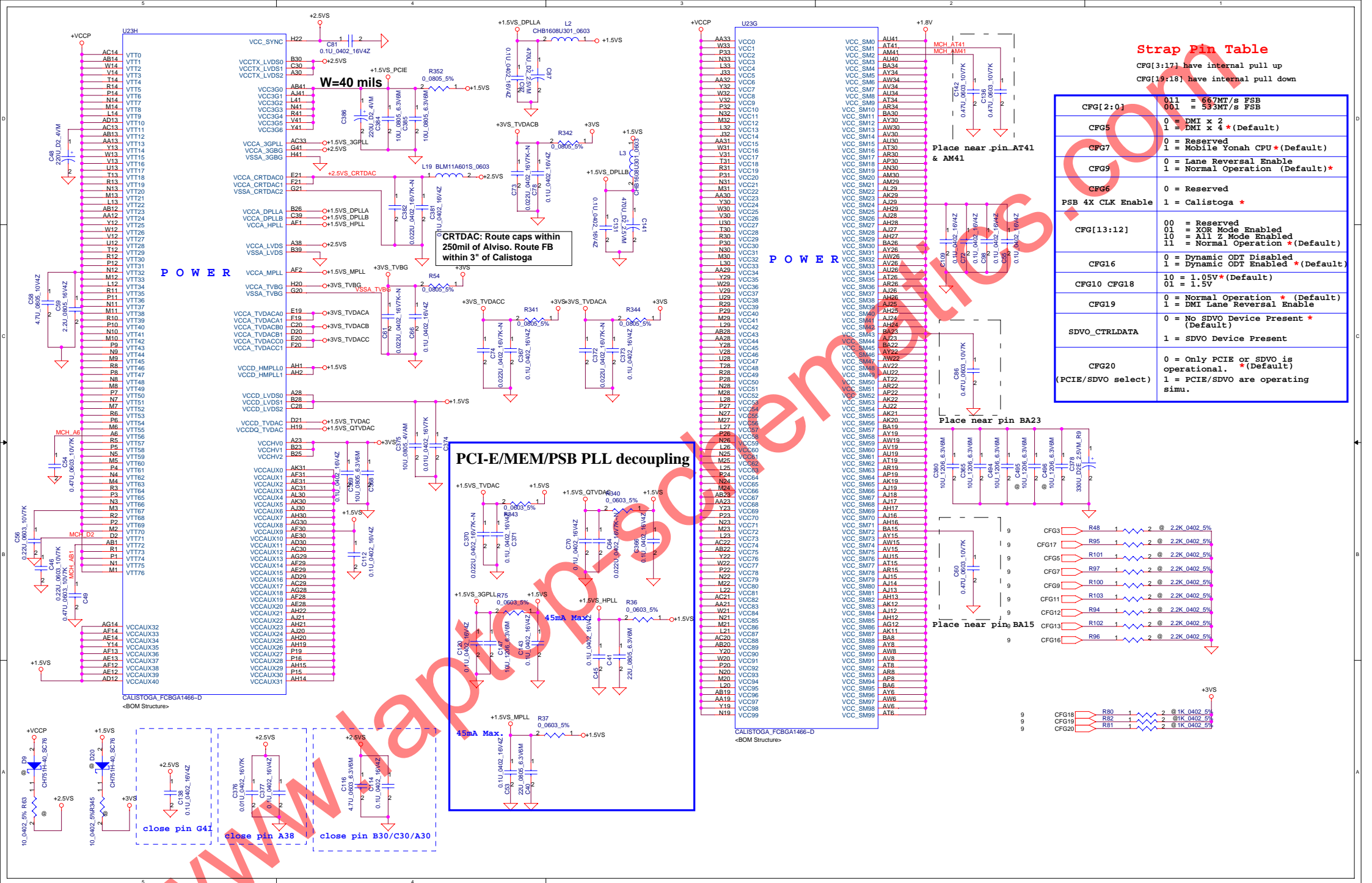


Table with columns for pin numbers (e.g., AC41, AC34, AC33, AC32, AC31, AC30, AC29, AC28, AC27, AC26, AC25, AC24, AC23, AC22, AC21, AC20, AC19, AC18, AC17, AC16, AC15, AC14, AC13, AC12, AC11, AC10, AC9, AC8, AC7, AC6, AC5, AC4, AC3, AC2, AC1) and corresponding signal names (e.g., VSS0, VSS1, VSS2, VSS3, VSS4, VSS5, VSS6, VSS7, VSS8, VSS9, VSS10, VSS11, VSS12, VSS13, VSS14, VSS15, VSS16, VSS17, VSS18, VSS19, VSS20, VSS21, VSS22, VSS23, VSS24, VSS25, VSS26, VSS27, VSS28, VSS29, VSS30, VSS31, VSS32, VSS33, VSS34, VSS35, VSS36, VSS37, VSS38, VSS39, VSS40, VSS41, VSS42, VSS43, VSS44, VSS45, VSS46, VSS47, VSS48, VSS49, VSS50, VSS51, VSS52, VSS53, VSS54, VSS55, VSS56, VSS57, VSS58, VSS59, VSS60, VSS61, VSS62, VSS63, VSS64, VSS65, VSS66, VSS67, VSS68, VSS69, VSS70, VSS71, VSS72, VSS73, VSS74, VSS75, VSS76, VSS77, VSS78, VSS79, VSS80, VSS81, VSS82, VSS83, VSS84, VSS85, VSS86, VSS87, VSS88, VSS89, VSS90, VSS91, VSS92, VSS93, VSS94, VSS95, VSS96, VSS97, VSS98, VSS99).



Place near pin AV1 & AV1

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Strap Pin Table

CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 553MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V *(Default) 01 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. *(Default) 1 = PCIe/SDVO are operating simu.

POWER

POWER

PCI-E/MEM/PSB PLL decoupling

close pin G41

close pin A38

close pin B30/C30/A30

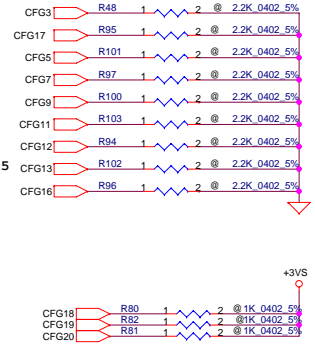
45mA Max.

45mA Max.

Place near pin_AT41 & AM41

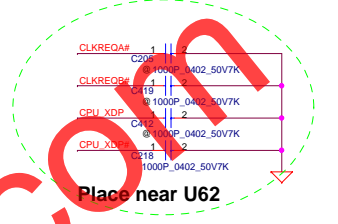
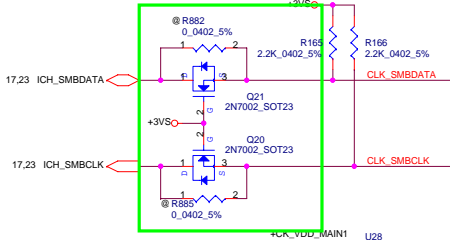
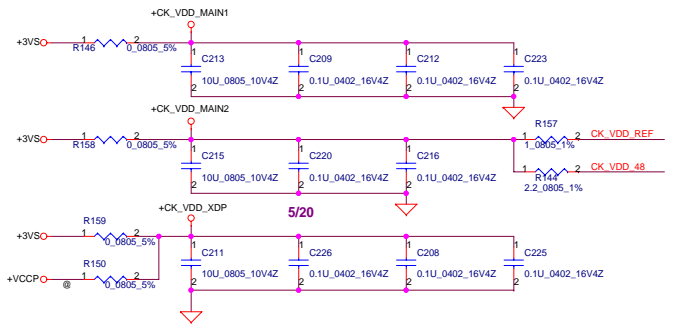
Place near pin_BA23

Place near pin_BA15

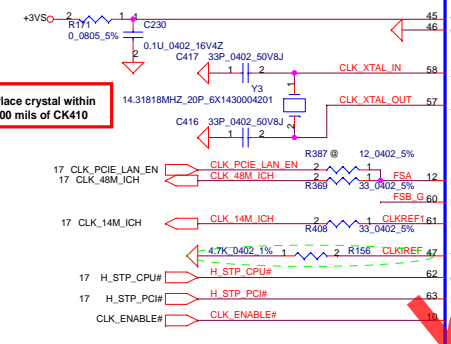
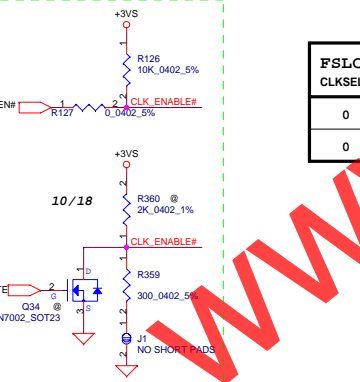
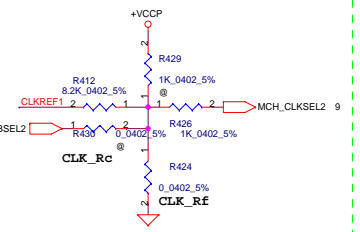
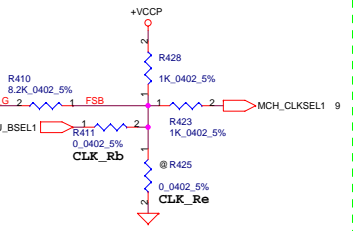
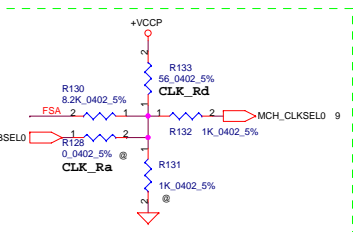


CALISTOGA_FCBGA1466-D
<BOM Structure>

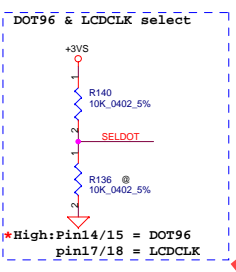
CALISTOGA_FCBGA1466-D
<BOM Structure>



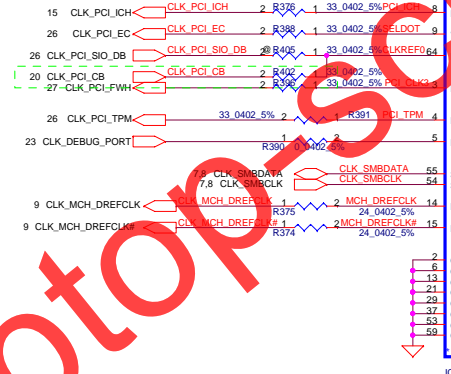
Place near U62



Place crystal within 500 mils of CK410



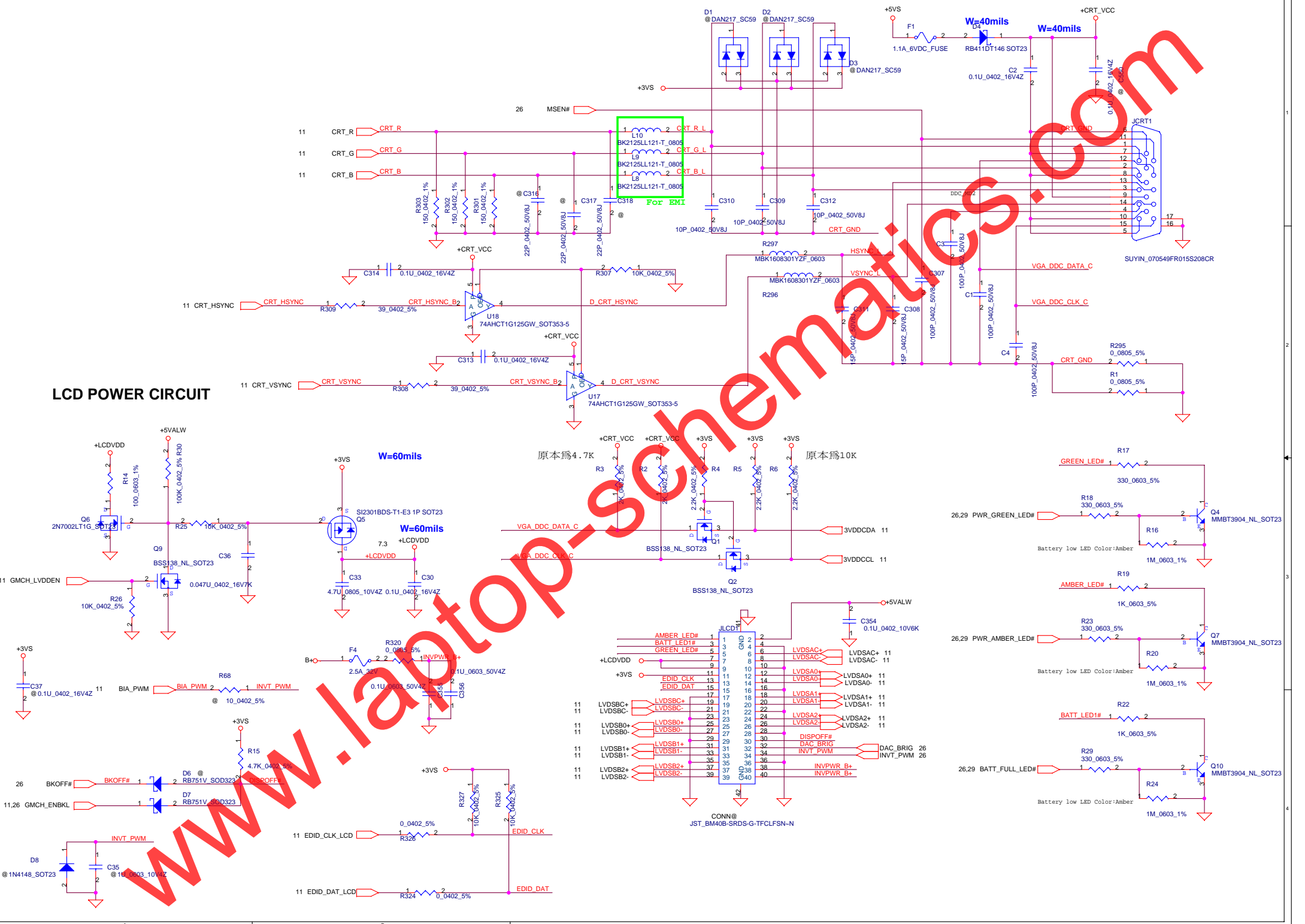
*High: Pin14/15 = DOT96
pin17/18 = LCDCLK



FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

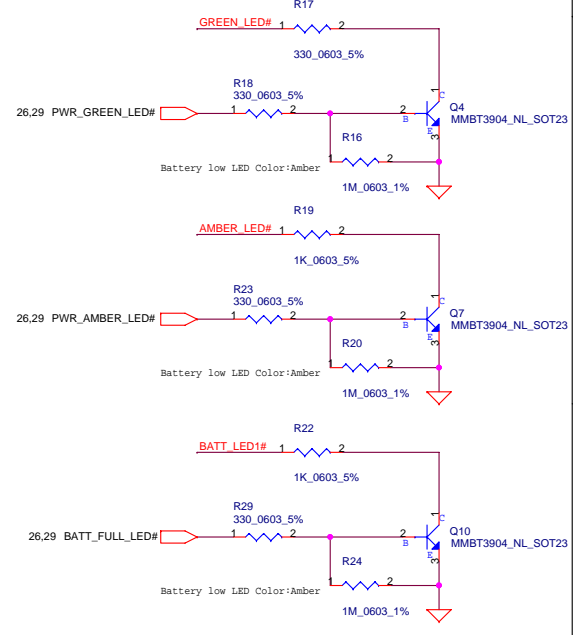
www.laptoprepair.com

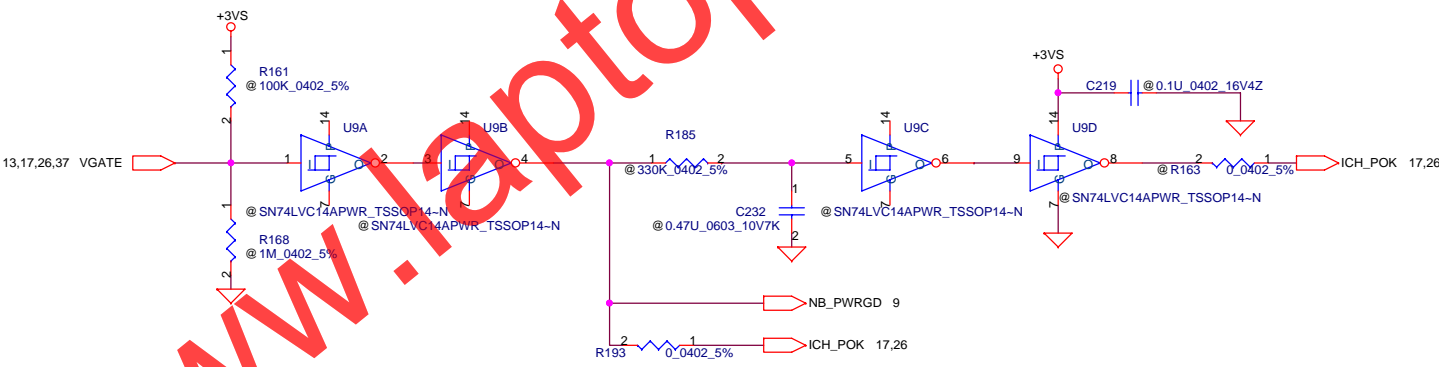
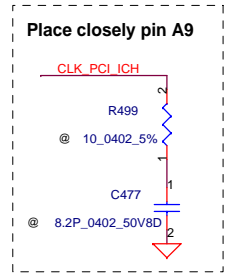
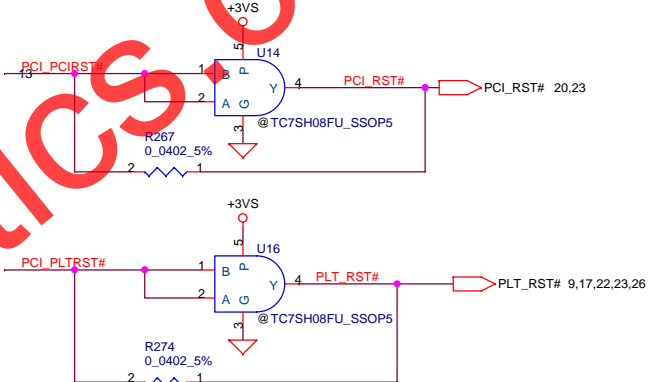
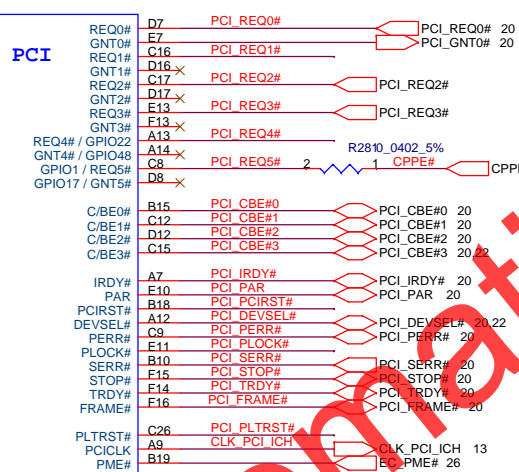
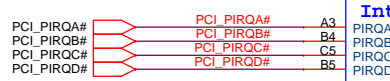
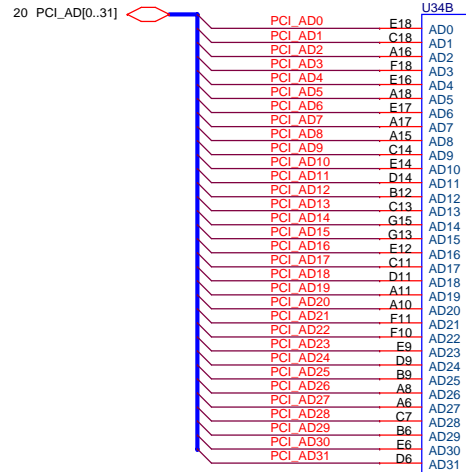
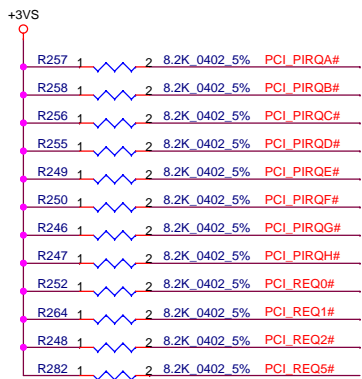
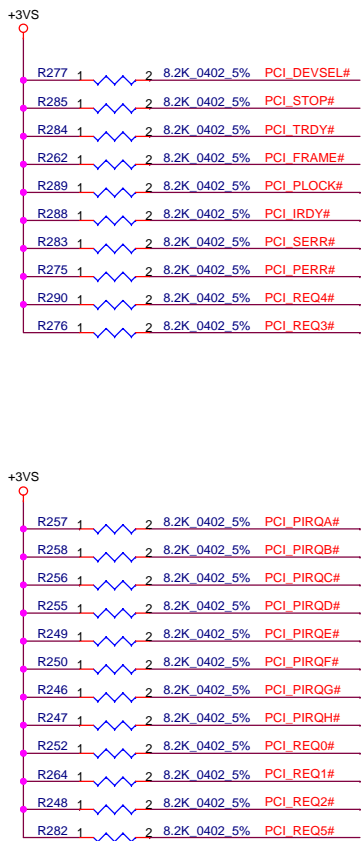
LCD POWER CIRCUIT



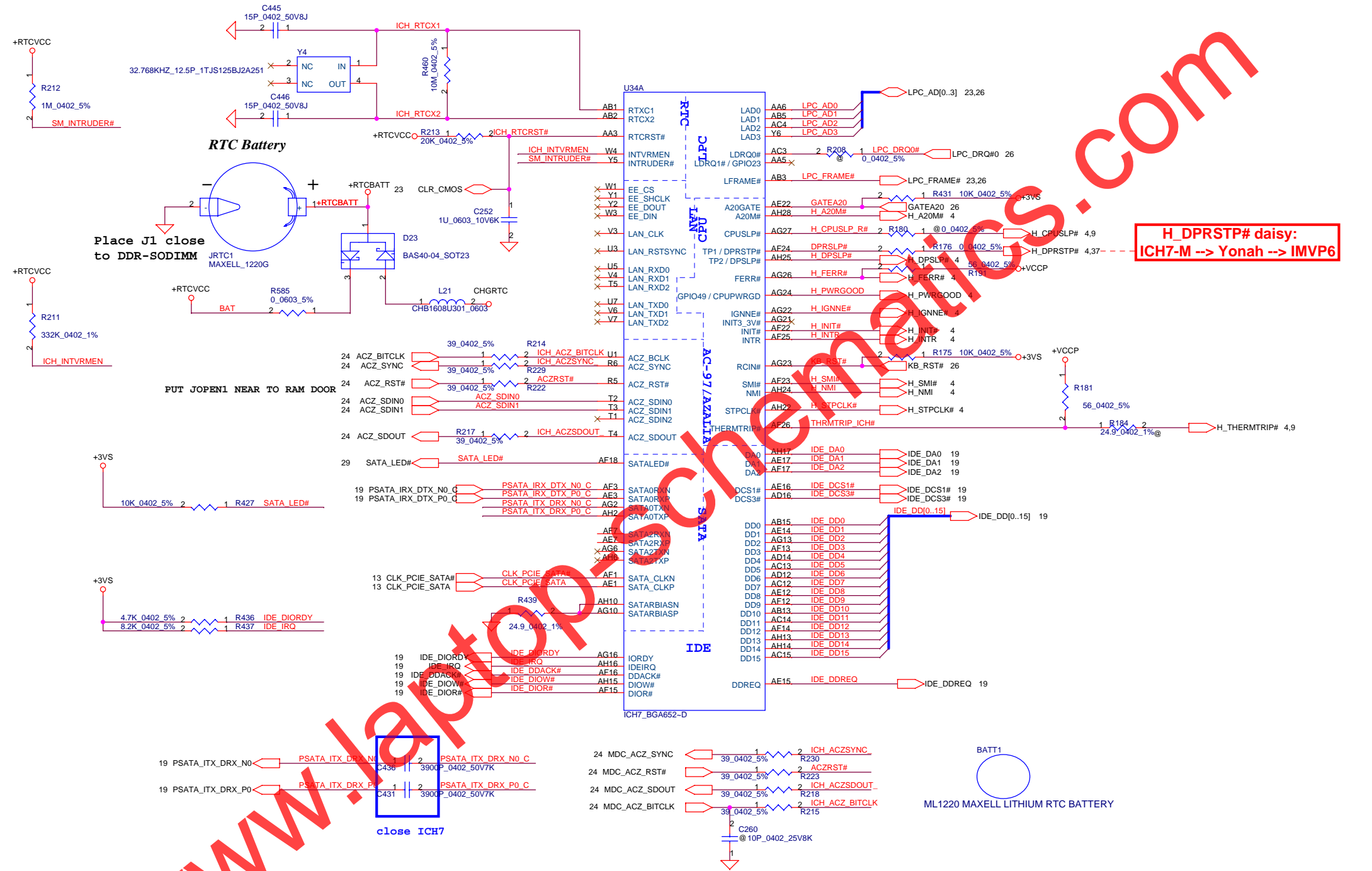
原本為4.7K
原本為10K

CONN@ JST_BM40B-SRDS-G-TFCLFSN-N





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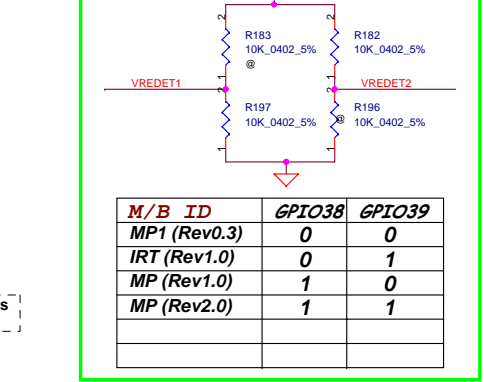
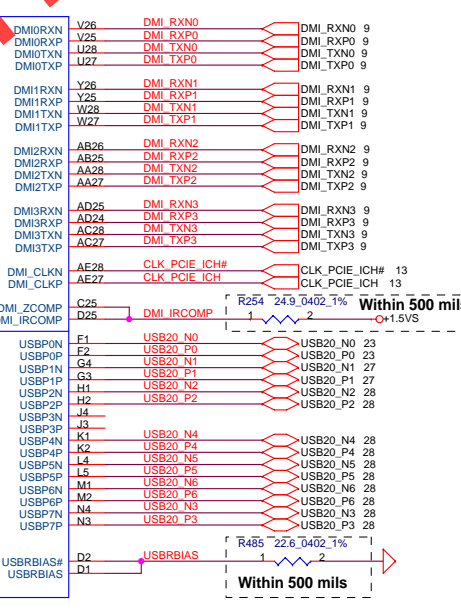
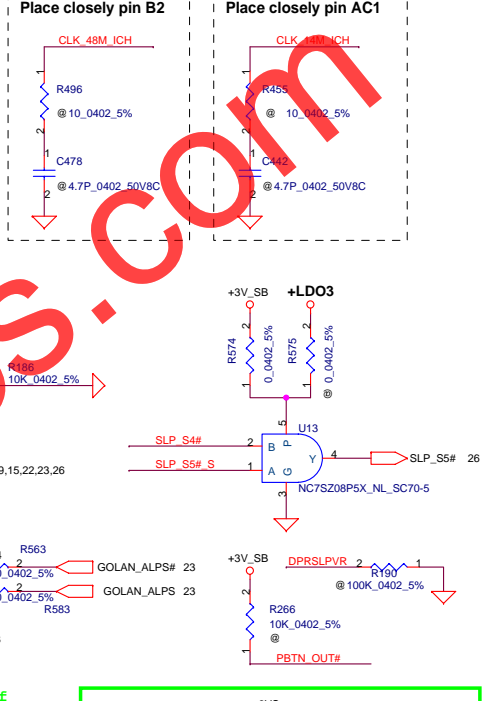
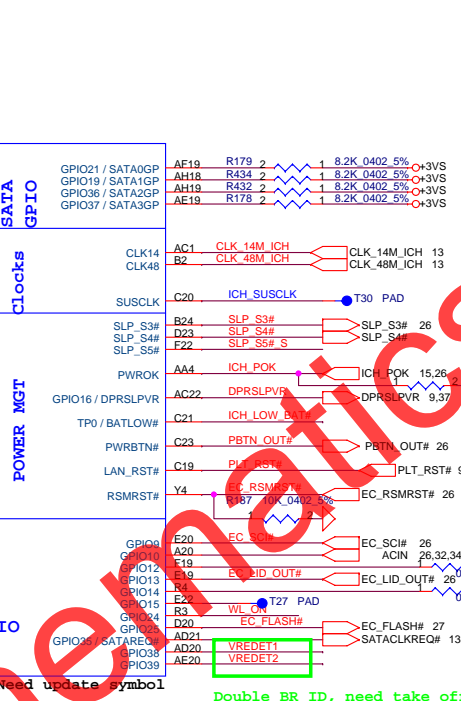
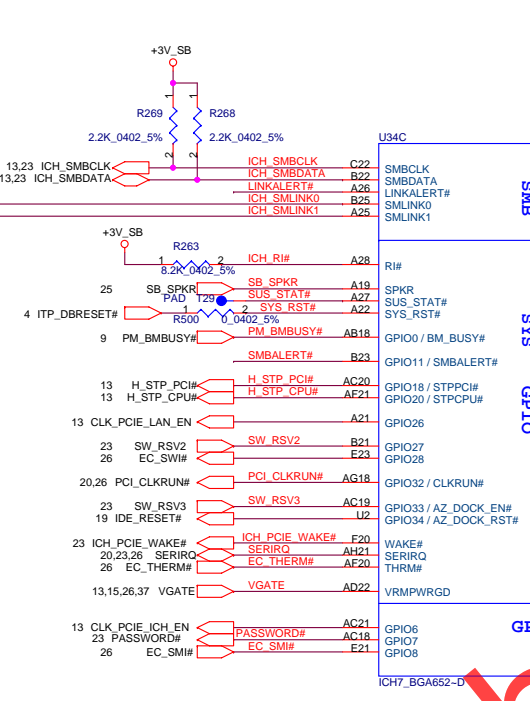
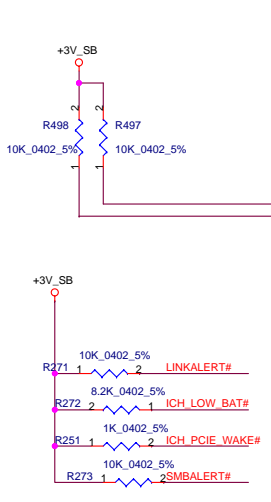
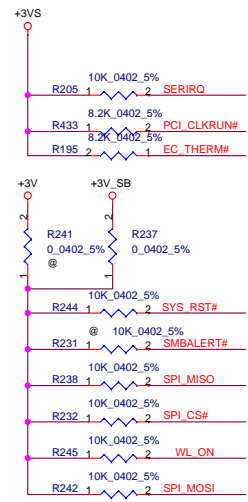
**H_DPRSTP# daisy:
ICH7-M --> Yonah --> IMVP6**

PUT JOPEN1 NEAR TO RAM DOOR

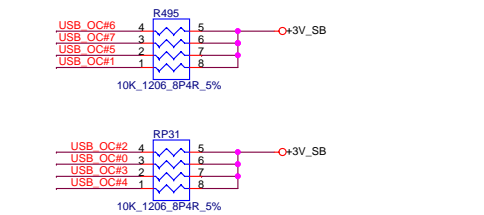
close ICH7

ML1220 MAXELL LITHIUM RTC BATTERY

www.laptopchips.com

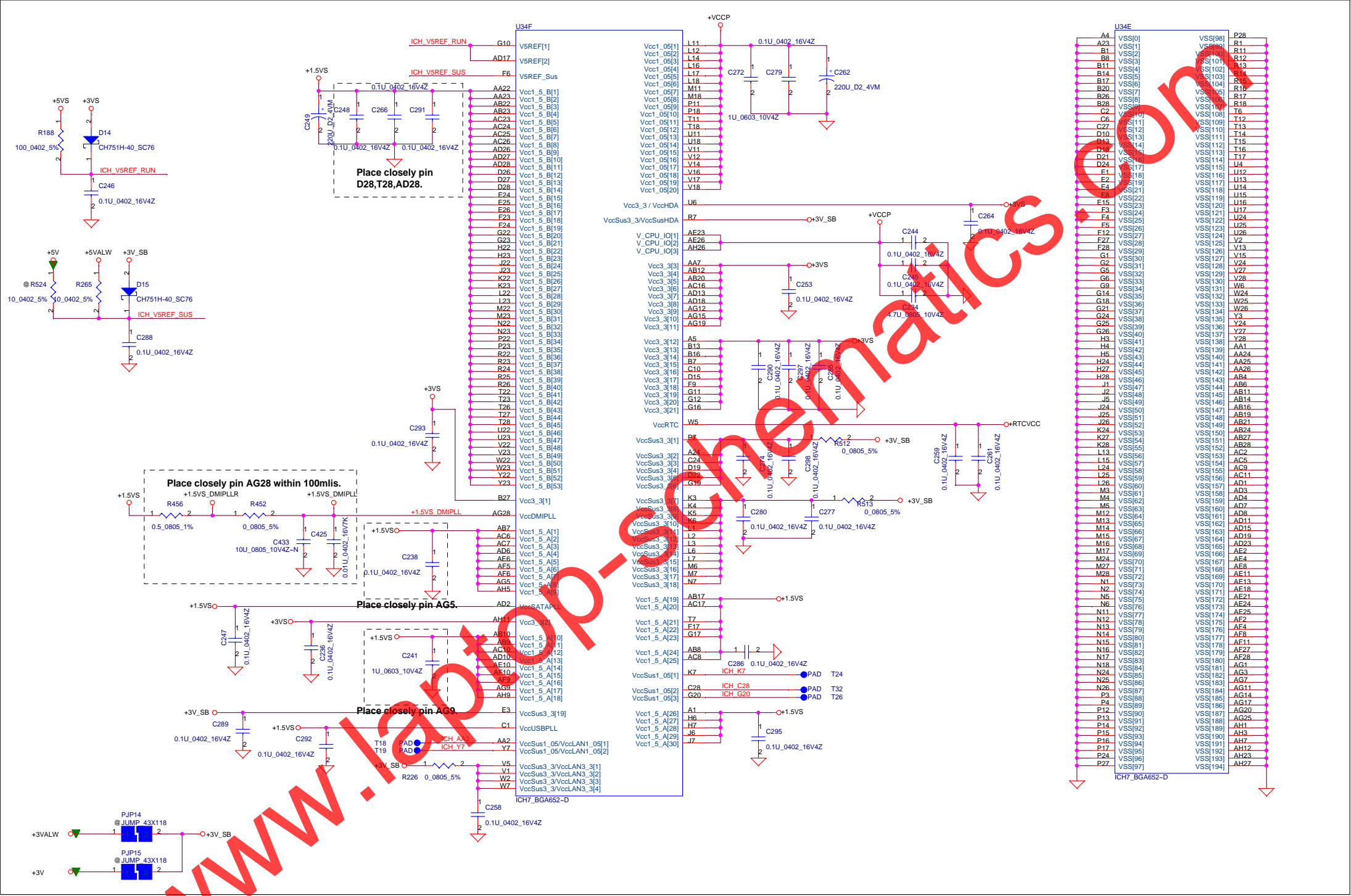


M/B ID	GPIO38	GPIO39
MP1 (Rev.0.3)	0	0
IRT (Rev1.0)	0	1
MP (Rev1.0)	1	0
MP (Rev2.0)	1	1



www.laptopcomponents.com

Need update symbol
Double BR ID, need take off



www.geminaelectronics.com

Place closely pin D28,T28,AD28.

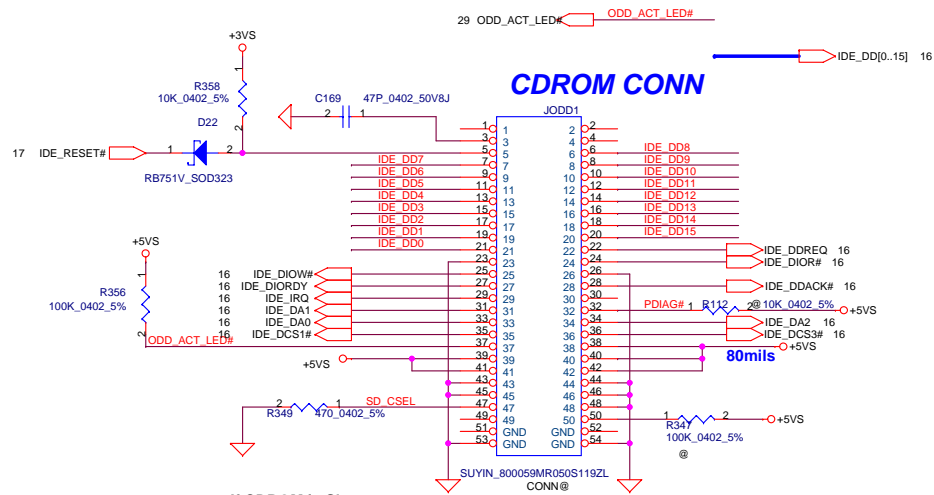
Place closely pin AG28 within 100mils.

Place closely pin AG5.

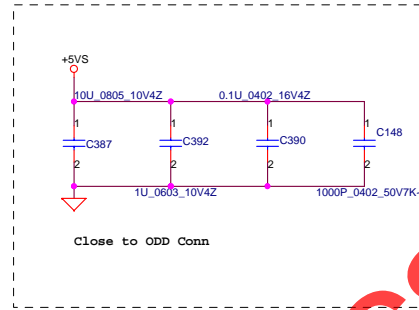
Place closely pin AG9.

PJP14 @ JUMP 43X118

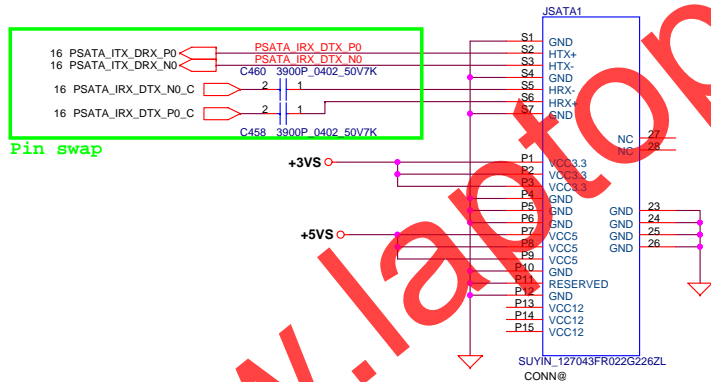
PJP15 @ JUMP 43X118



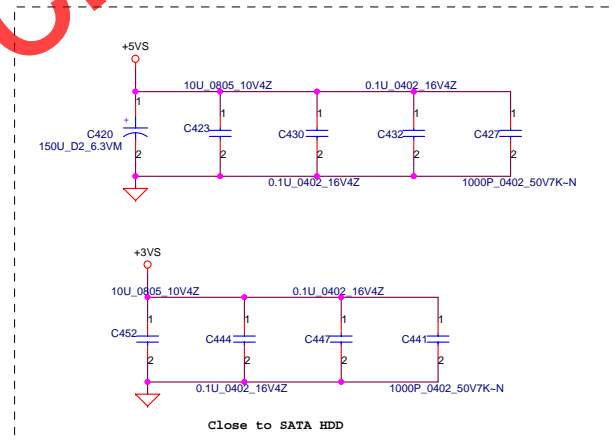
If CDROM is Slave
then SD_CSEL= Floating
else SD_CSEL= Low



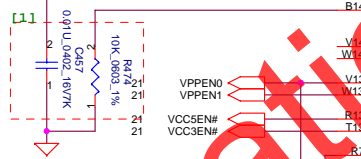
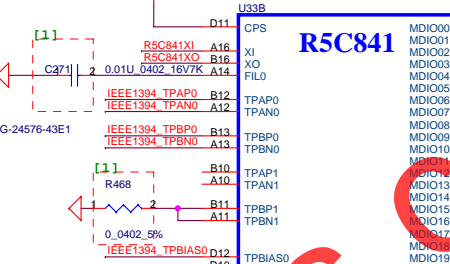
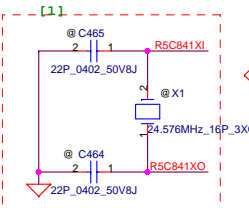
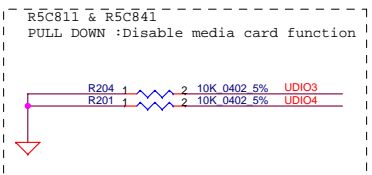
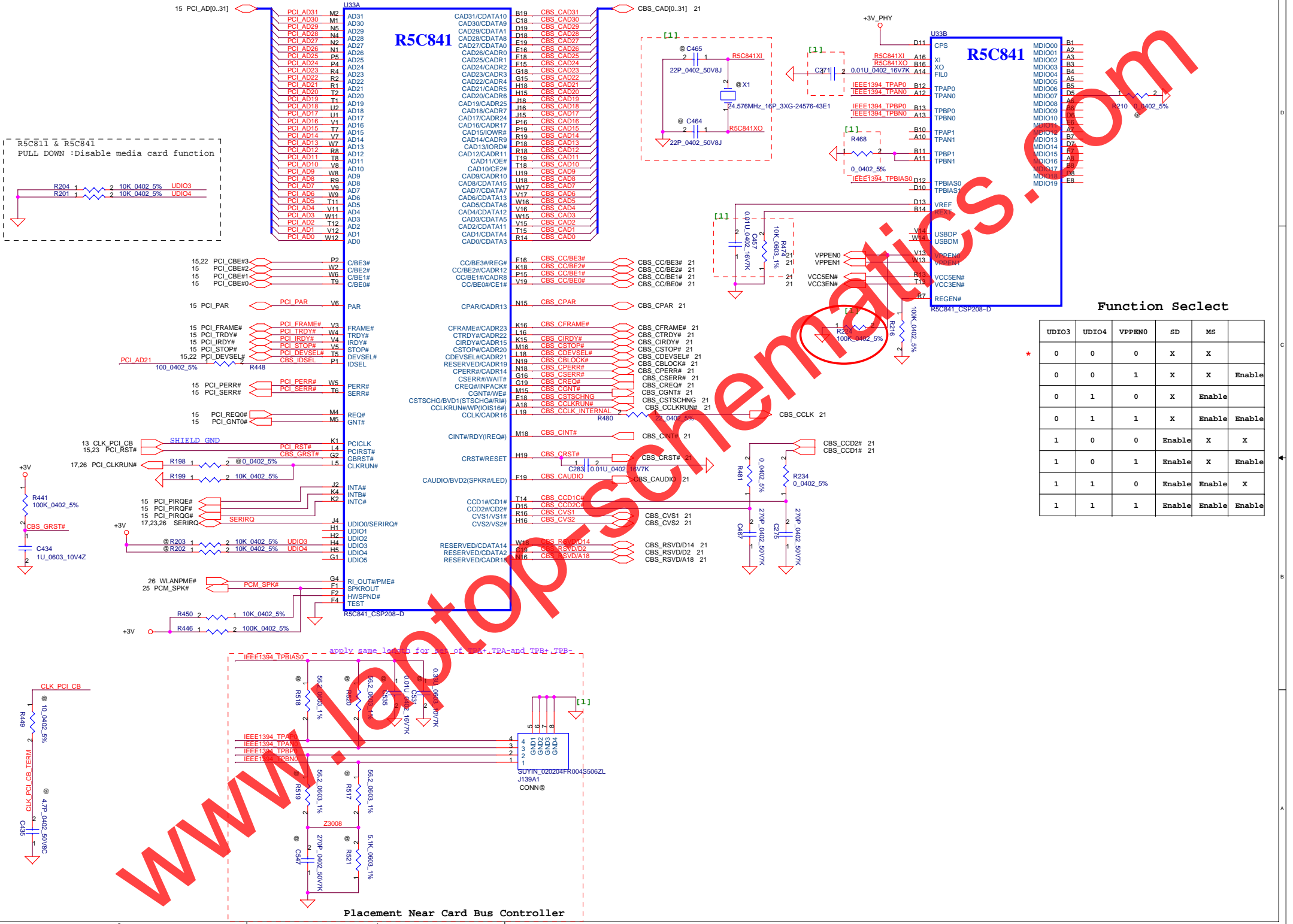
SATA HDD CONN



Pin swap

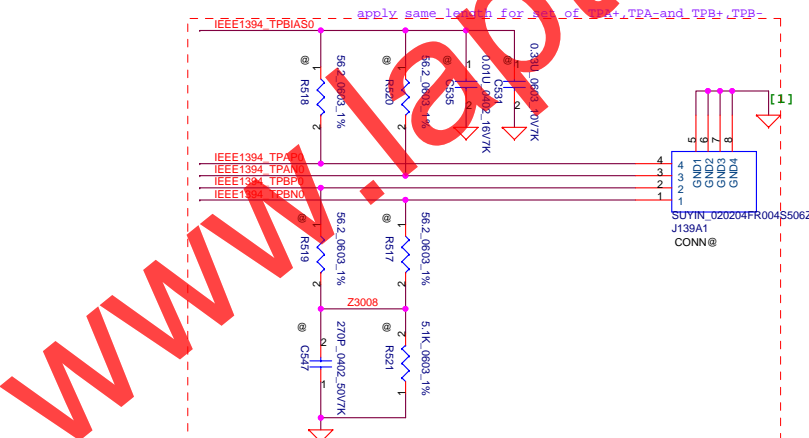


www.laptop-schematics.com

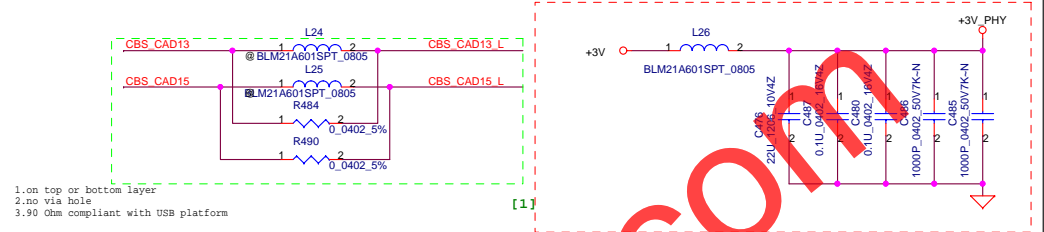
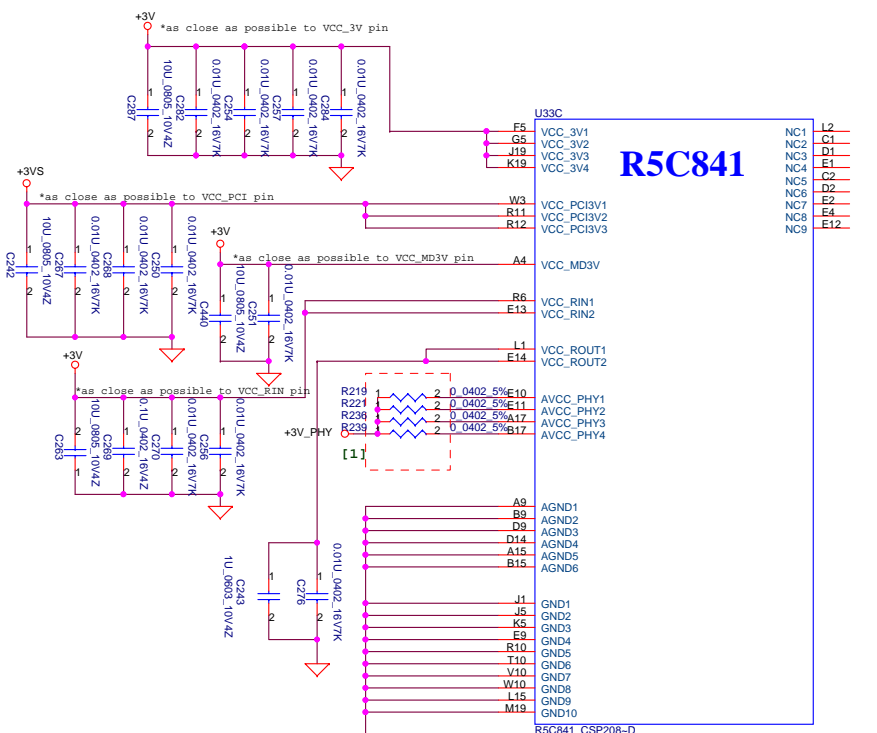


Function Select

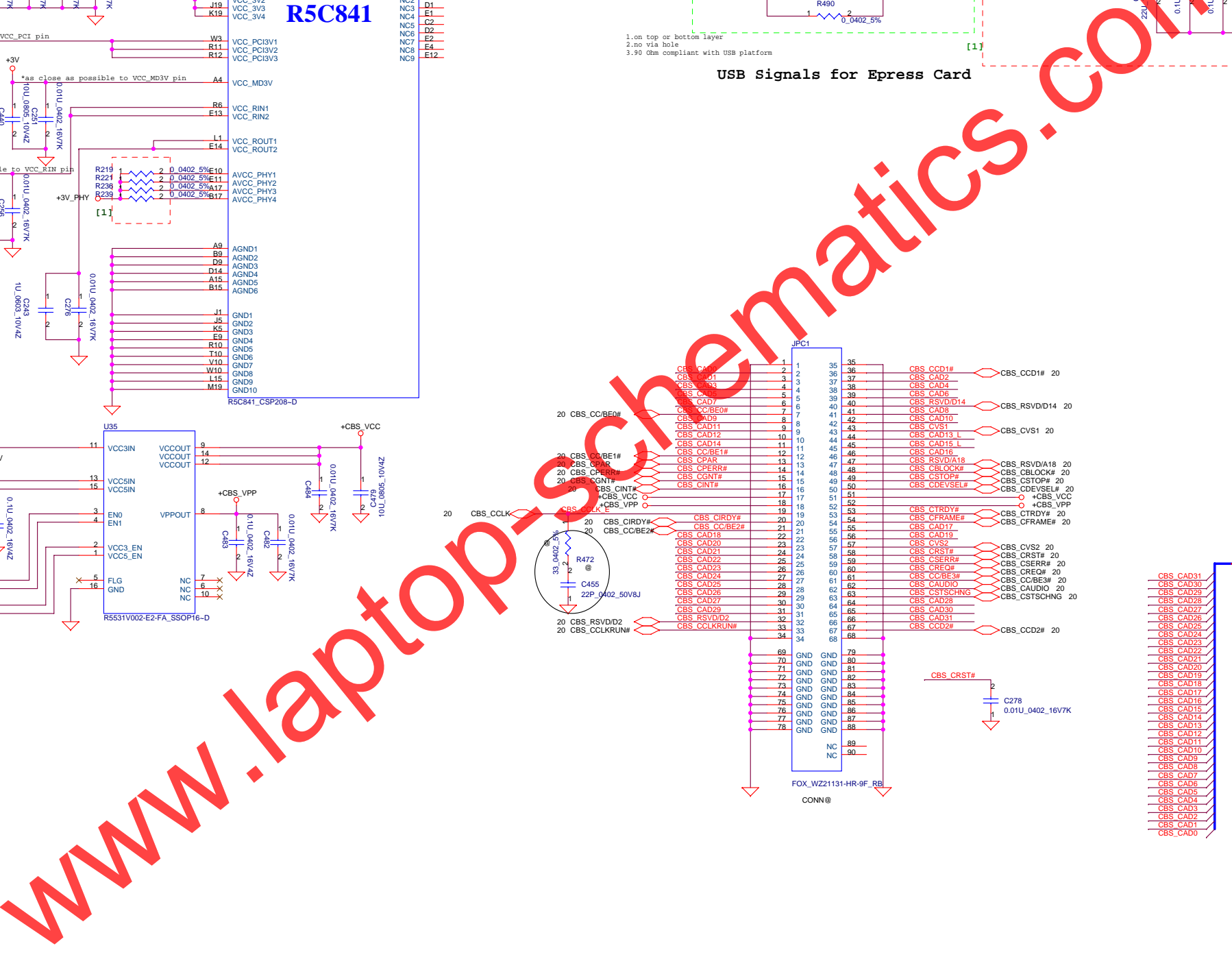
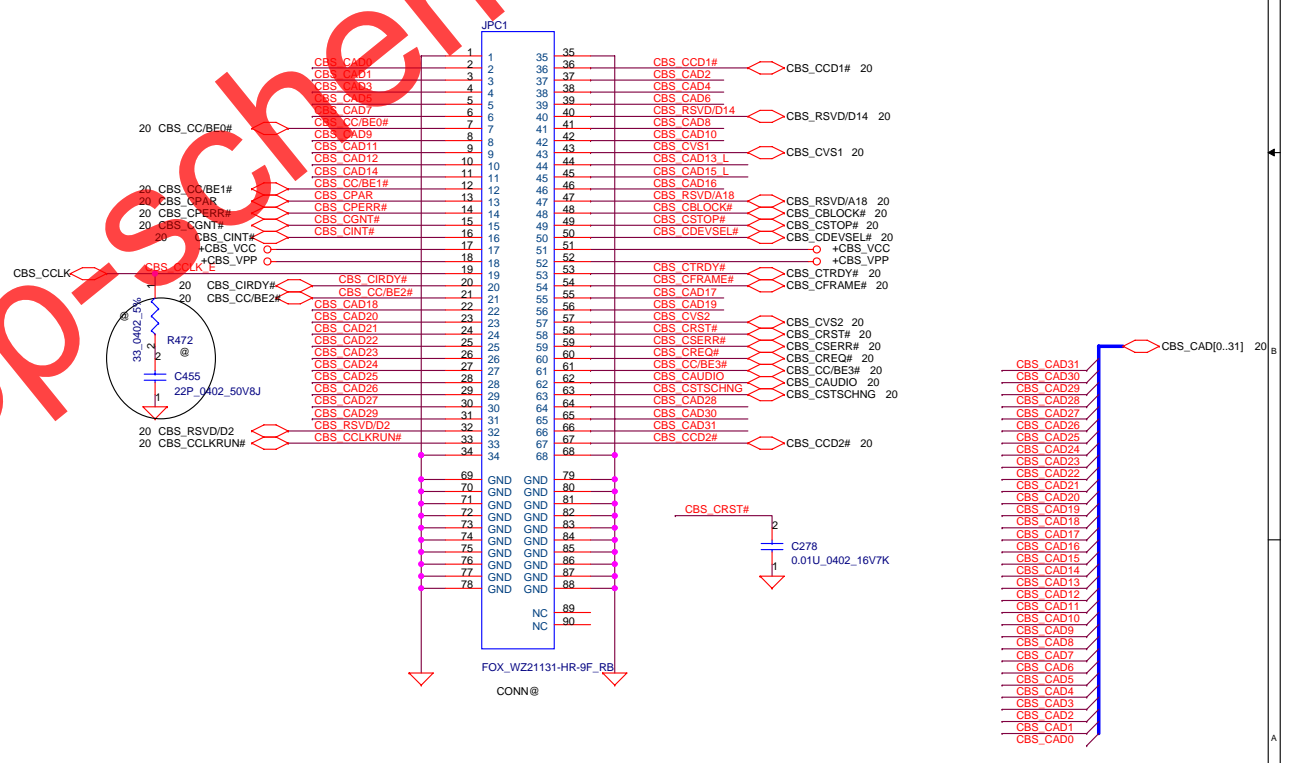
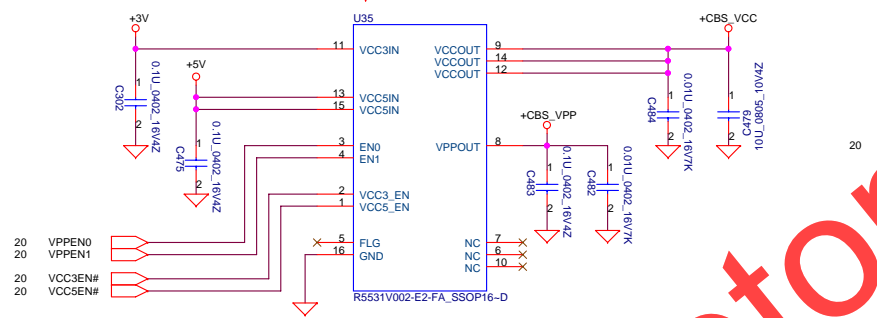
UDIO3	UDIO4	VPPEN0	SD	MS	
0	0	0	X	X	
0	0	1	X	X	Enable
0	1	0	X		Enable
0	1	1	X	Enable	Enable
1	0	0	Enable	X	X
1	0	1	Enable	X	Enable
1	1	0	Enable	Enable	X
1	1	1	Enable	Enable	Enable



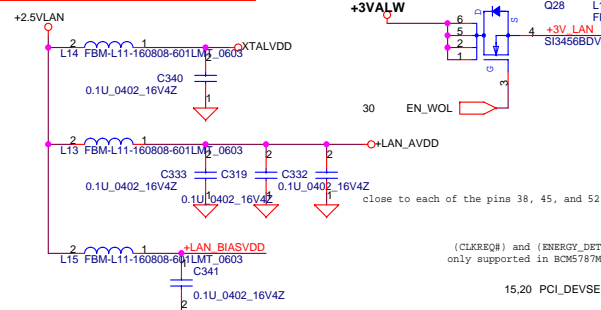
Placement Near Card Bus Controller



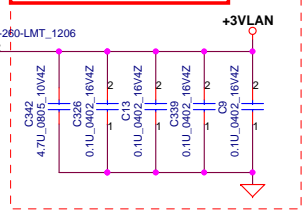
USB Signals for Express Card



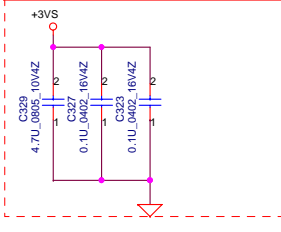
Layout Notice : Filter place as close chip as possible.



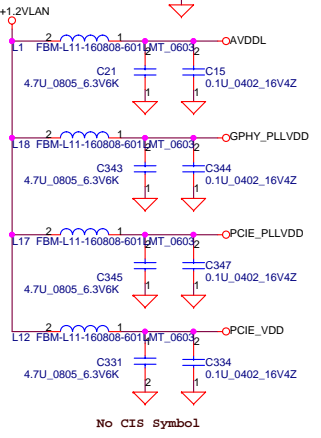
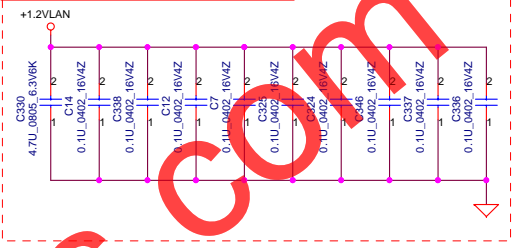
Layout Notice : Place as close chip as possible.



Layout Notice : 3.3V filter. Place as close chip as possible.

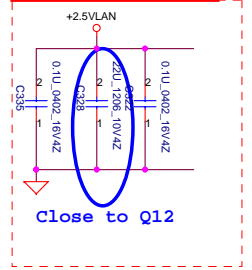


Layout Notice : 1.2V filter. Place as close chip as possible.



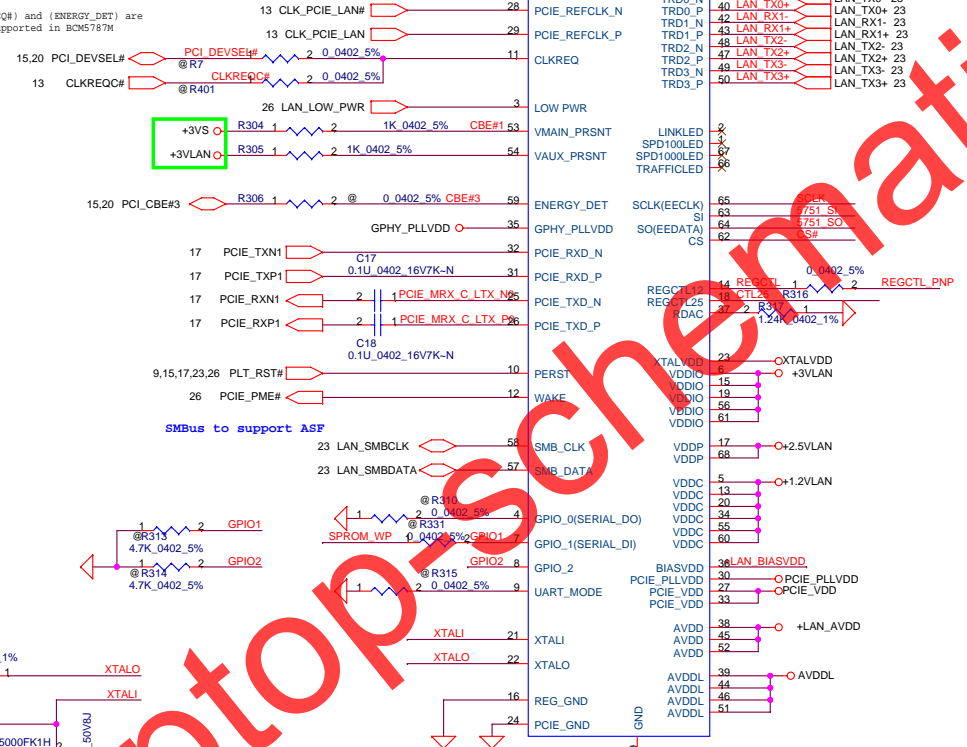
No CIS Symbol

Layout Notice : Place as close chip as possible.

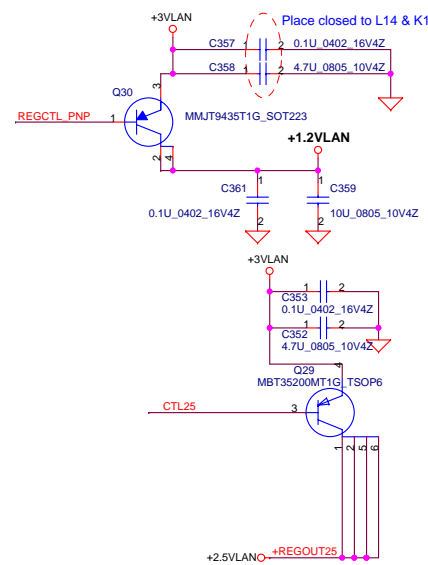


Close to Q12

(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M



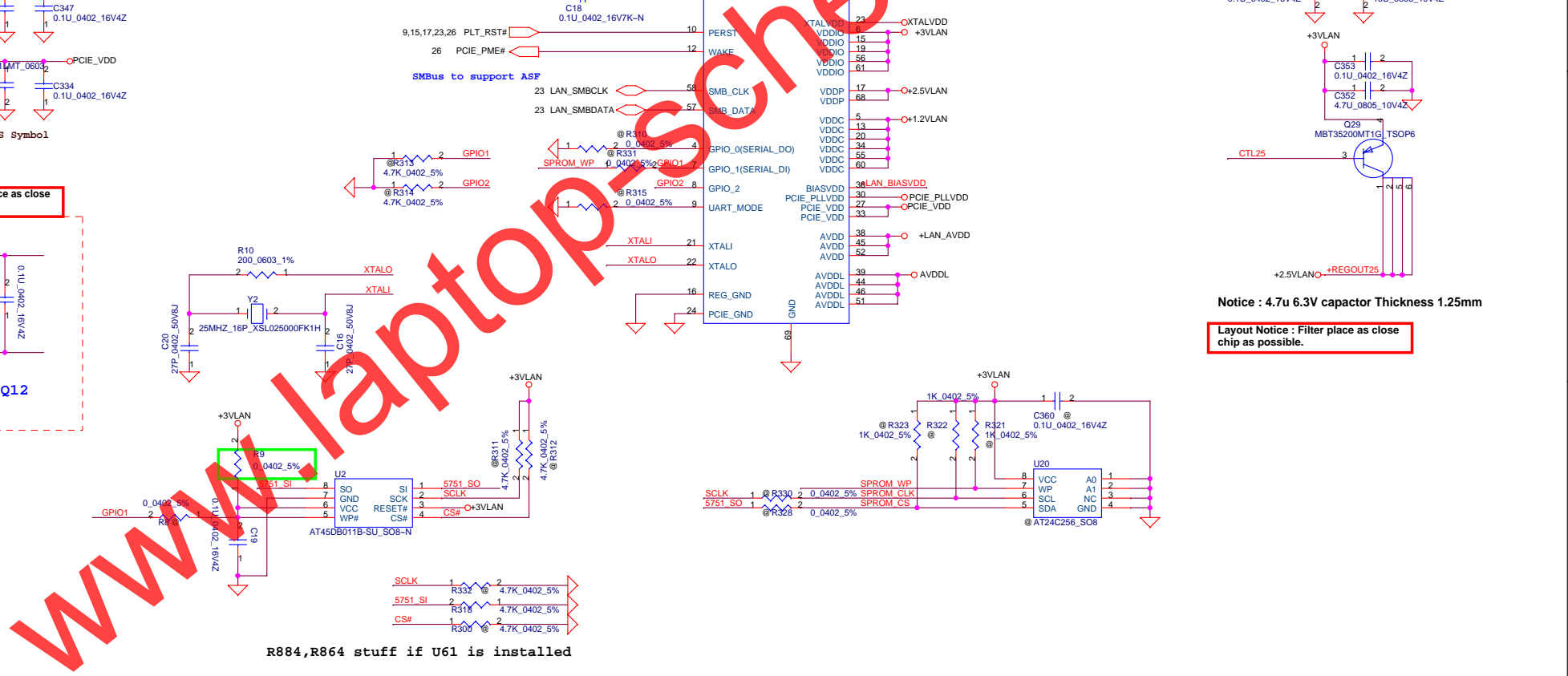
Place closed to L14 & K14

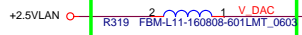


Notice : 4.7u 6.3V capacitor Thickness 1.25mm

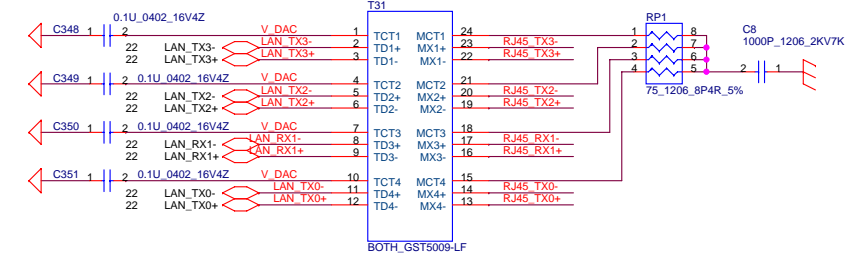
Layout Notice : Filter place as close chip as possible.

R884,R864 stuff if U61 is installed

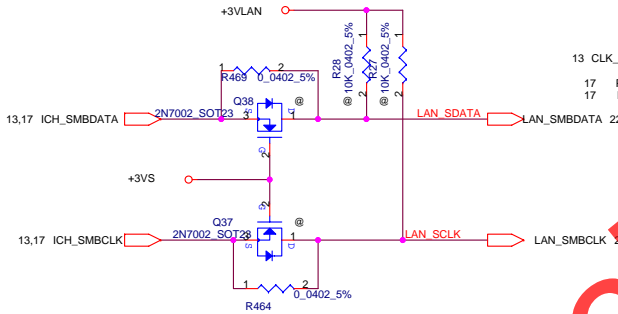
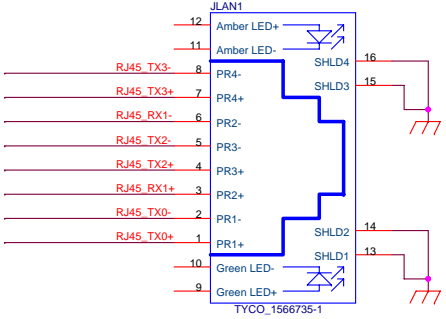




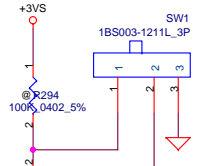
- ES2 by rework form 0805 to 0603
- Part name will modify in next phase



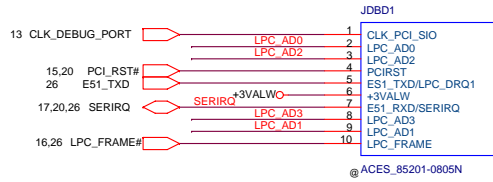
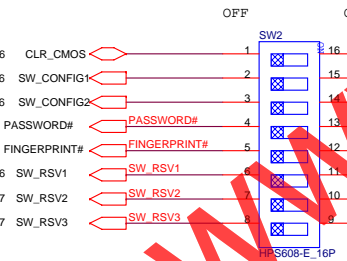
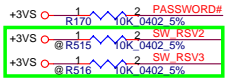
Layout Note
24HST1041A-3 pls close to conn.



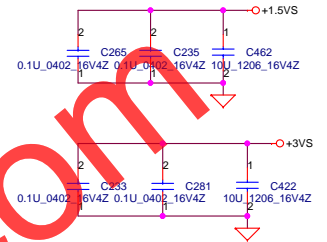
Wireless_BTN
Killer switch



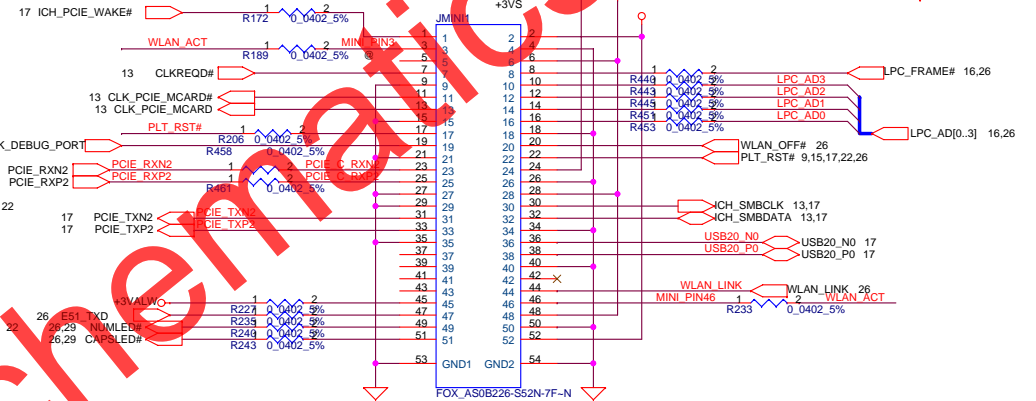
All 49.9 ohm + 0.1 uF termination components close to BCM5751M



For DEBUG

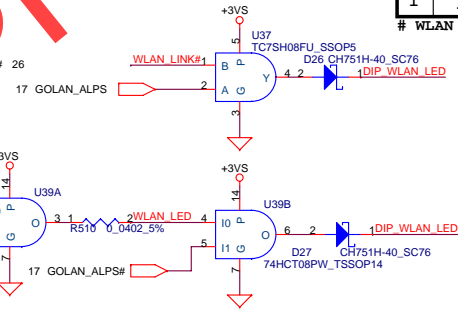


Mini-Express Card

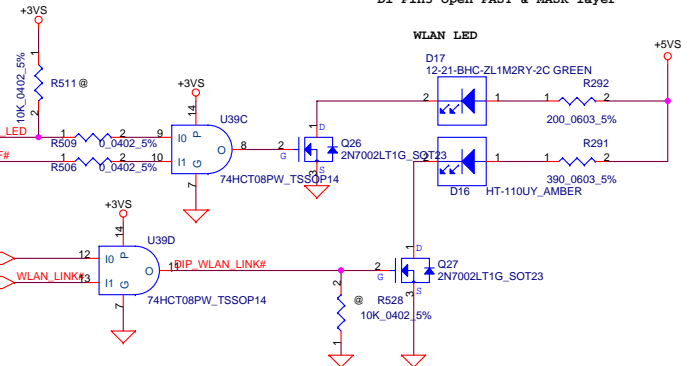


GOLAN_ALPS#	
0	GOLAN
1	ALPS

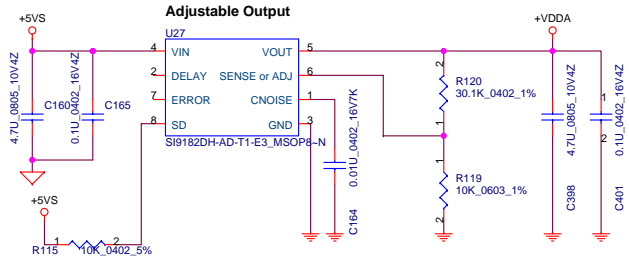
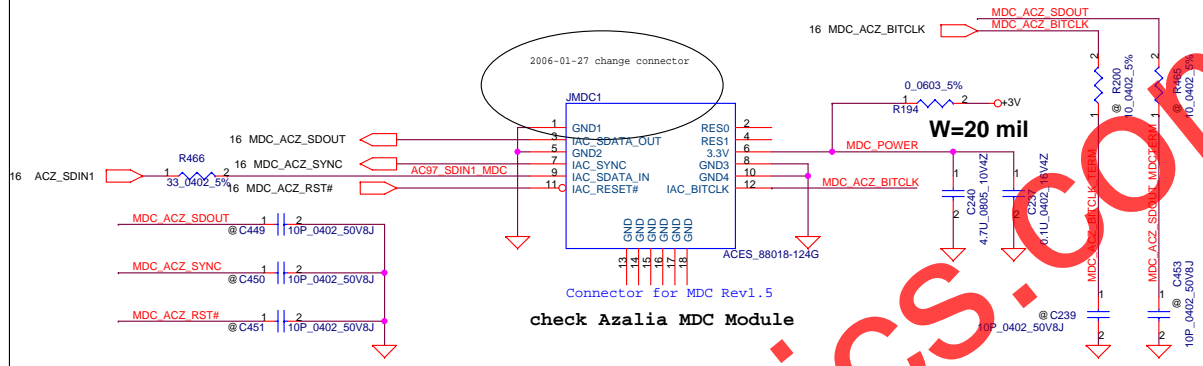
WLAN detect by BIOS and program GOLAN_ALPS# to control WLAN LED



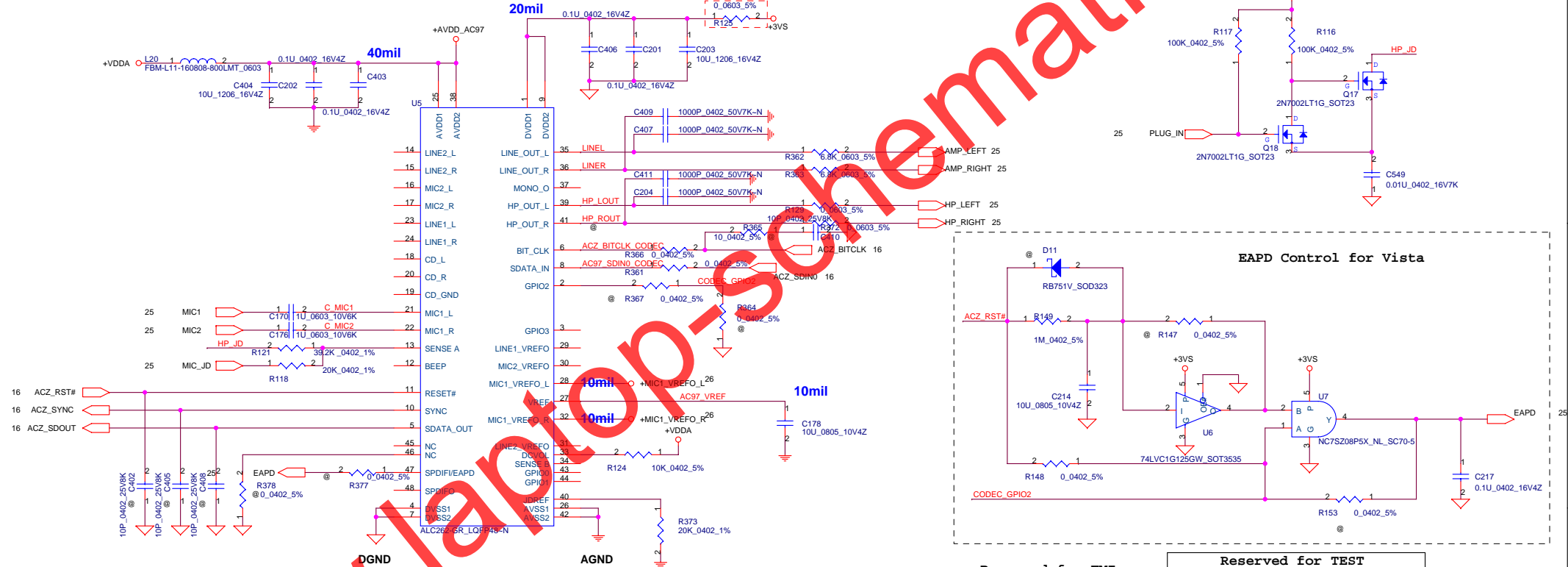
D1 Pin3 Open PAST & MASK layer



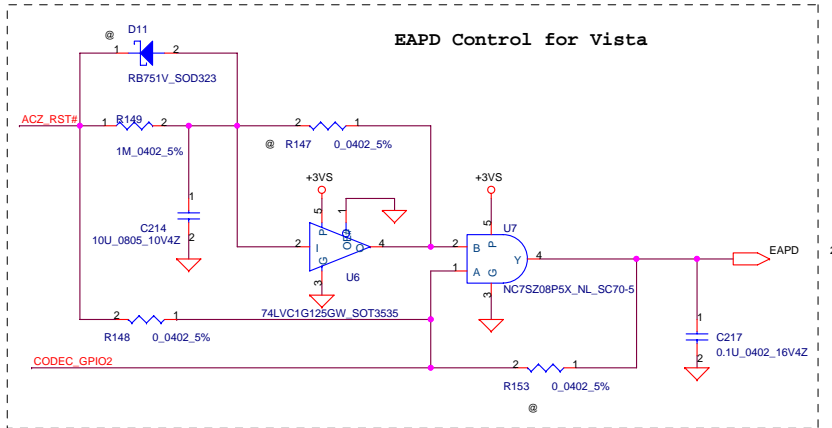
MDC CONN.



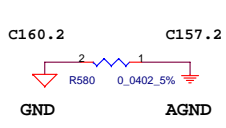
HD Audio Codec



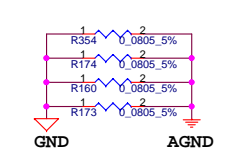
EAPD Control for Vista



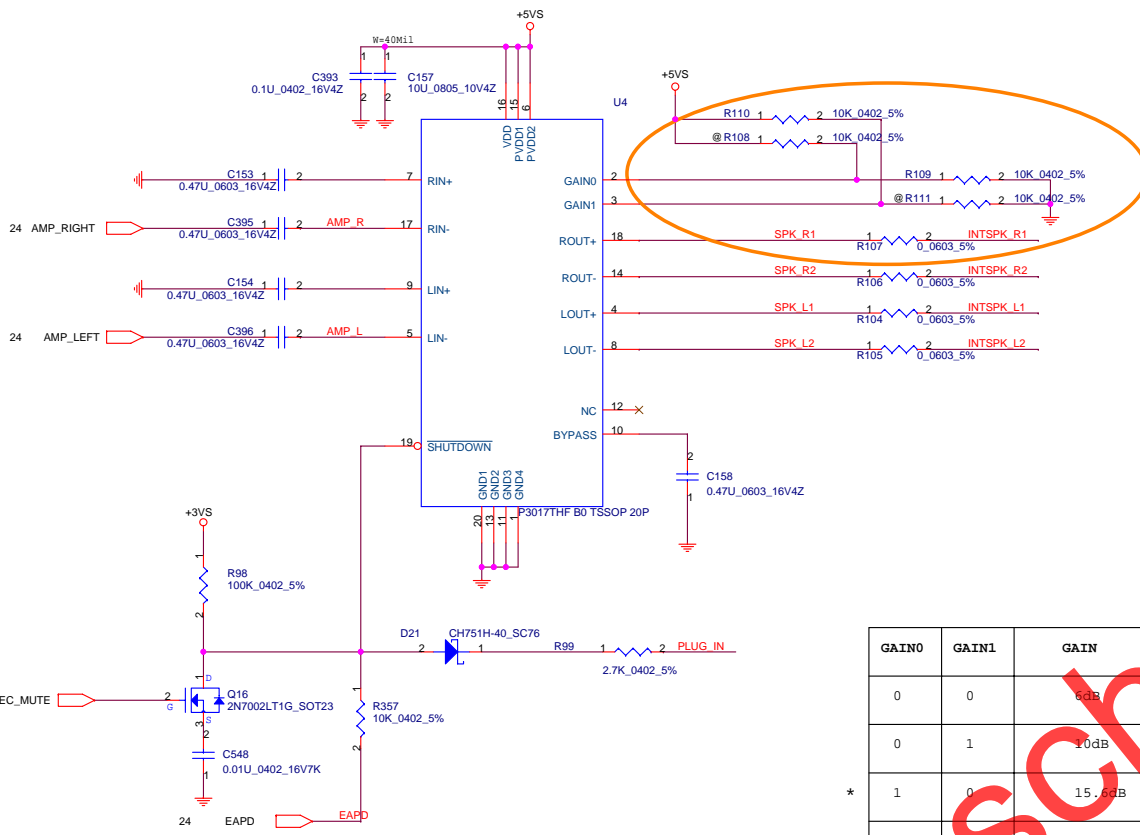
Reserved for EMI



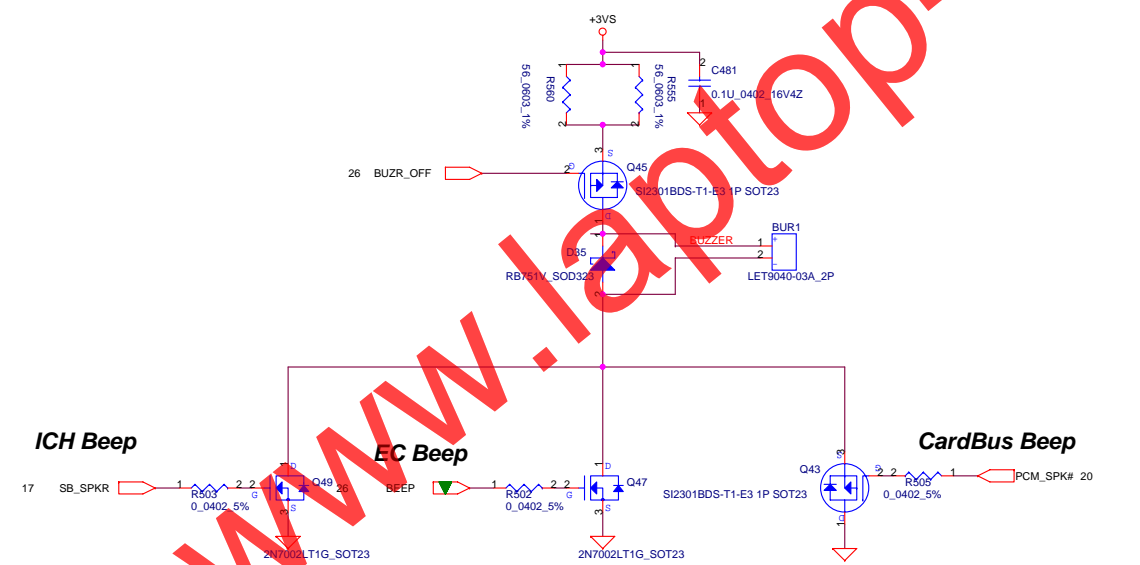
Reserved for TEST



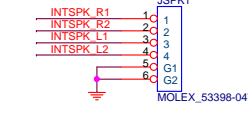
www.laptop-circuit.com



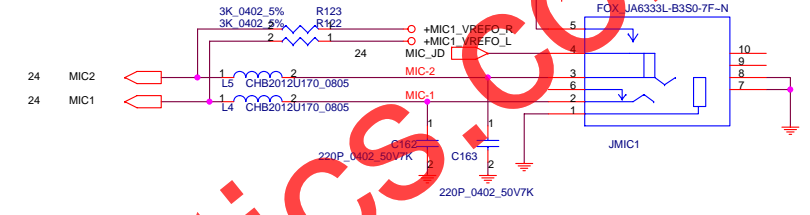
Buzzer need to support ICH/PCM_SPK/Battery_low and WL_on/off



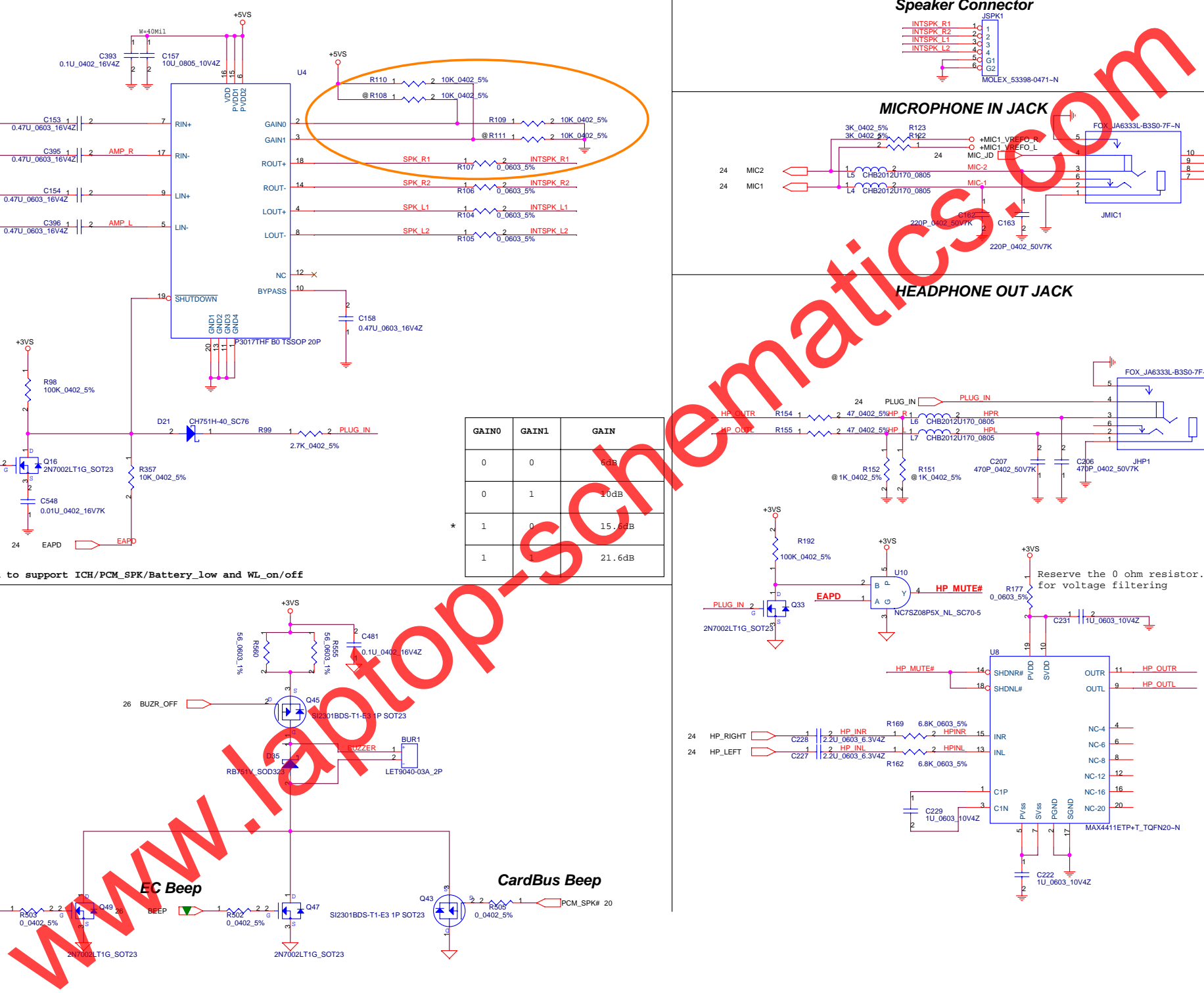
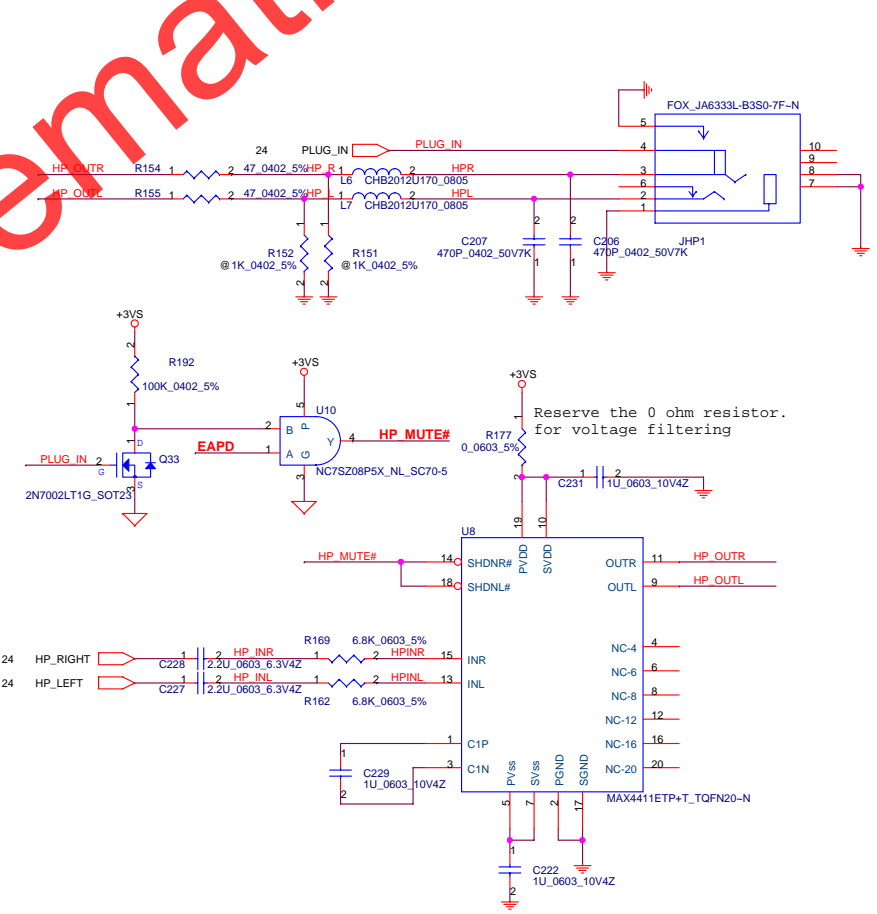
Speaker Connector

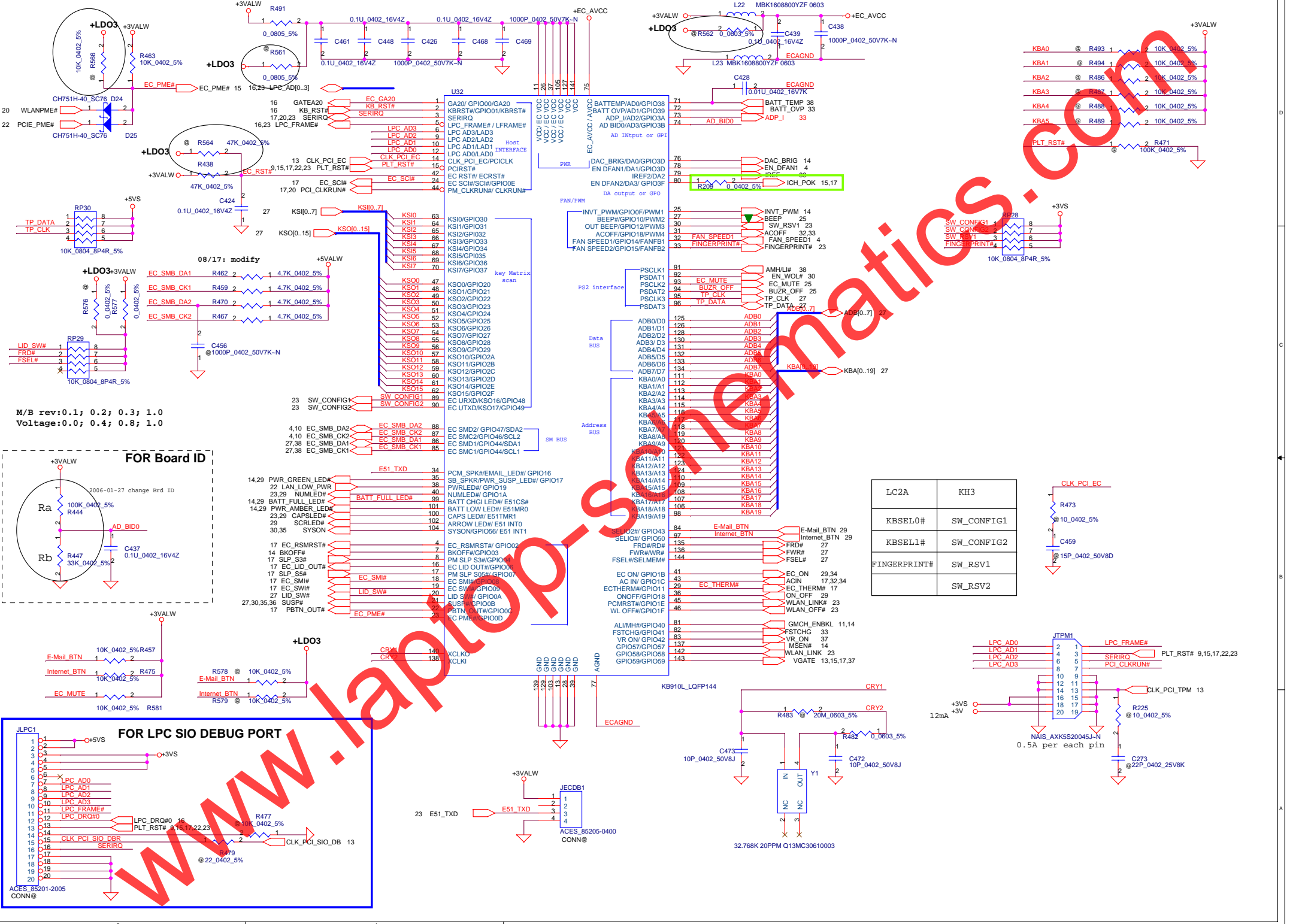


MICROPHONE IN JACK

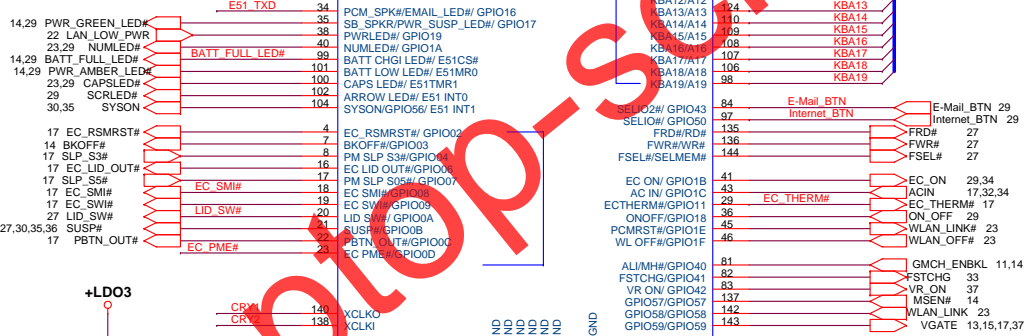
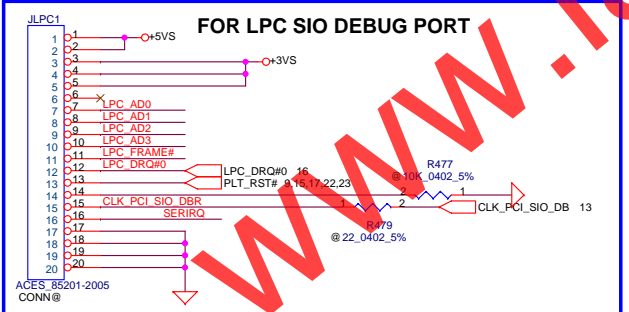
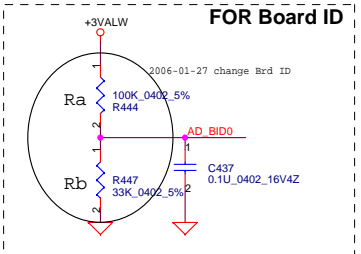


HEADPHONE OUT JACK

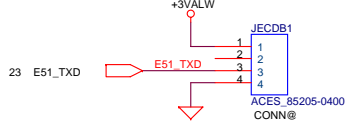
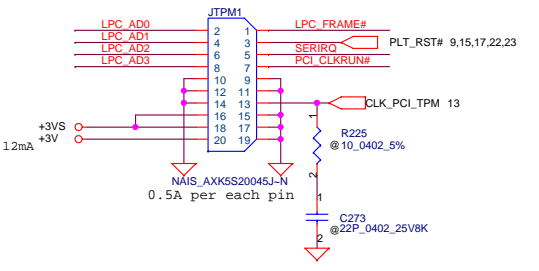
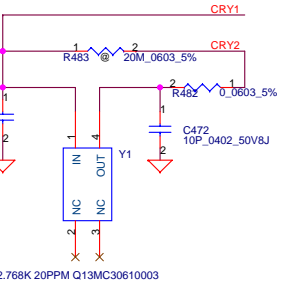
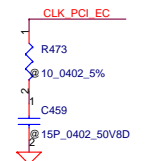


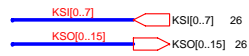
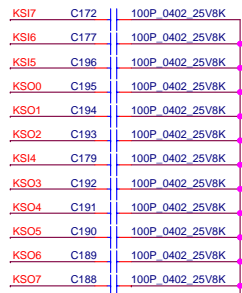
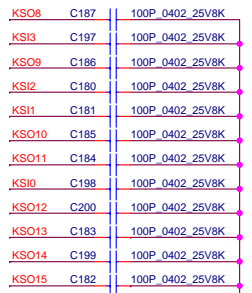


M/B rev:0.1; 0.2; 0.3; 1.0
Voltage:0.0; 0.4; 0.8; 1.0

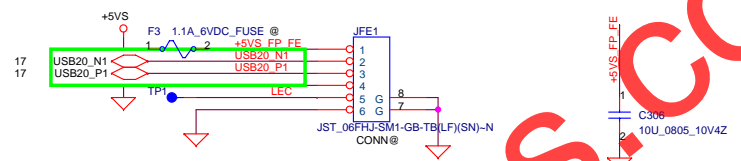


LC2A	KH3
KBSEL0#	SW_CONFIG1
KBSEL1#	SW_CONFIG2
FINGERPRINT#	SW_RS1
	SW_RS2

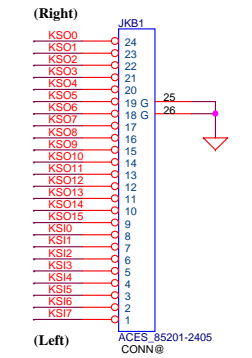




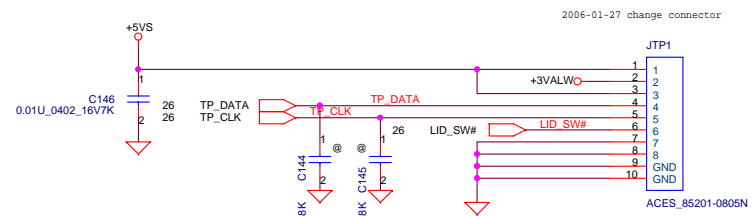
Felica Conn



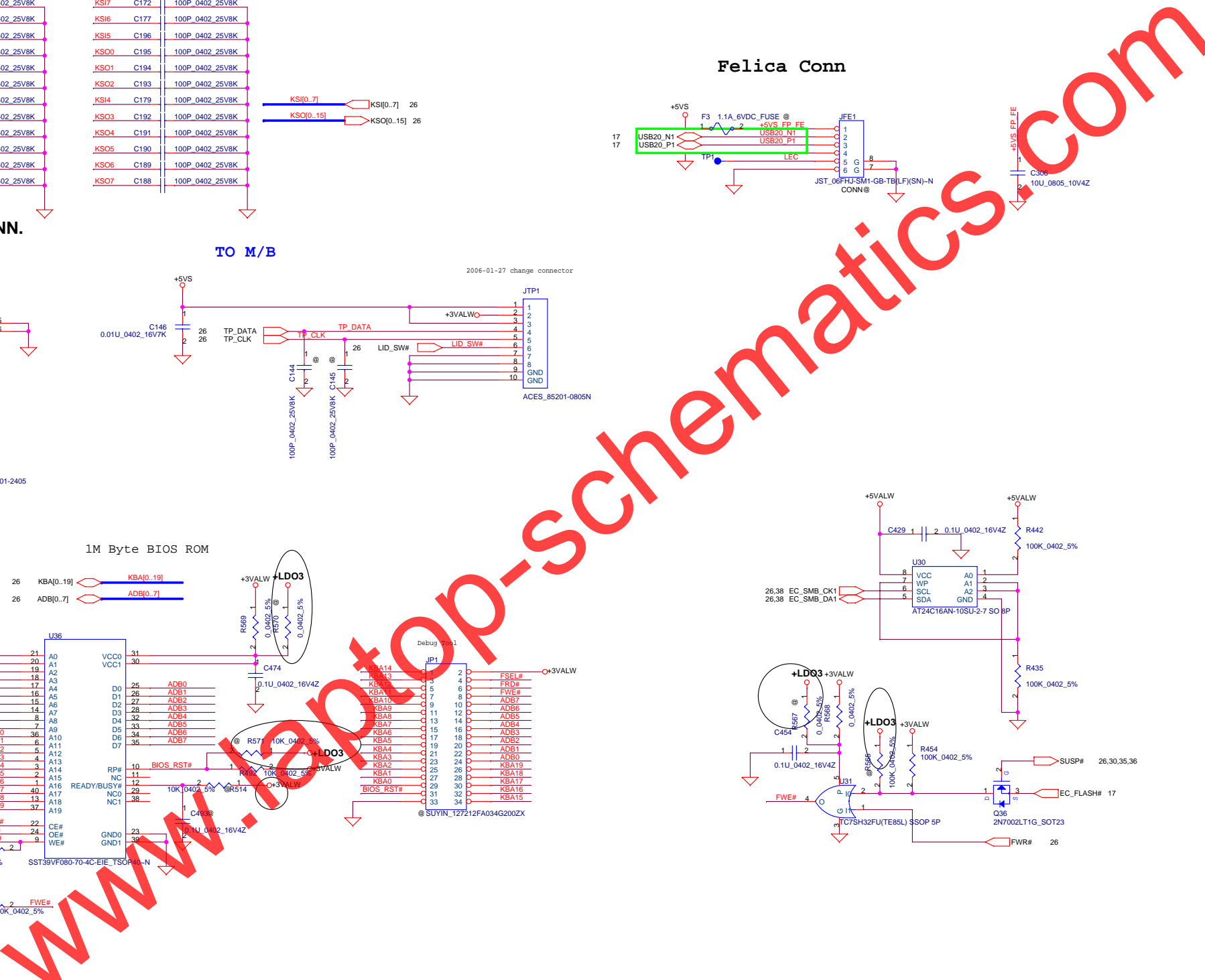
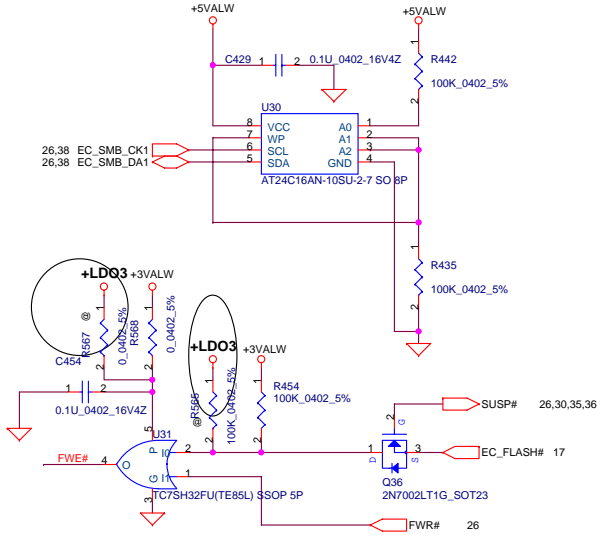
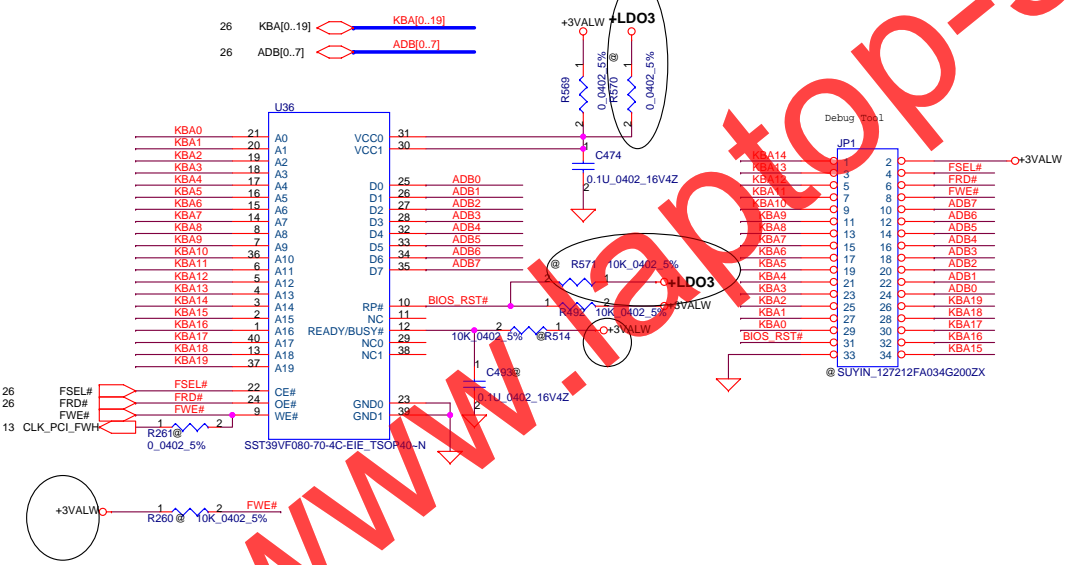
INT_KBD CONN.

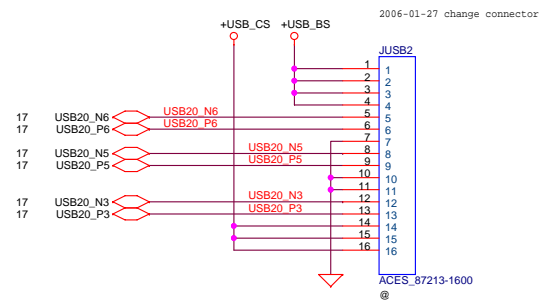
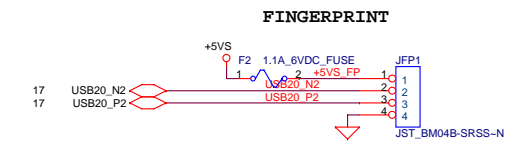
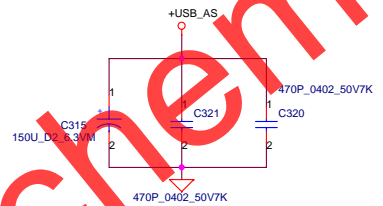
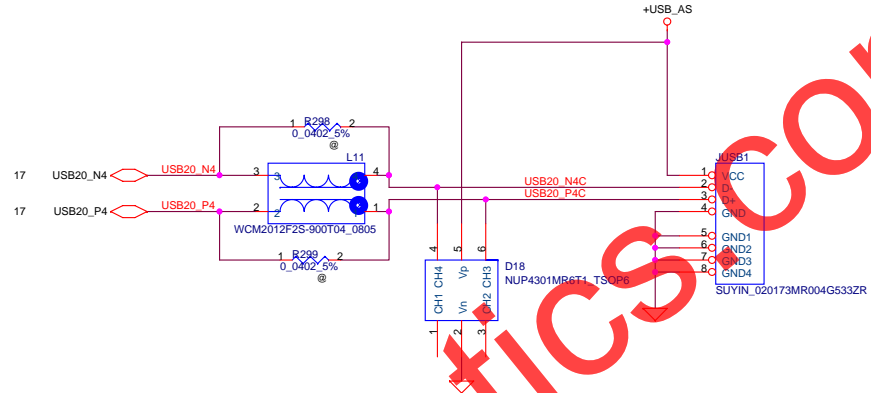
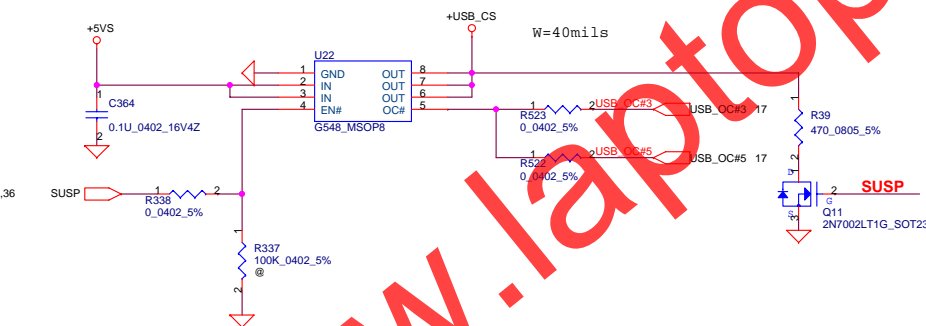
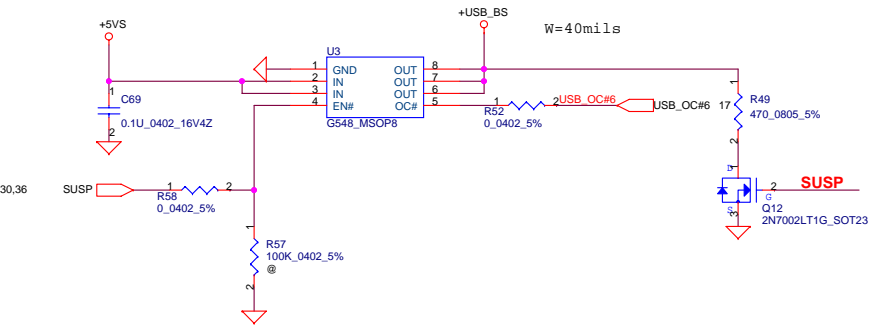
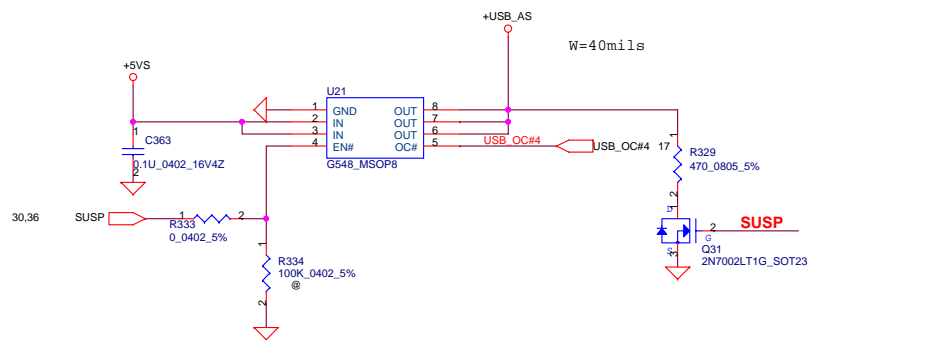


TO M/B



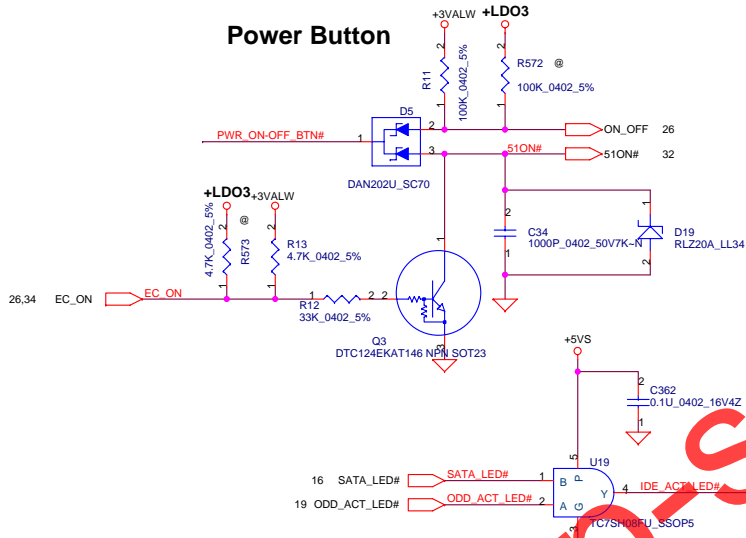
1M Byte BIOS ROM



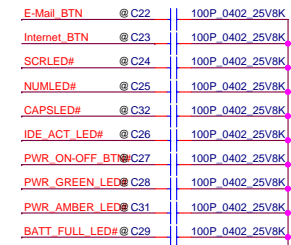
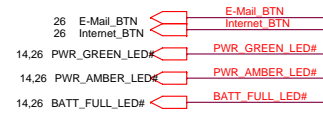
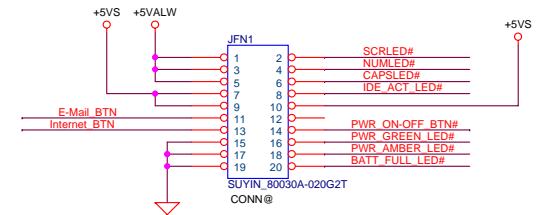
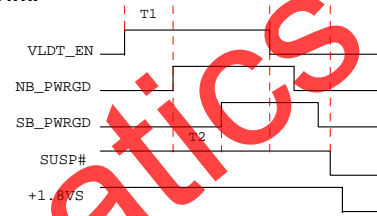


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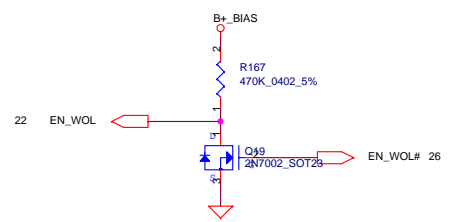
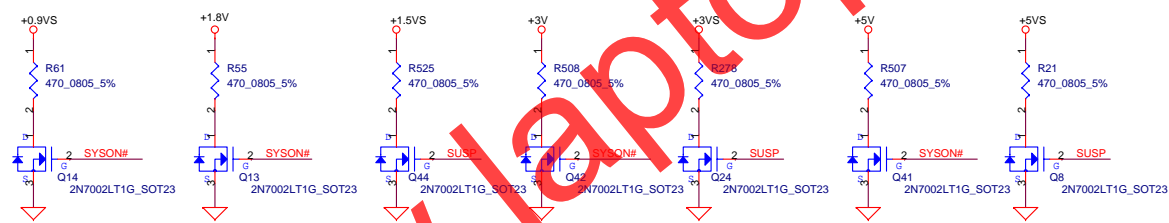
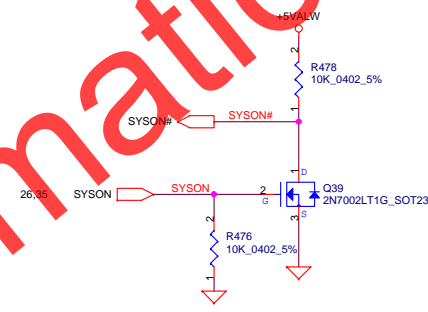
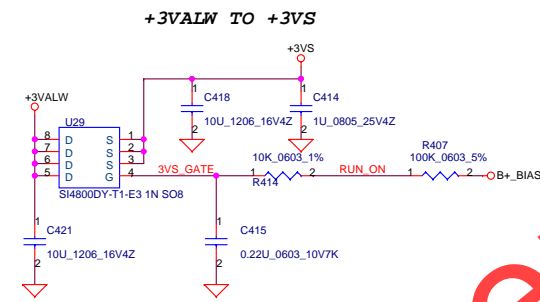
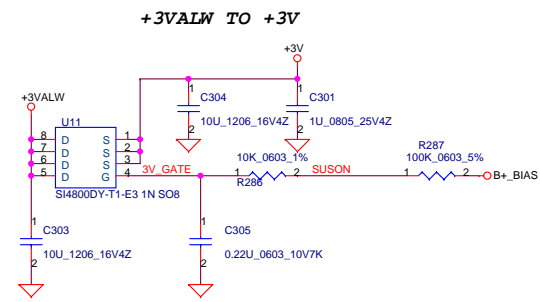
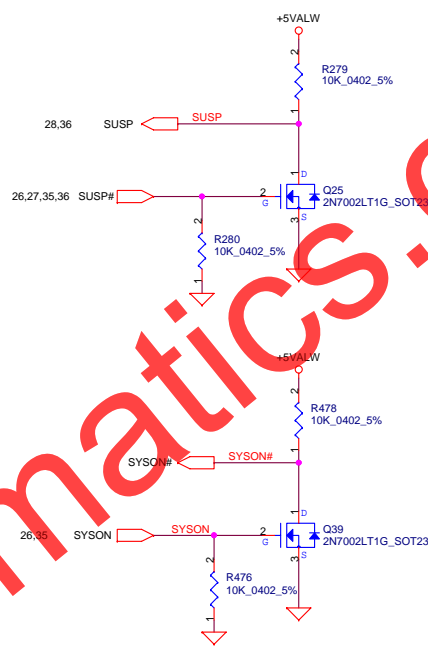
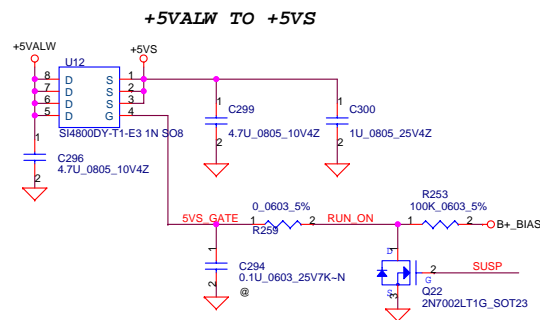
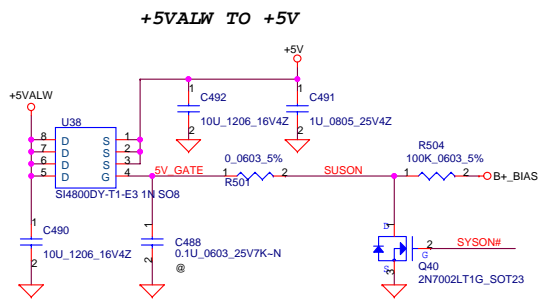
Power Button



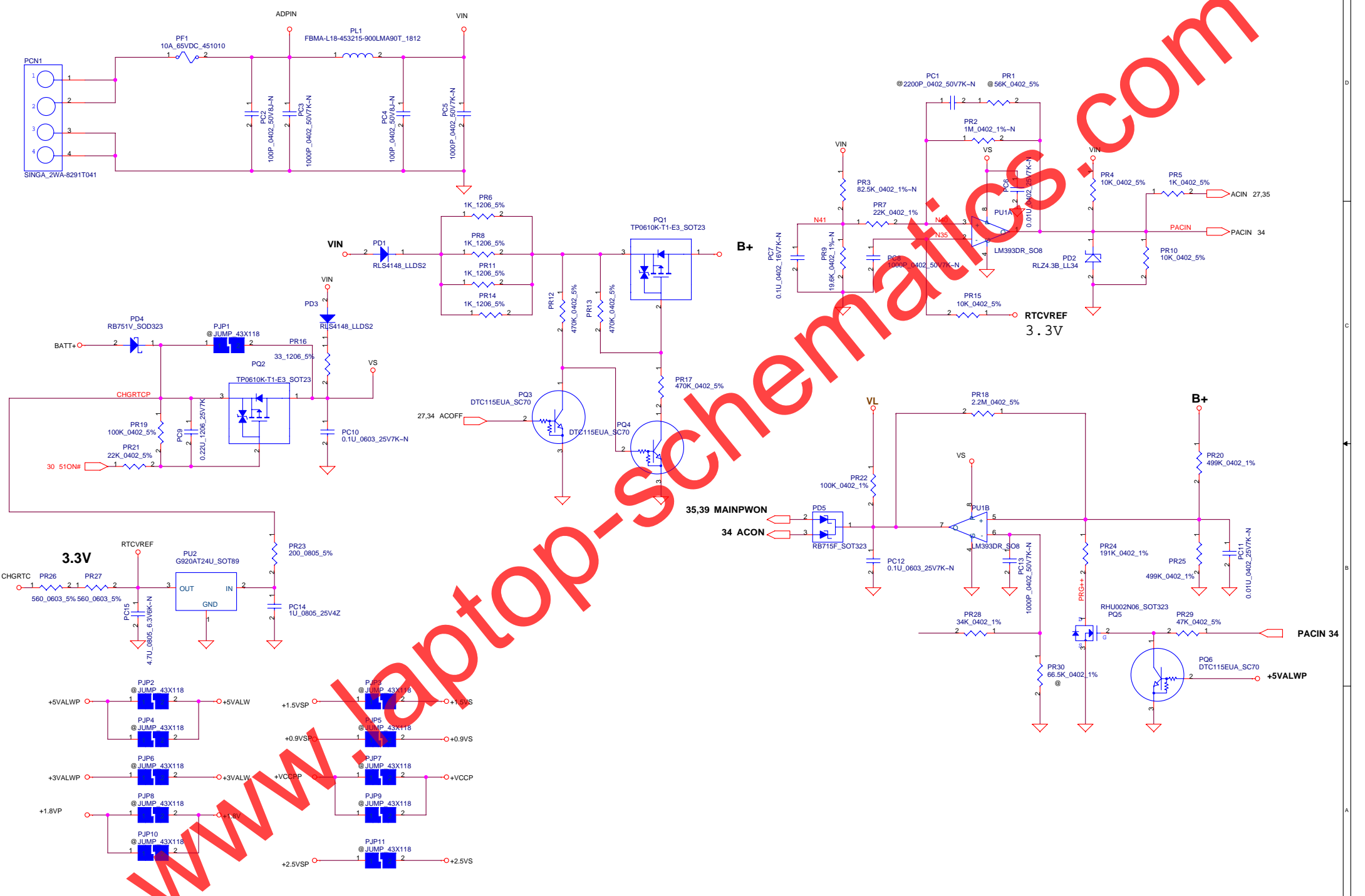
note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power
down.



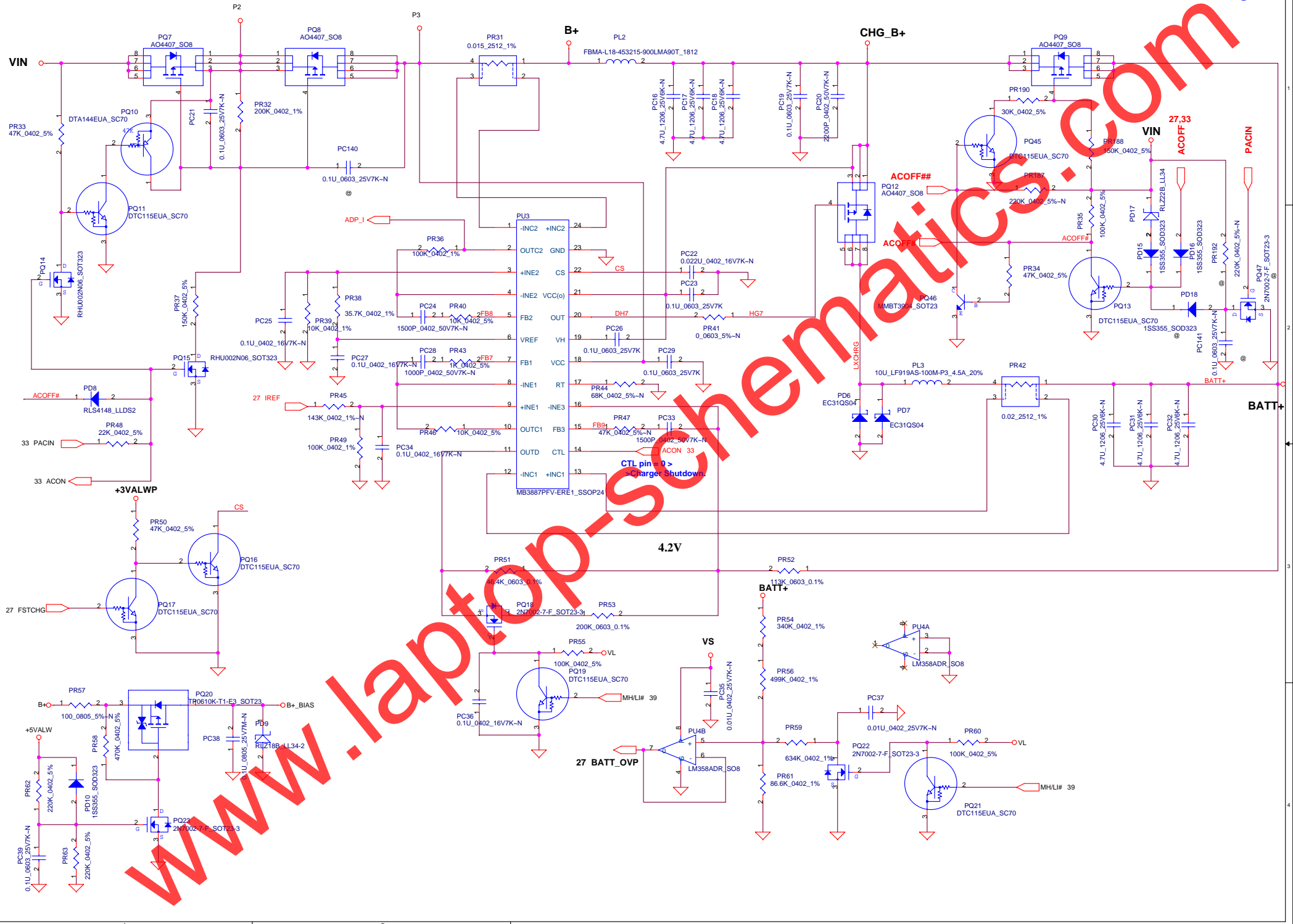
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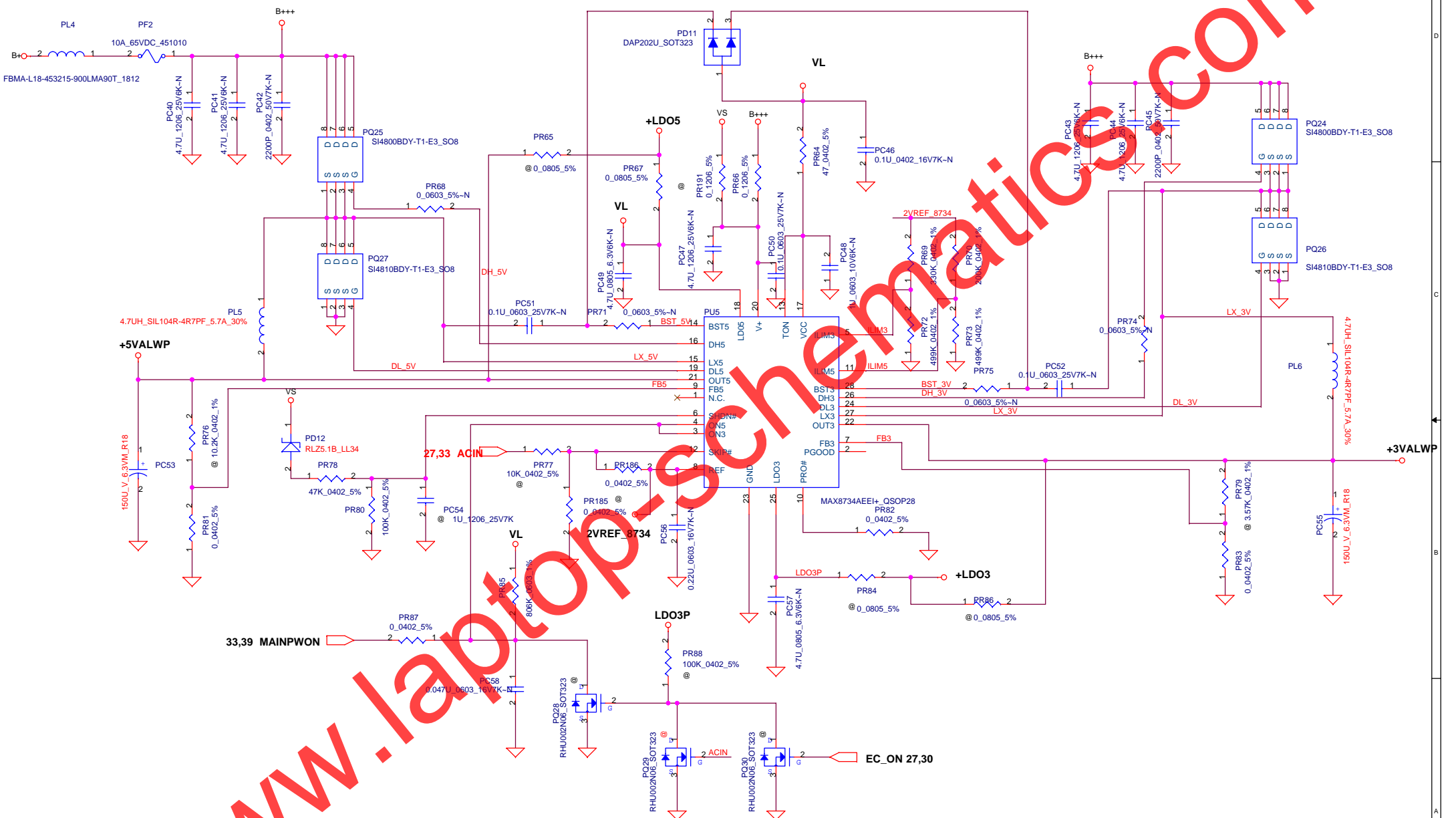


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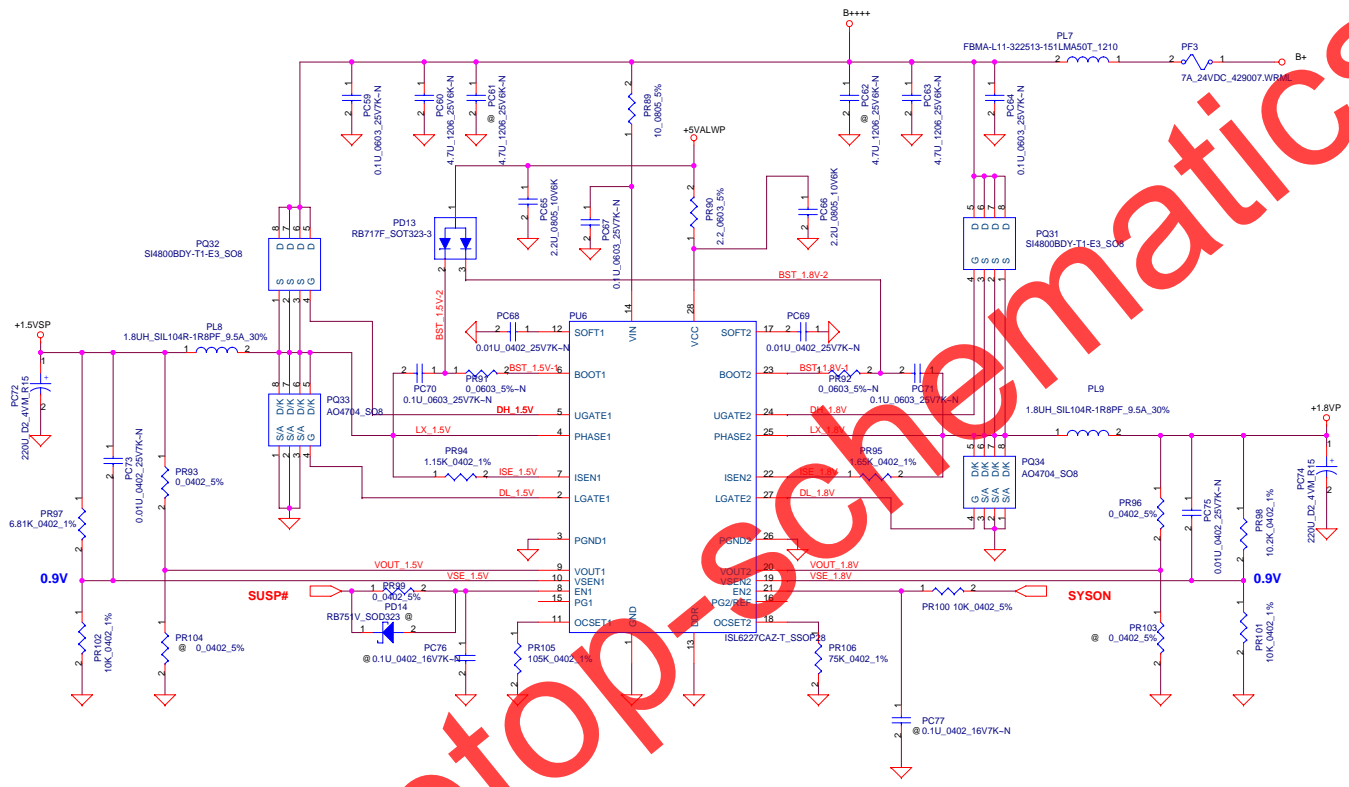
www.laptopSchematics.com

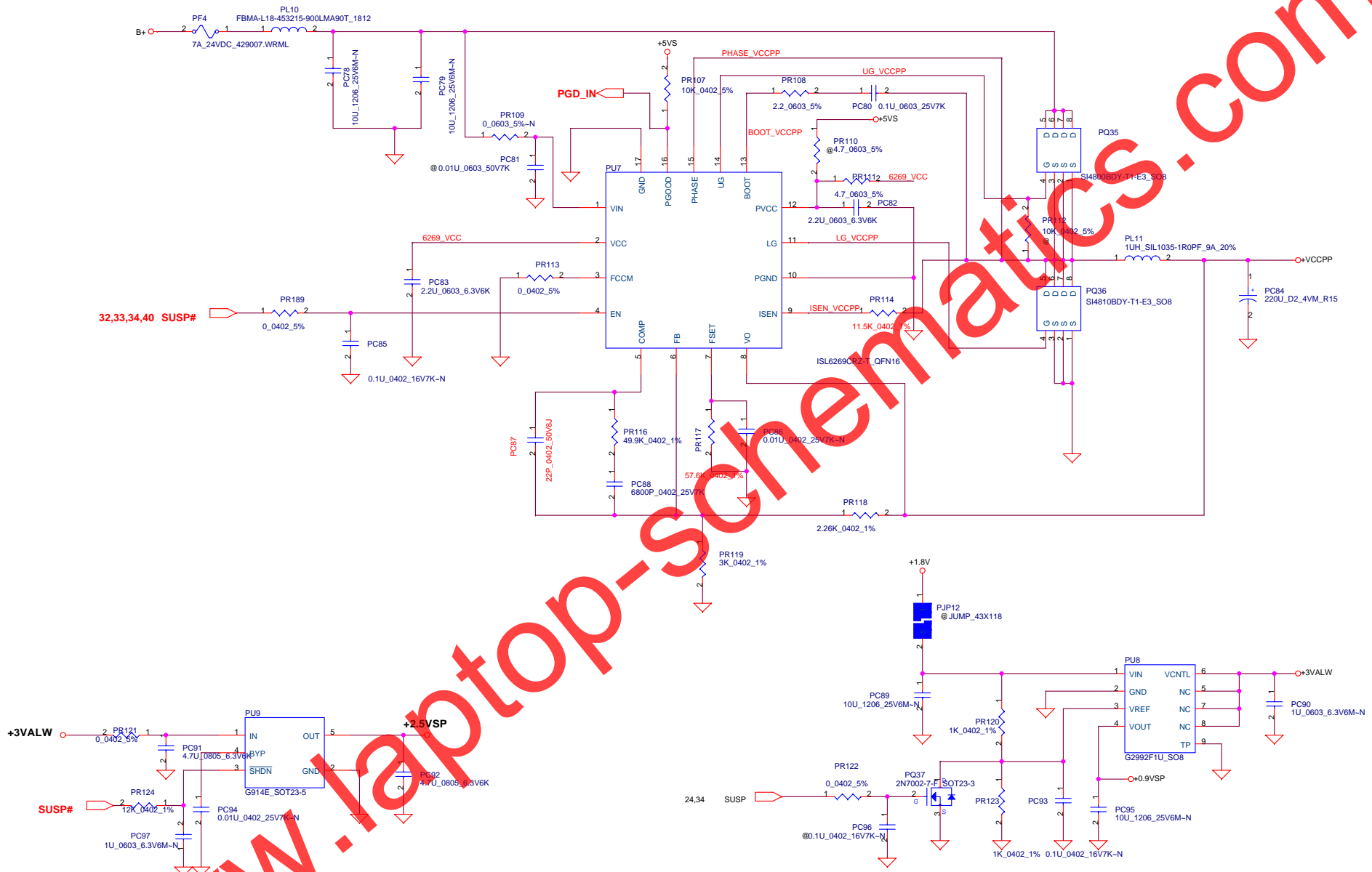
+3.3VALWP/+5VALWP



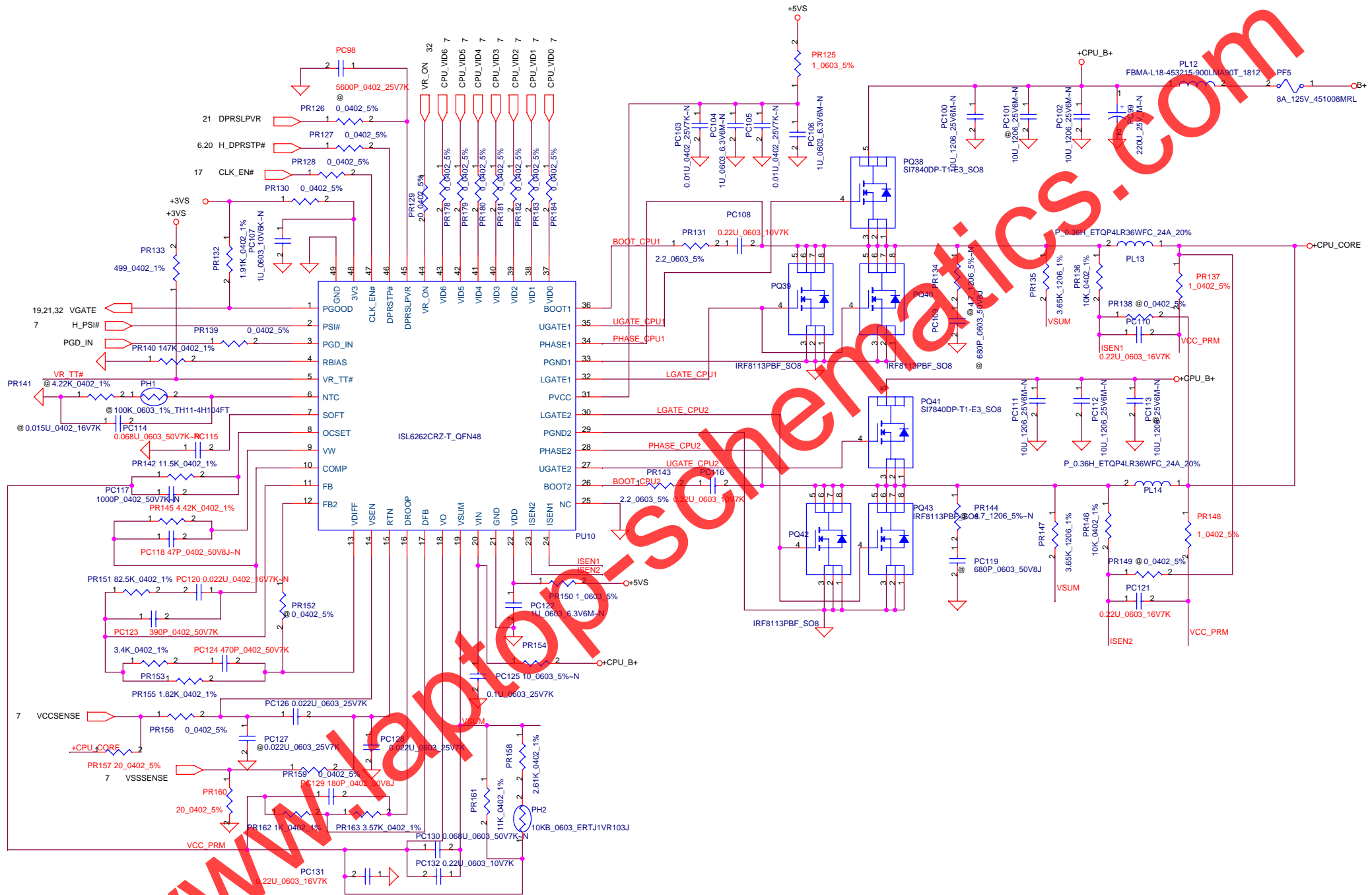
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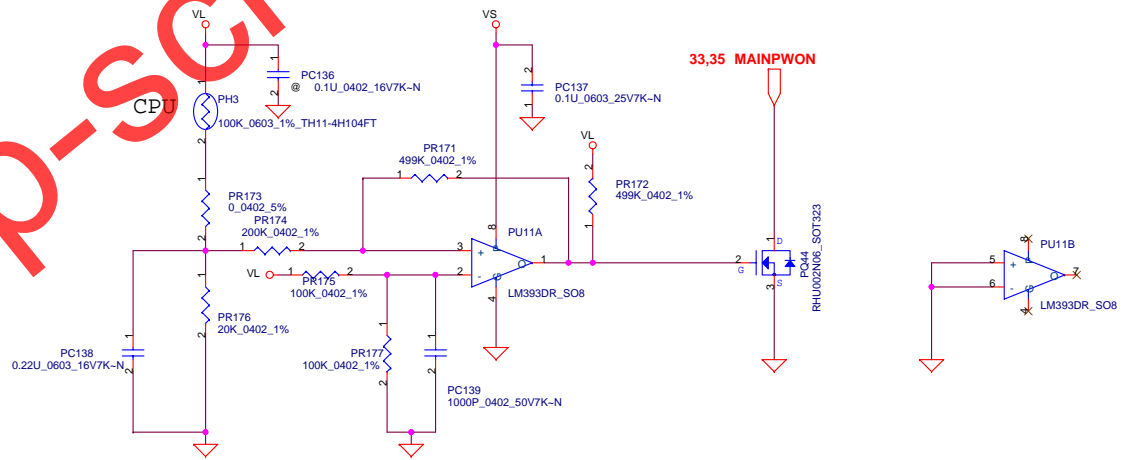
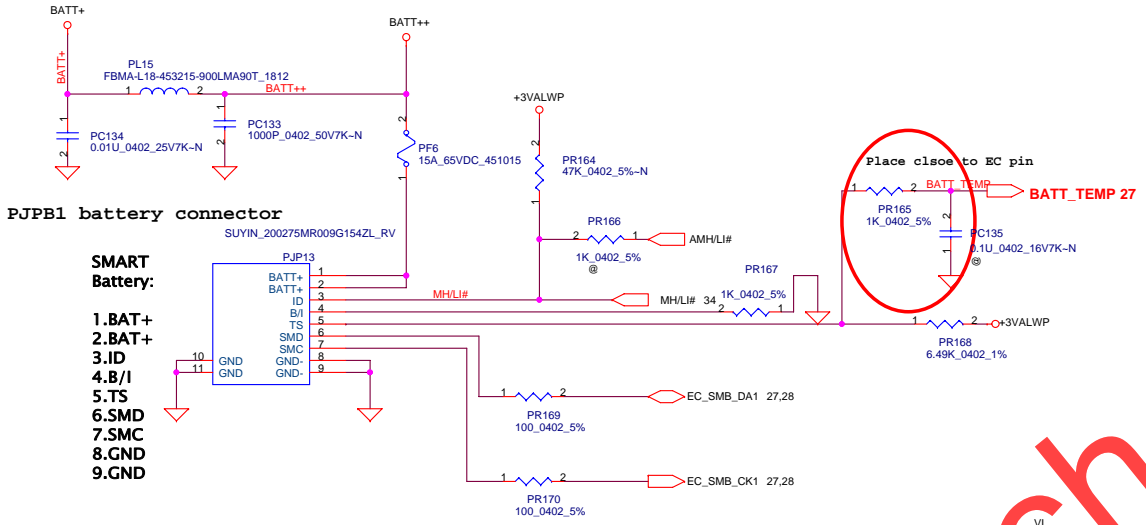


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Battery Connect/OTP



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