

Bond, SP6 BLOCK DIAGRAM

12L HDI

TOP
GND1
IN1
GND2
IN2
GND3
VCC
IN3
GND4
IN4
GND3
BOT

2'nd battery Docking
PAGE 40

SYSTEM CHARGER (ISL6251AHAZ-T)
PAGE 37

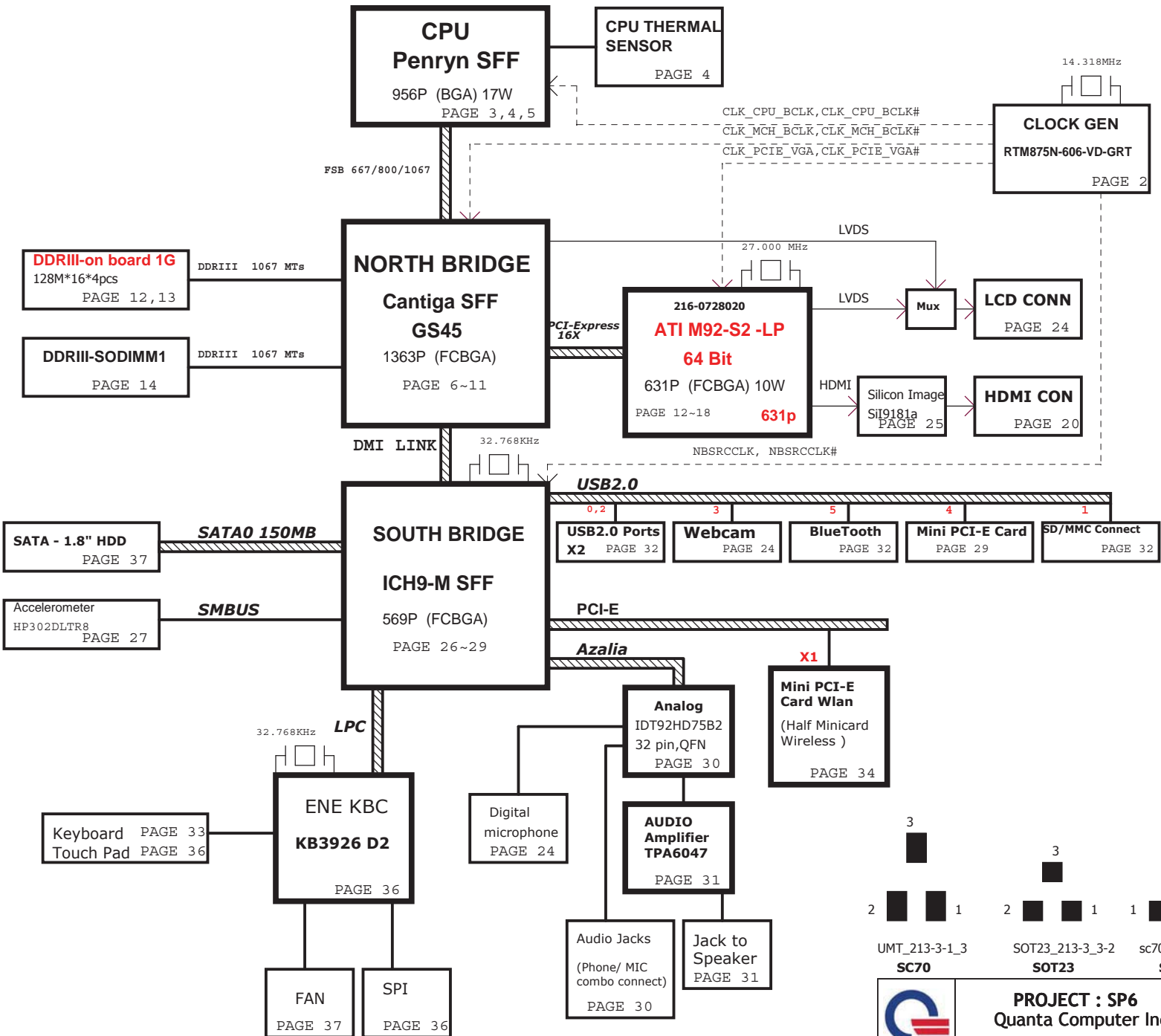
SYSTEM POWER ISL6237IRZ-T
PAGE 38

**DDR II SMD DR_VTERM
1.8V/1.8VSUS(TPS51116REGR)**
PAGE 42

**VCCP +1.5V AND GMCH
1.05V(RT8204)**
PAGE 39

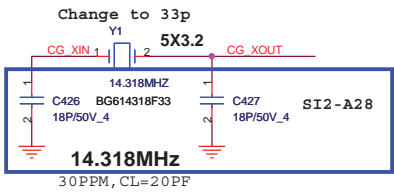
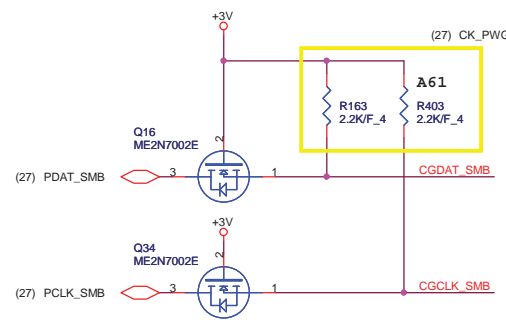
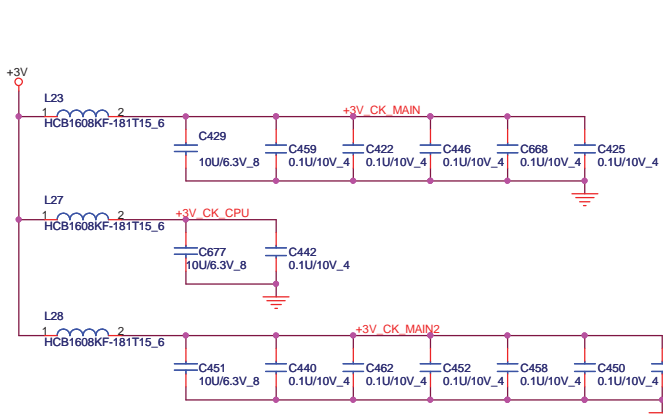
VGACORE(1.025V)Oz8119
PAGE 41

CPU CORE ISL6262A
PAGE 40



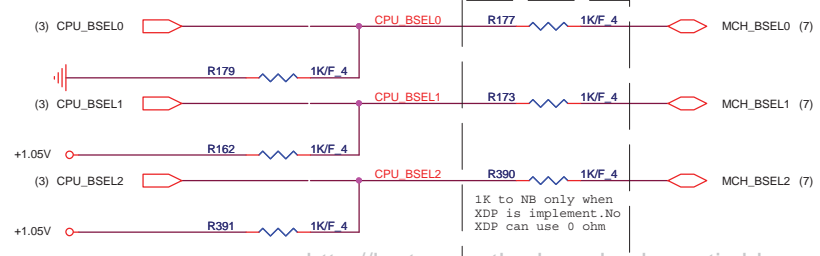
PROJECT : SP6
Quanta Computer Inc.

NB5	Size Custom	Document Number	Rev 1A
	Block Diagram		
Date: Tuesday, April 07, 2009		Sheet 1	of 49



27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

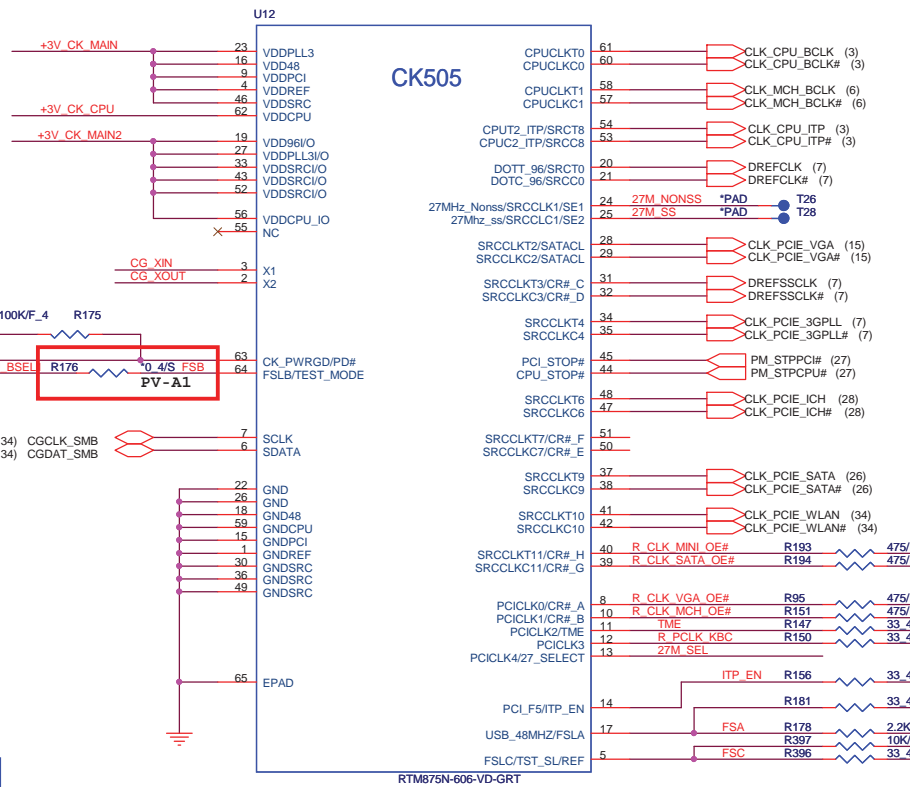
CPU Clock select



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

1K to NB only when XDP is implement. No XDP can use 0 ohm

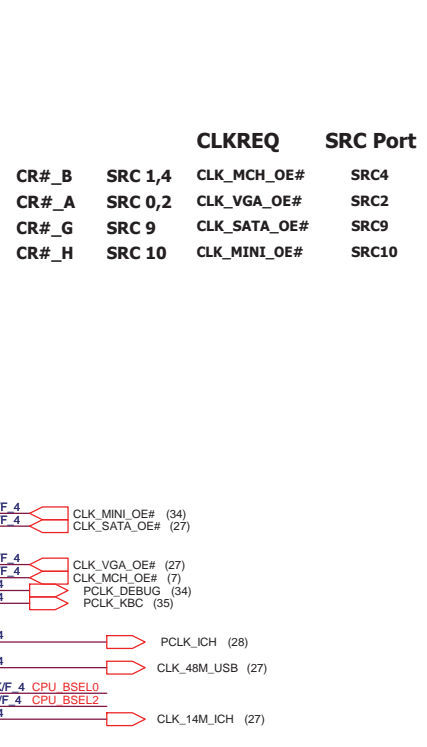
<http://laptop-motherboard-schematic.blogspot.com/>



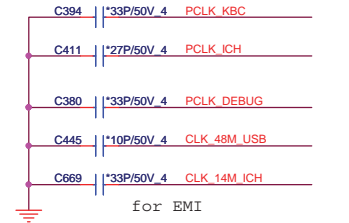
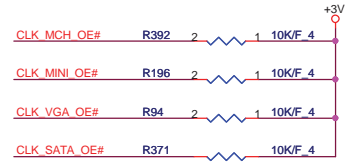
CK505
Realtek
Silego

QFN64

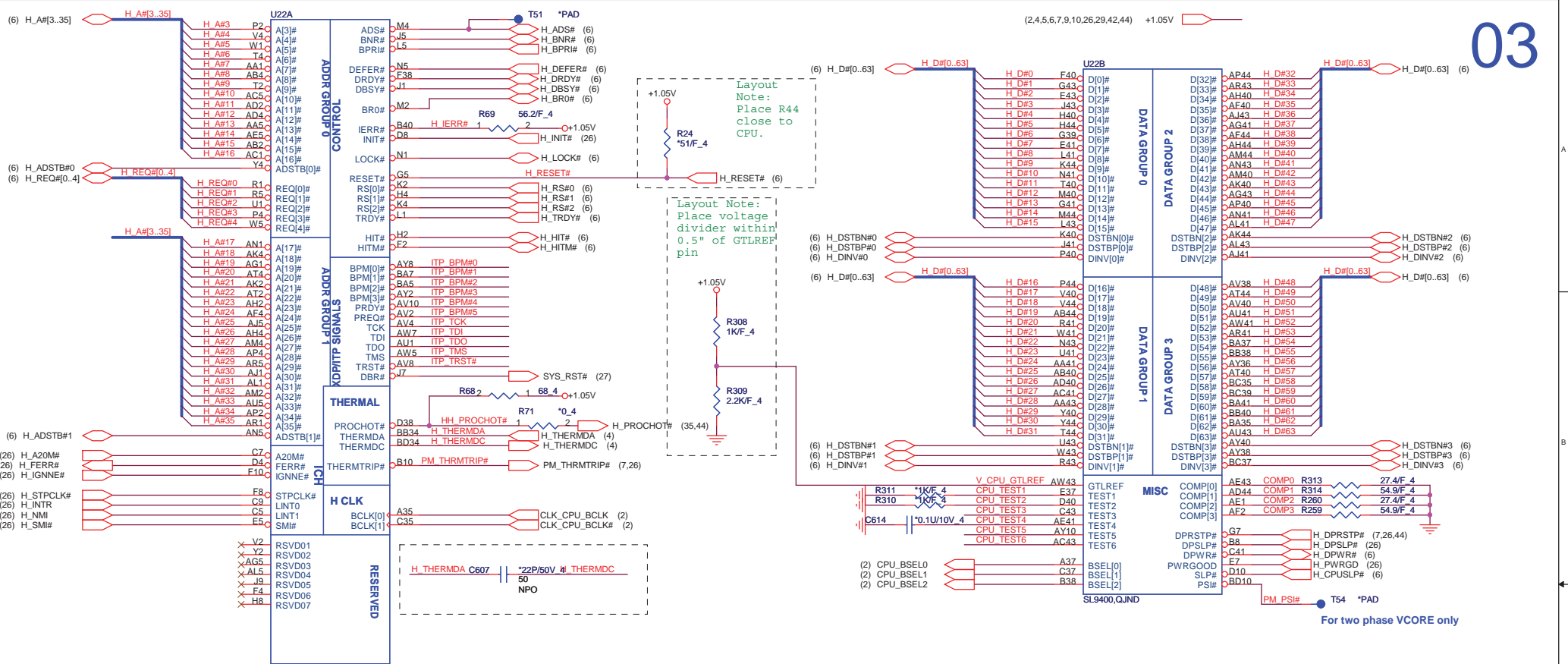
RTM875N-606-VD-GR AL000875000
SLG8SP513VTR AL8SP513000



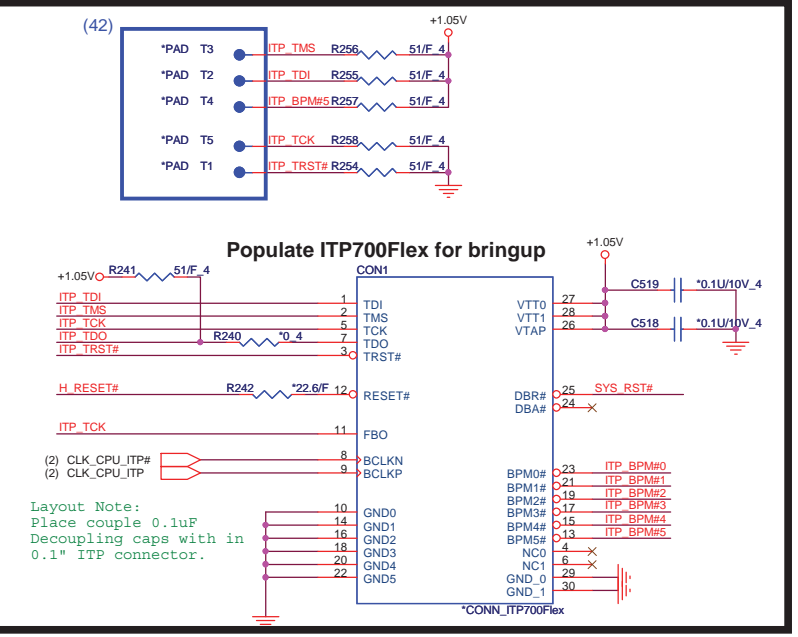
CR#	SRC	CLKREQ	SRC Port
CR#_B	SRC 1,4	CLK_MCH_OE#	SRC4
CR#_A	SRC 0,2	CLK_VGA_OE#	SRC2
CR#_G	SRC 9	CLK_SATA_OE#	SRC9
CR#_H	SRC 10	CLK_MINI_OE#	SRC10



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- SL9400: AJSLB66UT01 CPU(956P)PENRYN 1.86G SLB66(FCBGA)TOPB/S
- SL9400: AJSLB66UT02 CPU(956P)PENRYN 1.86G SLB66(FCBGA)
- SL9600: AJSLGEQUT01 CPU(956P)PENRYN 2.13G SLGEQ(BGA)TOPB/S
- SL9600: AJSLGEQUT00 CPU(956P)PENRYN 2.13G SLGEQ(BGA)



Signal | ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TMS	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TCK	680 ohm +/- 5%	VTT	Within 2.0" of the ITP
TDO	27 ohm +/- 5%	OpenGND	Within 2.0" of the ITP
ITP_EN	R268 Depop	VTT	Within 2.0" of the ITP
		+3VRUN	Close to CK410M Pin8

*PAD T78 CPU TEST3
 *PAD T53 CPU TEST5
 *PAD T77 CPU TEST6

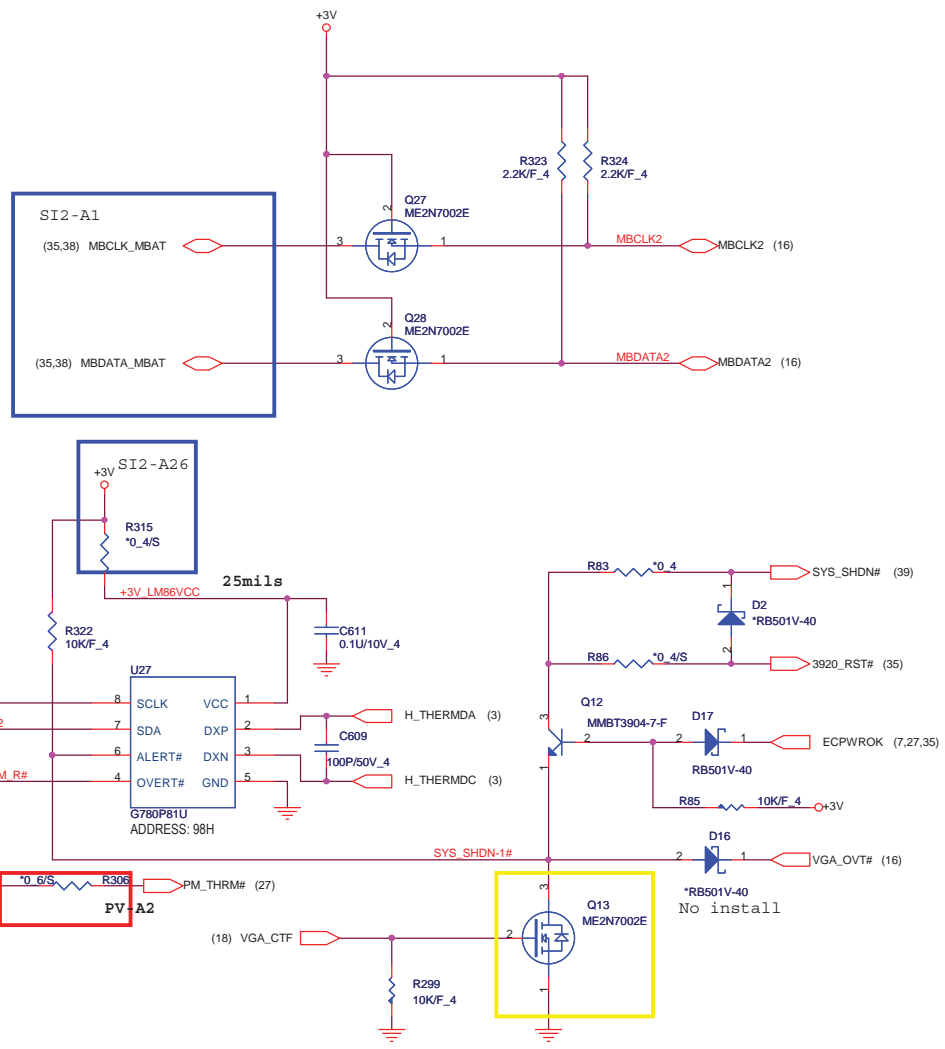
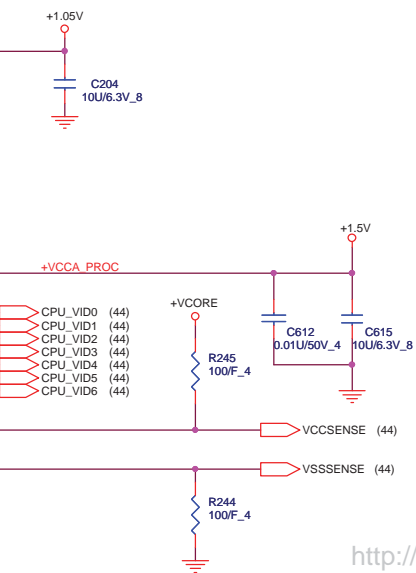
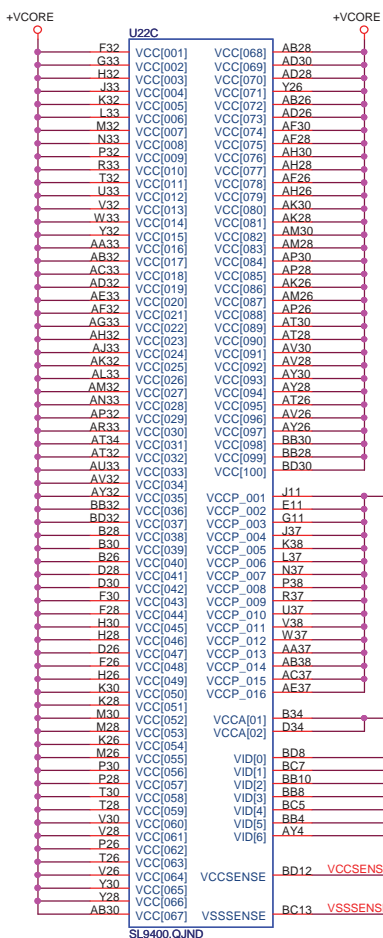
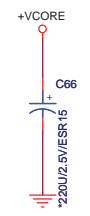
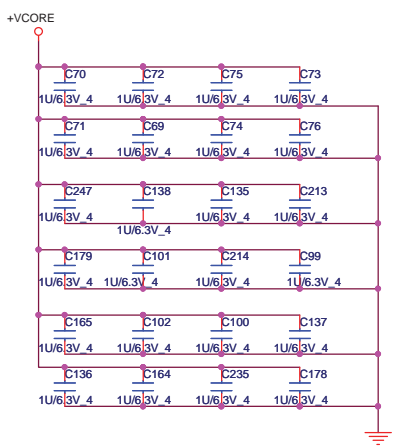
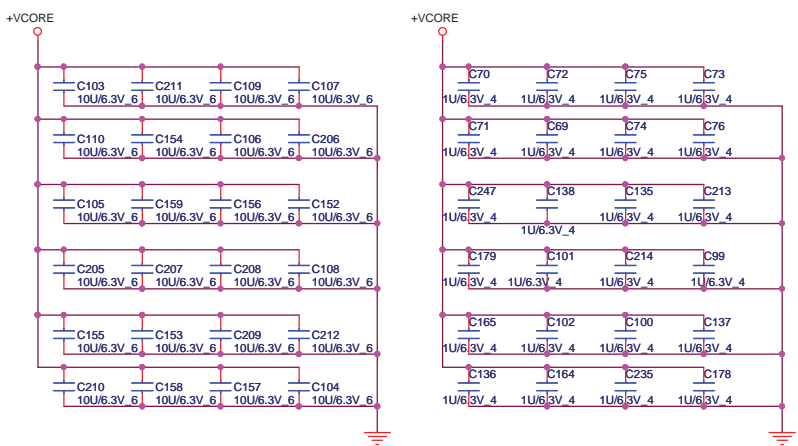
For the purpose of testability, route these signals through a ground referenced Z0 - 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

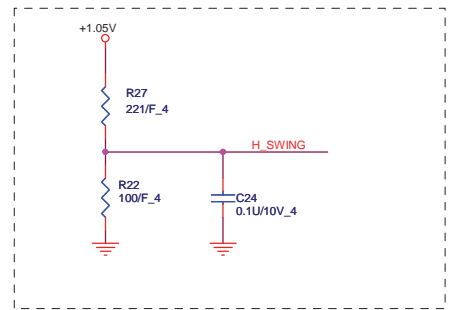
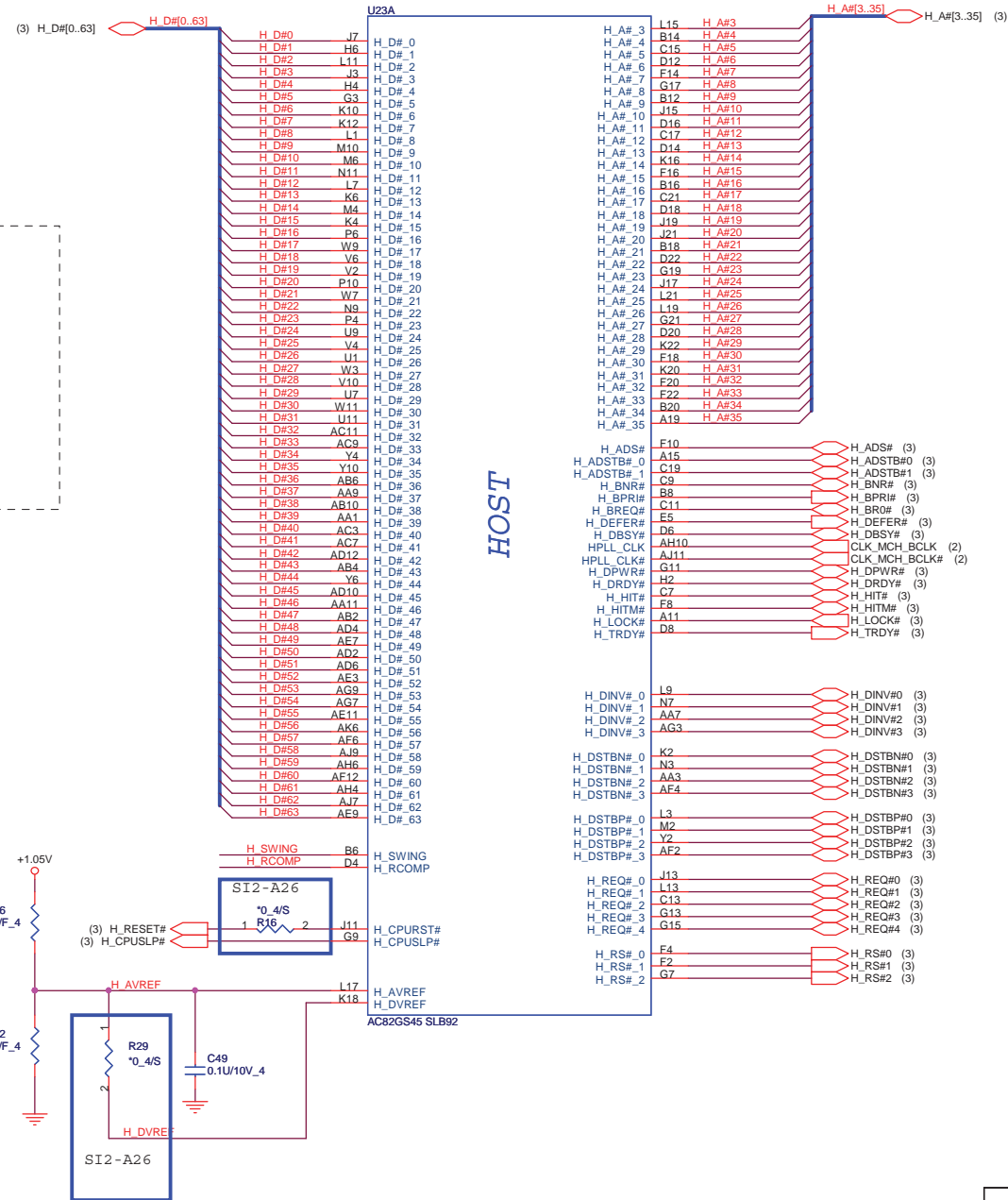
PROJECT : SP6
Quanta Computer Inc.

NBS

Size Custom | Document Number Penryn (HOST BUS) 1/3 | Rev 1A

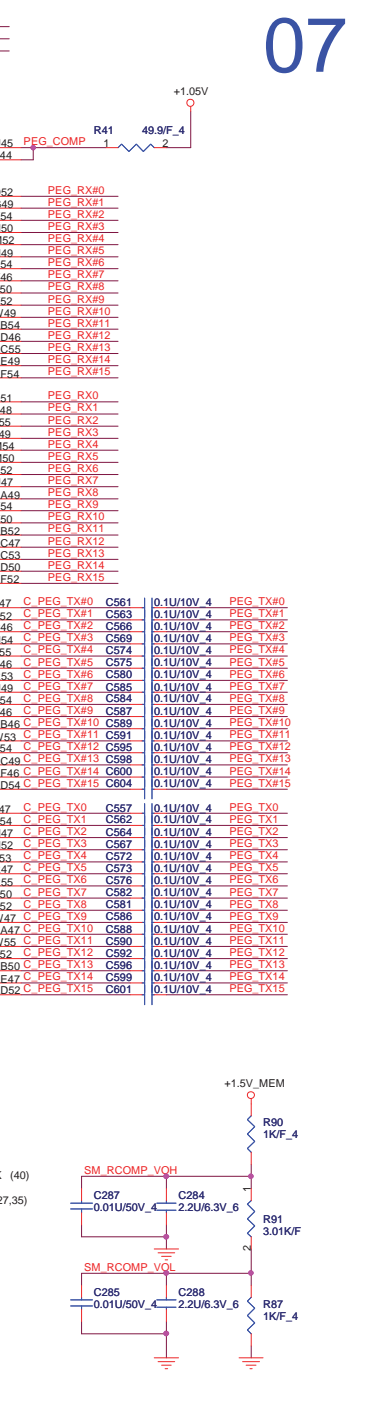
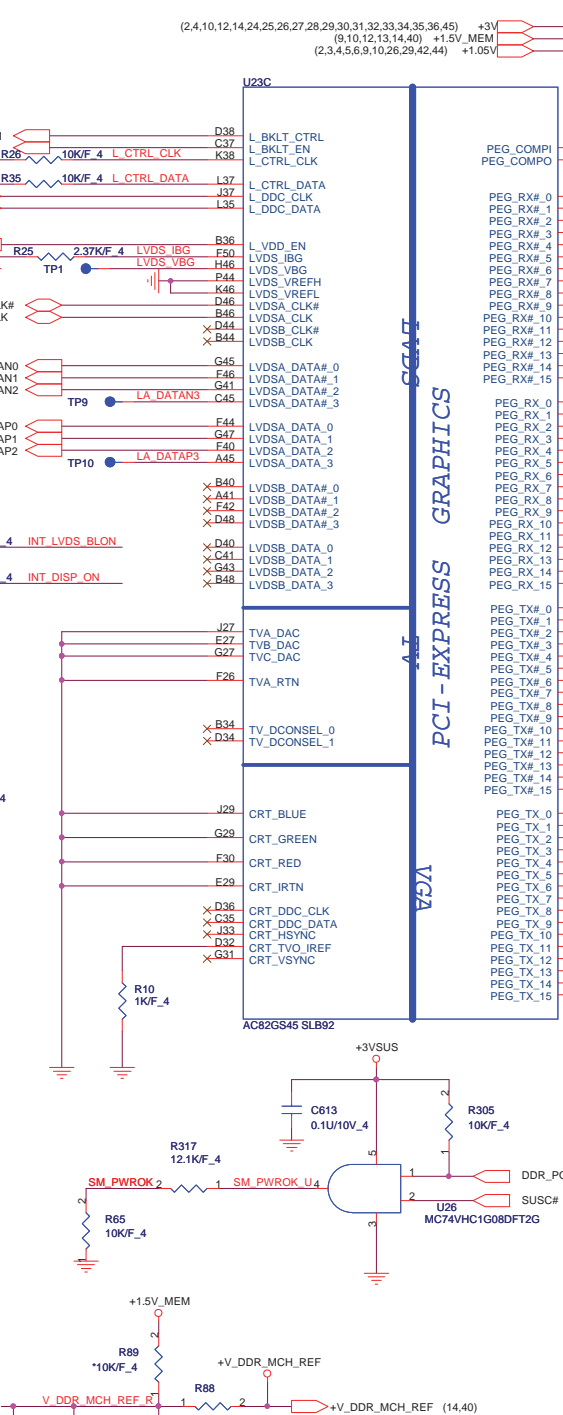
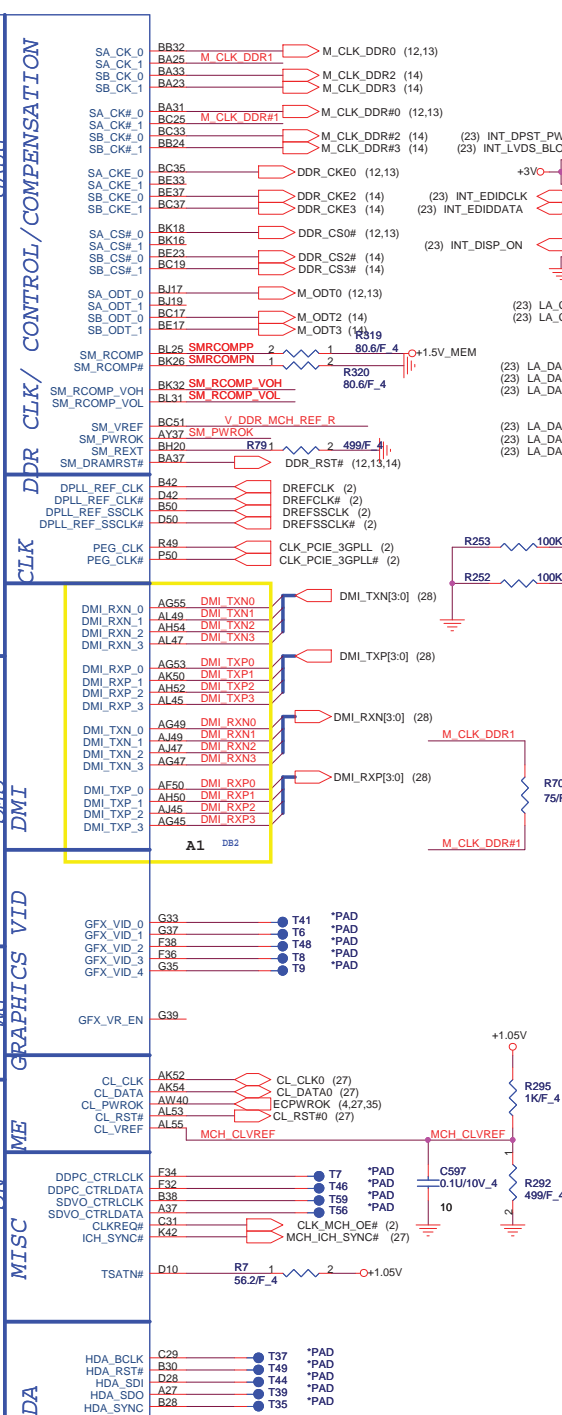
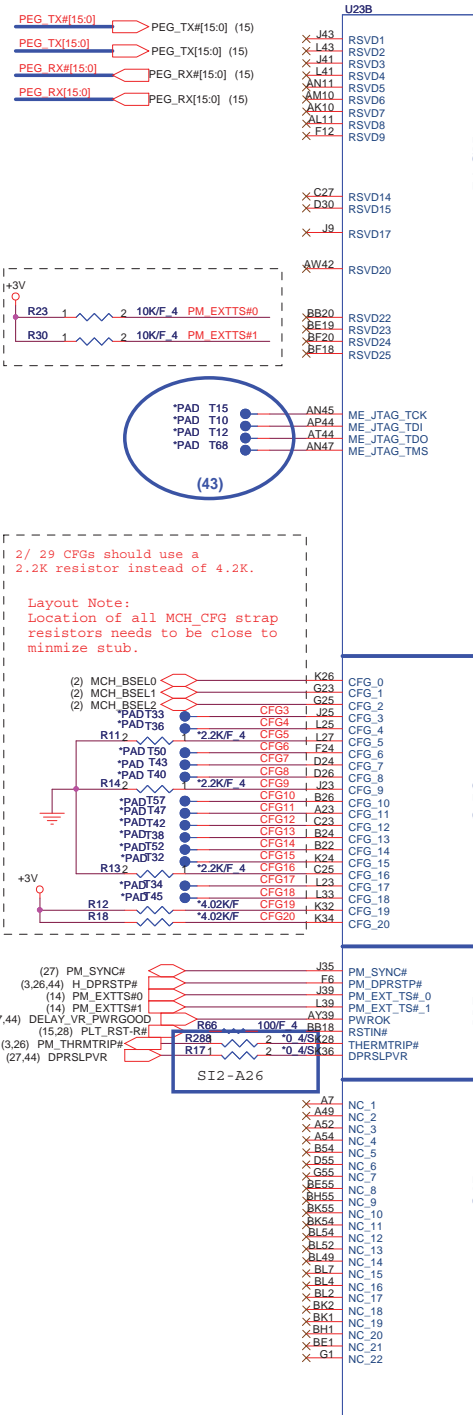
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Layout Note:
H_RCAMP trace should be
10-mil wide with 20-mil
spacing.

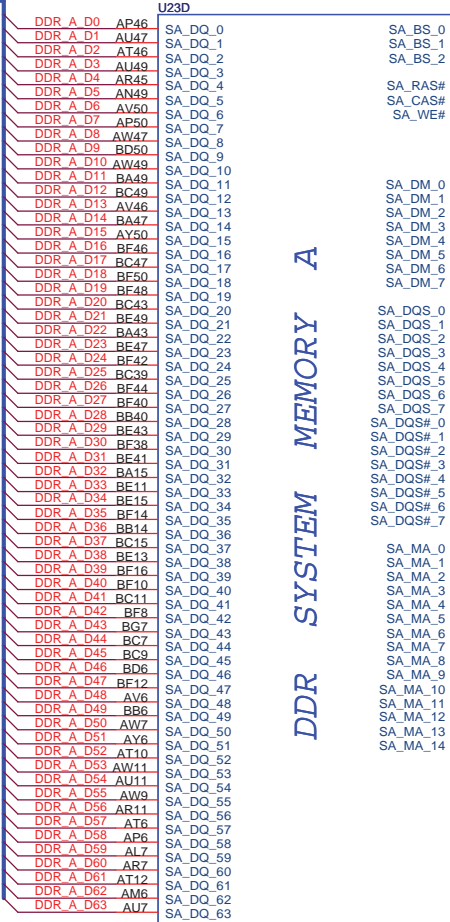
	PROJECT : SP6 Quanta Computer Inc.	
	Size Custom	Document Number Cantiga hot
Date: Tuesday, April 07, 2009		Sheet 6 of 49



PROJECT : SP6
Quanta Computer Inc.

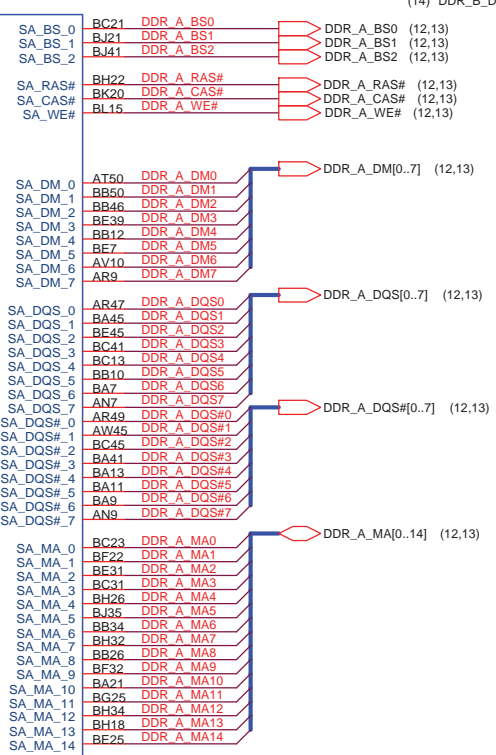
Size Custom Document Number Cantiga (VGA/DMI) Rev 1A
 Date: Tuesday, April 07, 2008 Sheet 7 of 49

(12,13) DDR_A_D[0..63]

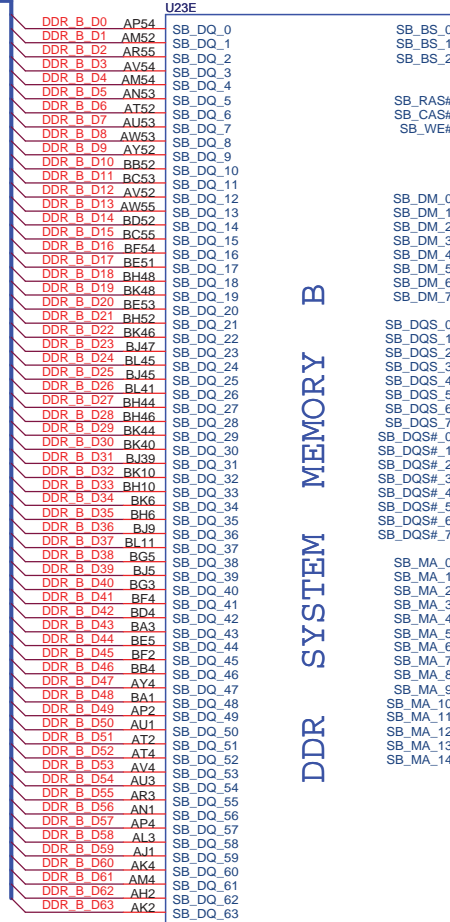


AC82GS45 SLB92

DDR SYSTEM MEMORY A

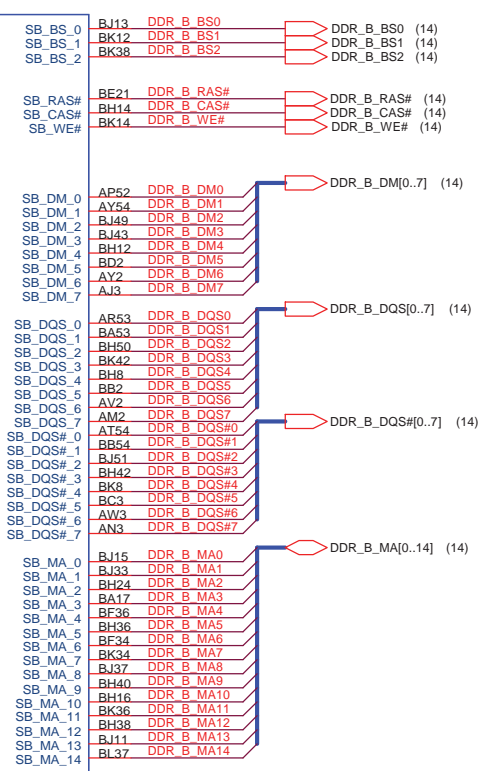


(14) DDR_B_D[0..63]



AC82GS45 SLB92

DDR SYSTEM MEMORY B

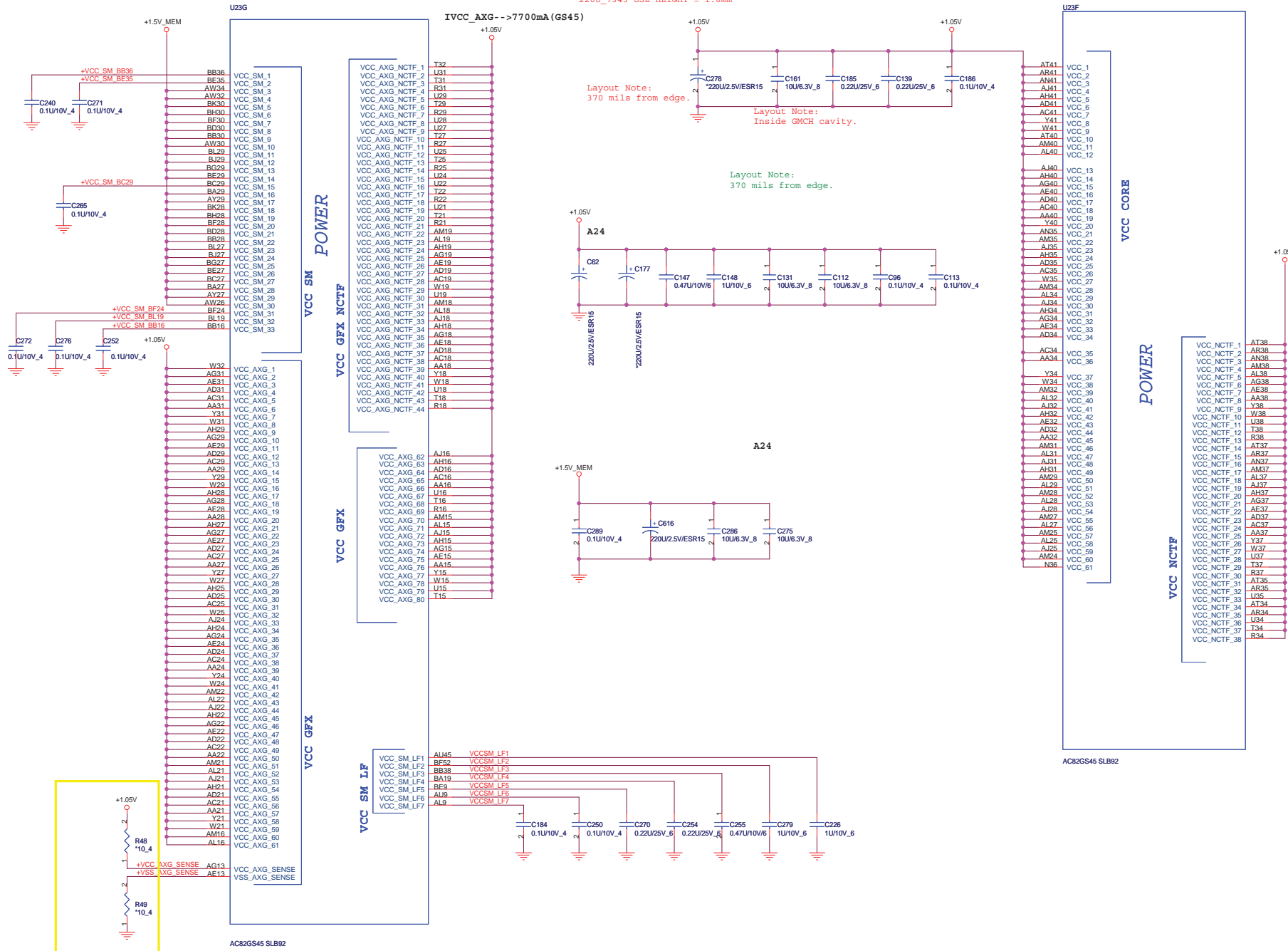


	PROJECT : SP6		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number Cantiga (DDR interface)	
Date: Tuesday, April 07, 2009		Sheet 8 of 49	

Ivcc_gm (DDR3, 1.5V, 1066MTs) -->4140mA

220U_7343 USE HEIGHT = 1.8mm

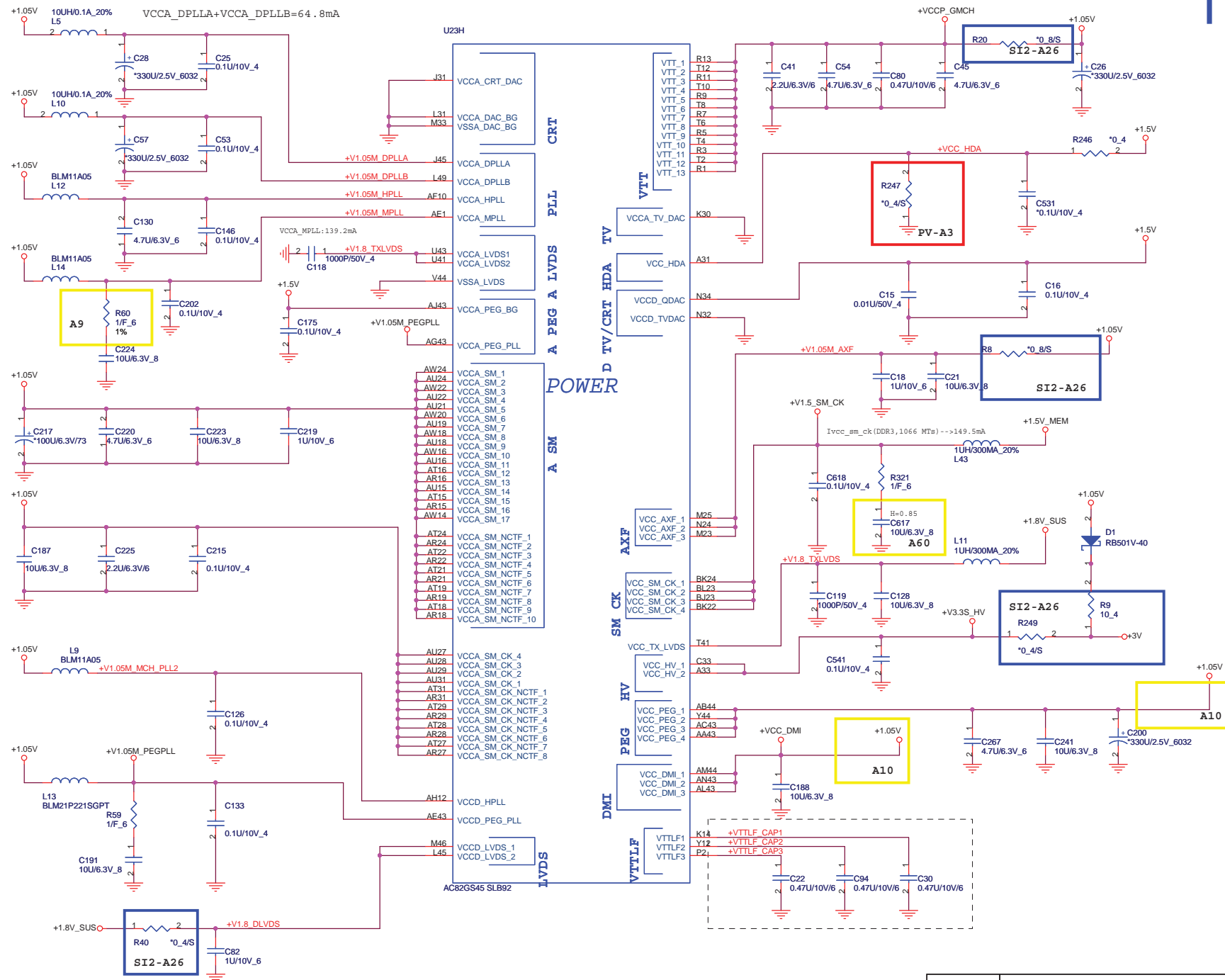
IVCC_AXG-->7700mA (GS45)




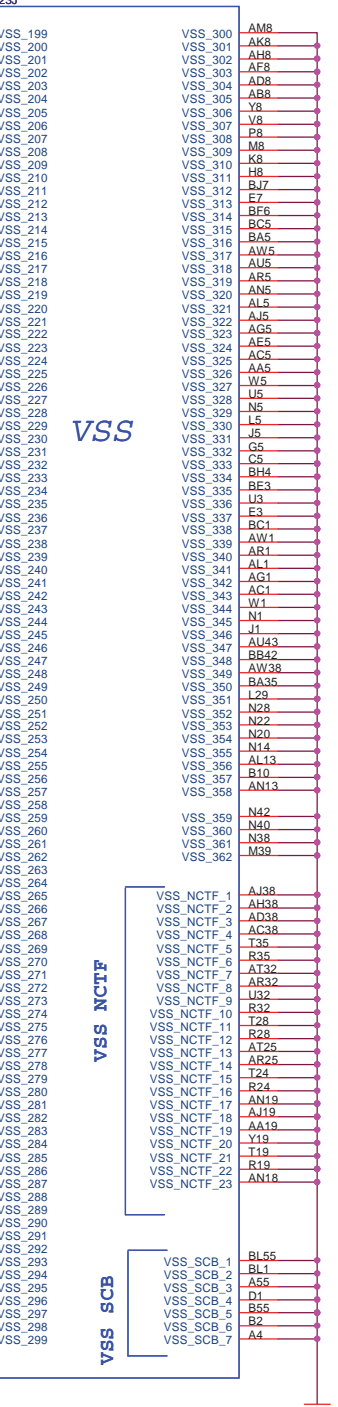
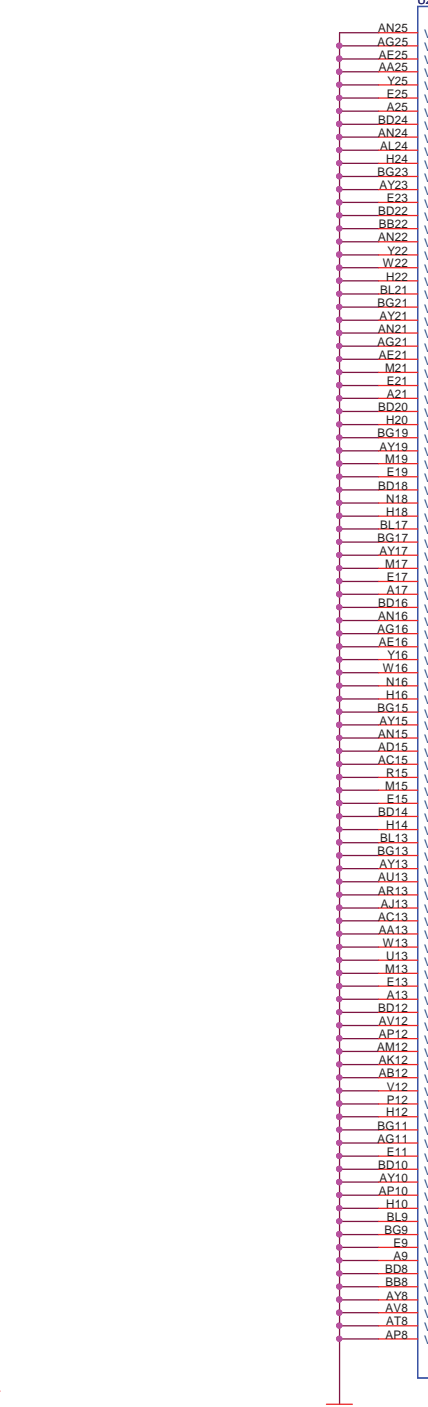
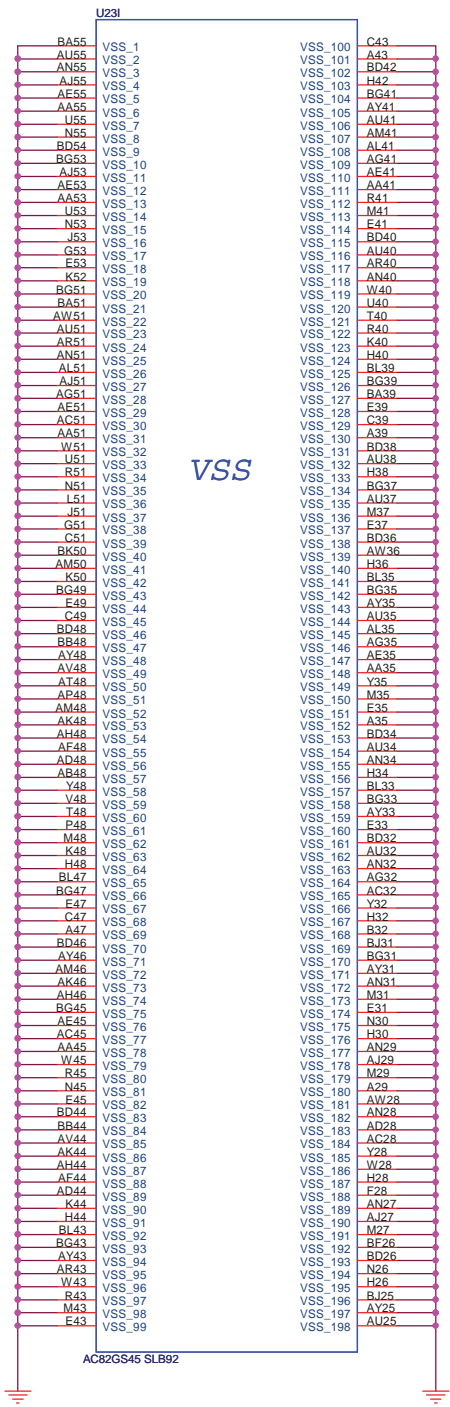
ACR2GS45 SLB92

render standby feature is not implemented can be left

	PROJECT : SP6		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number Cantiga (Vcc)	
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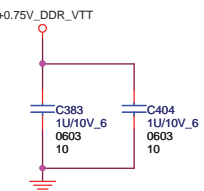
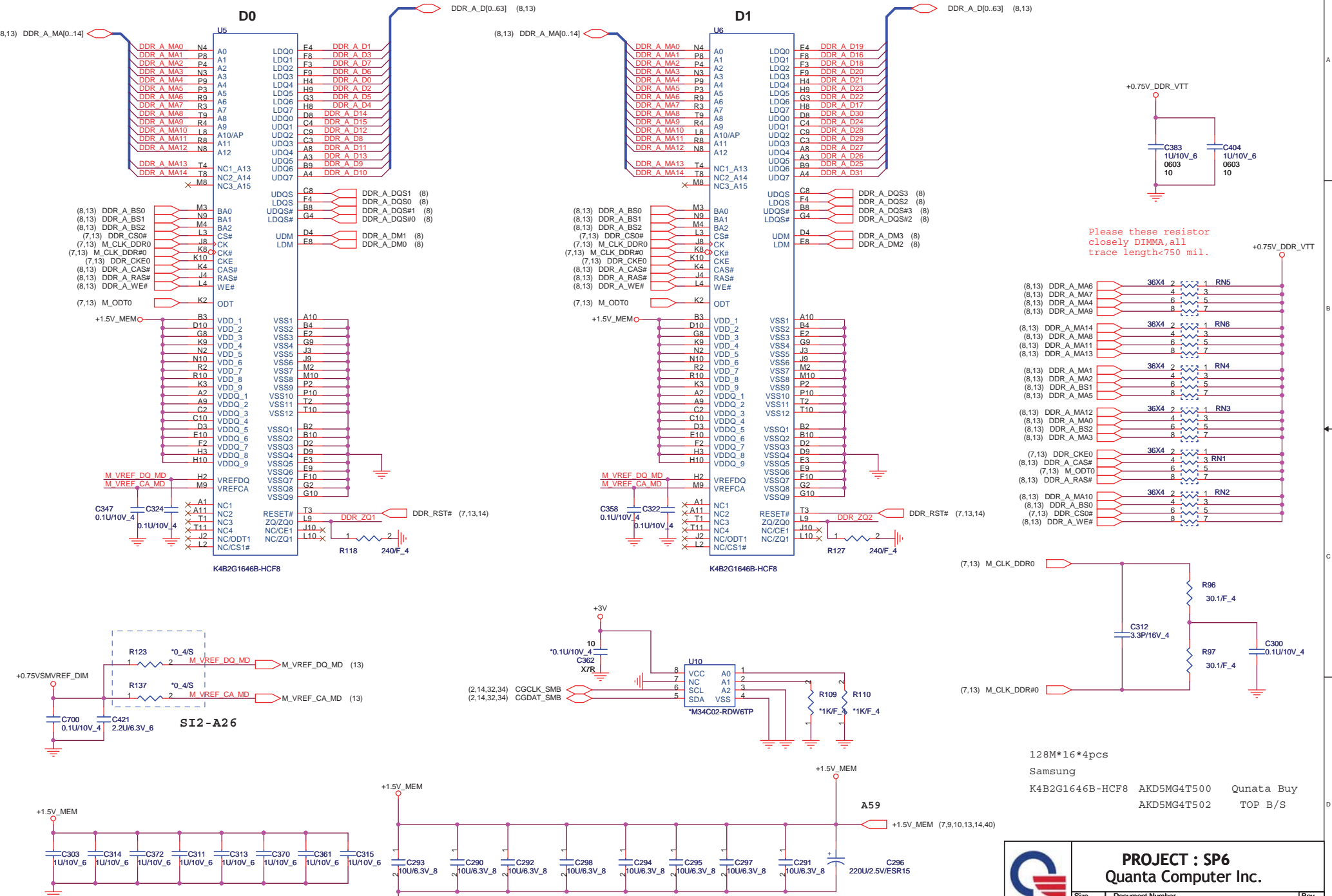
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	Size Custom Document Number Cantiga (Power)	Rev 1A
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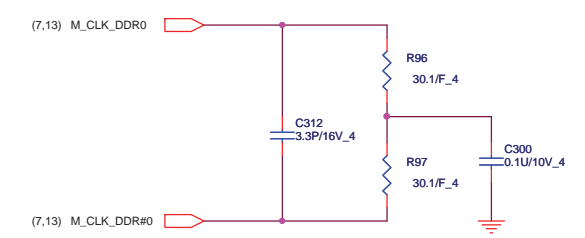
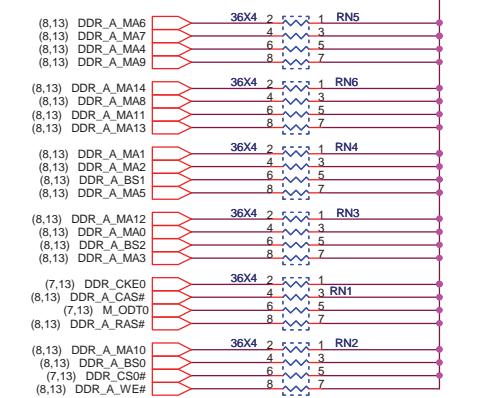
PROJECT : SP6
Quanta Computer Inc.

Size Custom	Document Number Cantiga (Vss)	Rev 1A
Date: Tuesday, April 07, 2009	Sheet 11 of 49	

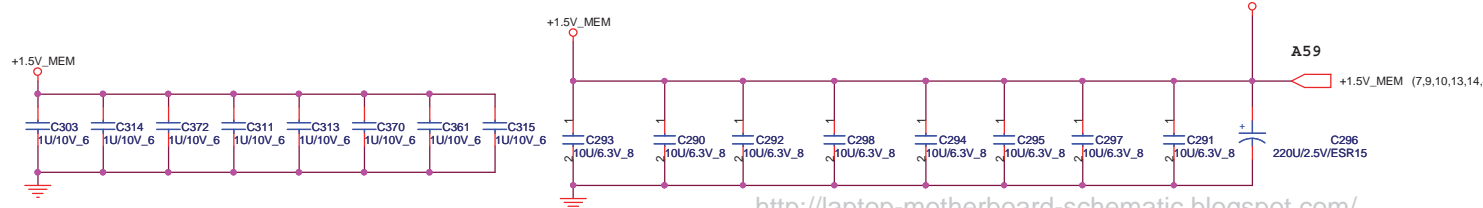
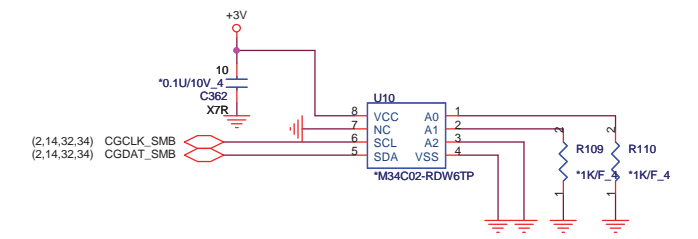
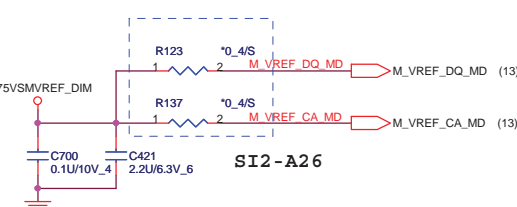
(7,9,10,13,14,40) +1.5V_MEM
(2,4,7,10,14,24,25,26,27,28,29,30,31,32,33,34,35,36,45) +3V
(7,14,40) +V_DDR_MCH_REF



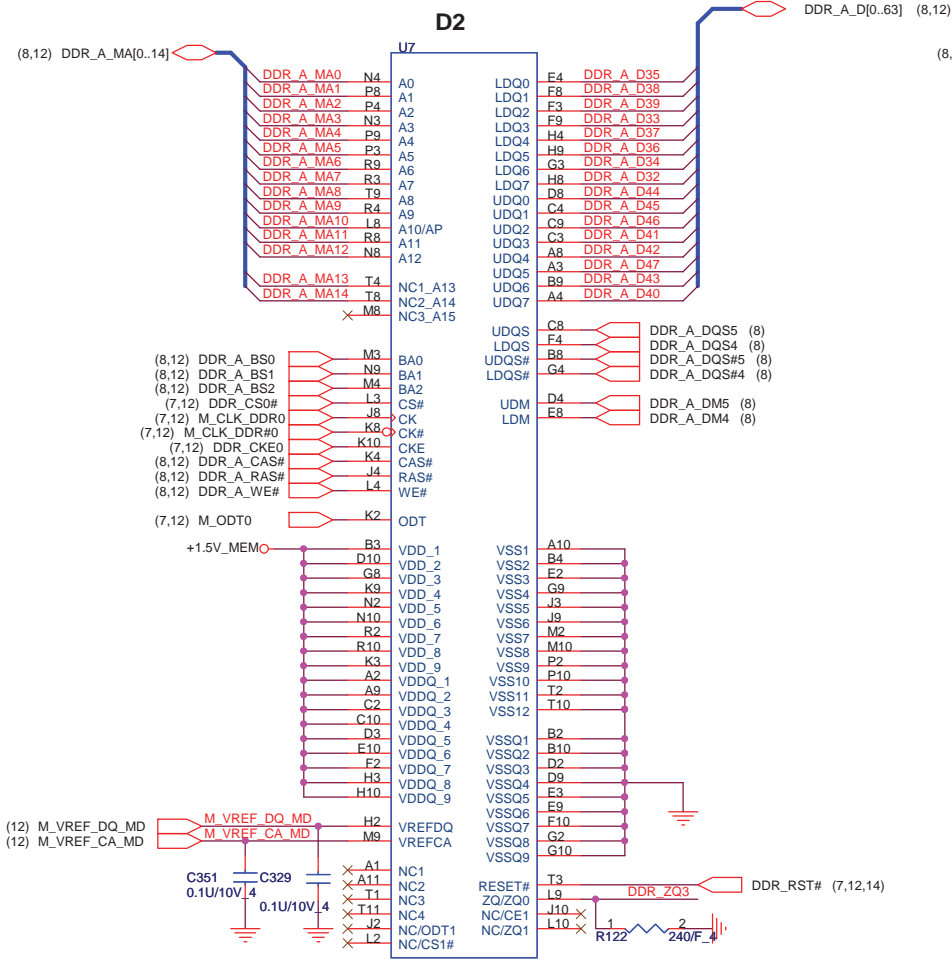
Please these resistor closely DIMMA, all trace length >= 750 mil.



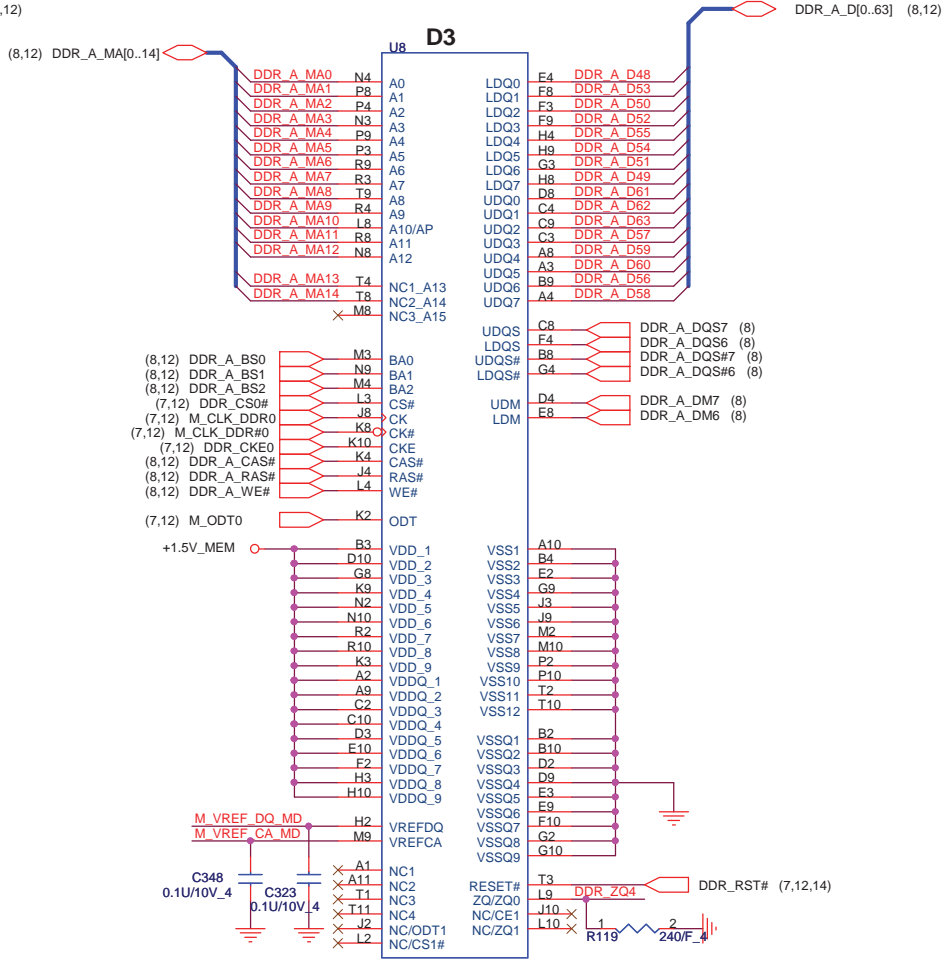
128M*16*4pcs
Samsung
K4B2G1646B-HCF8 AKD5MG4T500 Qunata Buy
AKD5MG4T502 TOP B/S



PROJECT : SP6
Quanta Computer Inc.
NB5
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K4B2G1646B-HCF8



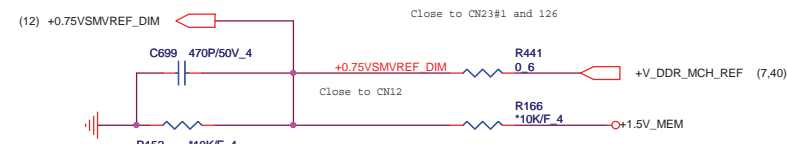
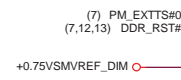
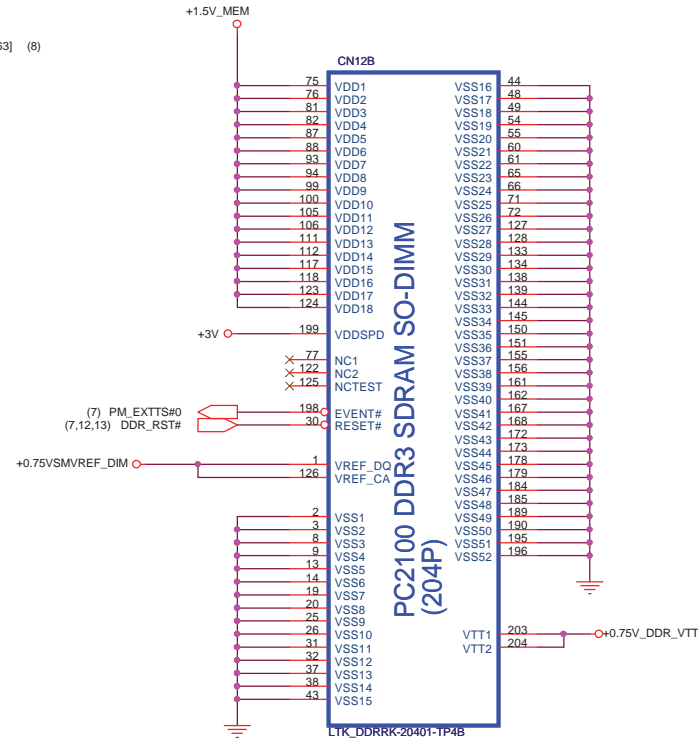
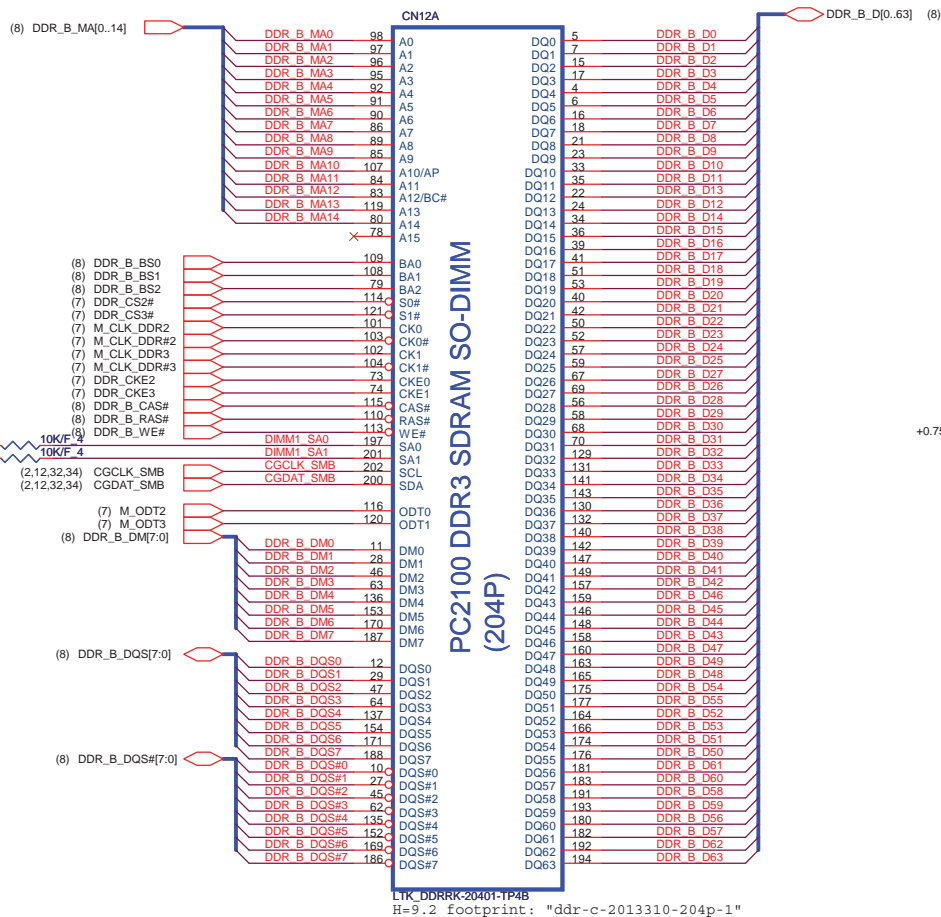
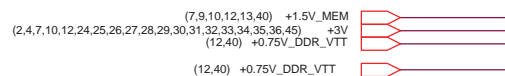
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PROJECT : SP6
Quanta Computer Inc.

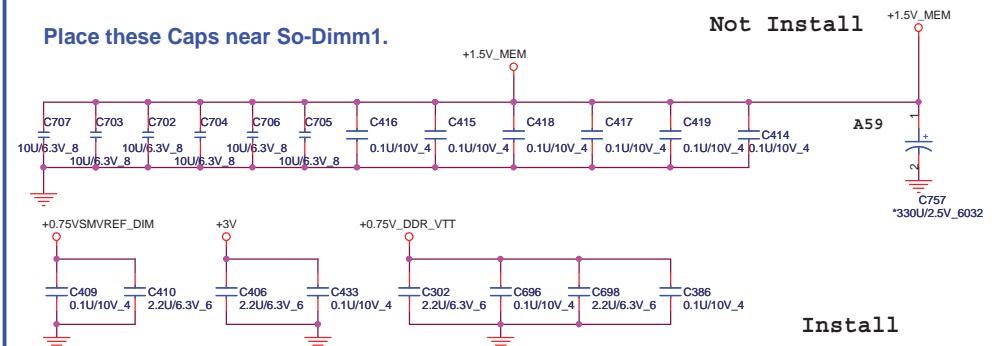
Size B	Document Number DDR3 (A) On Board_B,1Rank	Rev 1A
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0922-->CN23 update library to DDR-AS0A62X-U4RN-7F-204P type



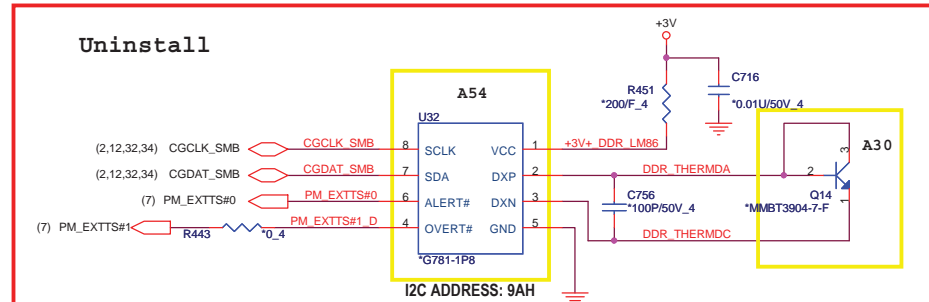
Place these Caps near So-Dimm1.

Not Install



Install

Uninstall



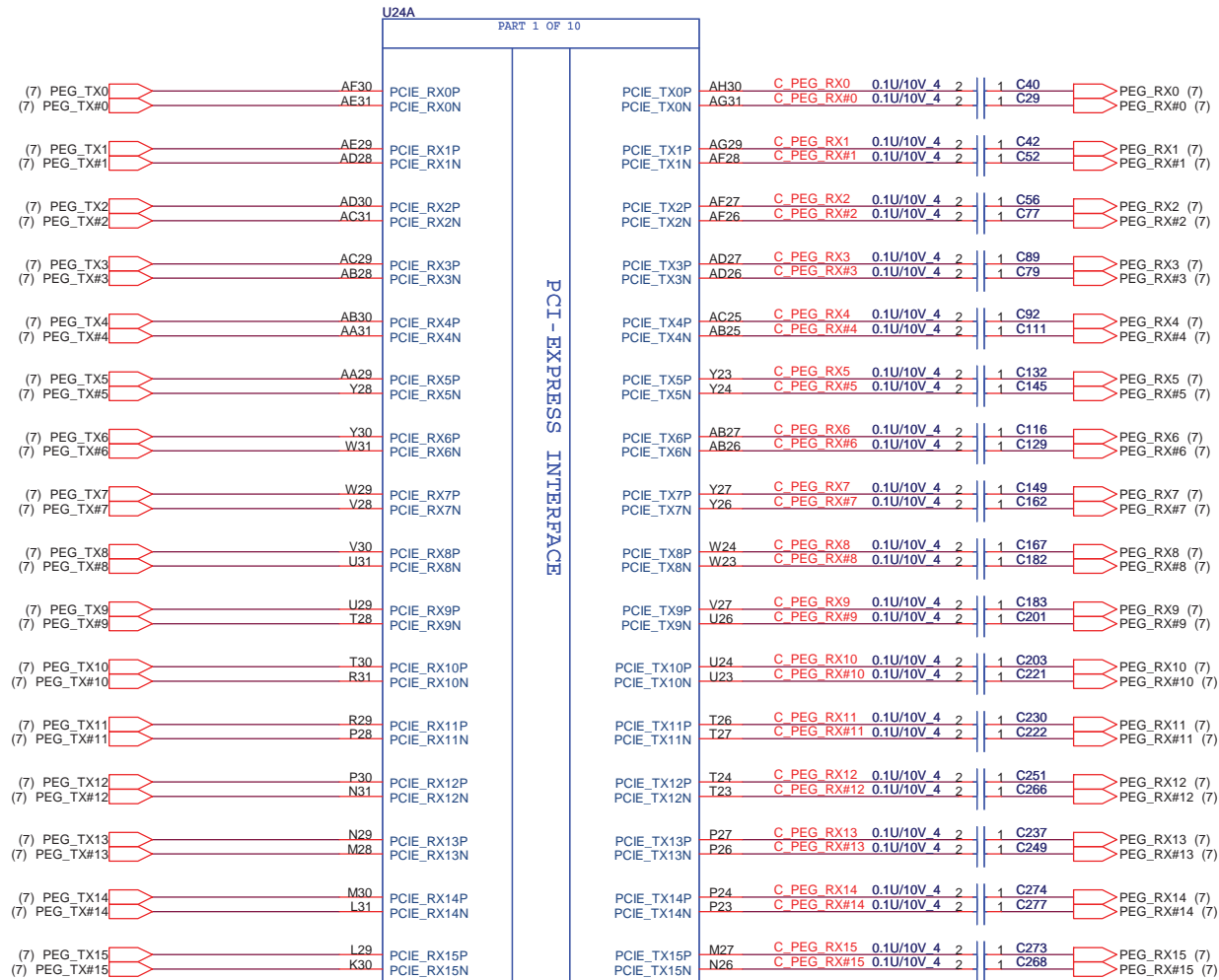
PROJECT : SP6
Quanta Computer Inc.

Size Custom Document Number
DDR3 Connect

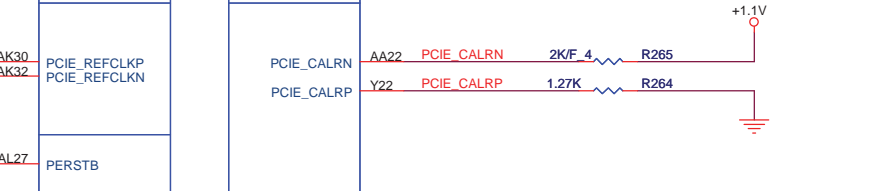
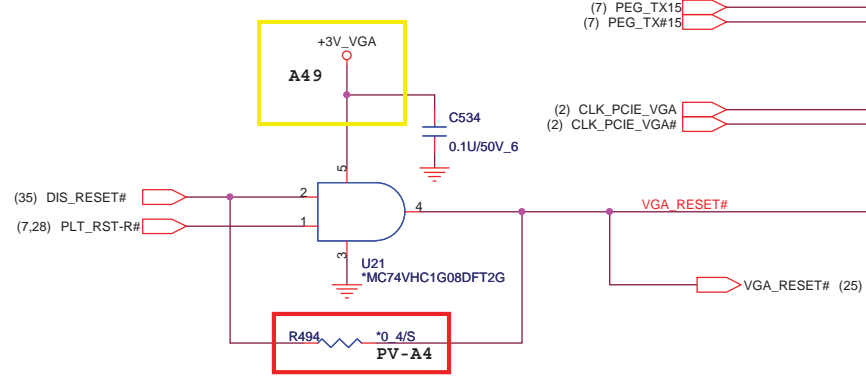
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Rev 1A

(17,18,19,20,40) +1.1V



100 MHz (+/-300 ppm)
input frequency, 0-0.7 V
single-ended swing.
clock must be provided
less than 400ns
after CLKREQ# is asserted



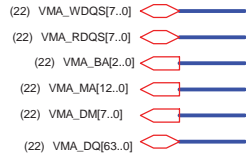
M92-S2-LP	AJ072800T18	100-CG1798 (216-0728020)
M92-S2-LP	AJ072800T21	100-CG1798 (216-0728020)



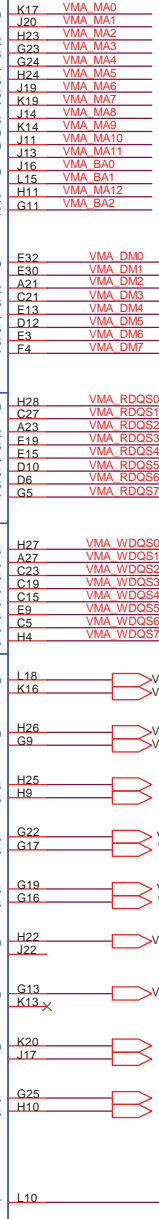
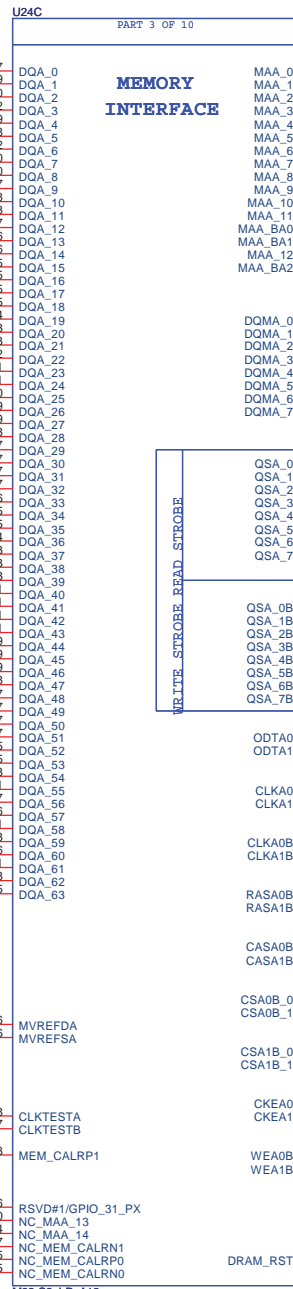
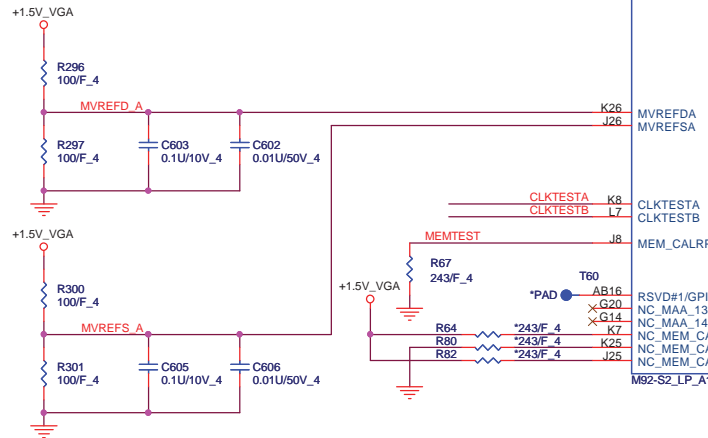
PROJECT : SP6
Quanta Computer Inc.

Size B	Document Number M92 PCIe interface	Rev 1A
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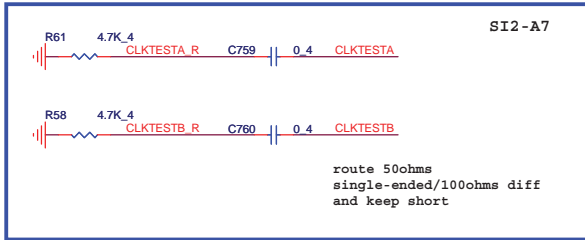
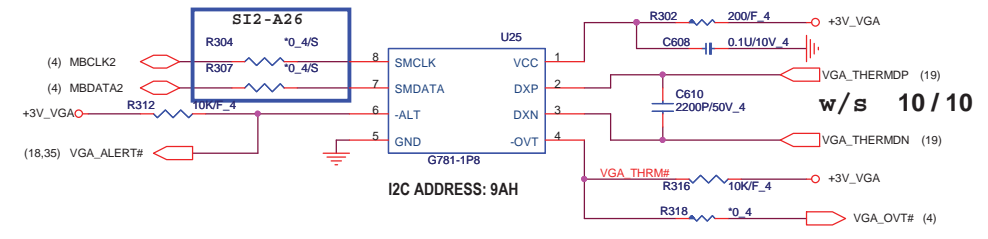
MEMORY INTERFACE



DIVIDER RESISTORS	DDR3
MVREF TO 1.5V	100R
MVREF TO GND	100R



THERMAL MONITOR



route 50ohms single-ended/100ohms diff and keep short

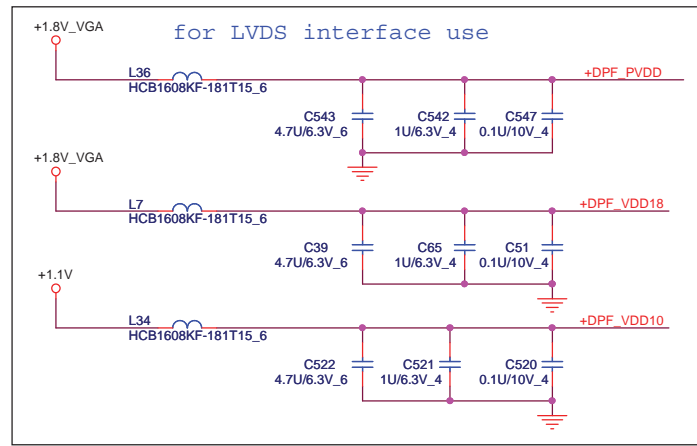
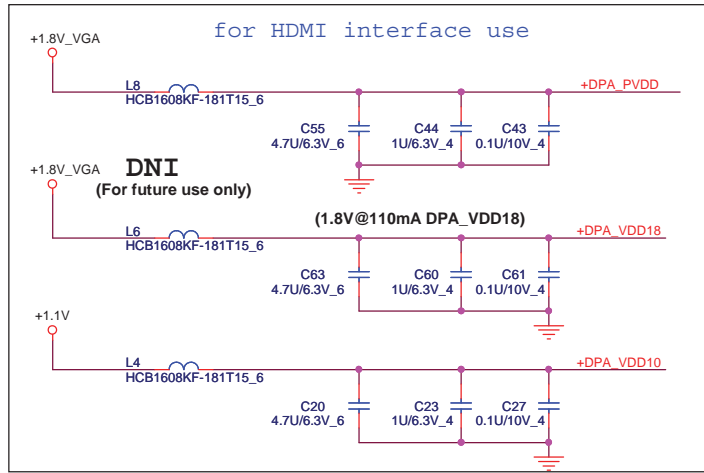
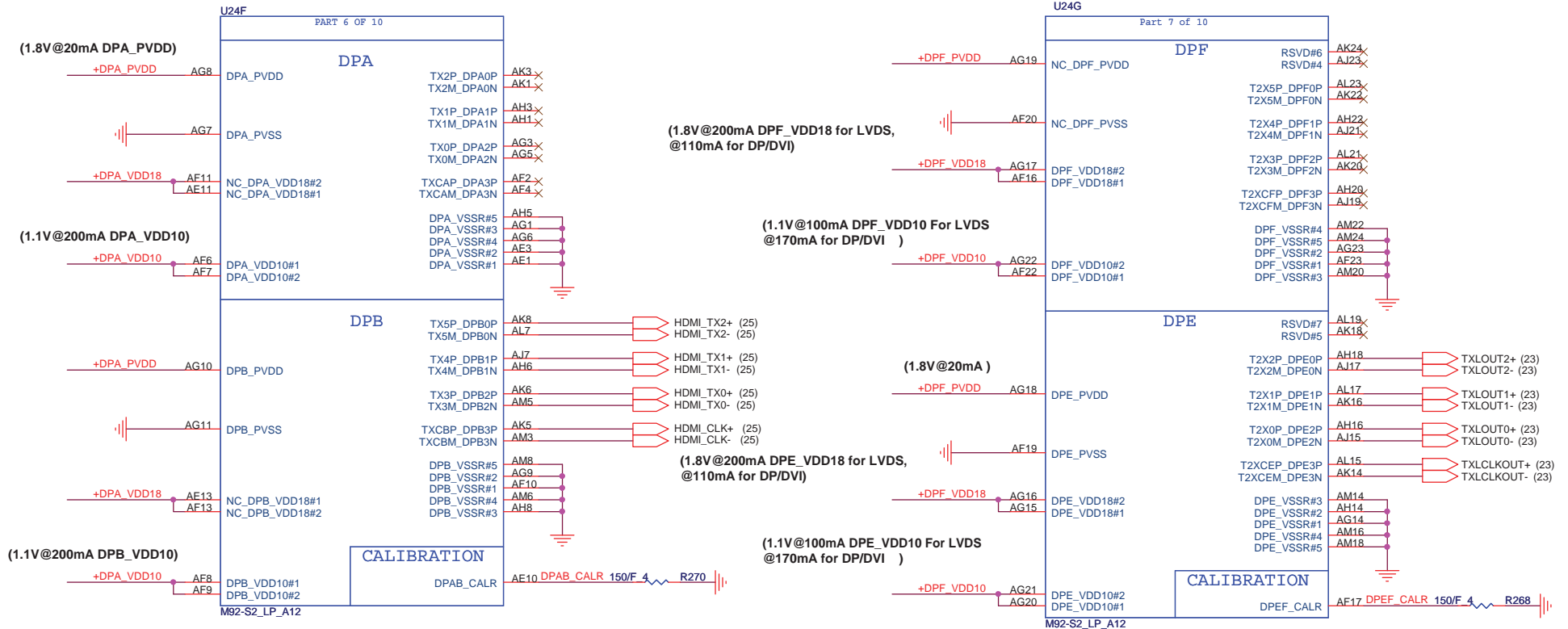
PROJECT : SP6
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
M92 Memory/Thermal		
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TMDP(HDMI) INTERFACE

(15,18,19,20,40) +1.1V

LVDS INTERFACE



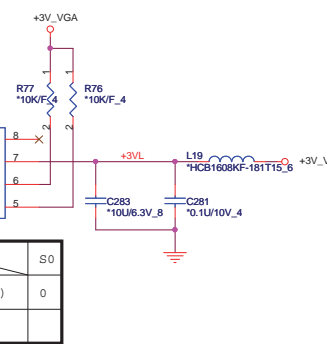
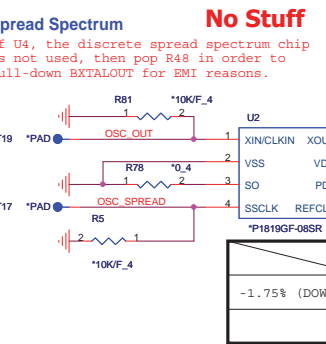
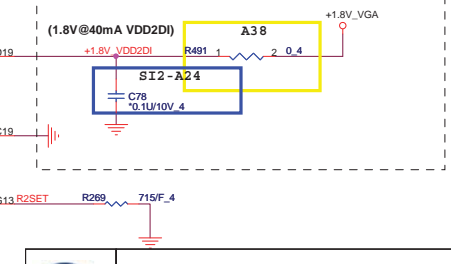
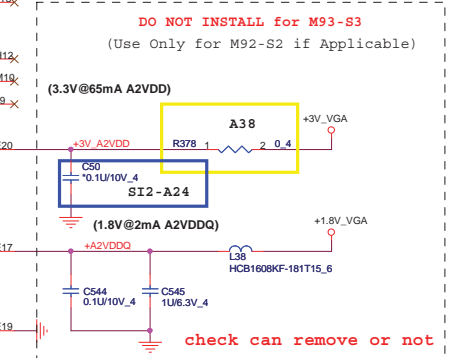
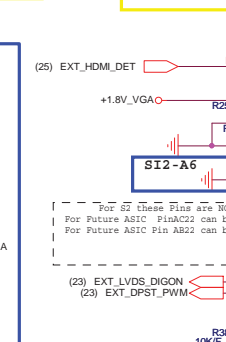
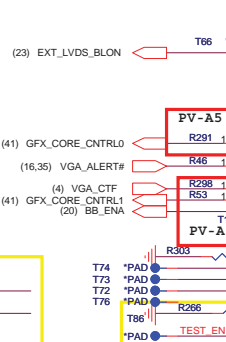
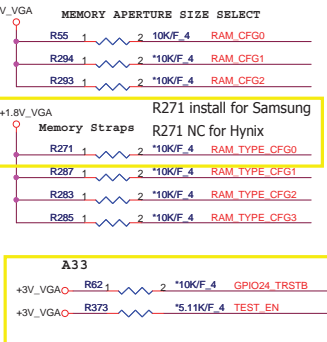
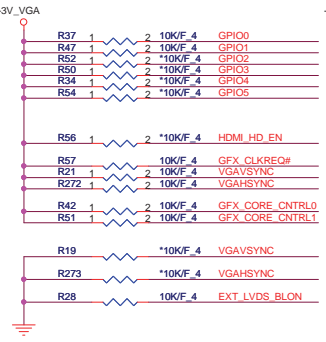
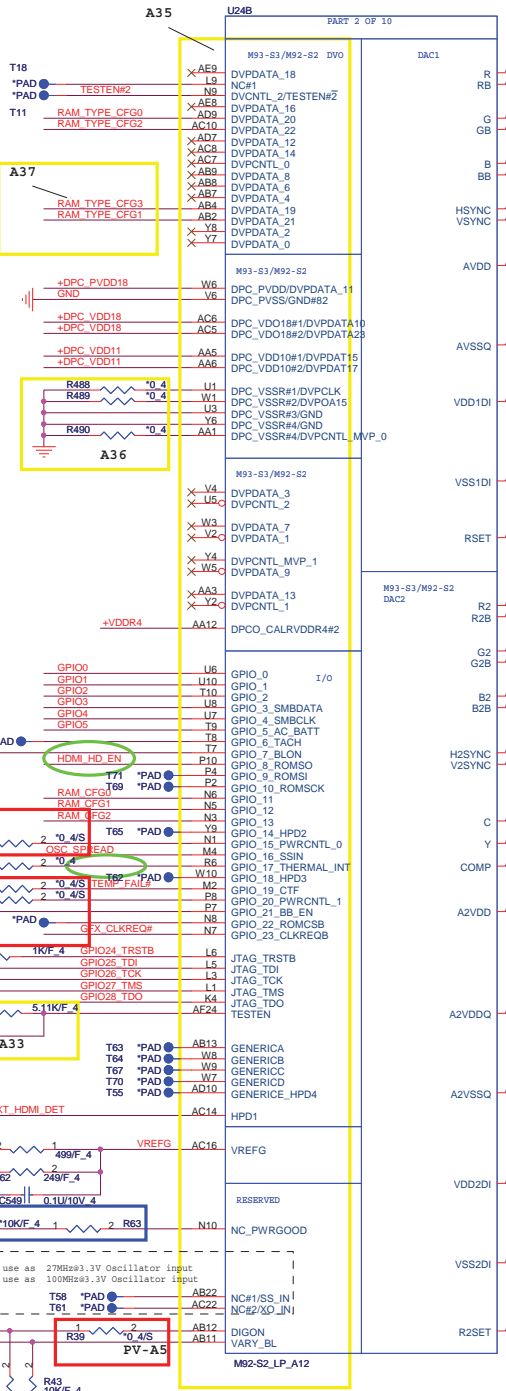
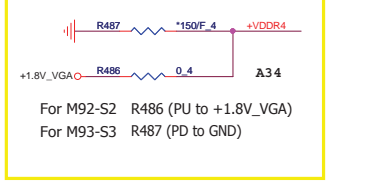
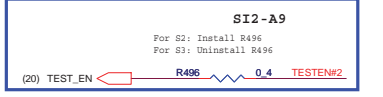
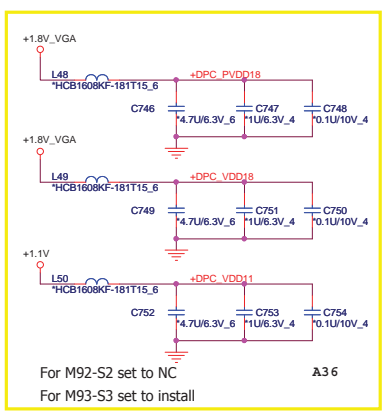
	PROJECT : SP6 Quanta Computer Inc.		Rev 1A
	Size B	Document Number M92 HDMI/LVDS interface	
		Sheet 17 of 49	

MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB		0	0	0
256MB		0	0	1
64MB		0	1	0
512MB		1	0	0

Default

Memory Straps	DDR3	RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0
667MHz K4W1G1646D-EC15 (64M*16) Samsung	X	X	0	1	
700MHz H5TQ1G63BFR-14C (64M*16) Hynix	X	X	0	0	
Blank	X	X	0	0	
Blank	X	X	0	0	

GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	SP6 setting
GPIO0	GPIO0 - TX_PWRS_ENB (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
GPIO1	GPIO1 - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
GPIO2	GPIO2 - BIF_GENZ_EN (5.0 Gt/s Enable) 0: Default (Driver Controlled Gen2) 1: Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO 5 AC_BATT 0: Battery saving mode = 0.0 V 1: AC (Performance mode) = 3.3 V	0
GPIO6	ATI Internal use only	0

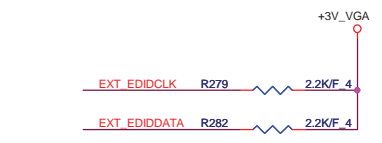
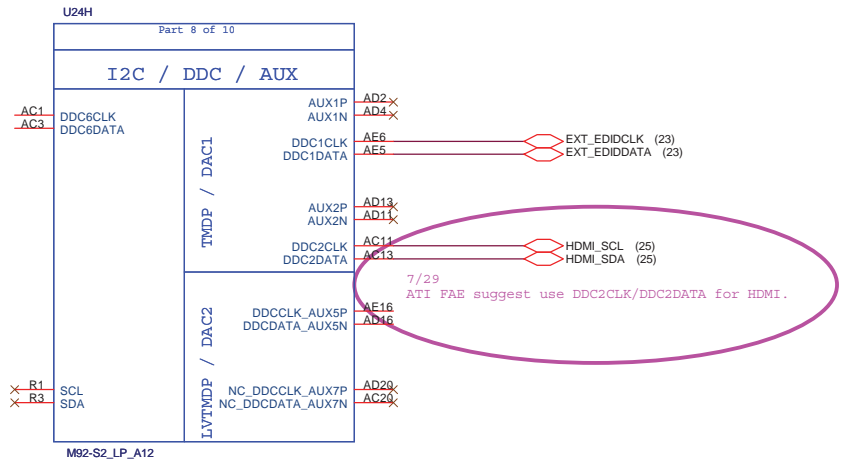
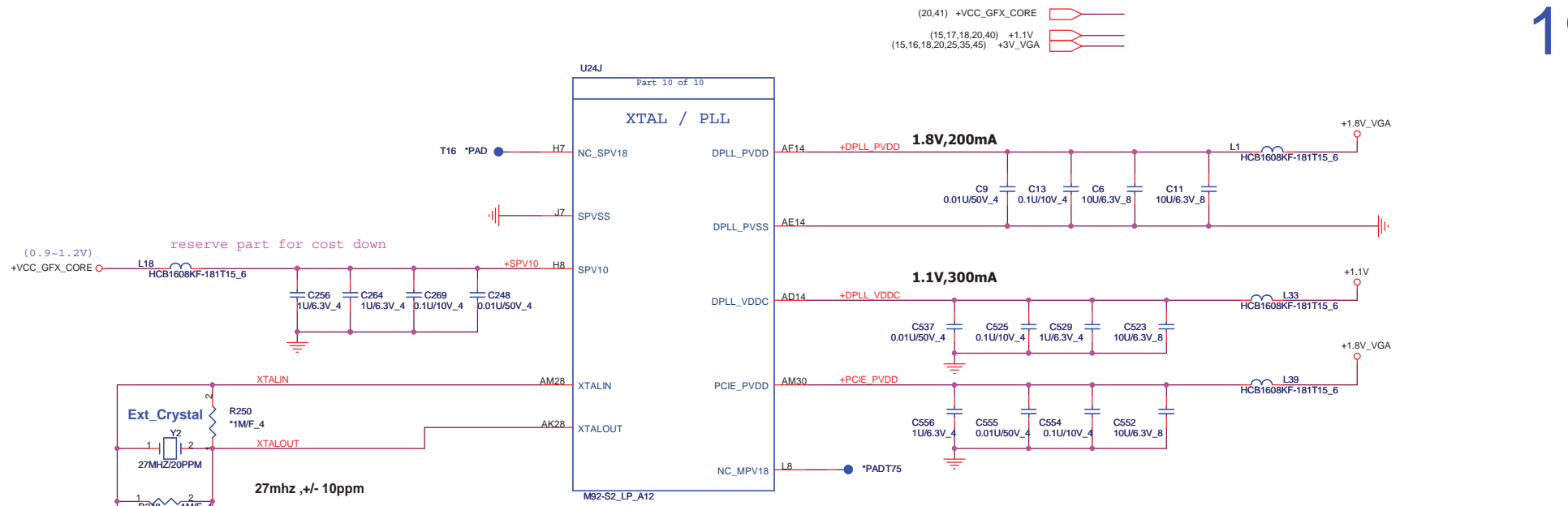


For S2 these Pins are NC
 For Future ASIC PinAC22 can use as 27MHz±3.3V Oscillator input
 For Future ASIC Pin AB22 can use as 10MHz±3.3V Oscillator input

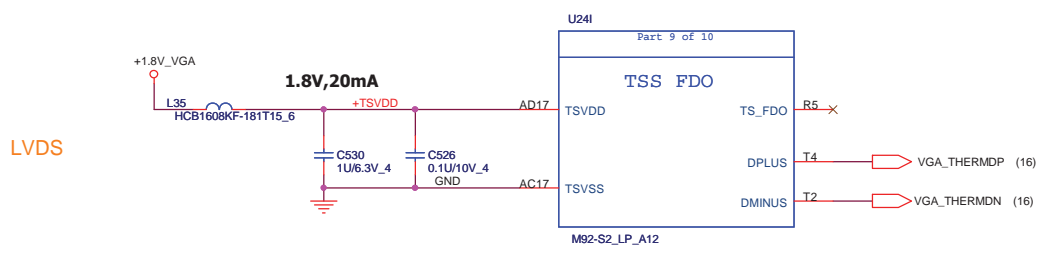
PROJECT : SP6
Quanta Computer Inc.

Size Custom Document Number M92 IO/GPIO Rev 2A

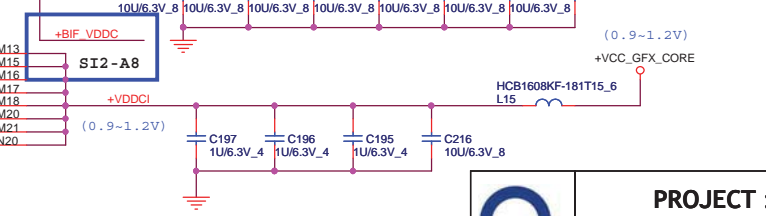
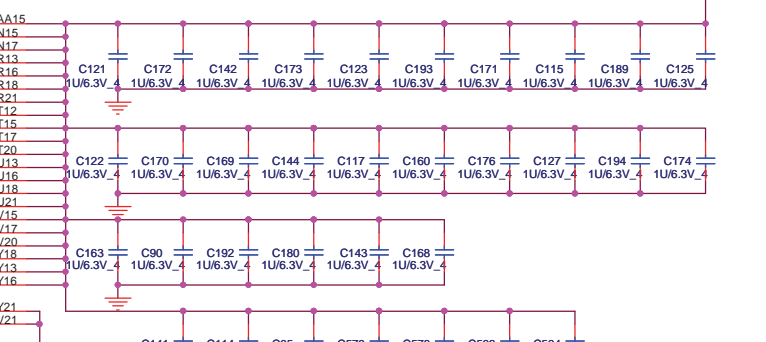
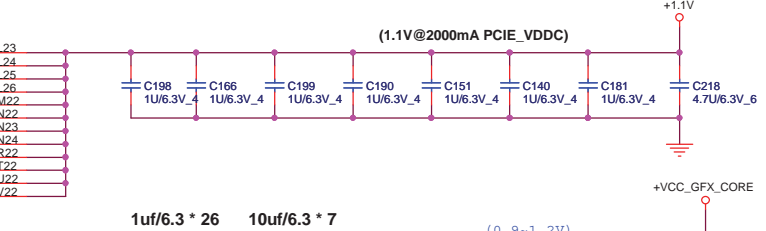
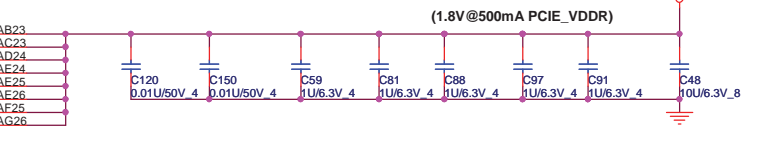
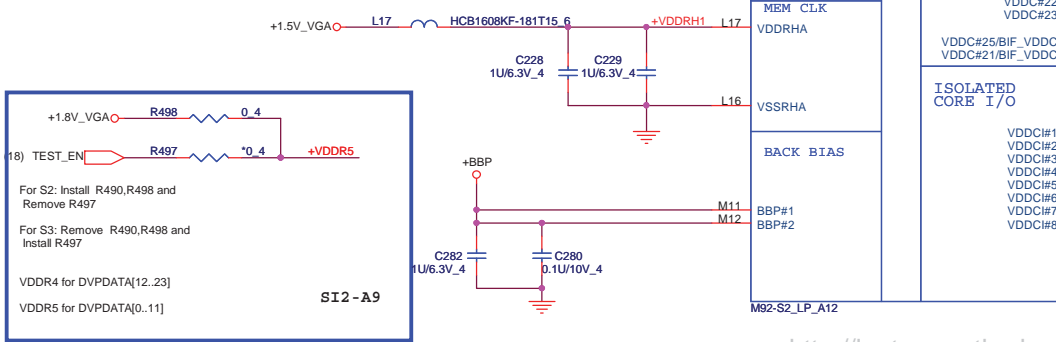
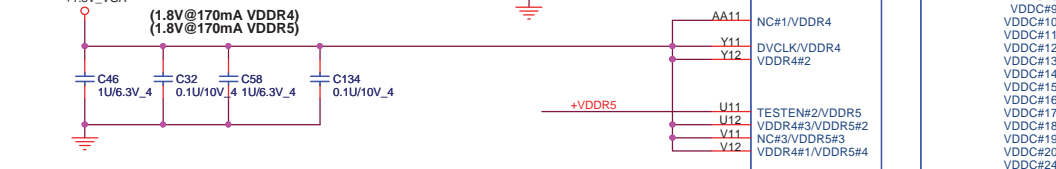
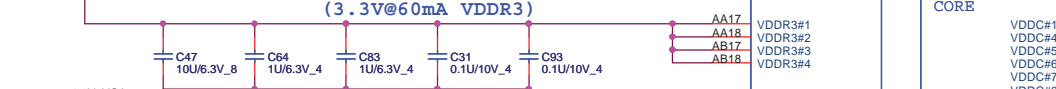
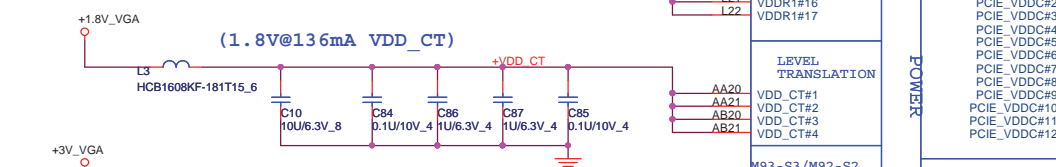
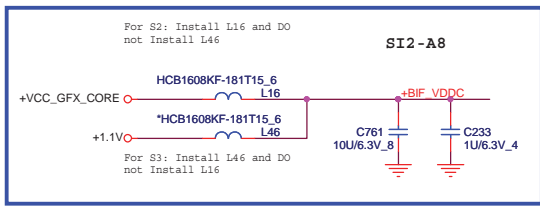
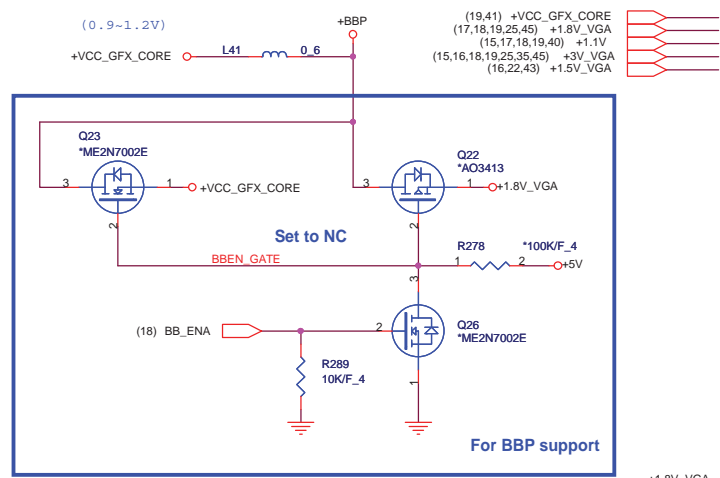
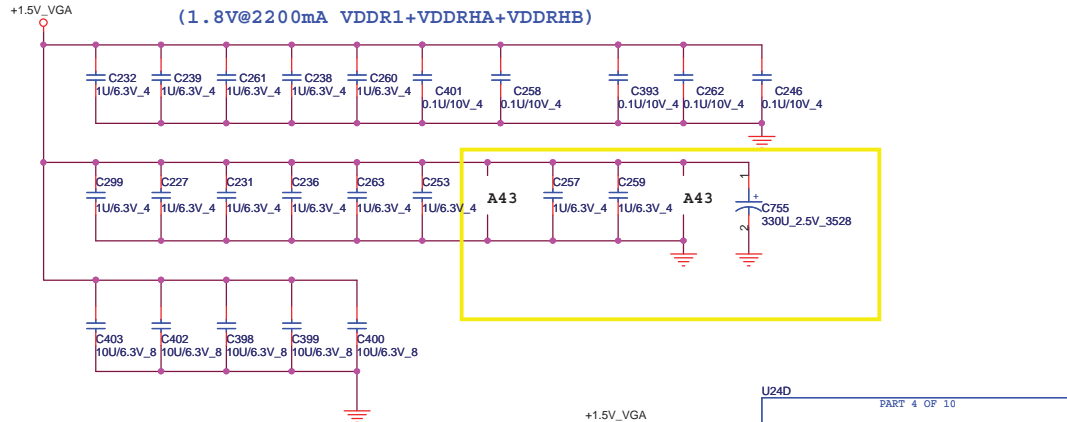
Date: Tuesday, April 07, 2009 Sheet 18 of 49



HDMI



	PROJECT : SP6 Quanta Computer Inc.	
	Size Custom	Document Number M92 XTAL/I2C
Date: Tuesday, April 07, 2009 Sheet 19 of 49		



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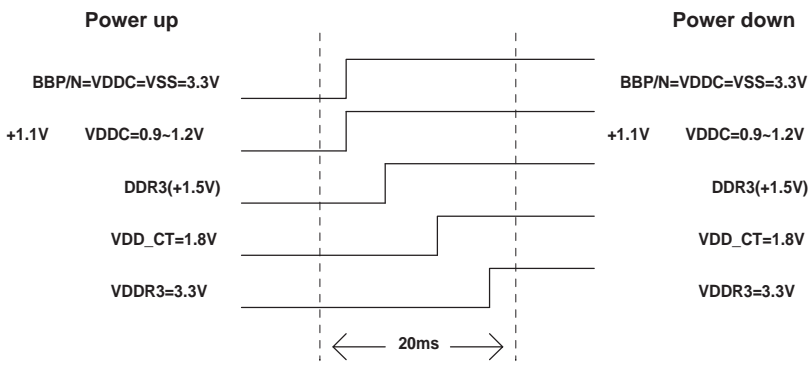
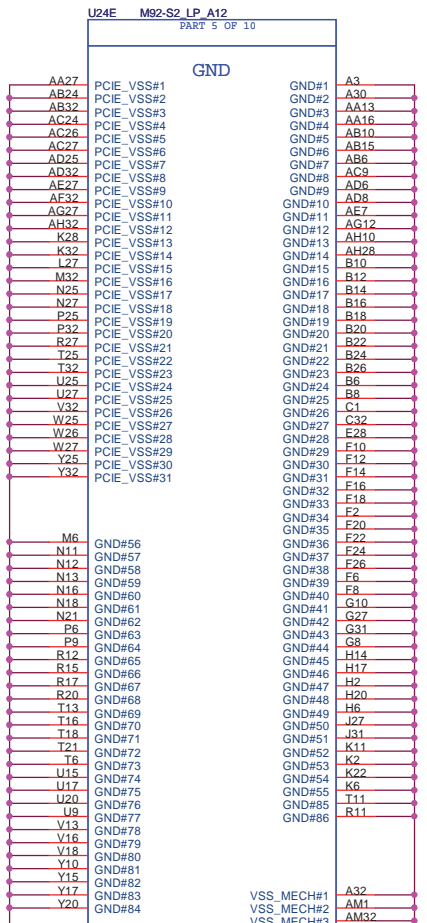
MEM I/O	
H13	VDDR1#1
H16	VDDR1#2
H19	VDDR1#3
J10	VDDR1#4
J23	VDDR1#5
J24	VDDR1#6
J9	VDDR1#7
K10	VDDR1#8
K23	VDDR1#9
K9	VDDR1#10
L11	VDDR1#11
L12	VDDR1#12
L13	VDDR1#13
L20	VDDR1#14
L21	VDDR1#15
L22	VDDR1#16
L22	VDDR1#17
LEVEL TRANSLATION	
AA20	VDD_CT#1
AA21	VDD_CT#2
AA20	VDD_CT#3
AB21	VDD_CT#4
M93-S3/M92-S2	
AA17	VDDR3#1
AA18	VDDR3#2
AB17	VDDR3#3
AB18	VDDR3#4
NC#1/VDDR4	
Y11	DVCLK/VDDR4
Y12	VDDR4#2
TESTEN#2/VDDR5	
U11	VDDR4#3/VDDR5#2
U12	VDDR4#3/VDDR5#2
V11	NC#3/VDDR5#3
V12	VDDR4#1/VDDR5#4
MEM CLK	
L17	VDDRHA
VDDRHA	
L16	VSSRHA
BACK BIAS	
M11	BBP#1
M12	BBP#2
M92-S2_LP_A12	

<http://laptop-motherboard-schematic.blogspot.com/> (For M96/92, 0.95V-1.1V@2A VDDCI)



PROJECT : SP6
Quanta Computer Inc.

Size Custom	Document Number M92 POWER/GND	Rev 2B
Date: Tuesday, April 07, 2009	Sheet 20 of 49	



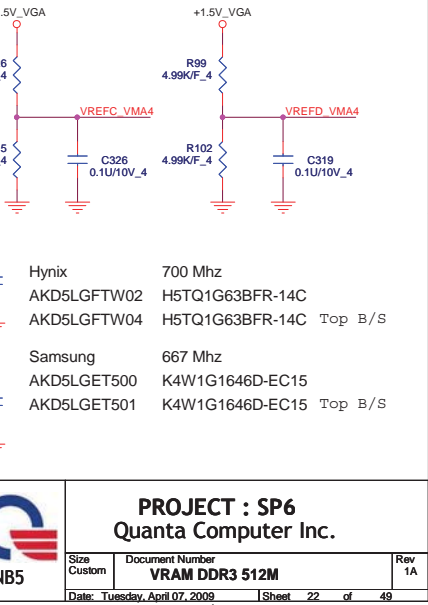
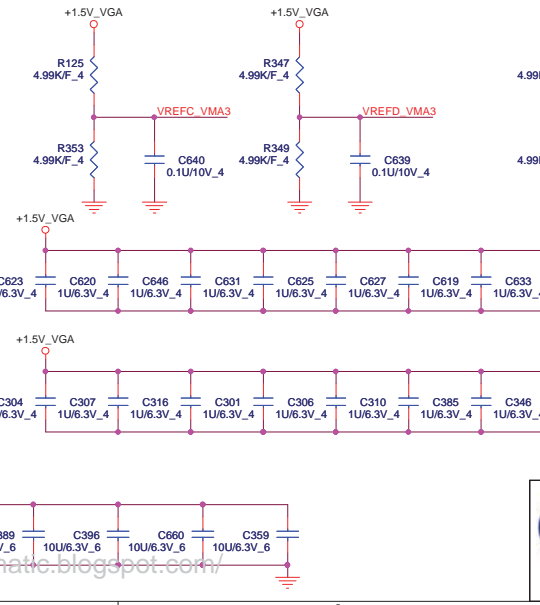
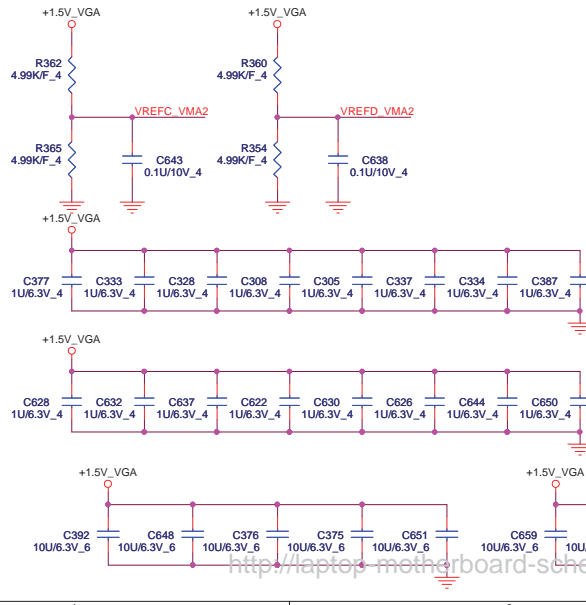
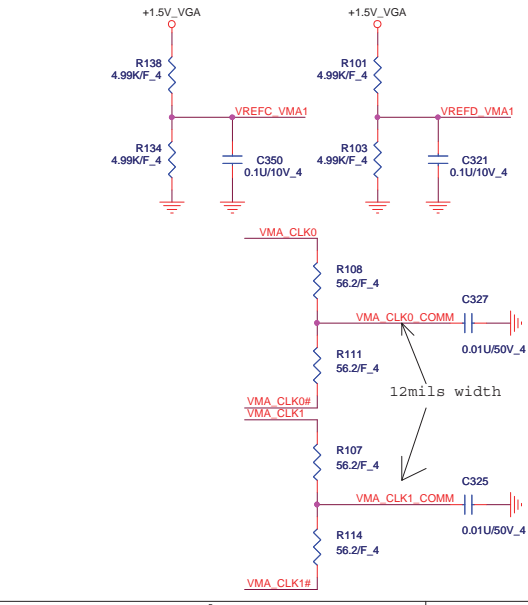
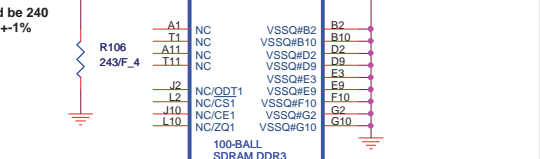
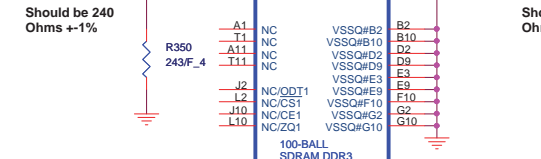
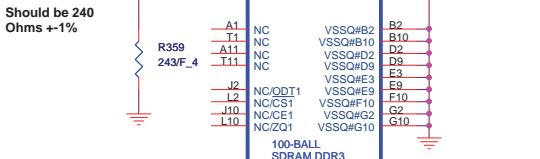
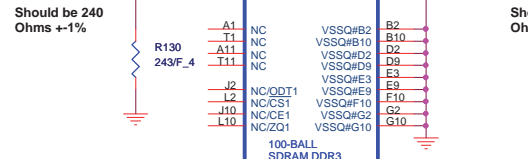
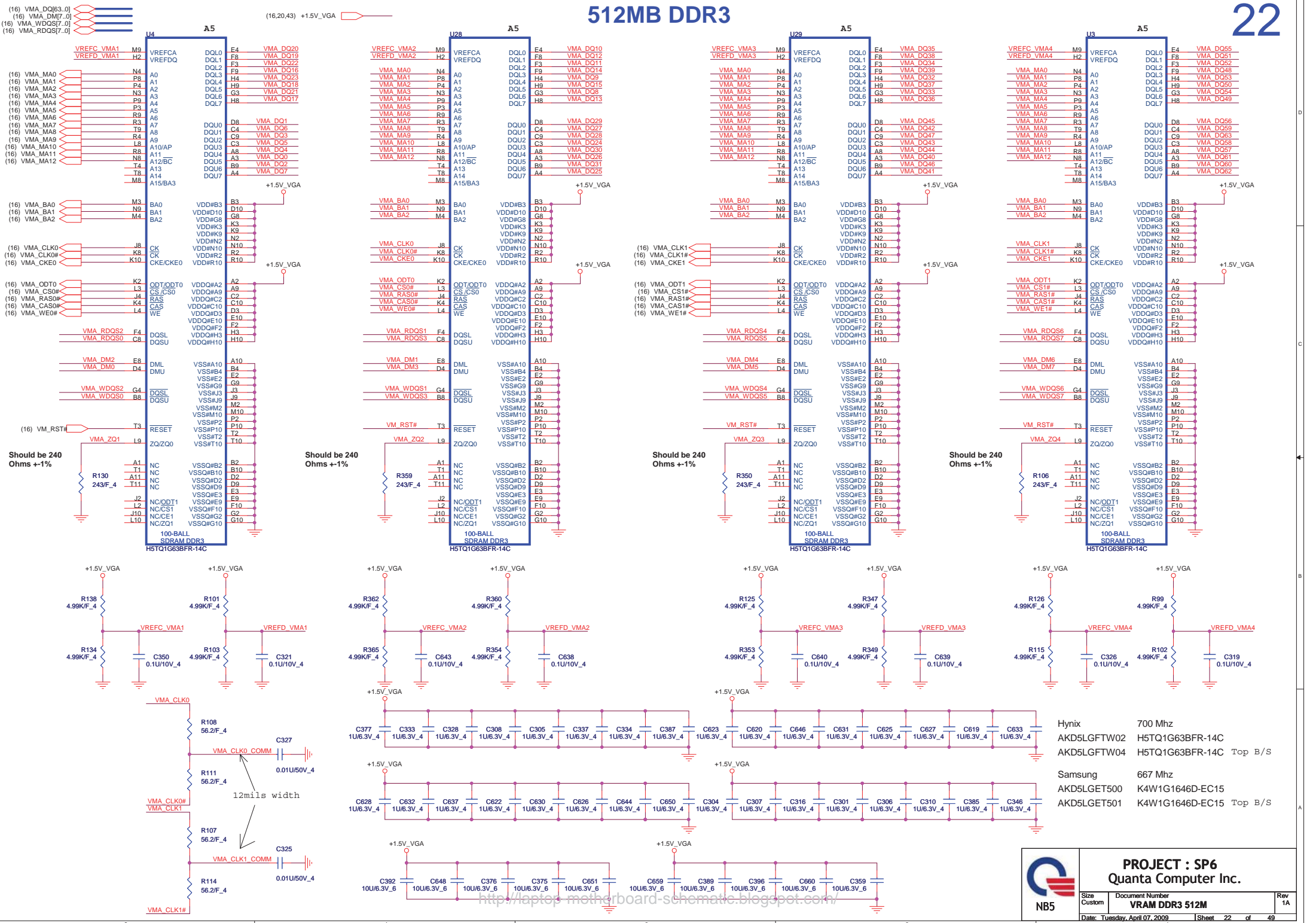
CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA= NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8		0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0]	0
AUD[0]	VSNC	0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X

PROJECT : SP6
Quanta Computer Inc.

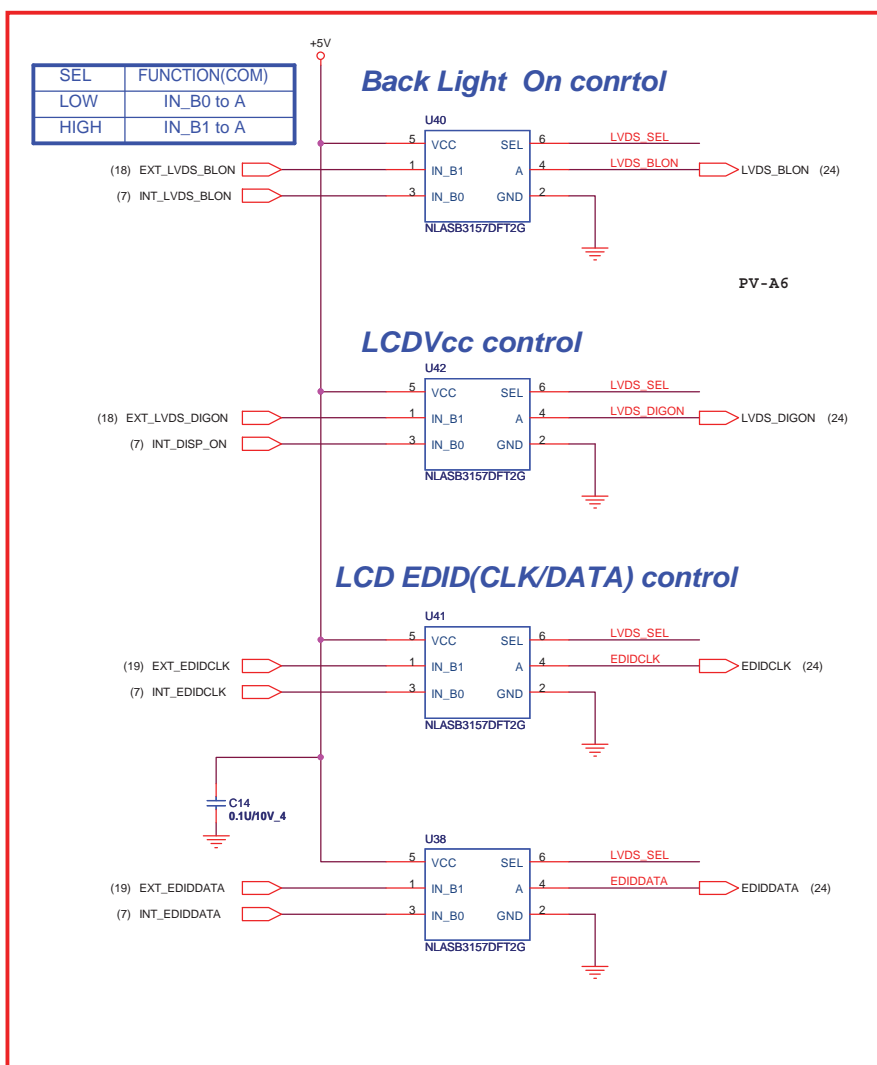
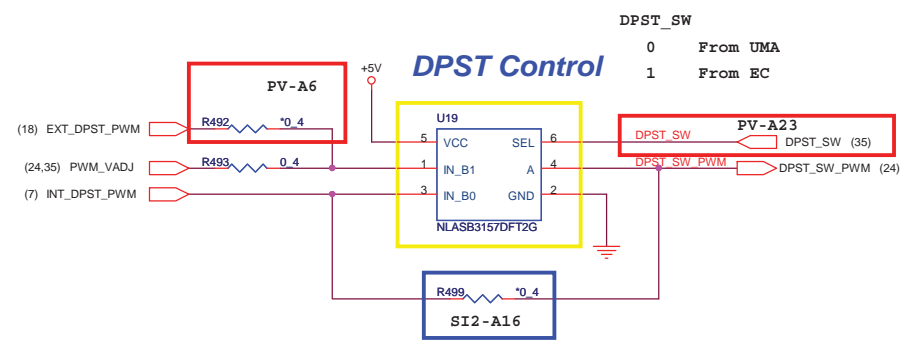
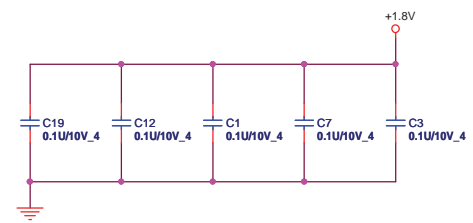
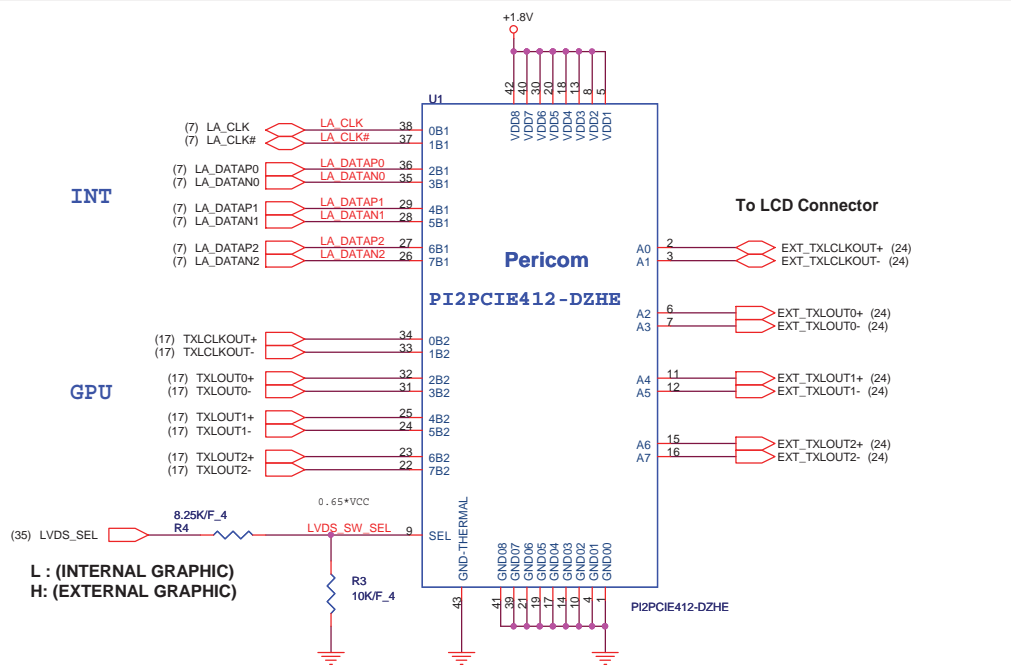
Size Custom Document Number M92-S2-LP_G_GND Rev 1A

Date: Tuesday, April 07, 2009 Sheet 21 of 49

512MB DDR3



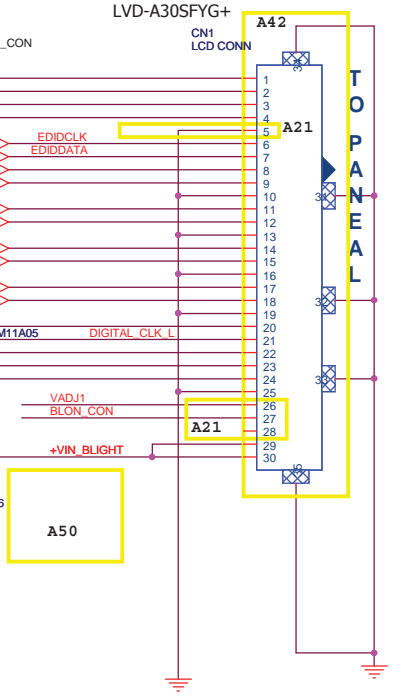
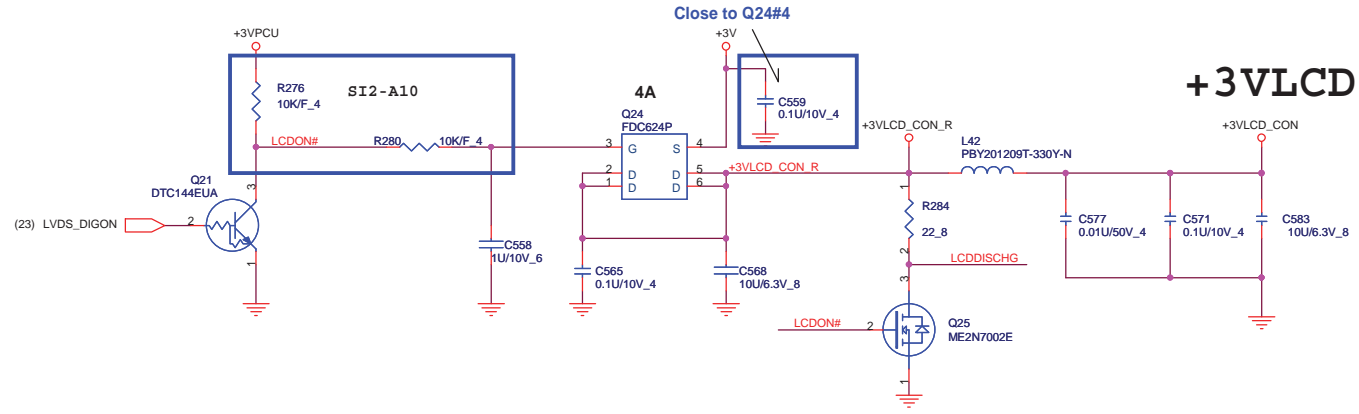
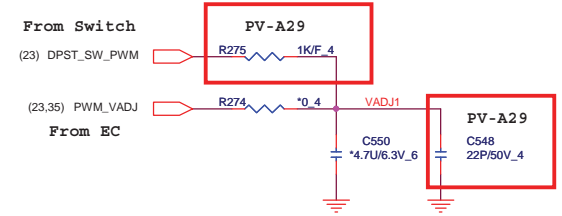
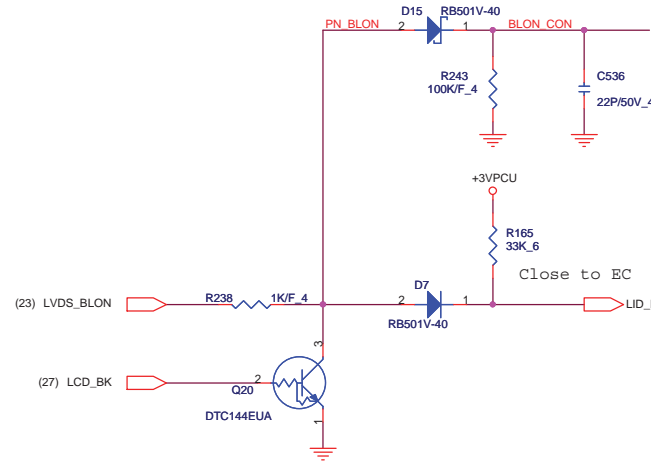
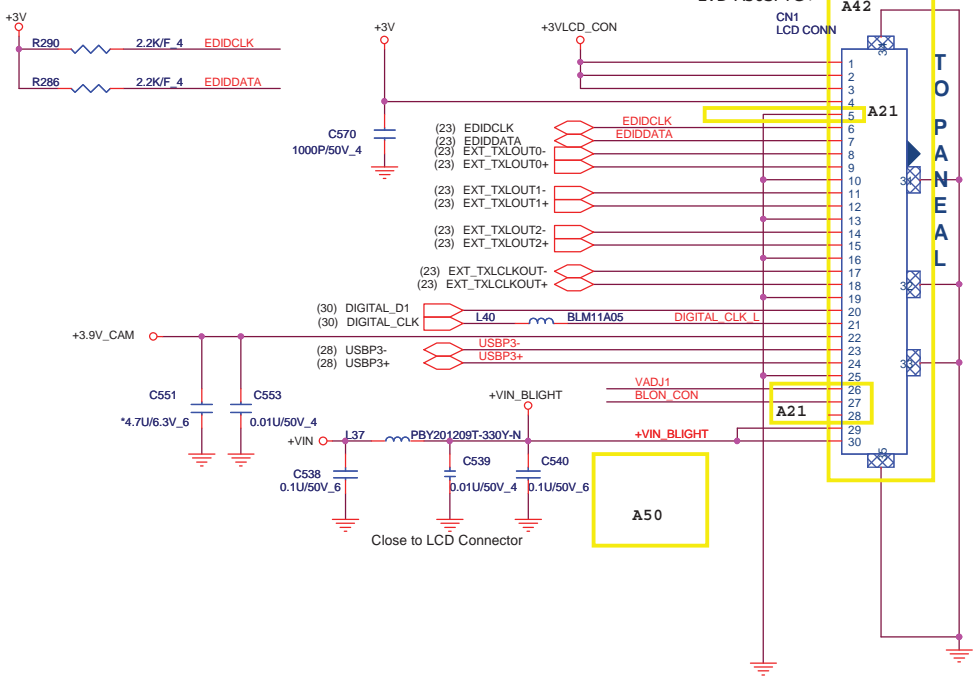
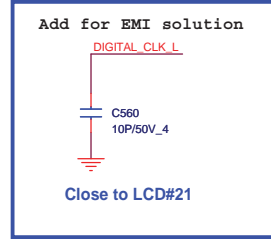
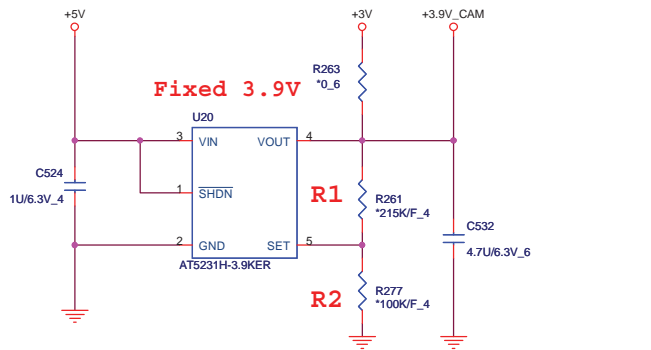
		PROJECT : SP6	
		Quanta Computer Inc.	
Size	Document Number	Rev	
Custom	VRAM DDR3 512M	1A	
Date:	Tuesday, April 07, 2009	Sheet	22 of 49



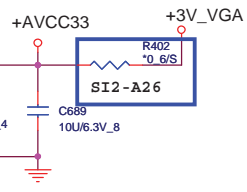
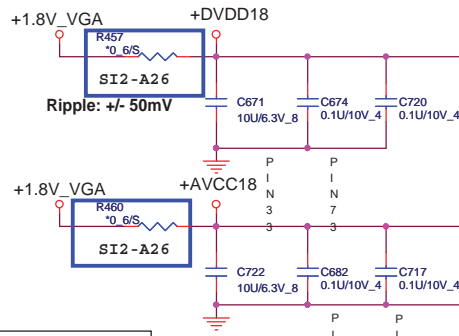
USB CAMERA /DIGITAL MIC CONNECT

- (2,4,7,10,12,14,25,26,27,28,29,30,31,32,33,34,35,36,45) +3V
- (20,23,25,29,31,36,45) +5V
- (37,39,40,41,42,43,44,45) +VIN
- (26,32,33,35,37,38,39,43,44,45) +3VPCU

$V_{out} = 1.25 (1 + R1/R2)$



	PROJECT : SP6 Quanta Computer Inc.	
	Size Custom	Document Number LVDS/Camera/Digital MIC
Date: Tuesday, April 07, 2009		Sheet 24 of 49



HPDIN

STATE	Status
LOW	Without HDMI Device
HIGH	HDMI Device detect

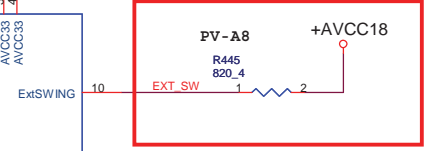
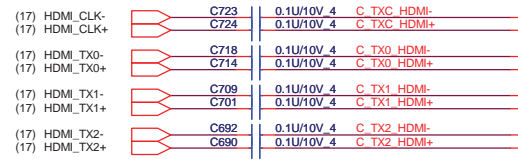
(TPWR/I2CADDR)

STATE	ADDRESS
LOW	0xC0/0xD0/0xE0 (DEFAULT)
HIGH	0xC4/0xD4/0xE4

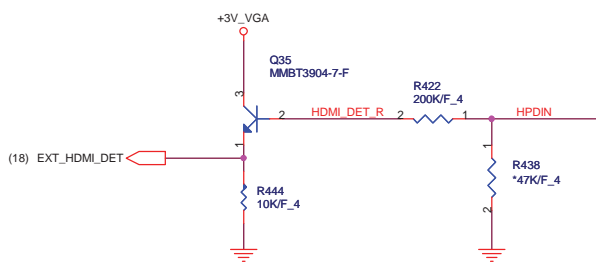
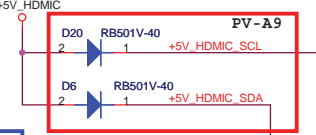
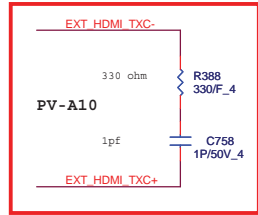
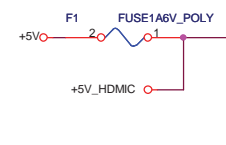
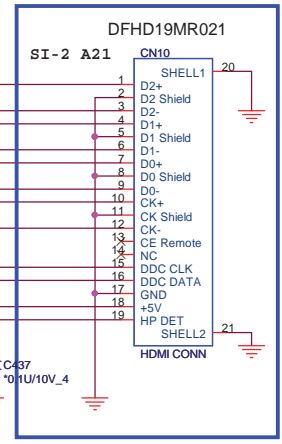
PLACE AC CAPS CLOSE TO CONNECTOR



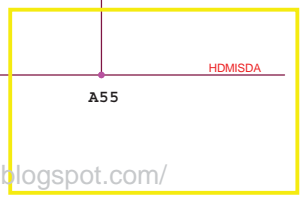
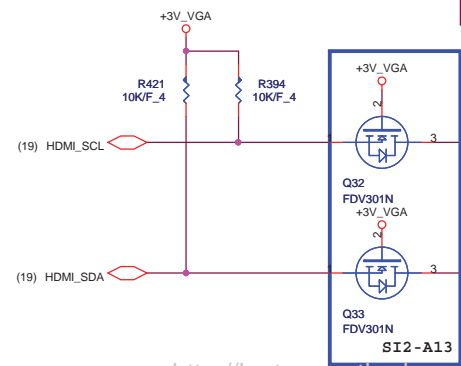
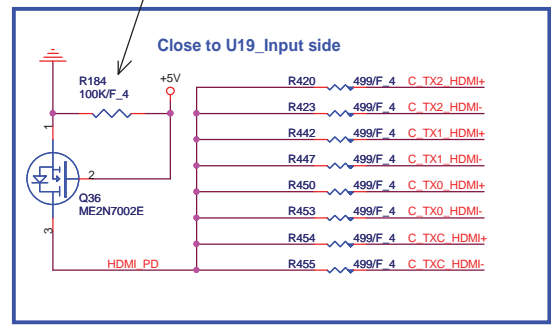
SI9181



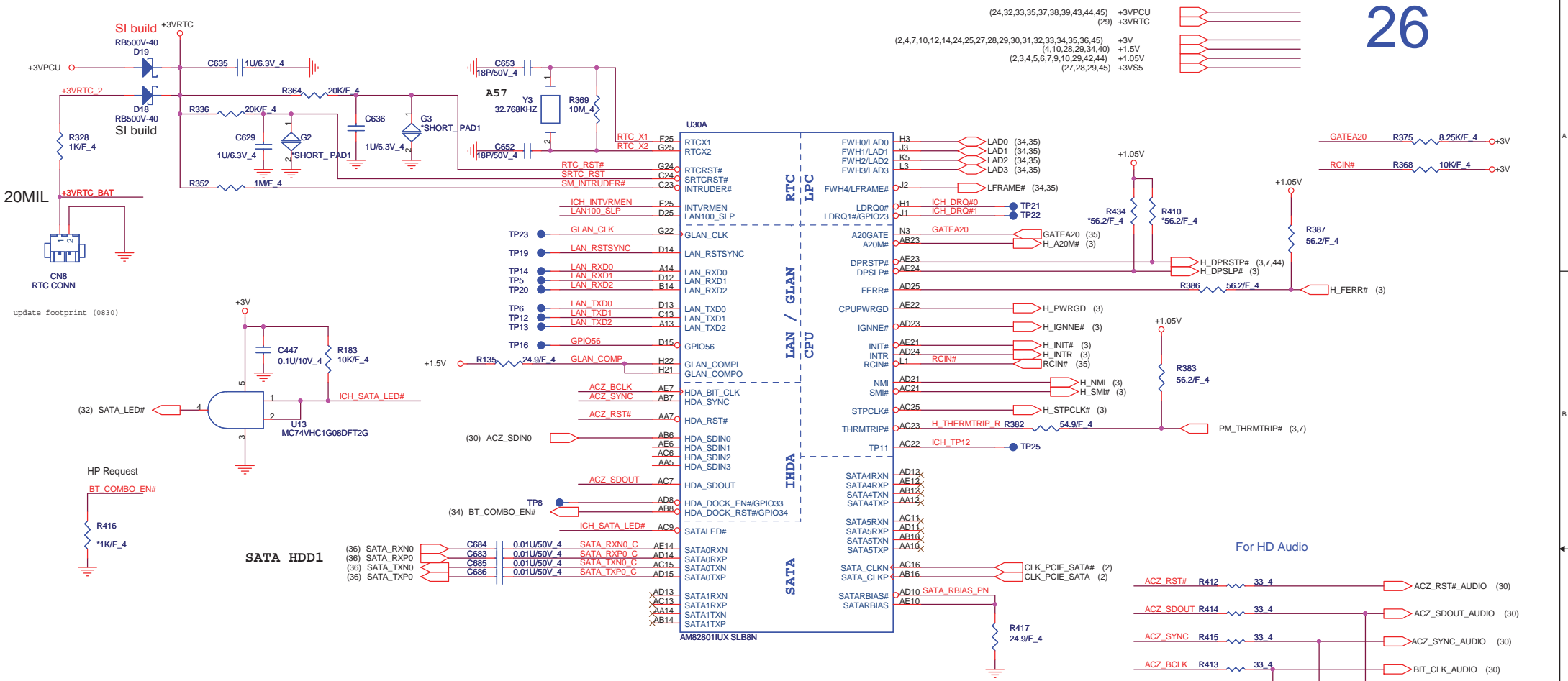
HDMI PORT



MAKE SURE THE MOSFET IS OFF DURING SYSTEM IN STANDBY



PROJECT : SP6
Quanta Computer Inc.



SB Strap

ICH9-M Internal VR Enable strap
 (Internal VR for VccSus1_05, VccSus1_5 and VccCL1_5)

ICH9-M LAN100_SLP Strap
 (Internal VR for VccLAN1_05 and VccCL1_05)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

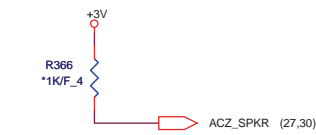
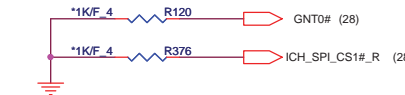
ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

No Reboot Strap

ACZ_SPKR	Low: Default Hi: No reboot
----------	-------------------------------

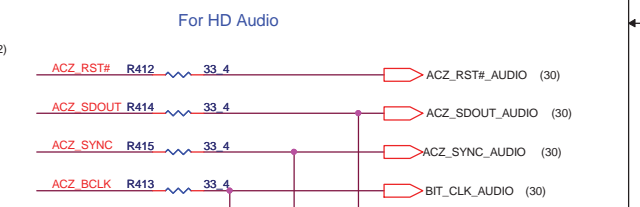
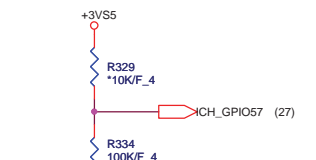
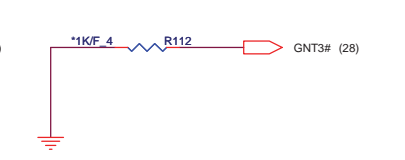
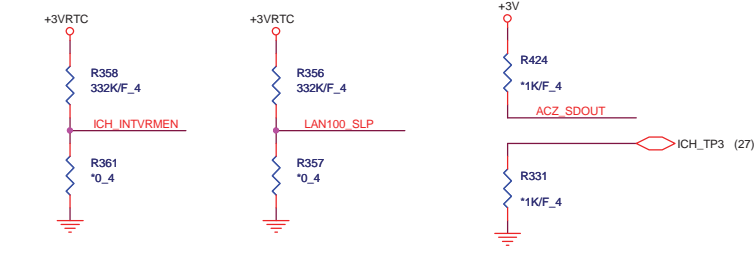


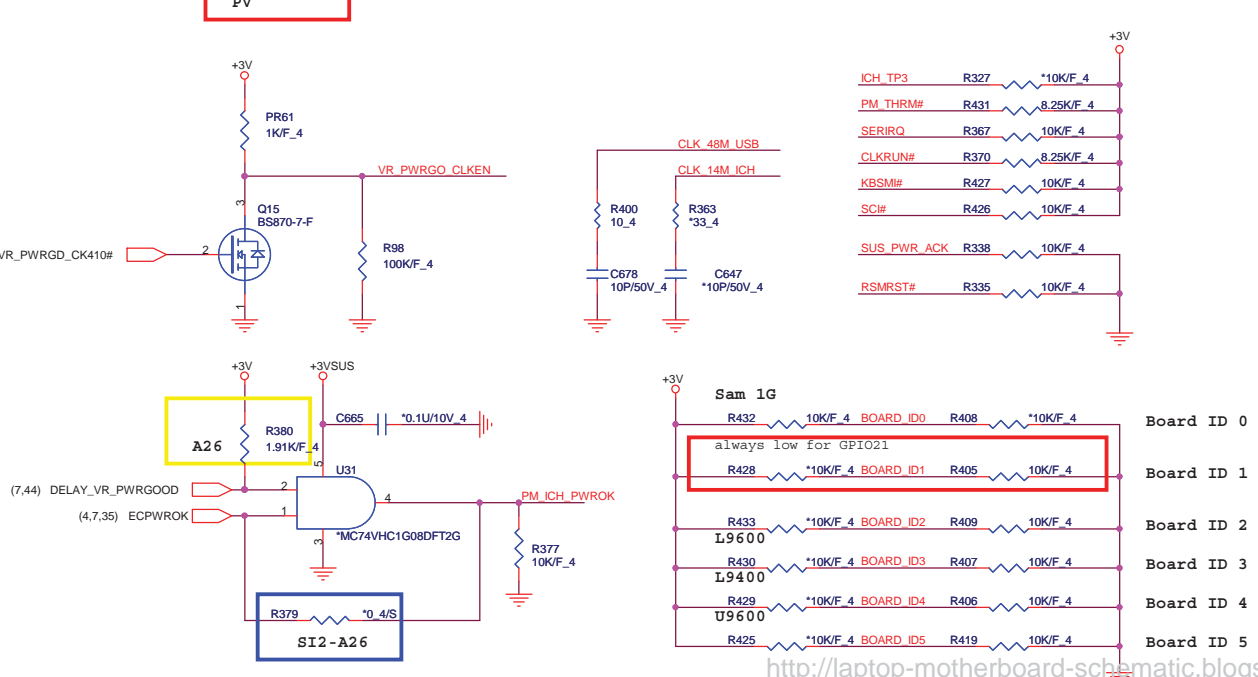
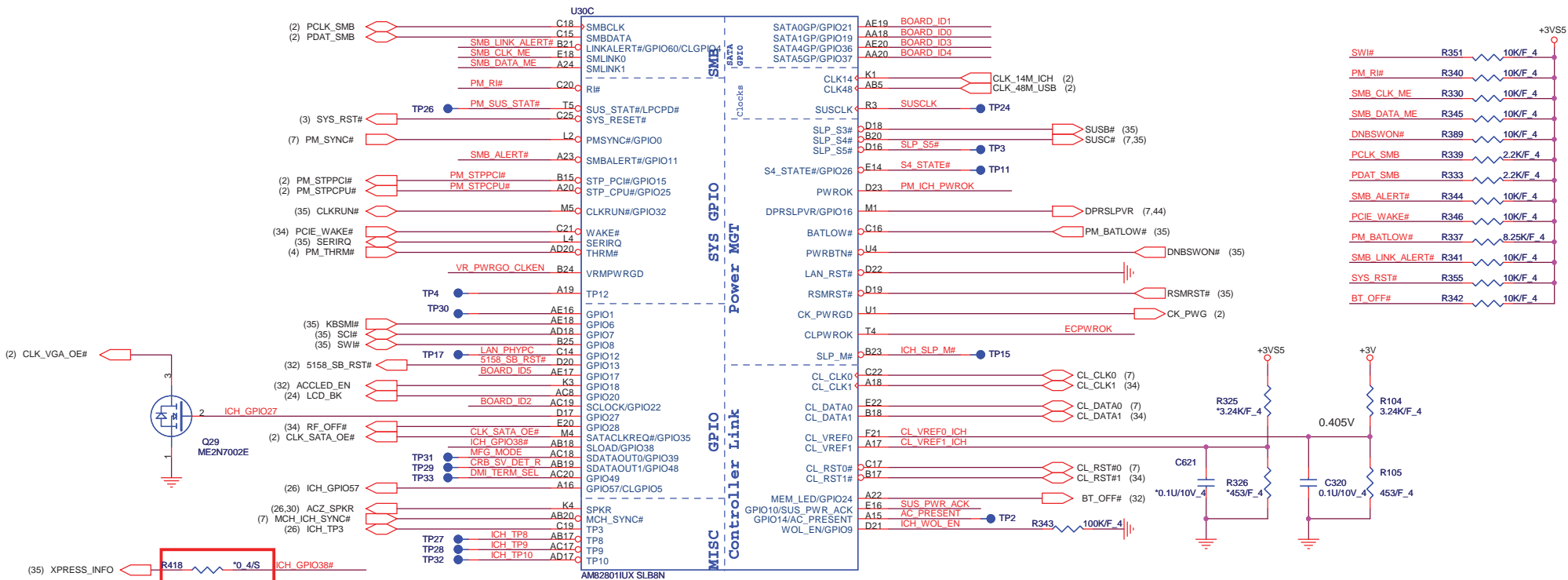
A16 swap override strap

PCI_GNT#3	Low = A16 swap override enabled Hi = Default
-----------	---

TPM physical presence

ICH_GPIO57	Low: Default
------------	--------------





PV

Update Board ID table

	Memory Select			CPU Select		
	Board ID 0 GPIO19	Board ID 1 GPIO21	Board ID 2 GPIO22	Board ID 3 GPIO36	Board ID 4 GPIO37	Board ID 5 GPIO17
RESERVE	0	0	0	0	0	0
Samsung 1G	1	0	0	0	0	0
RESERVE	0	0	0	0	0	0
RESERVE	0	0	0	0	0	0
L9600 2.13G	0	0	0	1	0	0
L9400 1.86G	0	0	0	0	1	0
U9600 1.6G	0	0	0	0	0	1

PROJECT : SP6
Quanta Computer Inc.

Size Custom Document Number **ICH9 (PM/GPIO)** Rev 1A

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Place TX DC blocking caps close ICH9.

WLAN

- (34) PCIE_RXN0
- (34) PCIE_RXP0
- (34) PCIE_TXN0
- (34) PCIE_TXP0

Delete R121,R378 due have the same pd in page 26

A3

U30D

- T25 PERN1
- T24 PERP1
- R24 PETN1
- R23 PETP1
- P25 PERN2
- P24 PERP2
- P21 PETN2
- P22 PETP2
- N23 PERN3
- N24 PERP3
- M21 PETN3
- M22 PETP3
- M25 PERN4
- M24 PERP4
- L24 PETN4
- L23 PETP4
- K24 PERN5
- K25 PERP5
- K21 PETN5
- K22 PETP5
- H24 PERN6/GLAN_RXN
- H25 PERP6/GLAN_RXP
- J24 PETN6/GLAN_TXN
- J23 PETP6/GLAN_TXP

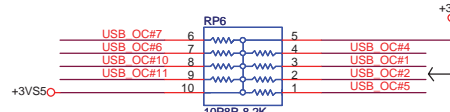
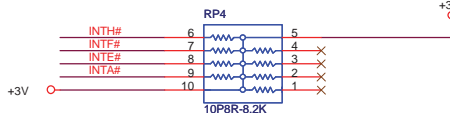
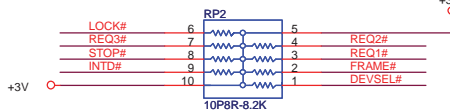
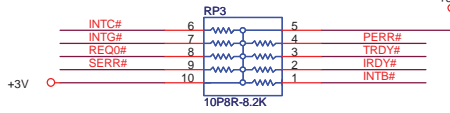
- DMIORXN
- DMIORXP
- DMIOTXN
- DMIOTXP
- DMH1RXN
- DMH1RXP
- DMH1TXN
- DMH1TXP
- DMH2RXN
- DMH2RXP
- DMH2TXN
- DMH2TXP
- DMH3RXN
- DMH3RXP
- DMH3TXN
- DMH3TXP
- DM1_CLKN
- DM1_CLKP
- DM1_ZCOMP
- DM1_IRCOMP

- V25 DML_RXN0 (7)
- V24 DML_RXP0 (7)
- U24 DML_TXN0 (7)
- U23 DML_TXP0 (7)
- W23 DML_RXN1 (7)
- W24 DML_RXP1 (7)
- V21 DML_TXN1 (7)
- V22 DML_TXP1 (7)
- Y24 DML_RXN2 (7)
- Y25 DML_RXP2 (7)
- Y21 DML_TXN2 (7)
- Y22 DML_TXP2 (7)
- AB24 DML_RXN3 (7)
- AB25 DML_RXP3 (7)
- AA23 DML_TXN3 (7)
- AA24 DML_TXP3 (7)
- T21 CLK_PCIE_ICH# (2)
- T22 CLK_PCIE_ICH (2)
- AB21 DMI_IRCOMP_R
- AB22

- USBP0- (32)
- USBP0+ (32)
- USBP1- (32)
- USBP1+ (32)
- USBP2- (32)
- USBP2+ (32)
- USBP3- (24)
- USBP3+ (24)
- USBP4- (34)
- USBP4+ (34)
- USBP5- (32)
- USBP5+ (32)
- USBP6
- USBP7
- USBP8
- USBP9
- USBP10
- USBP11

USB port	Assignment function
USB0	USB Connector
USB1	USB Card reader
USB2	USB Connector
USB3	USB Camera module
USB4	Reserve for Mini Card
USB5	Bluetooth
USB6	NA
USB7	NA
USB8	NA
USB9	NA
USB10	NA
USB11	NA

SI2-A23



SI2-A23



A14 R373 delete

U30B

- A11 AD0
- B12 AD1
- A10 AD2
- C12 AD3
- A8 AD4
- E10 AD5
- C11 AD6
- A7 AD7
- B9 AD8
- D8 AD9
- A4 AD10
- E8 AD11
- A3 AD12
- D9 AD13
- C2 AD14
- D7 AD15
- B3 AD16
- D11 AD17
- B6 AD18
- D5 AD19
- D3 AD20
- E3 AD21
- E4 AD22
- E2 AD23
- A4 AD24
- B2 AD25
- C4 AD26
- D1 AD27
- E2 AD28
- A3 AD29
- J4 AD30
- H2 AD31

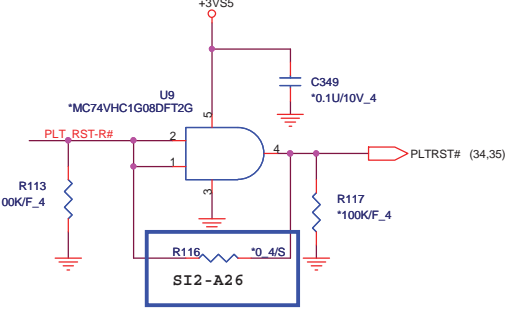
- REQ0#
- GNT0#
- REQ1#/GPIO50
- GNT1#/GPIO51
- REQ2#/GPIO52
- GNT2#/GPIO53
- REQ3#/GPIO54
- GNT3#/GPIO55
- C/BE#0
- C/BE#1
- C/BE#2
- C/BE#3
- IRDY#
- PAR
- PCIRST#
- PERR#
- DEVSEL#
- SERR#
- LOCK#
- SERR#
- STOP#
- TRDY#
- FRAME#
- PLTRST#
- PCICK#
- PME#

- G4 REQ0#
- E1 GNT0# (26)
- A9 REQ1#
- E12 GNT1#
- B11 REQ2#
- C10 GNT2#
- D6 REQ3#
- C6 GNT3# (26)
- D10
- A5
- E6
- C8
- C3 IRDY#
- B1
- A7
- D4
- C5
- H5
- A6
- A2
- B8
- A21
- B5
- T1

Interrupt I/F

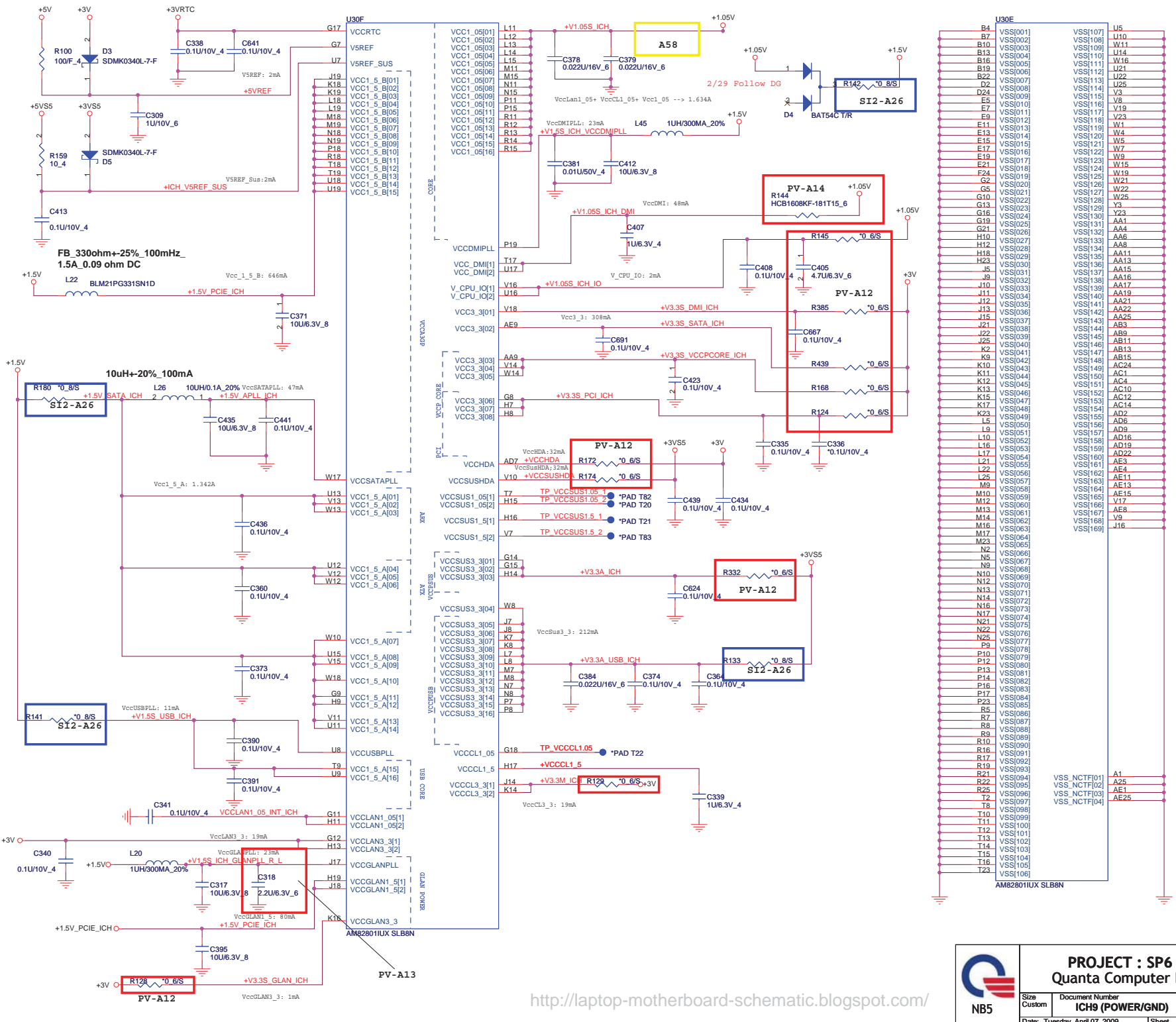
- F1 INTA#
- F5 INTB#
- F2 INTG#
- C7 INTD#

- G3 INTE#
- G1 INTF#
- E3 INTG#
- H4 INTH# (32)

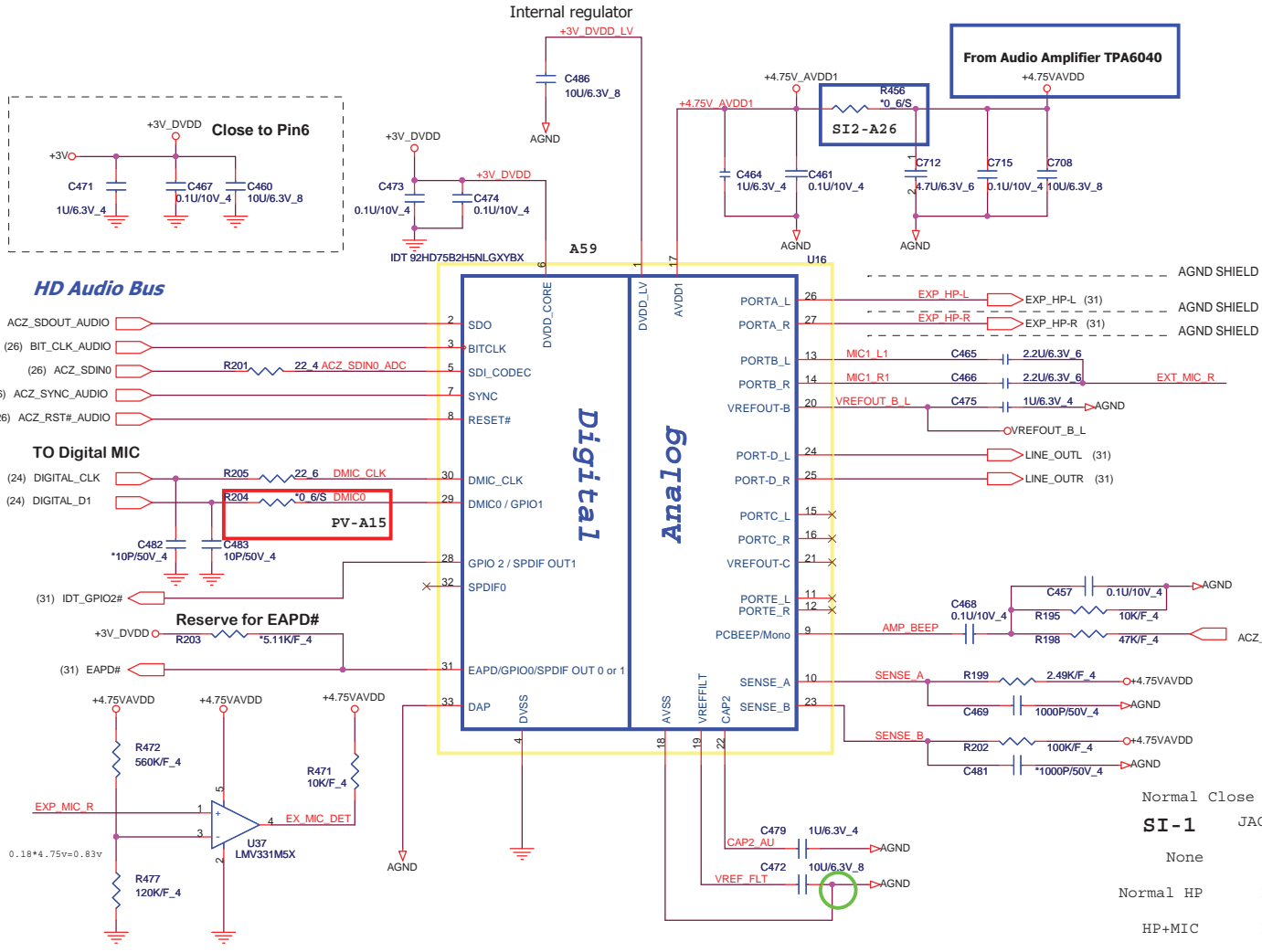


PROJECT : SP6
Quanta Computer Inc.

Size Custom	Document Number ICH9 (USB/PCIE/DMI)	Rev 1A
Date: Tuesday, April 07, 2009 Sheet 28 of 49		



	PROJECT : SP6 Quanta Computer Inc.	
	Size Custom Document Number ICH9 (POWER/GND)	Rev 1A
Date: Tuesday, April 07, 2009		Sheet 29 of 49

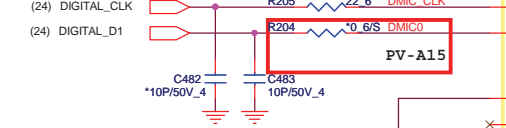


PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	External MIC
PORT C	X
PORT D	Internal Speckers
DM	DIGITAL MIC

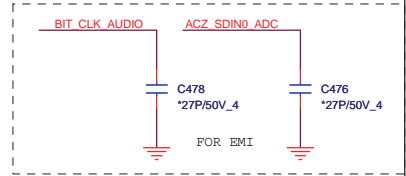
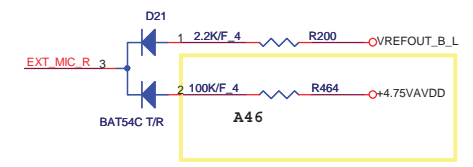
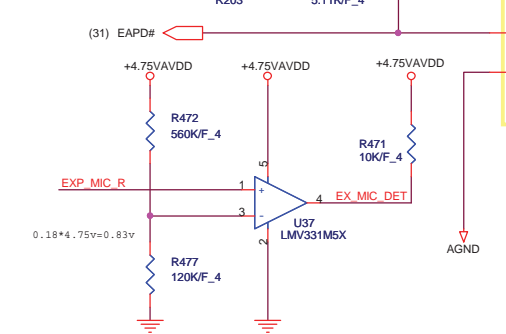
HD Audio Bus



TO Digital MIC

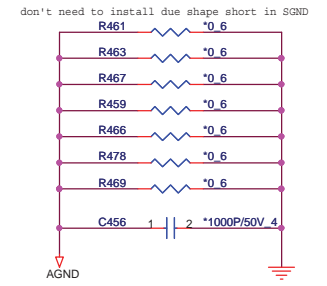


Reserve for EAPD#

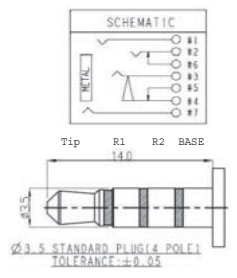
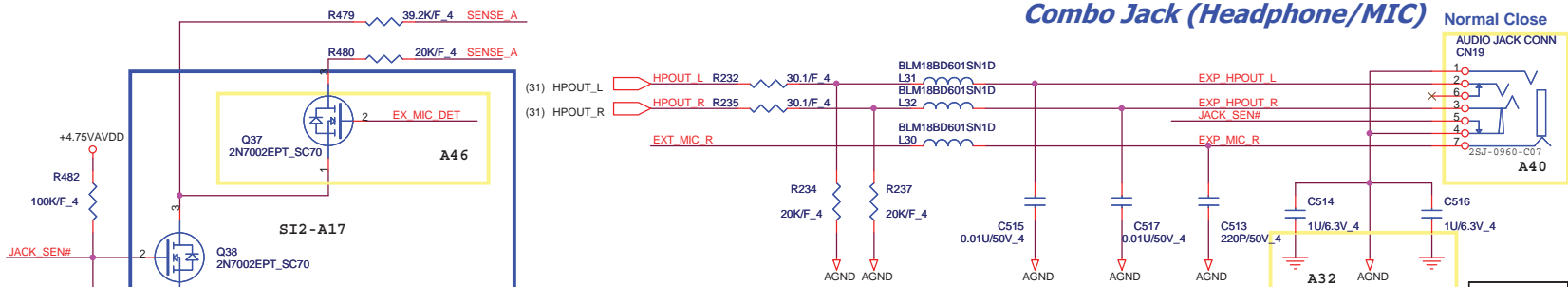


SA_A# --> Headphone out
SA_B# --> EXT MIC

Normal Close	JACK_SEN#	EX_MIC_DET
None	Low	HIGH
Normal HP	HIGH	Low
HP+MIC	HIGH	HIGH



Combo Jack (Headphone/MIC)



- TIP Headphone Left
- R1 Headphone Right
- R2 GND
- BASE MIC

<http://laptop-motherboard-schematic.blogspot.com/>

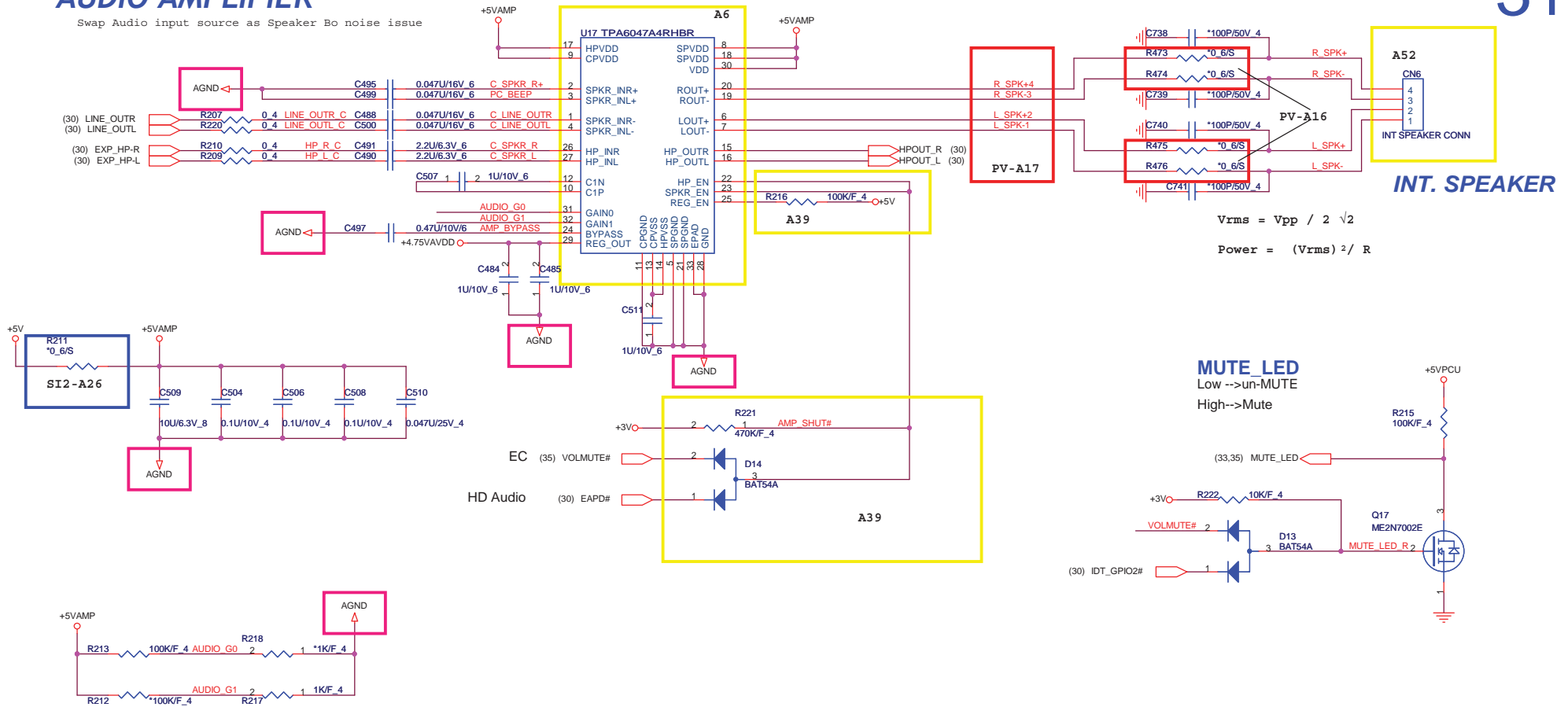


PROJECT : SP6
Quanta Computer Inc.

Size Custom	Document Number Azalia IDT92HD75B2	Rev 1A
Date: Tuesday, April 07, 2009		Sheet 30 of 49

AUDIO AMPLIFIER

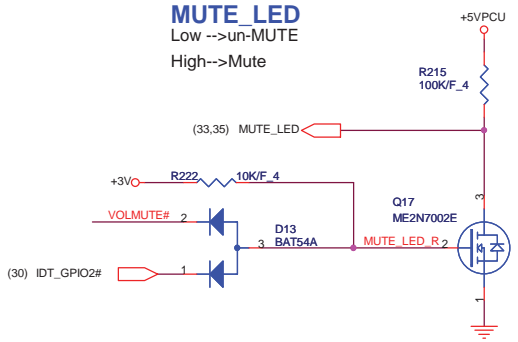
Swap Audio input source as Speaker Bo noise issue



$$V_{rms} = V_{pp} / 2 \sqrt{2}$$

$$Power = (V_{rms})^2 / R$$

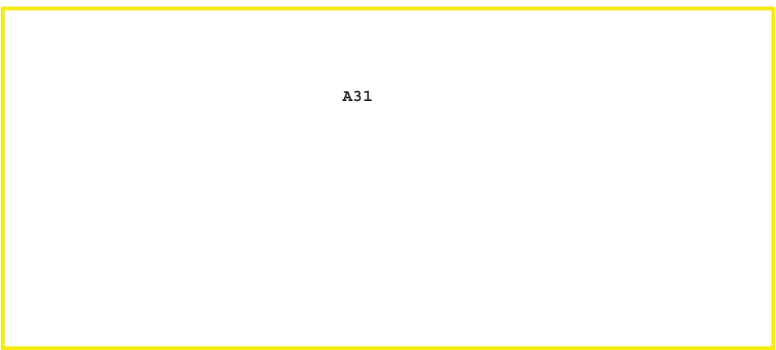
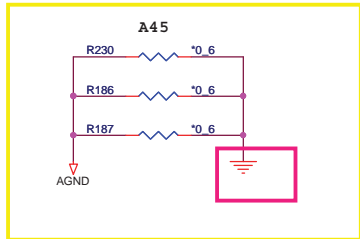
MUTE_LED
Low --> un-MUTE
High --> Mute



6047A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

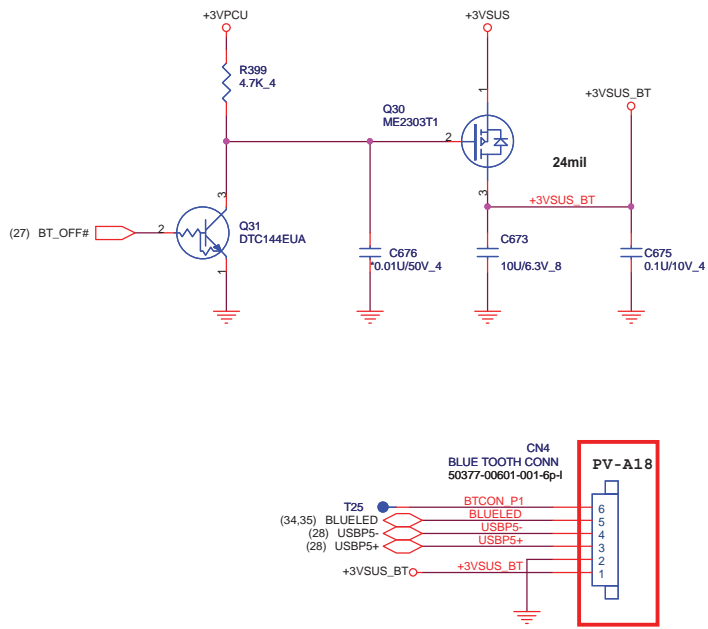
PIN23 SPKR_EN
TPA6047A4 High enable



PROJECT : SP6
Quanta Computer Inc.

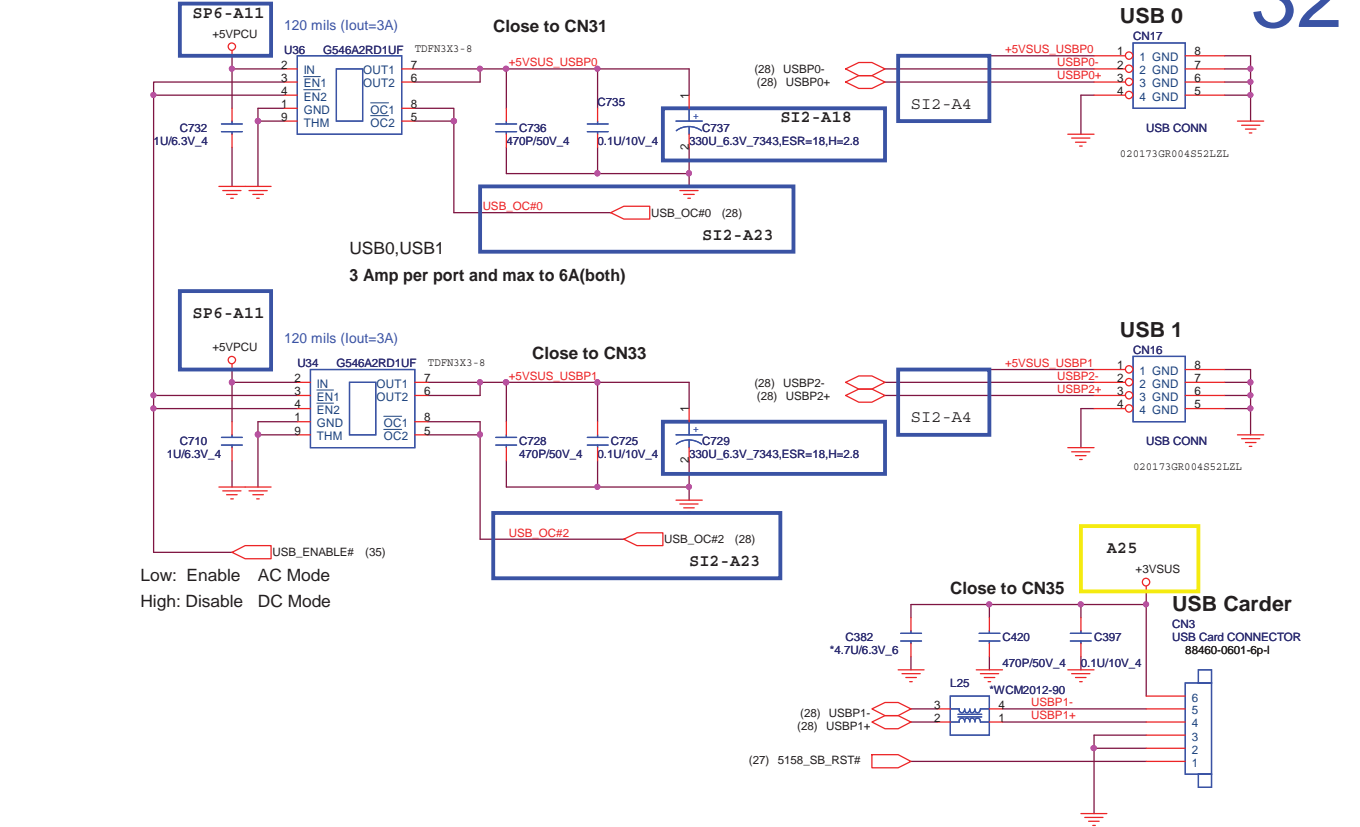
Size Custom	Document Number	Rev 1A
Audio Amplifier TPA6047A4		
Date: Tuesday, April 07, 2009	Sheet 31	of 49

BLUETOOTH



Change CN4 layout footprint to 50377-00601-001-6p-1

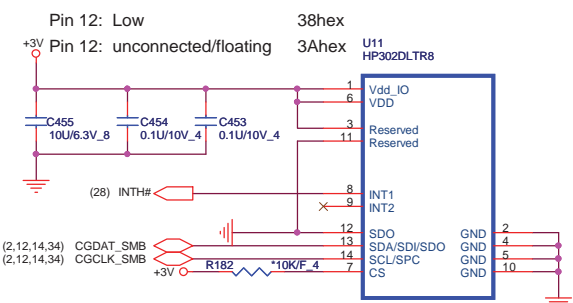
LEFT SIDE USBX2



Low: Enable AC Mode
High: Disable DC Mode

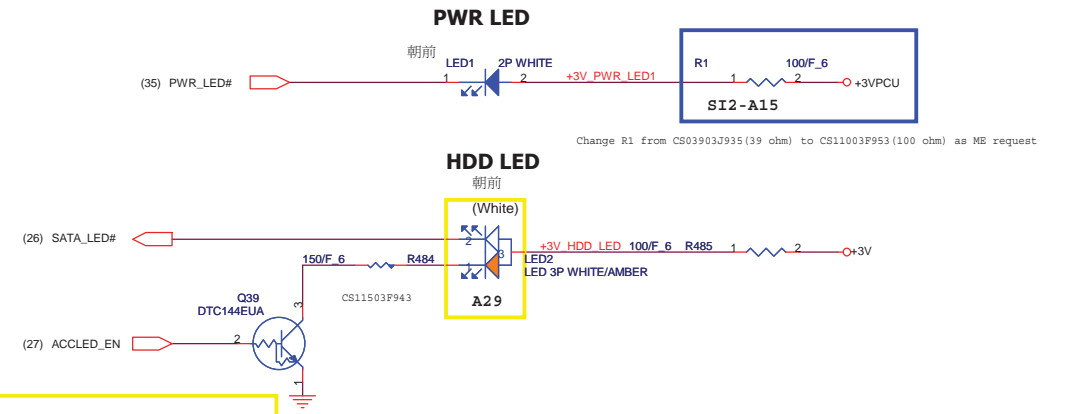
Accelerometer Sensor

SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



Change R181 to no stuff as internal pull high

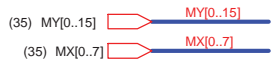
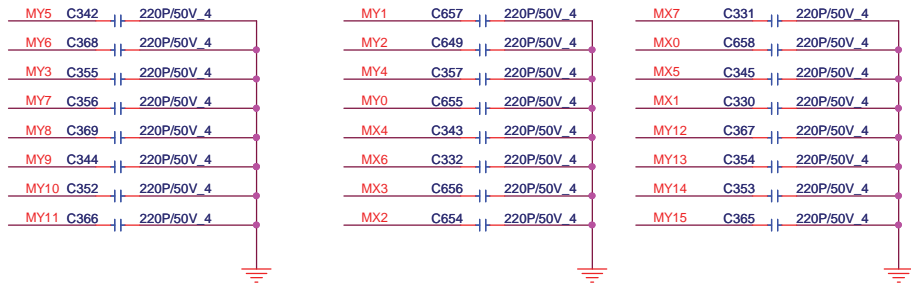
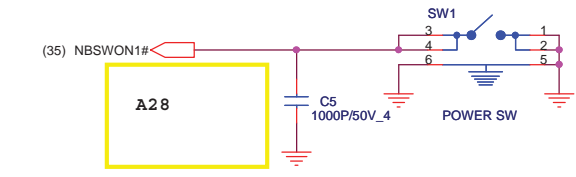
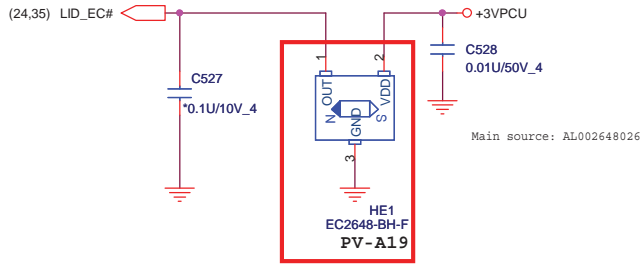
LED



use a single 80 mil copper fill between digital ground and audio ground. None of the 0 ohm resistors should be used.

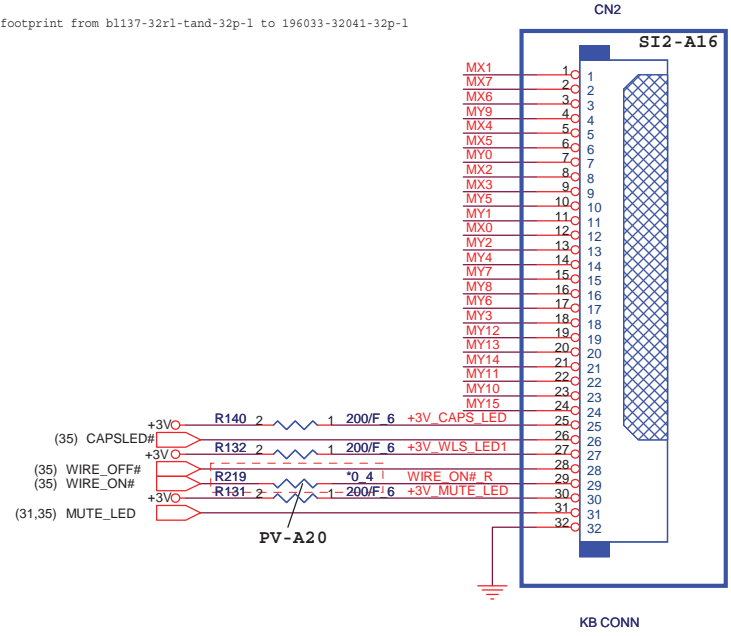
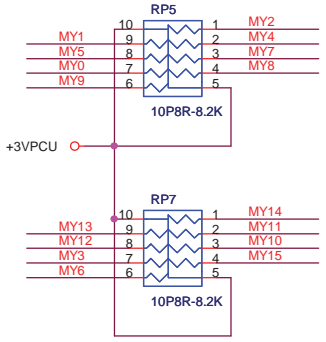
<http://laptop-motherboard-schematic.blogspot.com/>

	PROJECT : SP6 Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number BT/WC/FP/USB/G-sensor	
Sheet 32 of 49			



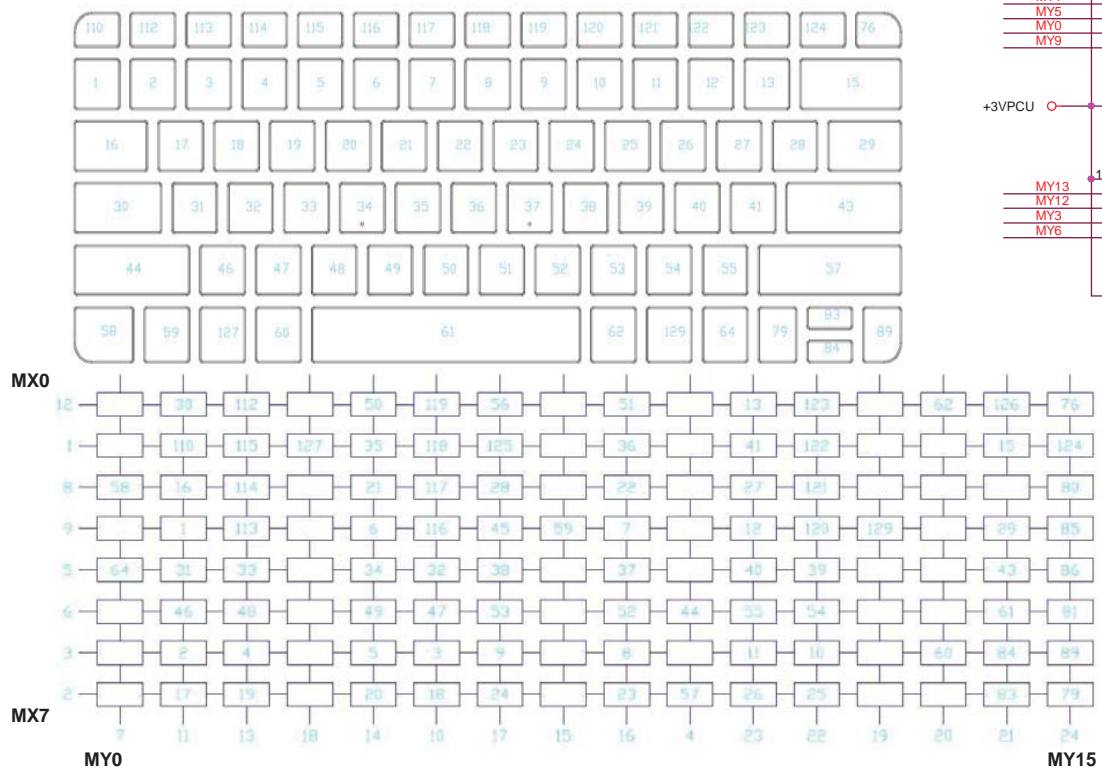
Modify CN2 footprint from b1137-32r1-tand-32p-1 to 196033-32041-32p-1

KEYBOARD PULL-UP



- Caps Lock LED 2 Pins 30mA
- Wireless LED 3 pins
- MUTE_LED 2 Pins
- Charge LED 3 pins

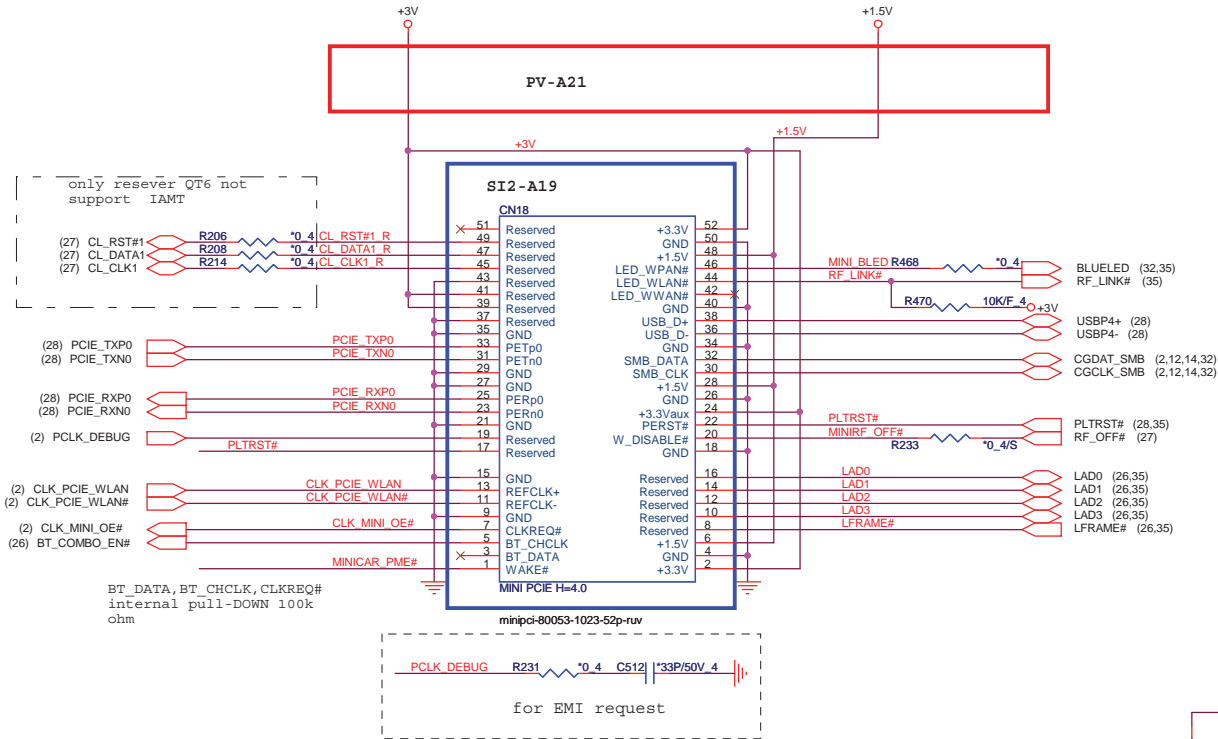
Pin 32 Pin 1



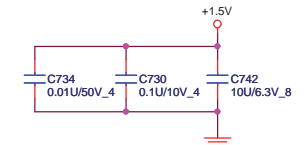
	PROJECT : SP6 Quanta Computer Inc.		Rev 1A
	Size B	Document Number KB/CAP	

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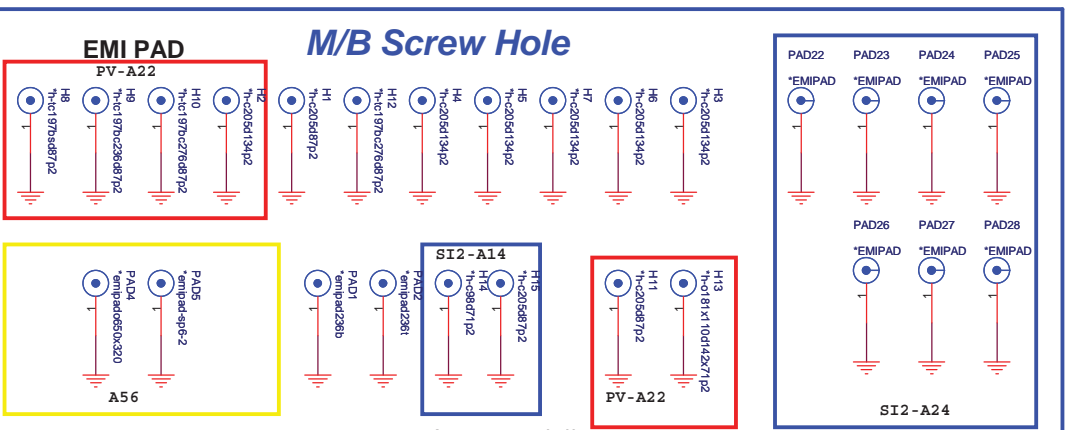
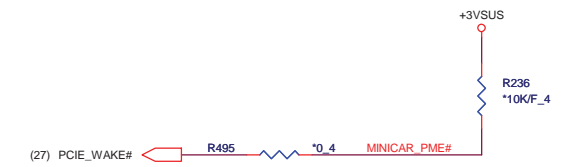
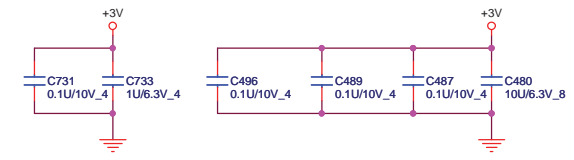
Full size Mini-Card
WLAN



Modify CN18 footprint from from minipci-asob241-r40n-7h-52p-ruv to minipci-80053-1023-52p-ruv



Close to CN38



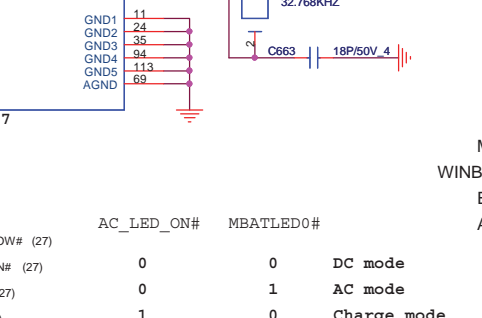
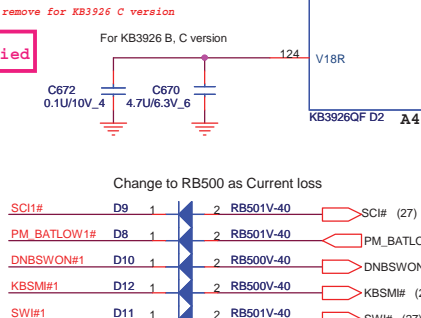
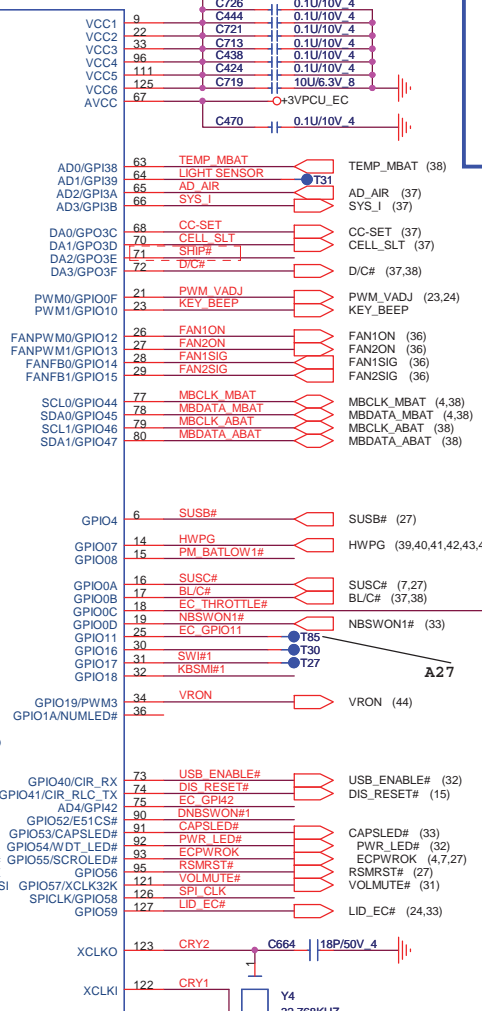
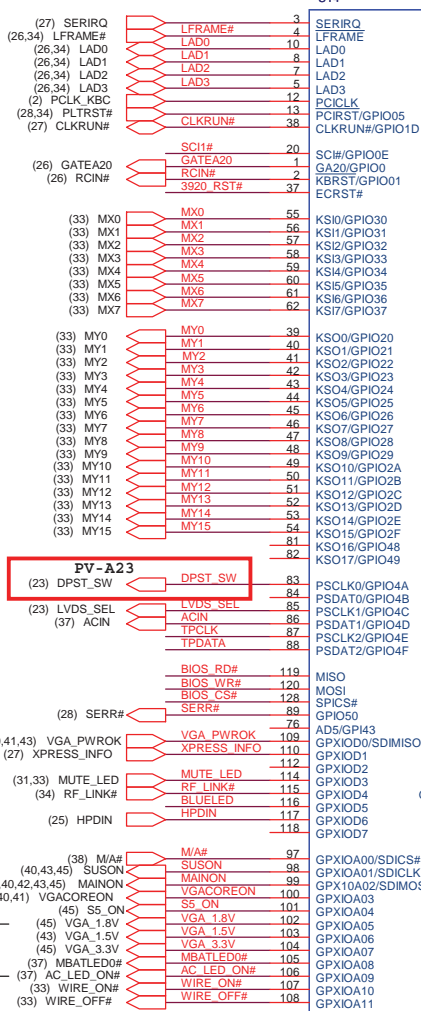
Delete PAD3, PAD6 and add H15

<http://laptop-motherboard-schematic.blogspot.com/>

	PROJECT : SP6 Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number MINIPCIE/Hole	Date: Tuesday, April 07, 2009
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Change U20 layout footprint

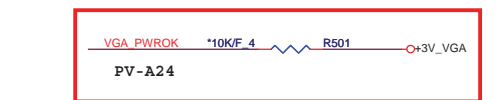
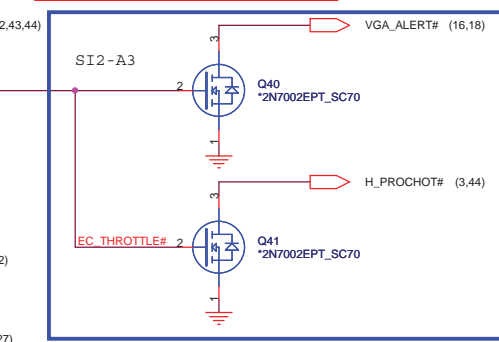
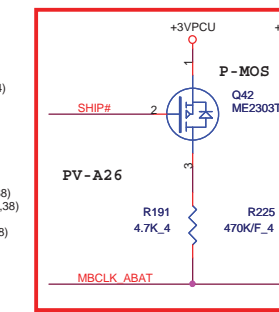
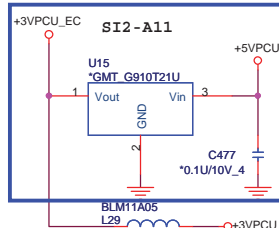
to LQFP128-16X16-4-AA1



Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier

Add T37,T38,T39 for EC

Delete T10 and tie pin 117 from Lan for DSM



Socket: DG008000031

DB-2 From SI-1

8M bit 16M bit

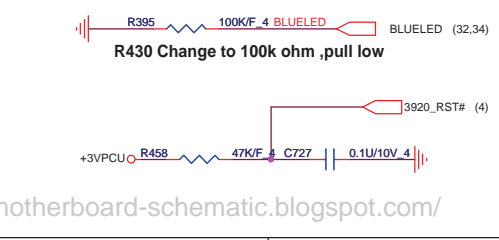
MXIC AKE5GFK0Z09 AKE38FP0Z00

WINBOND AKE3GFP0N08 AKE38ZP0N01 AKE38FP0N01

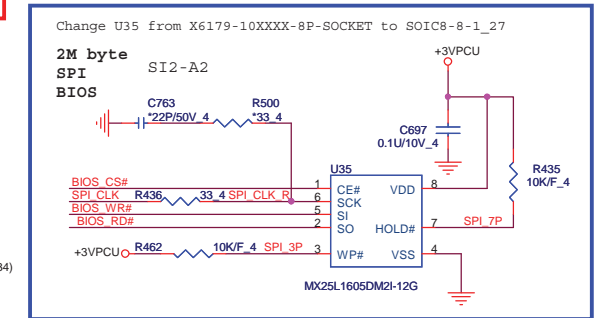
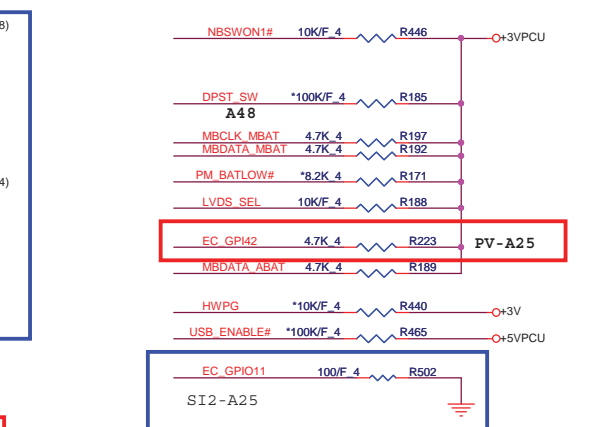
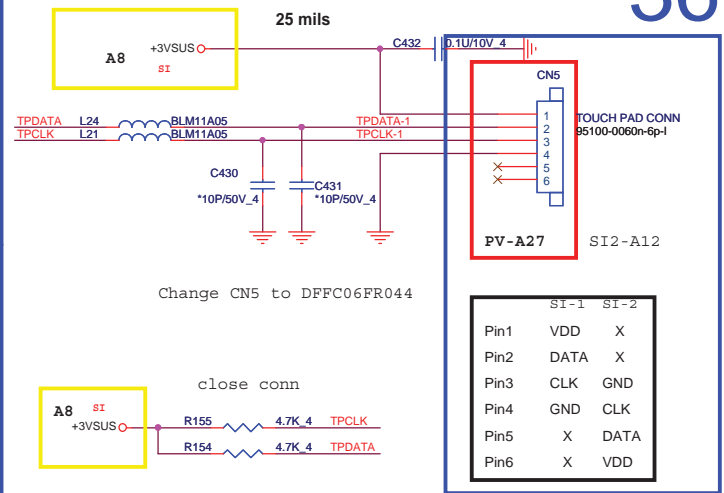
EON AKE3GZP0Q00 AKE38ZA0Q00

AMIC AKE3GZP0801 AKE38ZN0800

R430 Change to 100k ohm ,pull low



TOUCH PAD CONNECTOR



Change U35 from X6179-10XXXX-8P-SOCKET to SOIC8-8-1_27

2M byte SPI BIOS

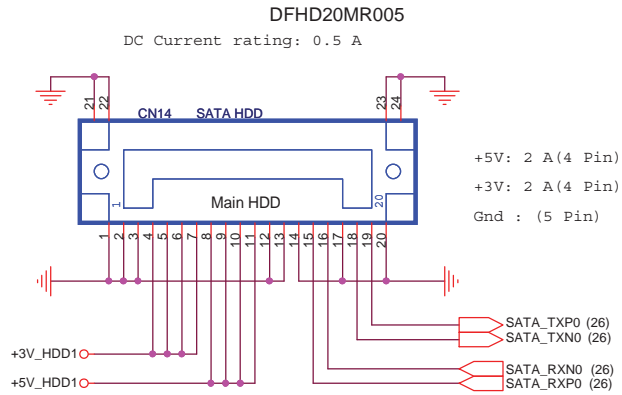
MX25L1605DM21-12G

PROJECT : SP6
Quanta Computer Inc.

Size Custom Document Number KB3926/ROM/TP Rev 2B

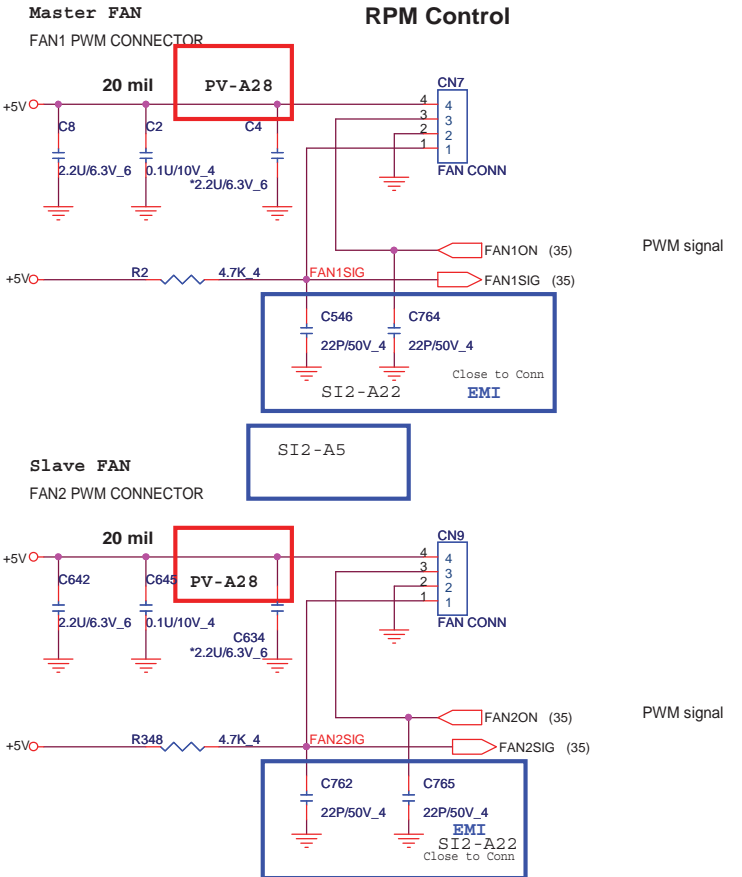
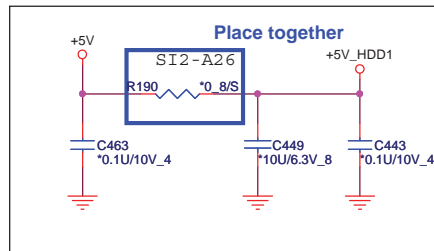
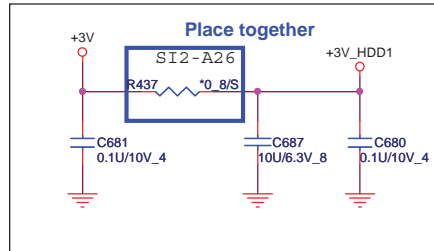
Date: Tuesday, April 07, 2009 Sheet 35 of 49

SATA 1.8" HDD CONNECTOR



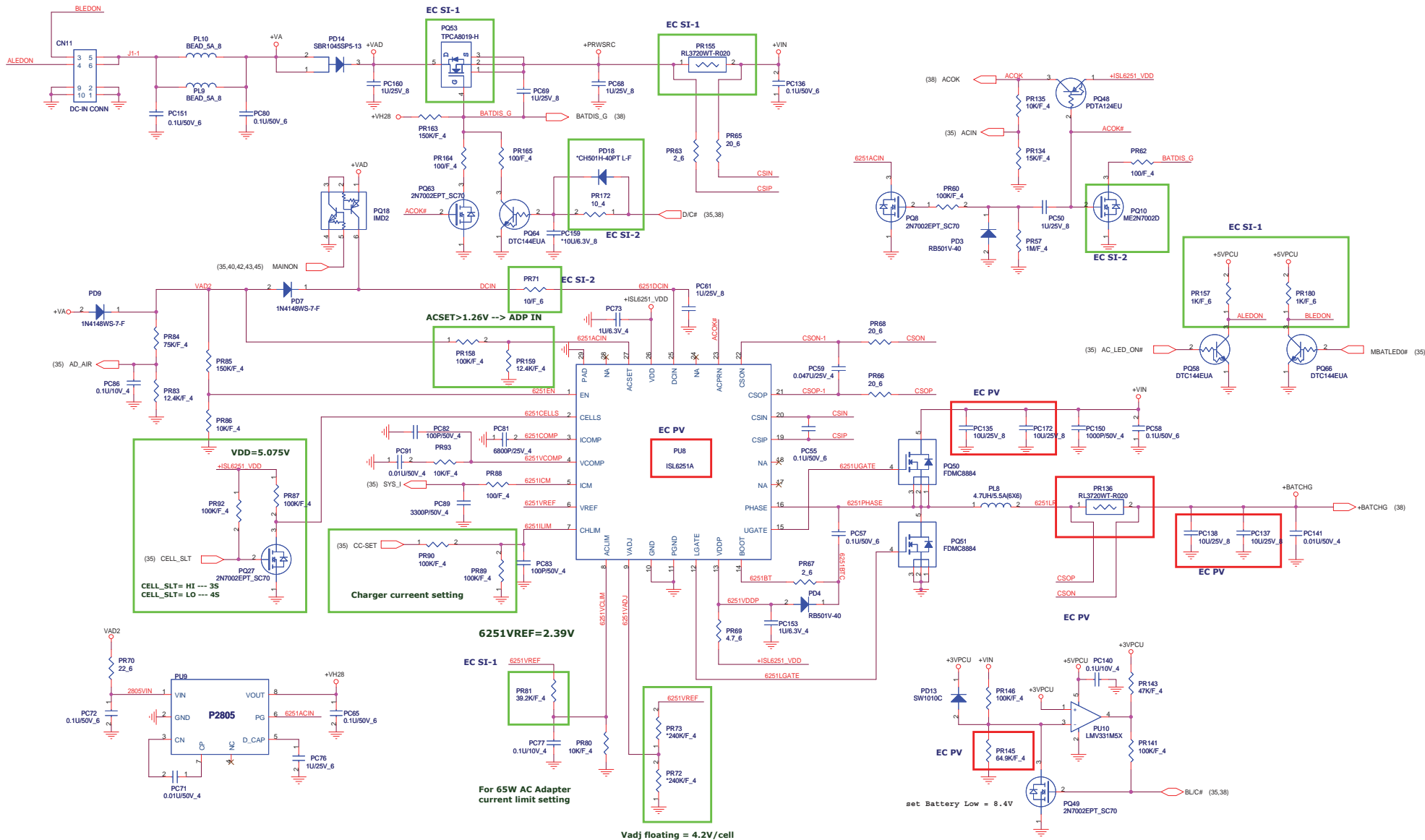
Modify 固定孔 Size as SMT request

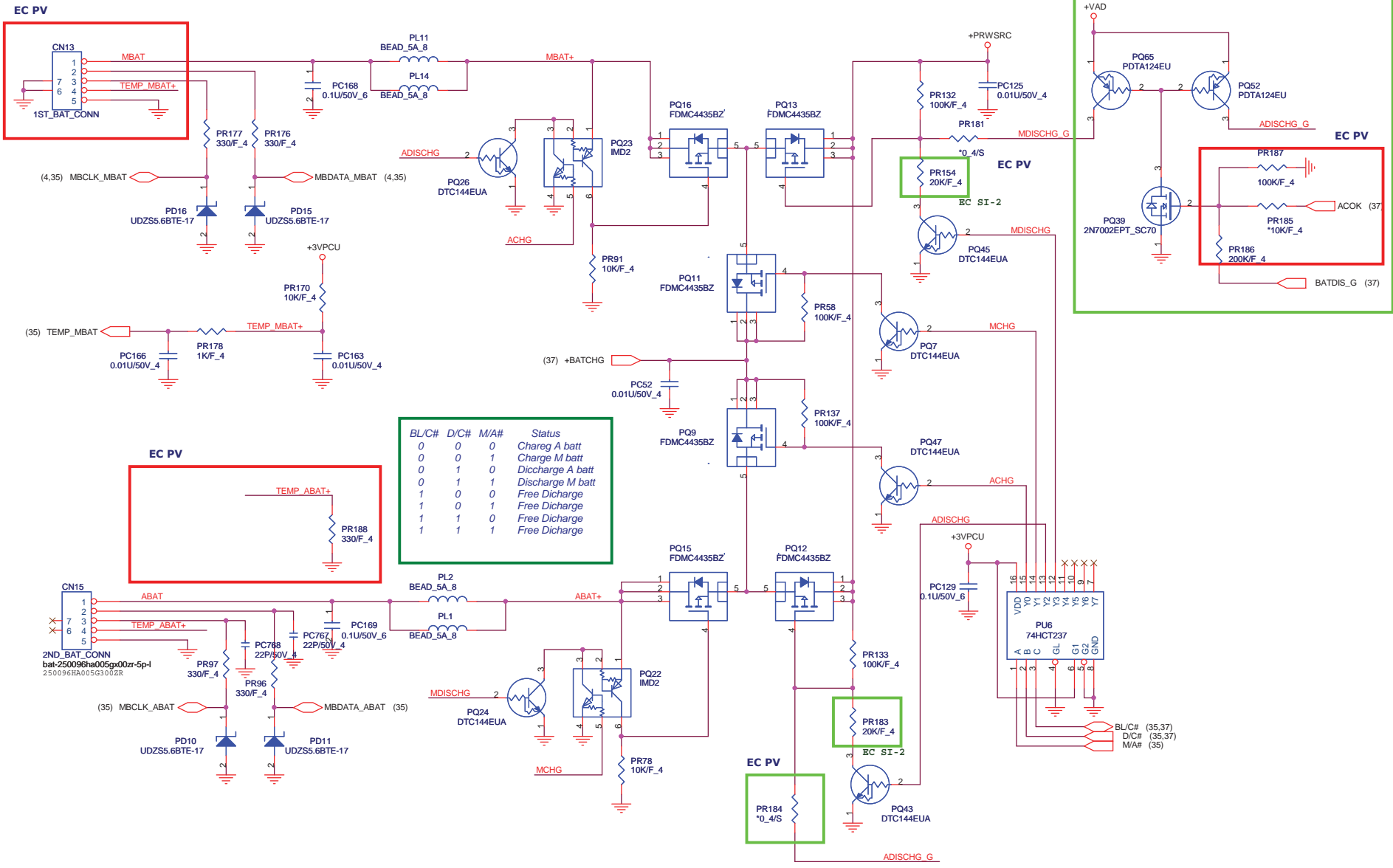
GS12201-1011-9F-20P-L-QT6



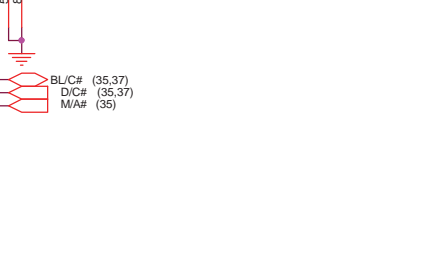
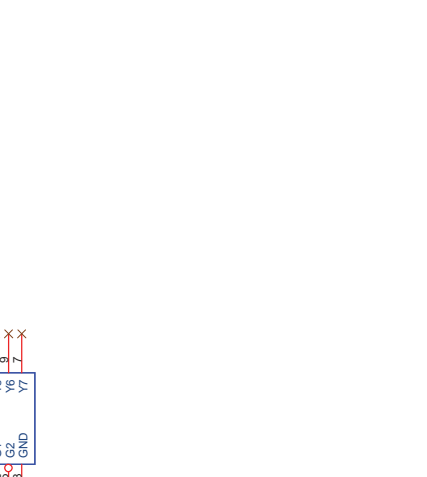
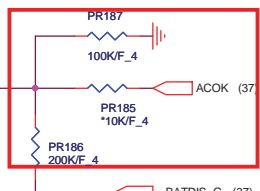
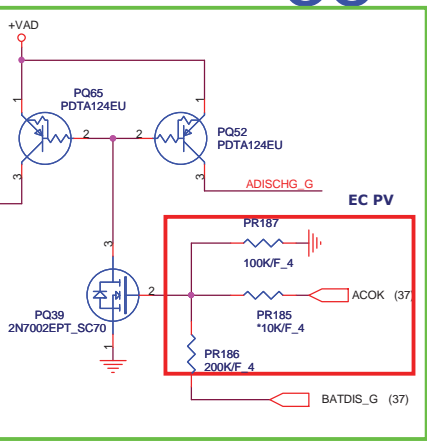
PROJECT : SP6
Quanta Computer Inc.

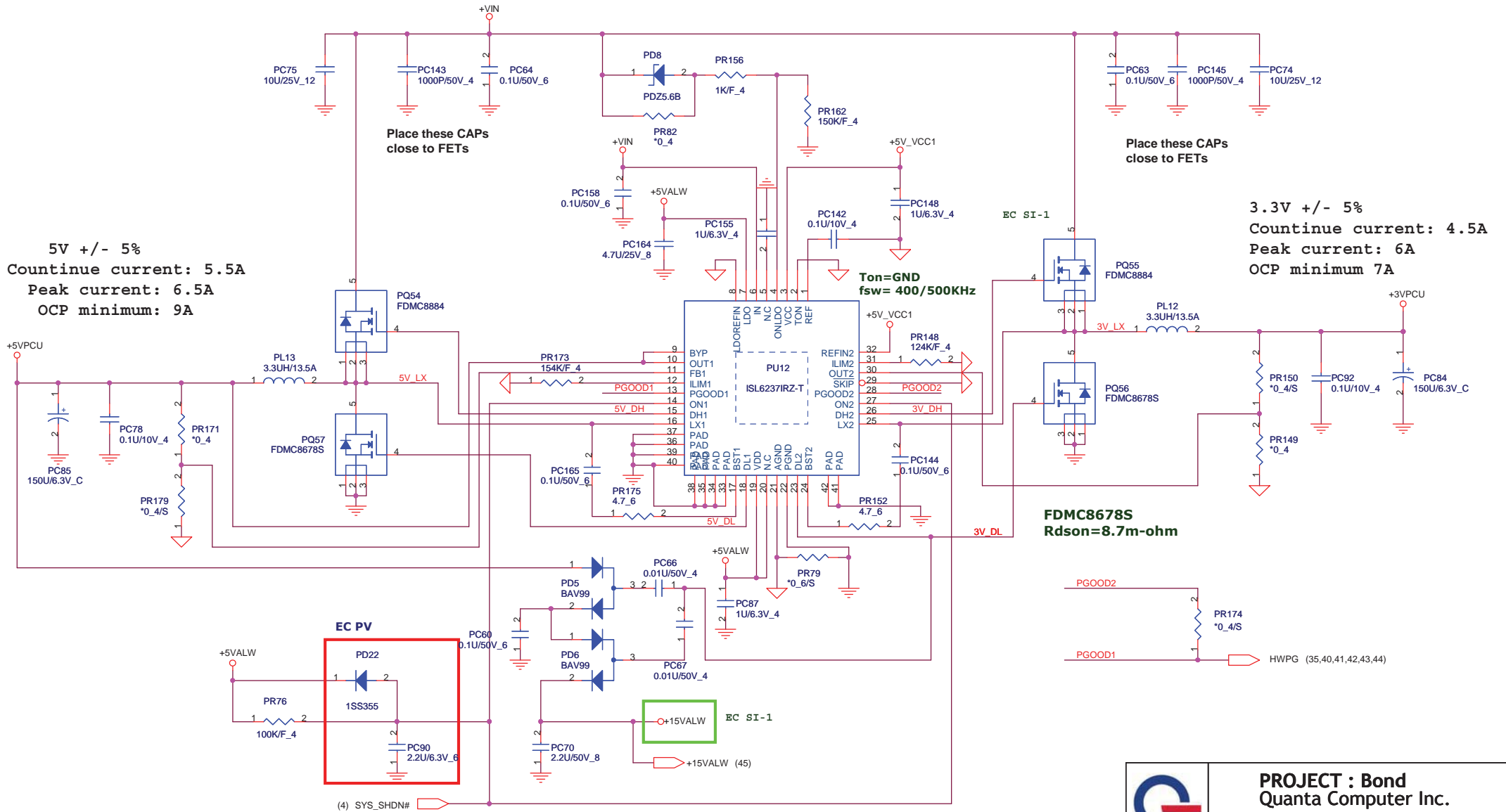
Size B	Document Number Fan1 and Fan2	Rev 1A
Date: Tuesday, April 07, 2009		Sheet 36 of 49






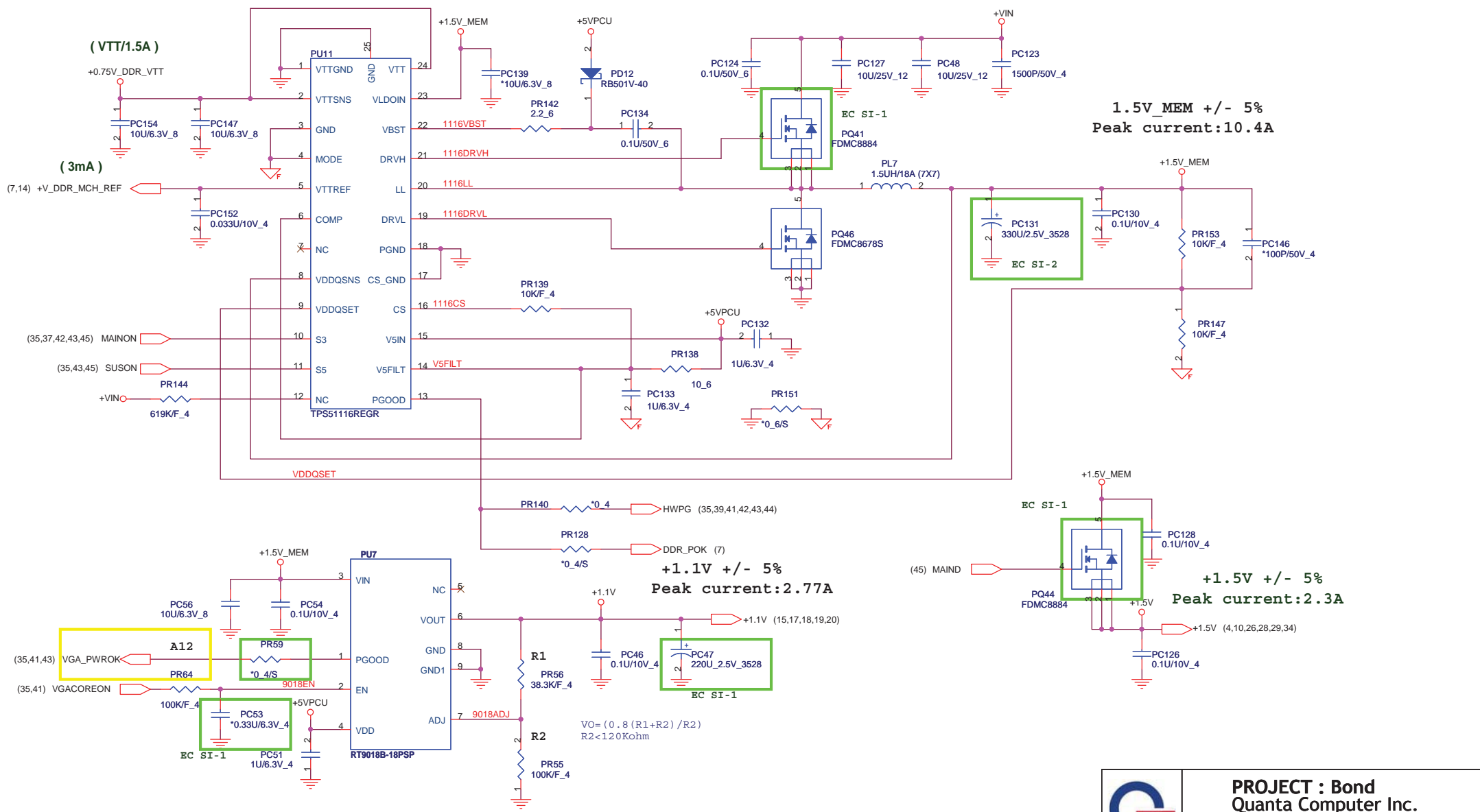
BL/C#	D/C#	M/A#	Status
0	0	0	Charge A batt
0	0	1	Charge M batt
0	1	0	Discharge A batt
0	1	1	Discharge M batt
1	0	0	Free Discharge
1	0	1	Free Discharge
1	1	0	Free Discharge
1	1	1	Free Discharge





	PROJECT : Bond Quanta Computer Inc.	
	Size B Date: Tuesday, April 07, 2009	Document Number +5V/+3V Sheet 39 of 49

(7,9,10,12,13,14) +1.5V_MEM



1.5V_MEM +/- 5%
Peak current: 10.4A

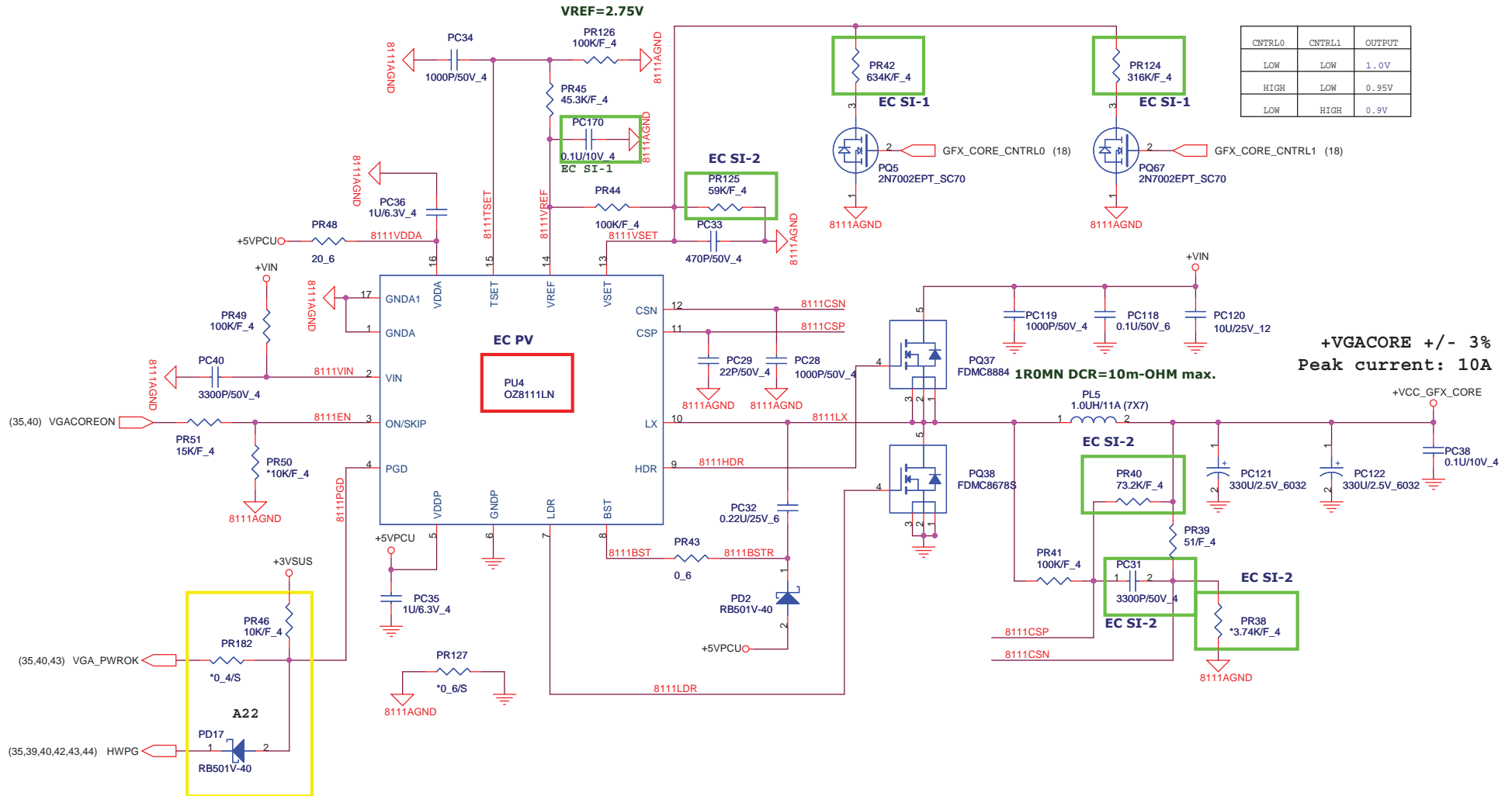
+1.1V +/- 5%
Peak current: 2.77A

+1.5V +/- 5%
Peak current: 2.3A



PROJECT : Bond
Quanta Computer Inc.

Size B	Document Number +1.5V_MEM+1.1V	Rev 1A
Date: Tuesday, April 07, 2009 Sheet 40 of 49		



CNTRL0	CNTRL1	OUTPUT
LOW	LOW	1.0V
HIGH	LOW	0.95V
LOW	HIGH	0.9V

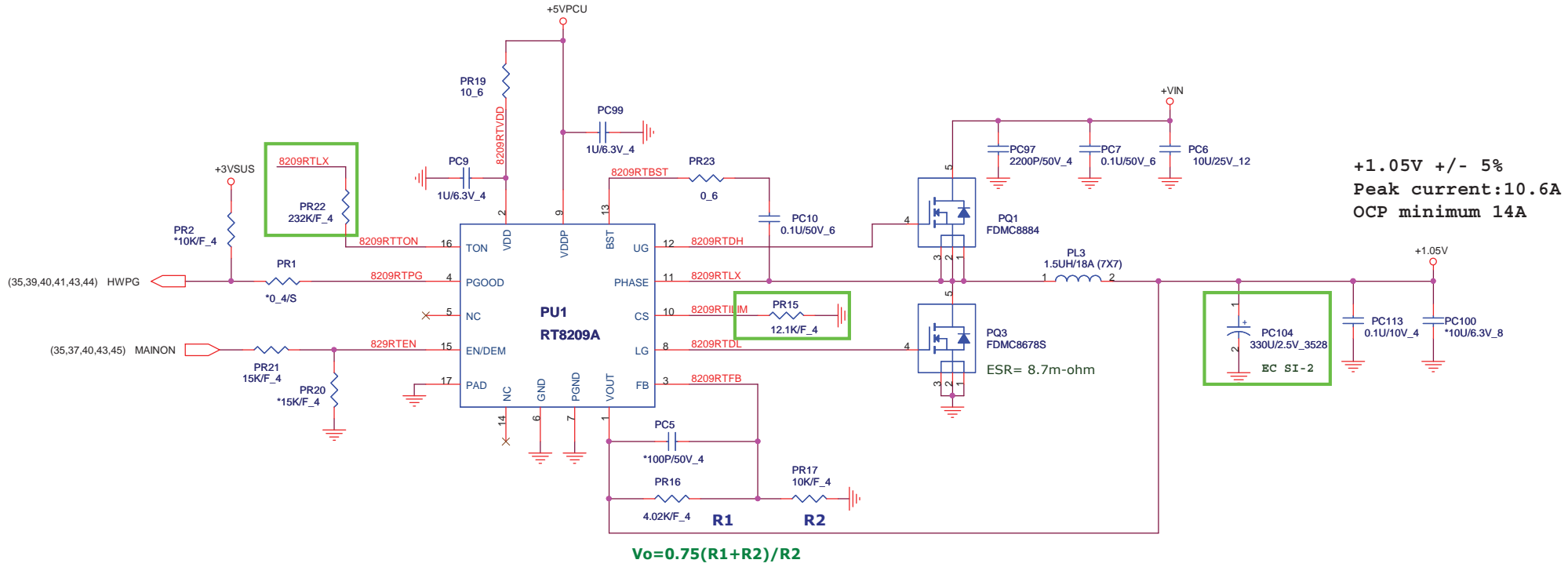
+VGACORE +/- 3%
Peak current: 1.0A




PROJECT : Bond
Quanta Computer Inc.

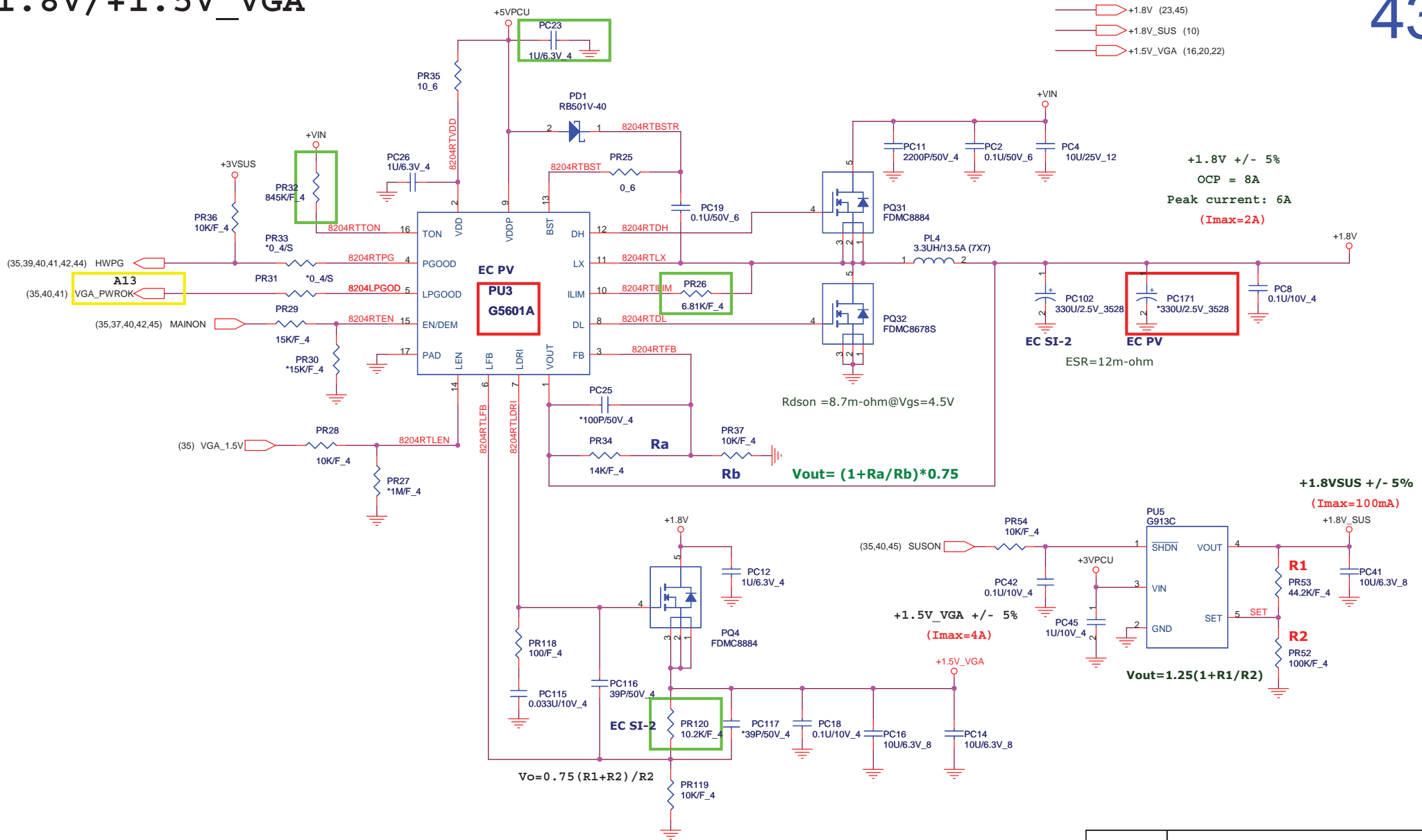
Size B	Document Number VGACORE	Rev 1A
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VCCP1.05V



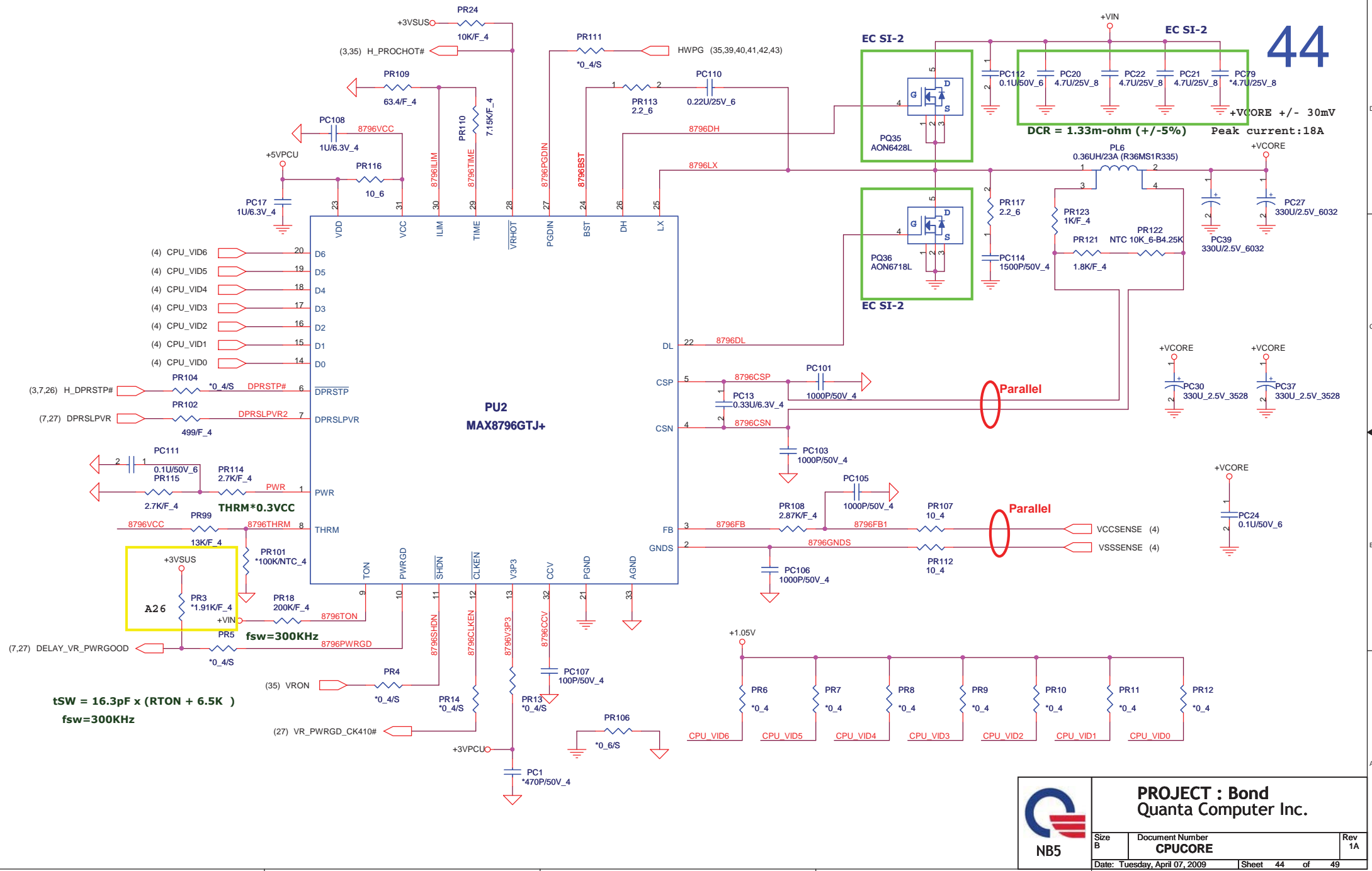
	PROJECT : Bond Quanta Computer Inc.	
	Size B Date: Tuesday, April 07, 2009	Document Number +1.05V/+1.5V

+1.8V/+1.5V_VGA



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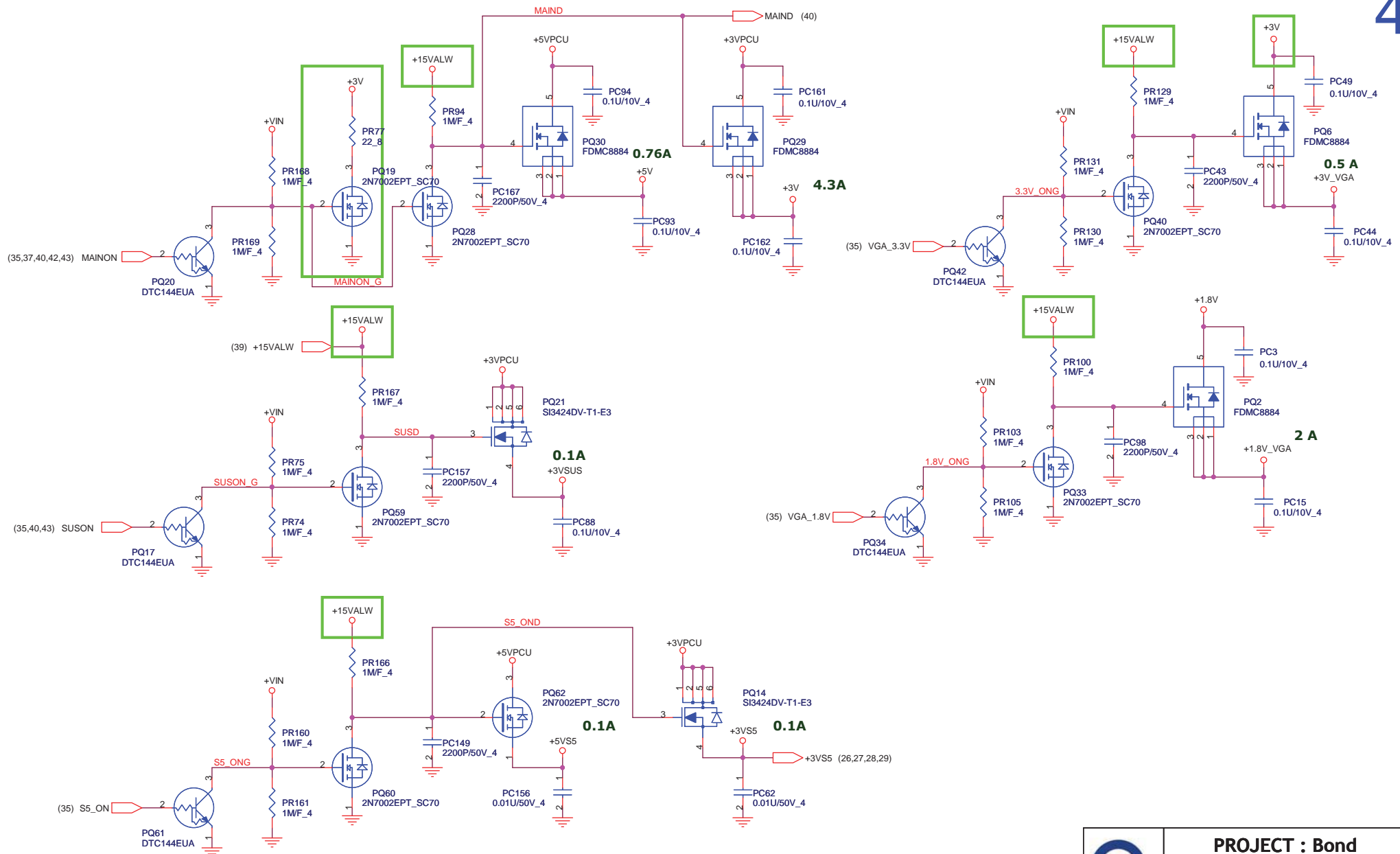


$t_{SW} = 16.3pF \times (R_{TON} + 6.5K)$
 $f_{sw} = 300KHz$



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 Quanta Computer Inc.**

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DISCHARGER		
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