

- POWER**
- AC/BATT CONNECTOR
- BATT CHARGER
- CPU CORE
- 5V/ 3.3VSTBY
- 1.5V/ 0.75_VTT_DDR
- 1.1VS
- 1.05VS
- 1.8VS LDO
- 2.5VS LDO
- 1.1VSTBY_SB LDO
- DGPU VCORE
- SUS/ RUN PWR Switch

- EMI/ Moat CAP
- History

DDR3-SODIMM Page 5 DDR III 1066/ 1333MHZ

DDR3-SODIMM Page 6 DDR III 1066/1333MHZ

Dual/ Single Core CPU AMD Danube Dual:35W Page 2, 3, 4

DGPU with Muxless ATI Seymour/ Whistler

15.6"/17.3" Muxless Hybrid:
Seymour 64bit 15W + DDR3 x4
Whistler 128bit 25W + DDR3 x8
M2 package 29 x 29 FCBGA962

Seymour XT:
HPMH-10-0020000049G

Whistler Pro:
HPMH-10-0020000050G

Page 15, 16, 17, 18, 19, 20, 21

North Bridge ATI RS880M

HPMH-10-0010000096G

Page 7, 8, 9, 10

HDD Conn 2nd for 17.3" only Page 27

HDD Conn Cable SATA 3: 6Gbps

ODD Conn Cable SATA 2: 3Gbps
Zero Power ODD Intel Saving 100 ~ 160mW

WebCam Conn Cable
White LED: Enable Sensor OVT 9726 Dual Mic Page 28

Fingerprint Cable
Validity Module VFM5131 Dual LED x1: White normal, Amber not recognized Page 28

SIO ITE8518 Page 29

SPI 512KB 2.5

Crystal Free 32.768K

Charge LED

HP Logo LED Module

Thermal Page 30

FAN Conn Page 30

Keyboard Conn Page 29

Touchpad Conn Page 28

Lid Switch Page 28

PWR Button / White LEDx1 Blink White: Standby

Quick Web Button / LED x1

South Bridge AMD SB820M

HPMH-10-0010000106G

Page 11, 12, 13, 14

SPI BIOS SPI

G SENSOR ST Micro HP3DC Page 27

RTC Cell Conn Cable LPC

AUDIO CODEC IDT 92HD80TA Page 35, 36, 37

LDO TPS793475DBVR

SPK AMP TPA3113D2

HP AMP TPA6130A2

Woofer AMP TPA3111D1

Realtek Gb LAN RTL8111E-VB-GR W/ASPM Page 32

No cable: NIC auto disabled.

Magnetic

RJ45 LED White x1 for connectivity, Amber x1 for activity

Internal Speaker Conn x4 speakers

Internal DMic Conn To Webcam

Microphone x1

Headphone Microphone Combo Conn x2

WOOFER CONN

HDMI Conn Page 25

D-sub Conn Page 26

LVDS + Touch Page 24
15"/17": 2 ch HD+ 1600x900
2 ch FHD 1920x1080

Cardreader Realtek RTS5209 Page 31

USB3.0 TI TUSB7320 Page 33

WLAN Half MINI-CARD Page 30

USB Conn Wake Up

USB Conn Wake Up

Standby LED White blink

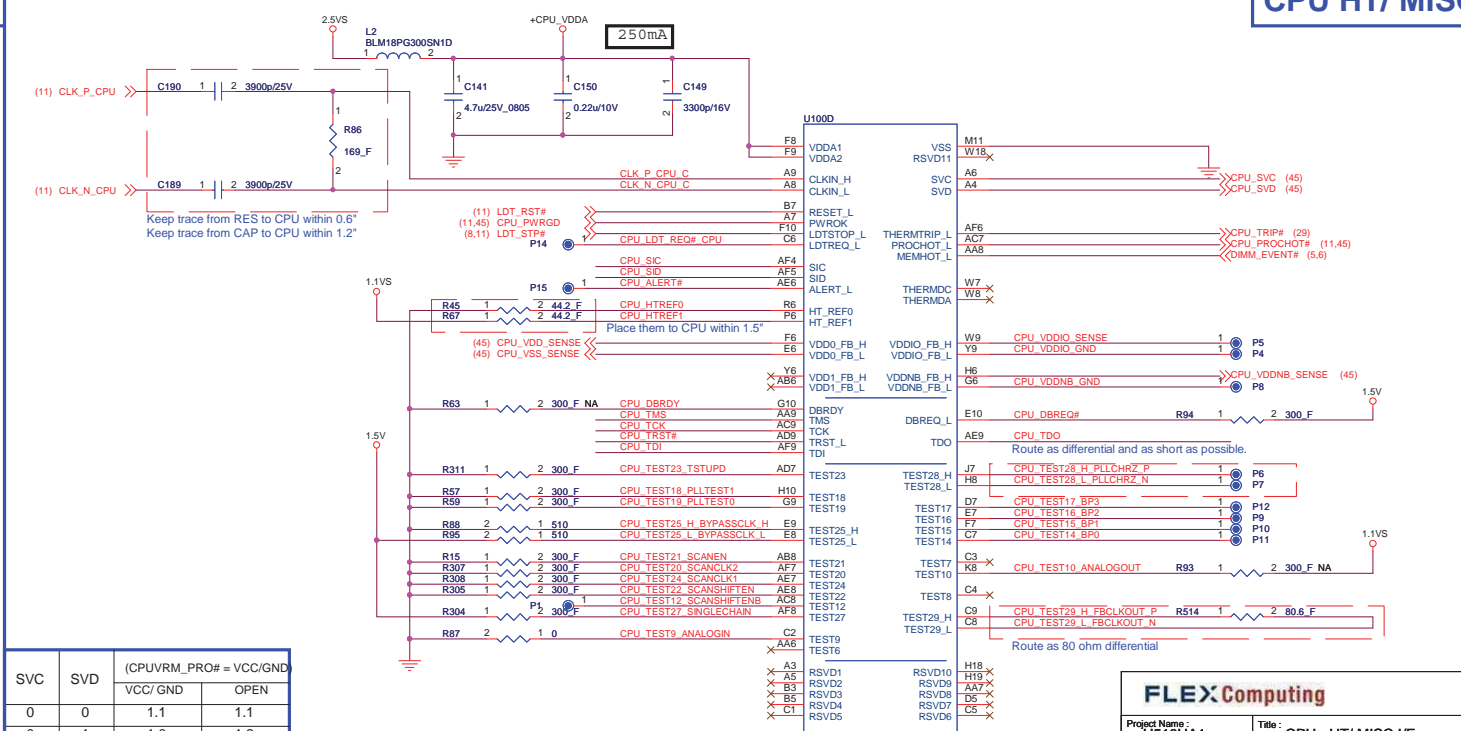
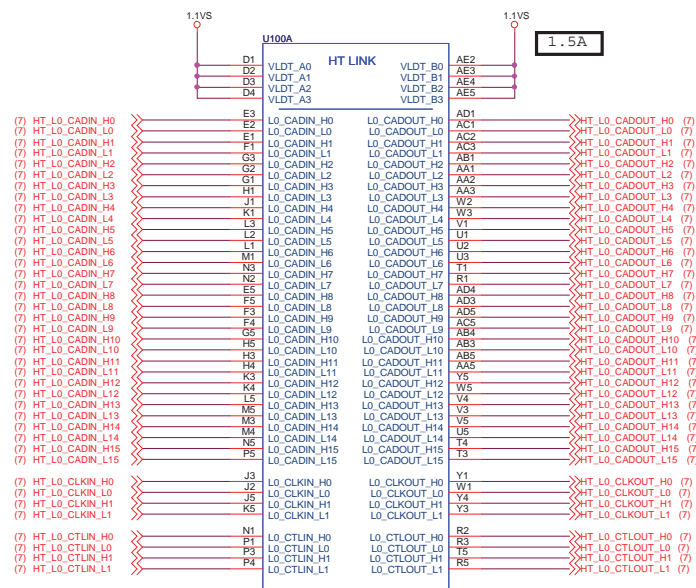
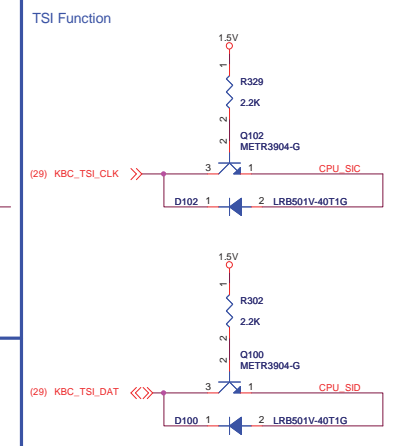
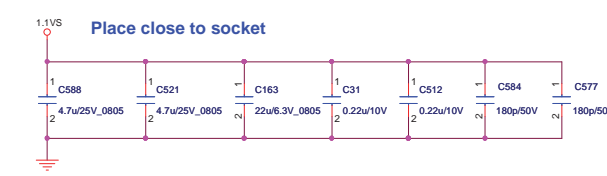
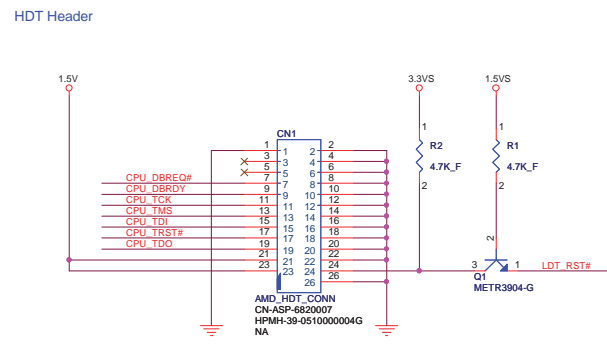
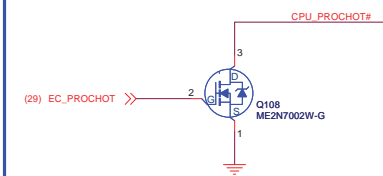
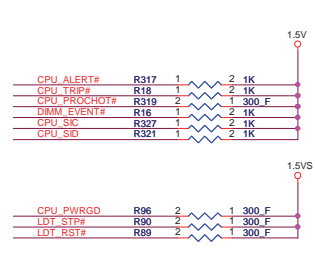
HDD LED Dual LED White: Normal , Amber: Park

FLEX Computing

Project Name: H510UA1	Title: Block Diagram
Size:	Document Number: HPMH-40GAB6300-D
Date: Thursday, December 30, 2010	Rev: D
Sheet: 1	of 51

AMD Debug Termination

Signal Name	Type	Connection	Termination	Voltage
TEST6 TEST7 TEST8		Remain unconnected	-	-
TEST9	I	Tie to VSS	-	VSS
TEST10		S1g2: Leave unconnected	-	-
		S1g3: Pulled up to VLDT (0603 DND)	-	-
TEST12		Test point access required for scan function. Connection to scan header preferred but not required.	1 K Ω to VSS No pop	VSS
TEST14 TEST15 TEST16 TEST17		Test point access required, header is preferred	-	-
TEST18			1 K Ω to VSS No pop	VSS
TEST19			1 K Ω to VSS No pop	VSS
TEST20		Test point access required for scan function. Connection to scan header preferred but not required.	300 Ω^6	VSS
TEST21			300 Ω^6	VSS
TEST22			1 K Ω to VSS No pop	VSS
TEST23			300 Ω^6	VSS
TEST24	I	Test point access required for scan function. Connection to scan header preferred but not required.	300 Ω^6	VSS
TEST25_H			510 Ω^6	VSS
TEST25_L			510 Ω^6	VDDIO
TEST27 TEST28_H TEST28_L TEST29_H TEST29_L		Need test point on board	-	-



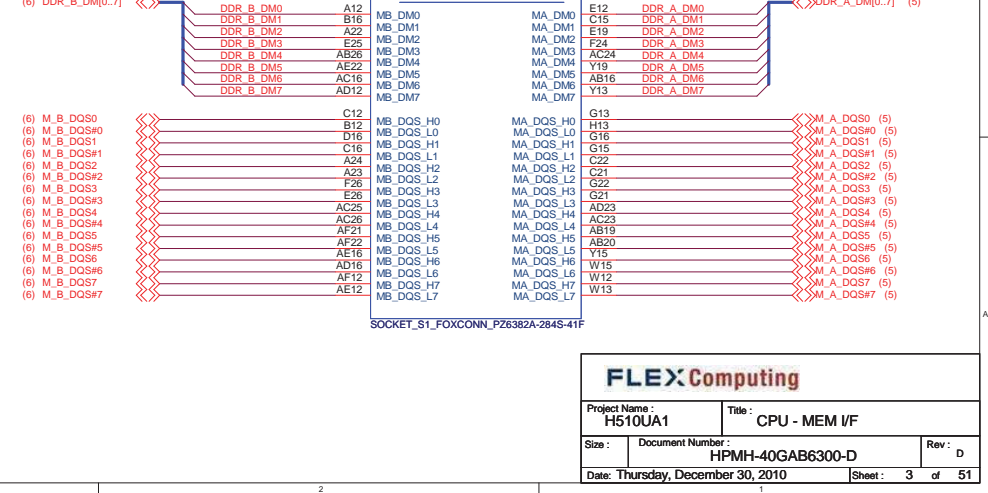
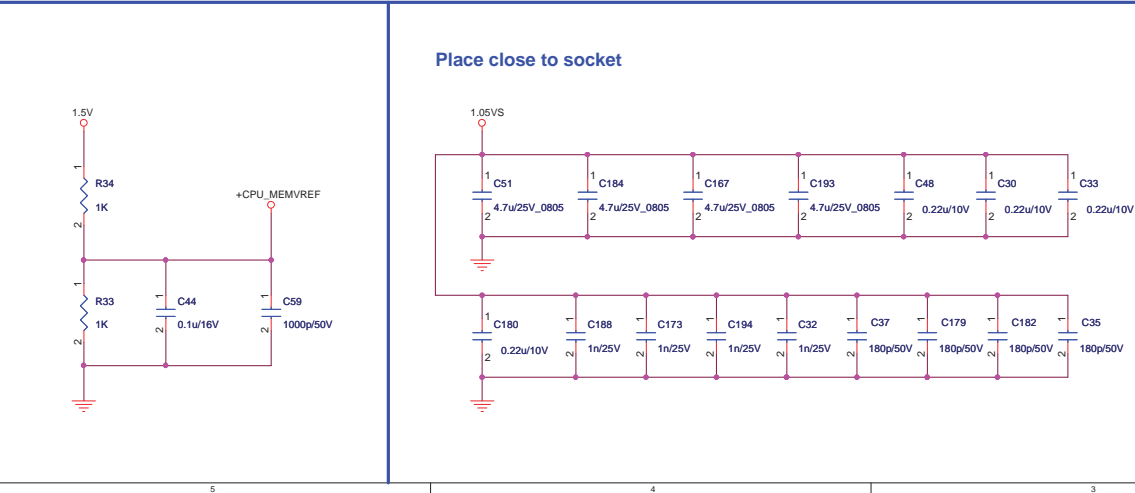
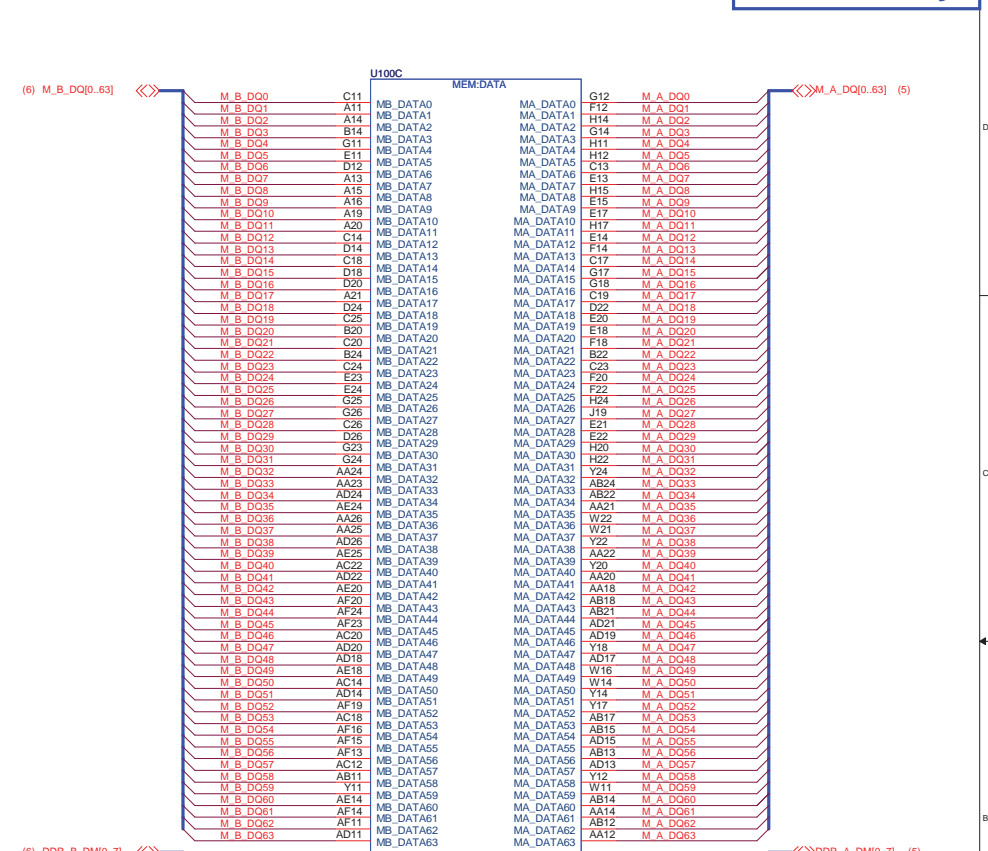
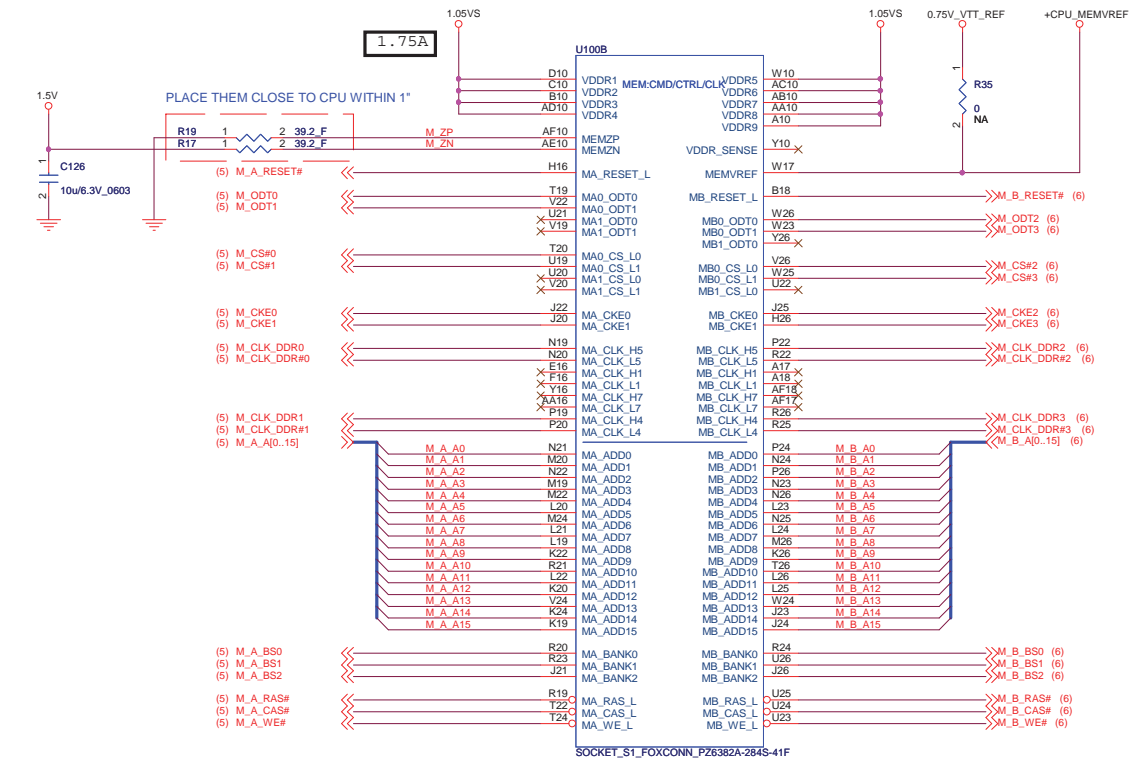
SVC	SVD	(CPUVRM_PRO# = VCC/GND)	VCC/GND	OPEN
0	0	1.1	1.1	
0	1	1.0	1.2	
1	0	0.9	1.0	
1	1	0.8	0.8	

FLEX Computing

Project Name: H510UA1 Title: CPU - HT/ MISC I/F

Size: Document Number: HPMH-40GAB6300-D Rev: D

Date: Thursday, December 30, 2010 Sheet: 2 of 51



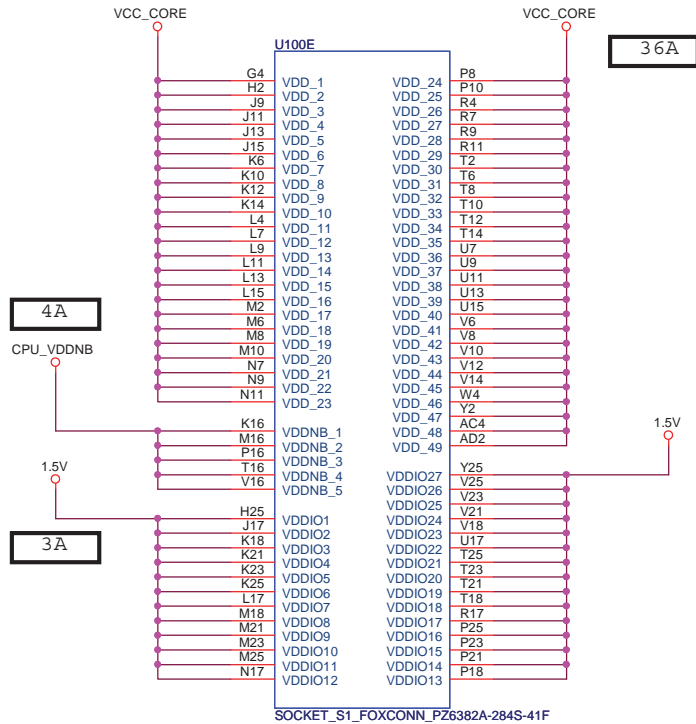
FLEXComputing

Project Name : H510UA1 Title : CPU - MEM I/F

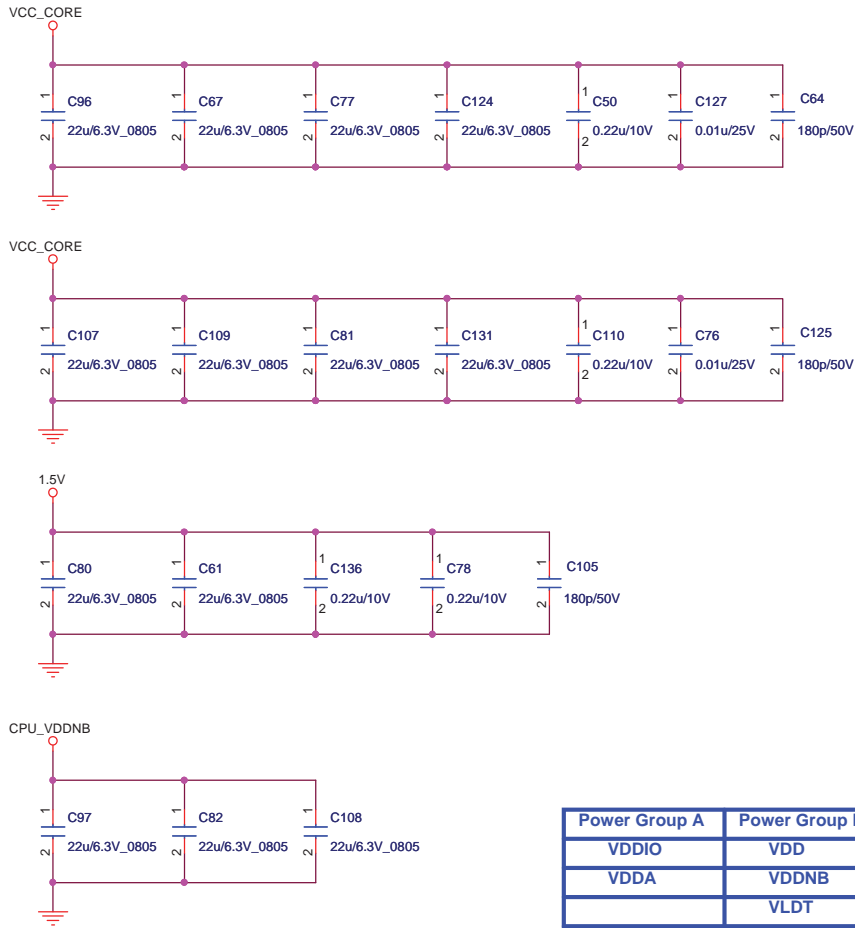
Size : Document Number : HPMH-40GAB6300-D Rev : D

Date : Thursday, December 30, 2010 Sheet : 3 of 51

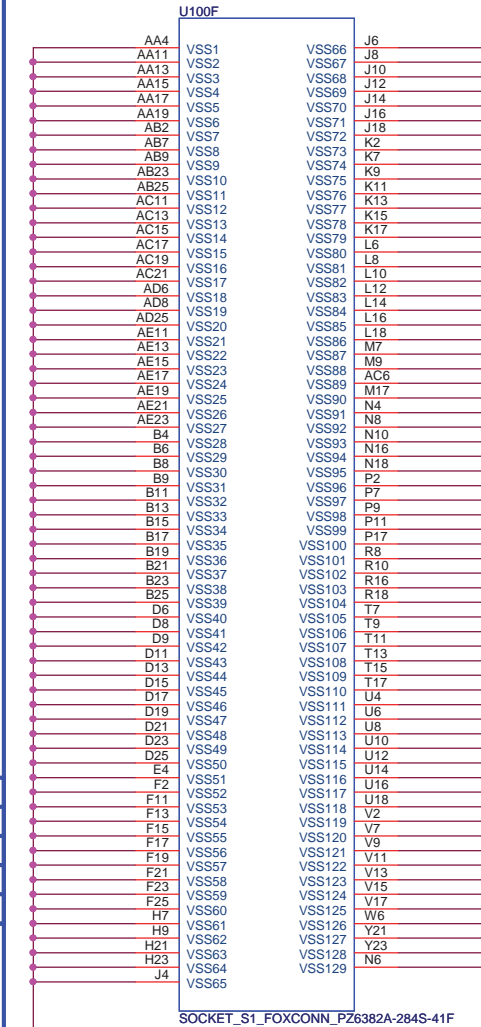
CPU PWR



BOTTOM SIDE DECOUPLING

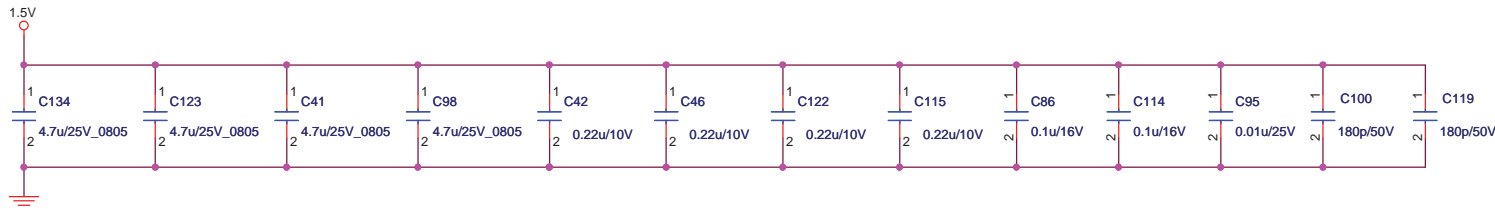


CPU GND



DECOUPLING BETWEEN PROCESSOR AND DIMMs

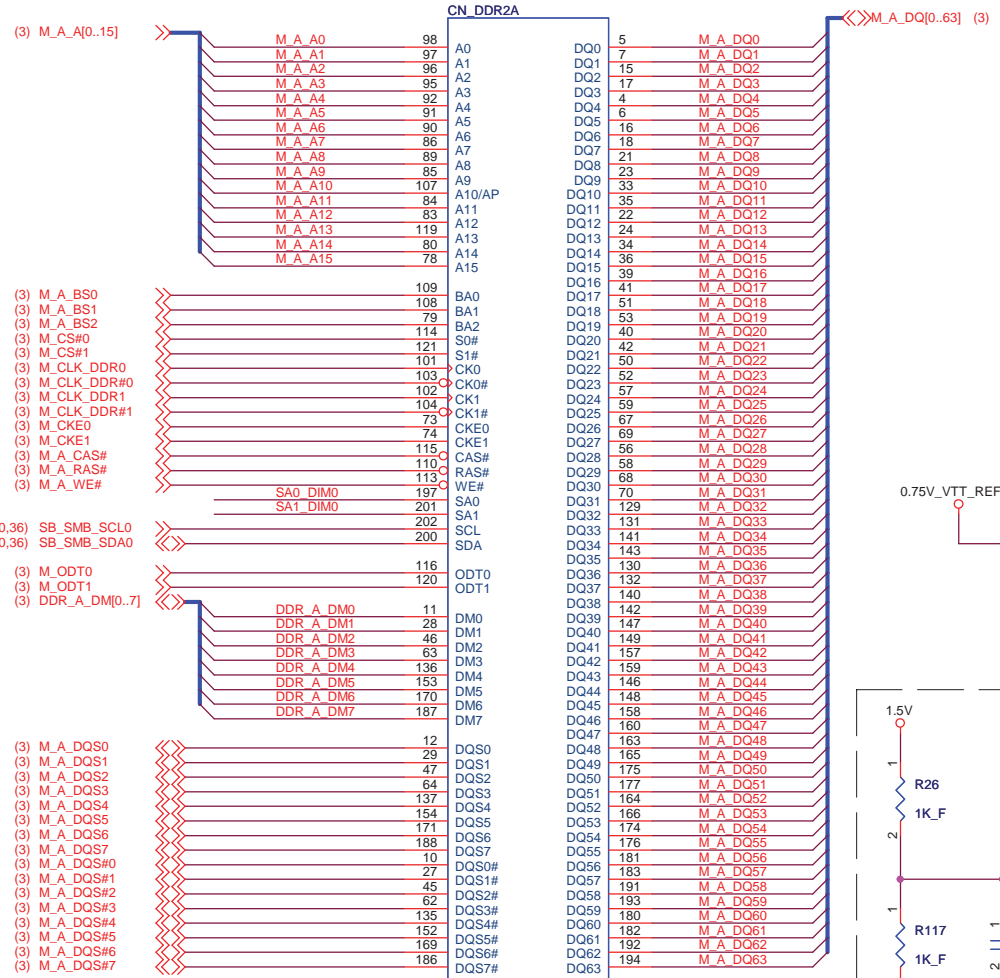
PLACE CLOSE TO PROCESSOR AS POSSIBLE



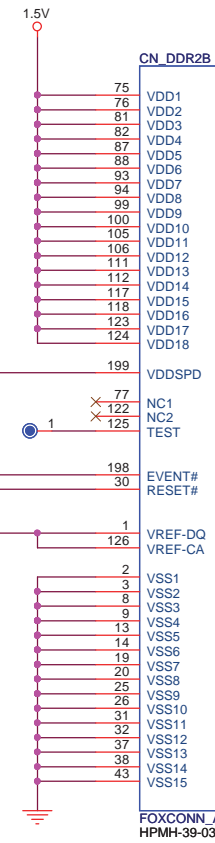
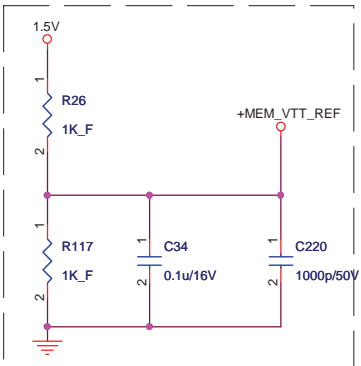
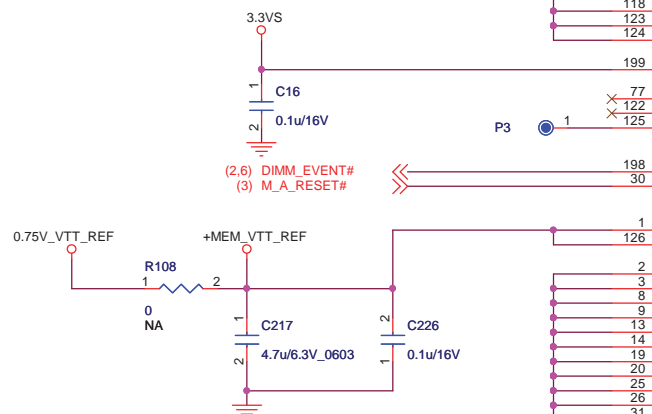
FLEX Computing

Project Name : H510UA1		Title : CPU - PWR/ GND	
Size :	Document Number :	HPMH-40GAB6300-D	
Date : Thursday, December 30, 2010		Rev :	D
		Sheet :	4 of 51

MEM CH-A

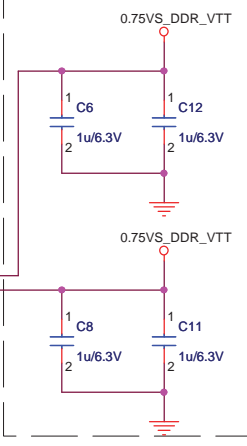


FOXCONN_AS0A626-JASG-7H
HPMH-39-037000032G

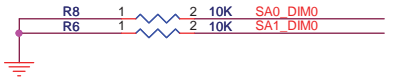
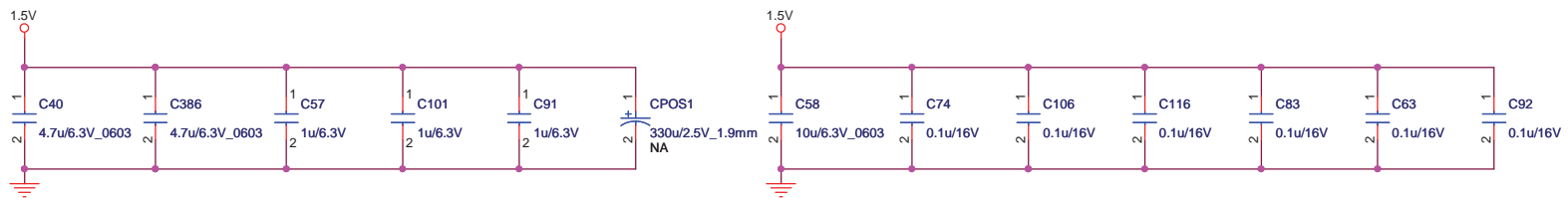


FOXCONN_AS0A626-JASG-7H
HPMH-39-037000032G

Layout
Place these caps close to Pin203 and 204.



Layout
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM and close to VDD Pin .

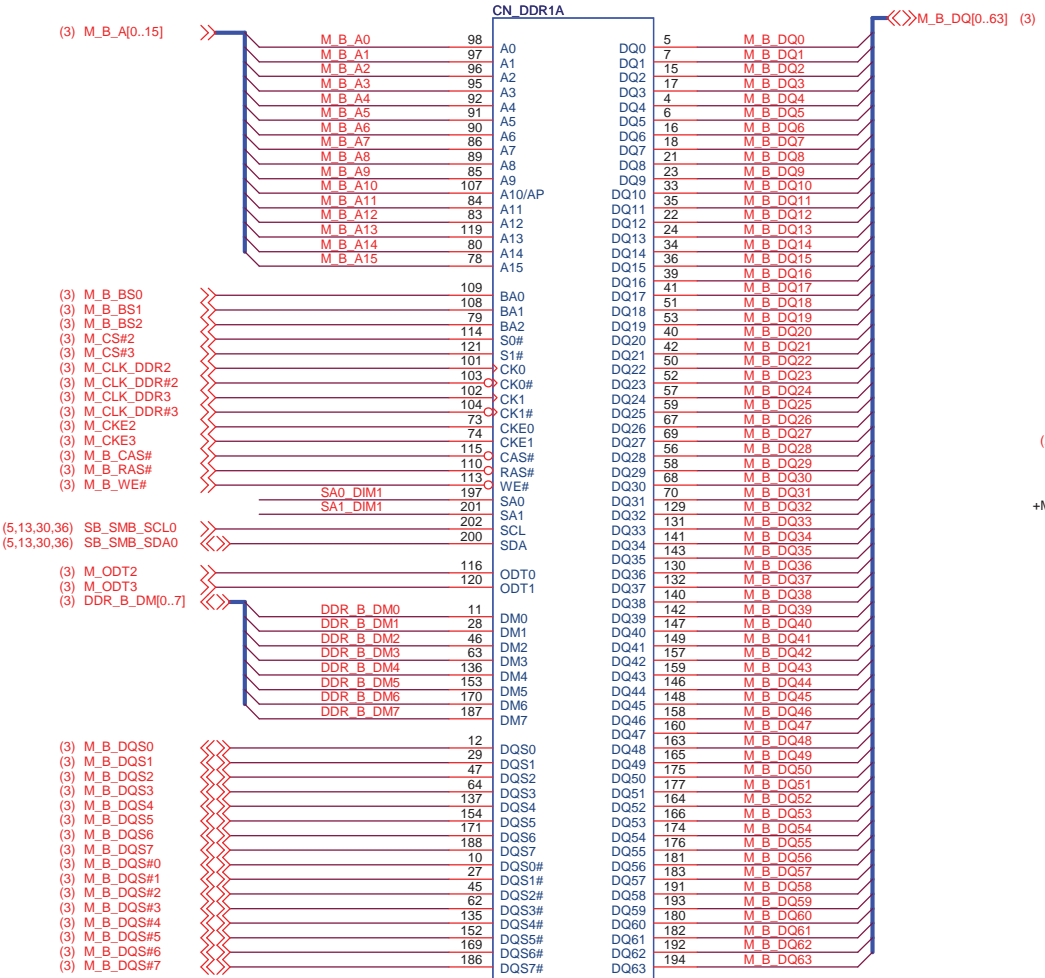


FLEX Computing

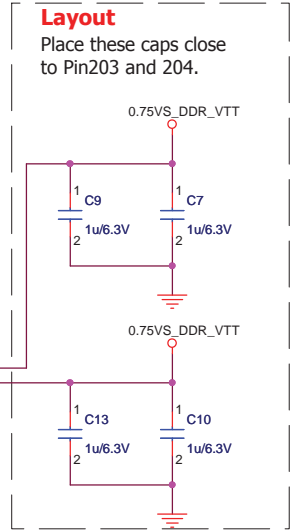
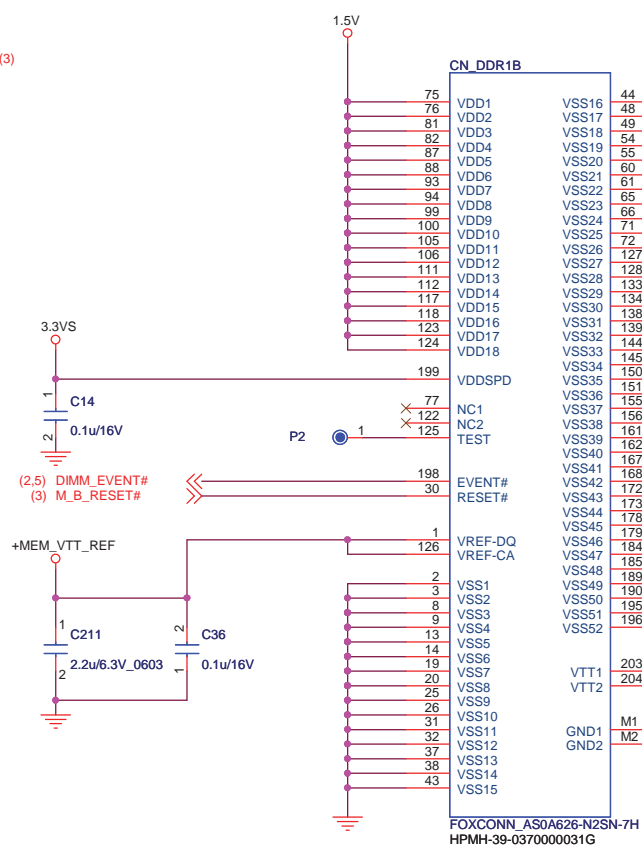
Project Name : H510UA1 Title : SO-DIMM Channel - A

Size : Document Number : HPMH-40GAB6300-D Rev : D

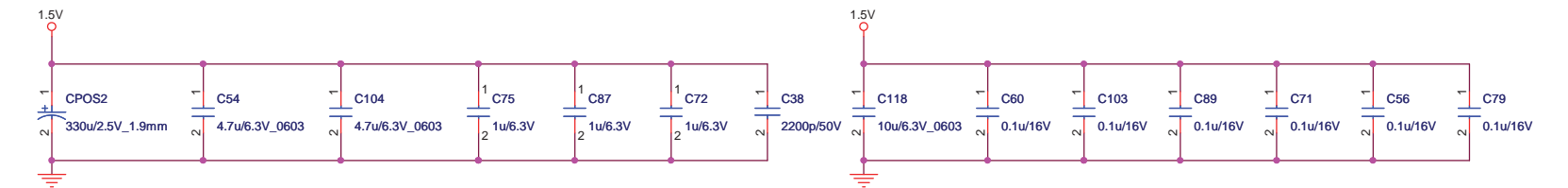
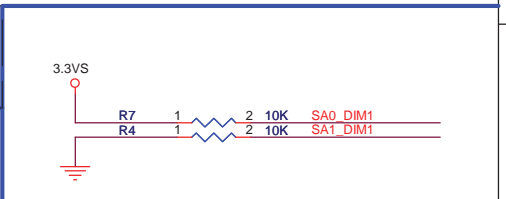
Date : Thursday, December 30, 2010 Sheet : 5 of 51



FOXCONN_AS0A626-N25N-7H
HPMH-39-0370000031G



Layout
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM
and close to VDD Pin .



FLEX Computing

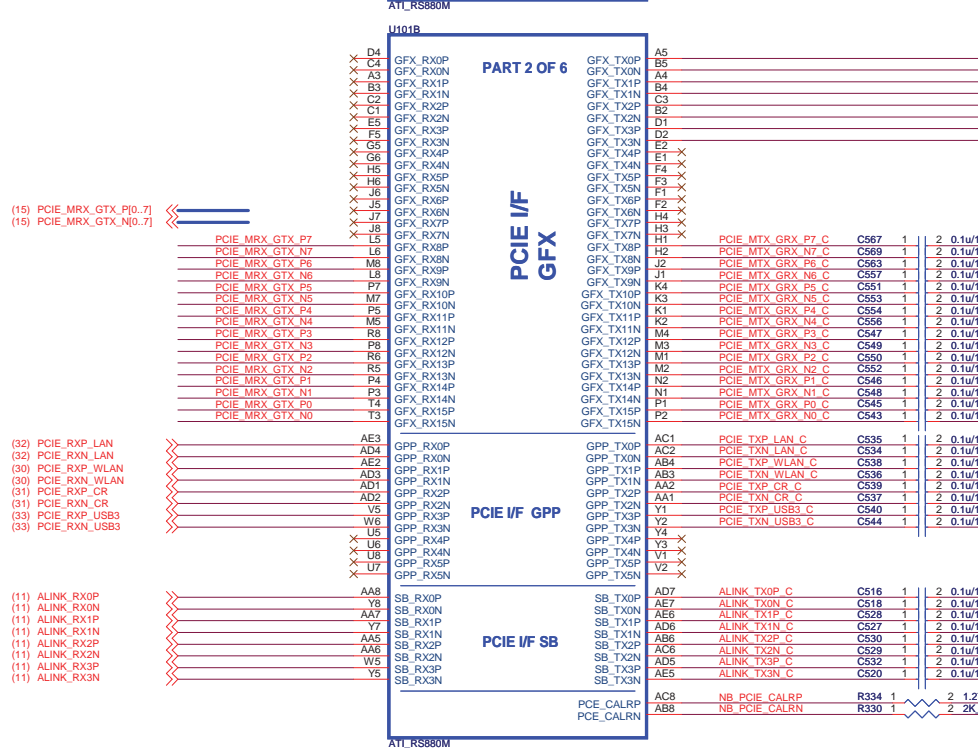
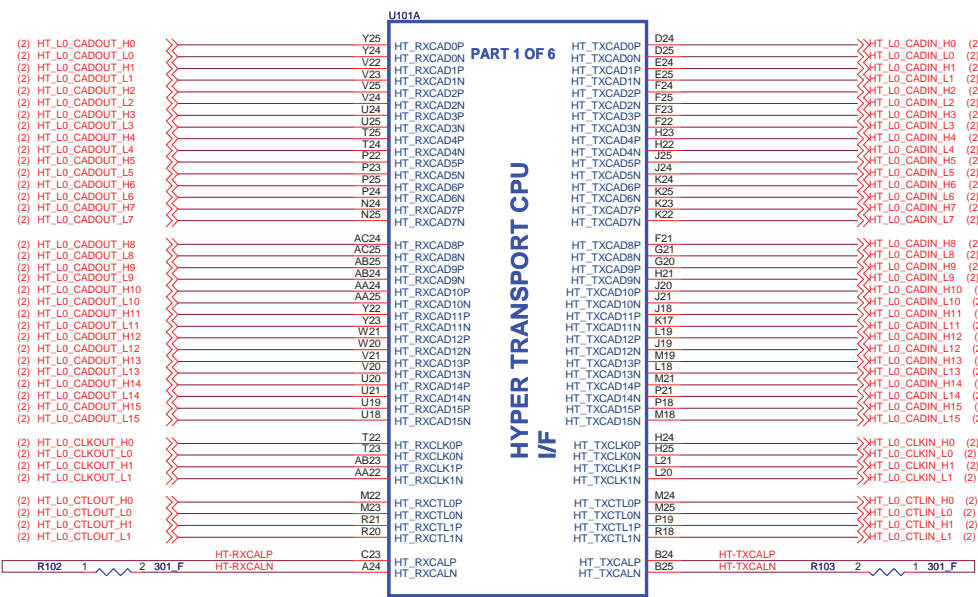
Project Name : H510UA1 Title : SO-DIMM Channel - B

Size : Document Number : HPMH-40GAB6300-D Rev : D

Date : Thursday, December 30, 2010 Sheet : 6 of 51

NB HT/ PCIE

Flex P/N: HPMH-10-001000096G
 HP B&S P/N: HPMJ-534109-001 (UMA)
 HPMJ-604096-001 (DGPU)



GFX RX

GFX TX

LAN RX
 WLAN RX
 Card Reader RX
 USB3.0 RX

LAN TX
 WLAN TX
 Card Reader TX
 USB3.0 TX

A-LINK RX

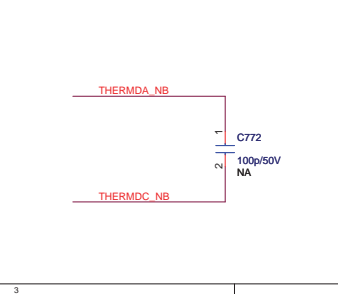
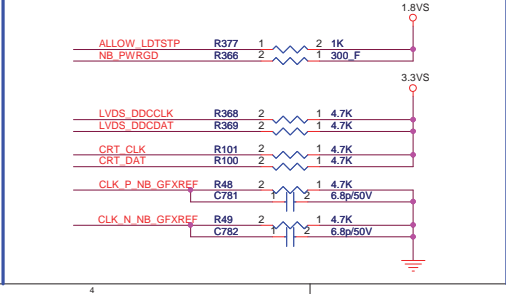
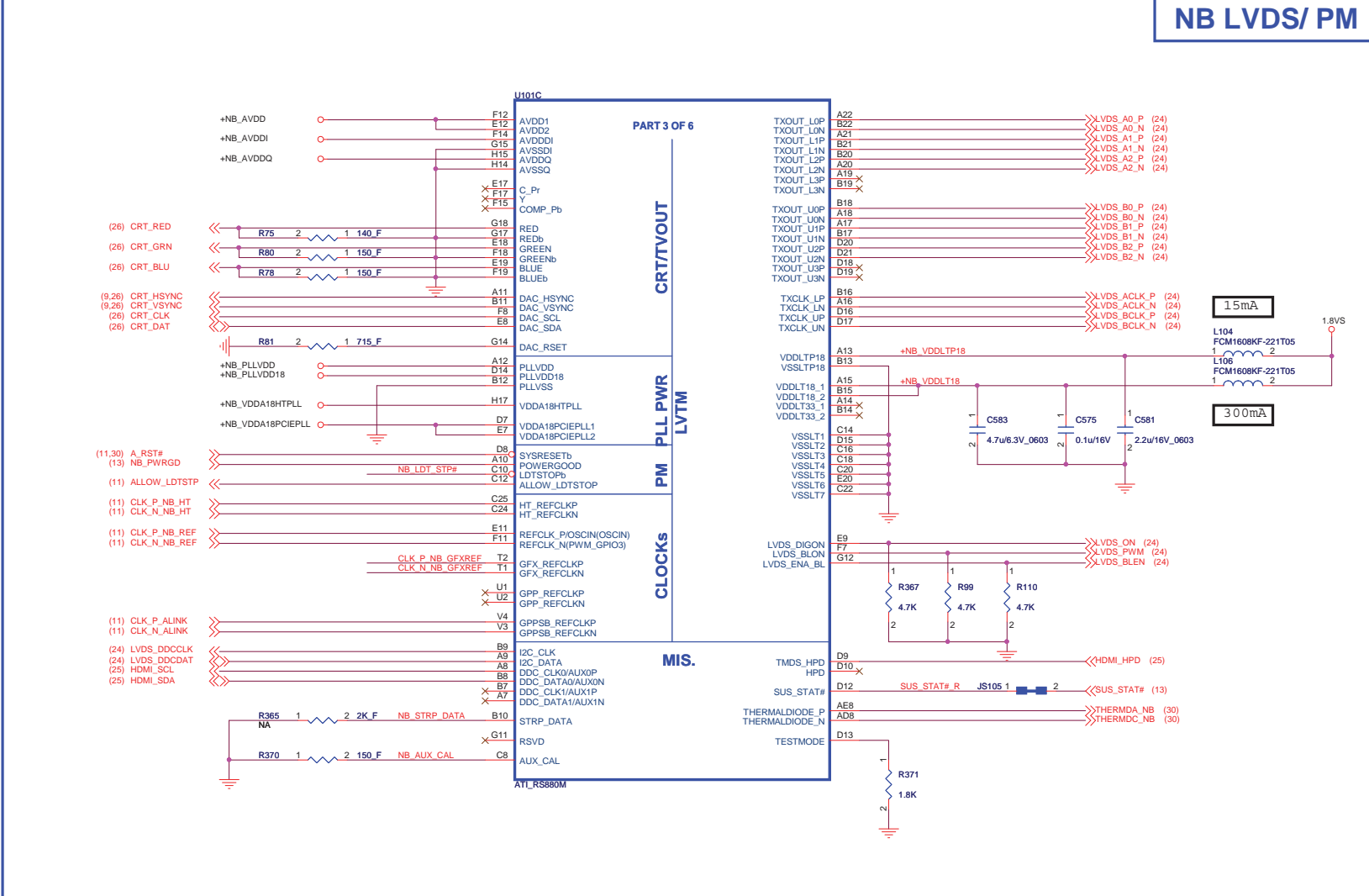
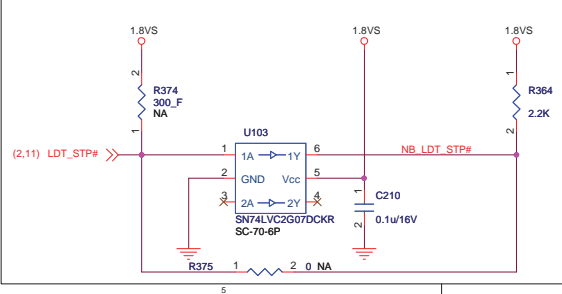
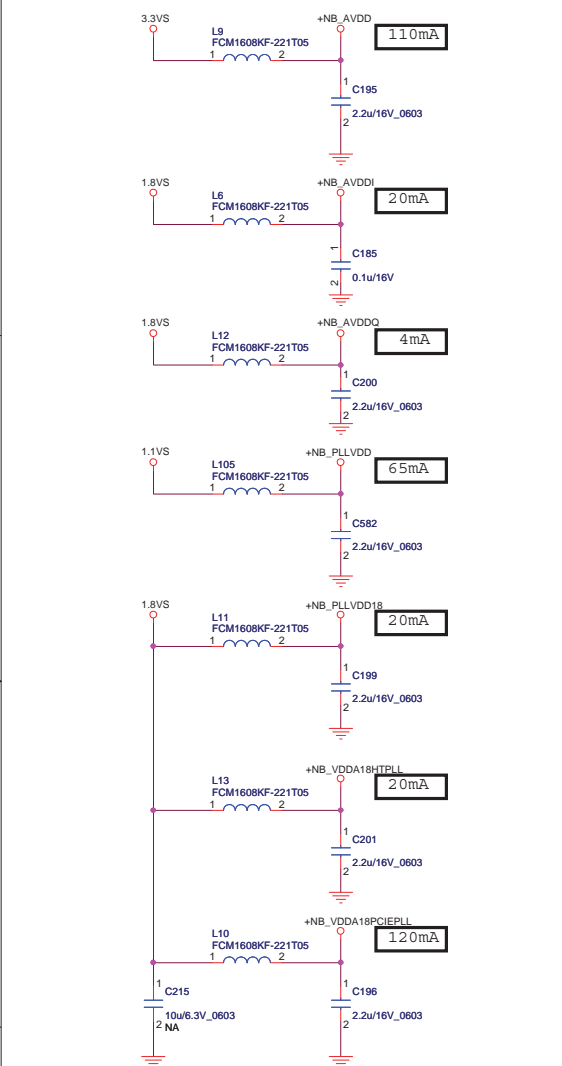
A-LINK TX

FLEX Computing

Project Name: H510UA1 Title: RS880M - HT/ PCI-E I/F

Size: Document Number: HPMH-40GAB6300-D Rev: D

Date: Thursday, December 30, 2010 Sheet: 7 of 51



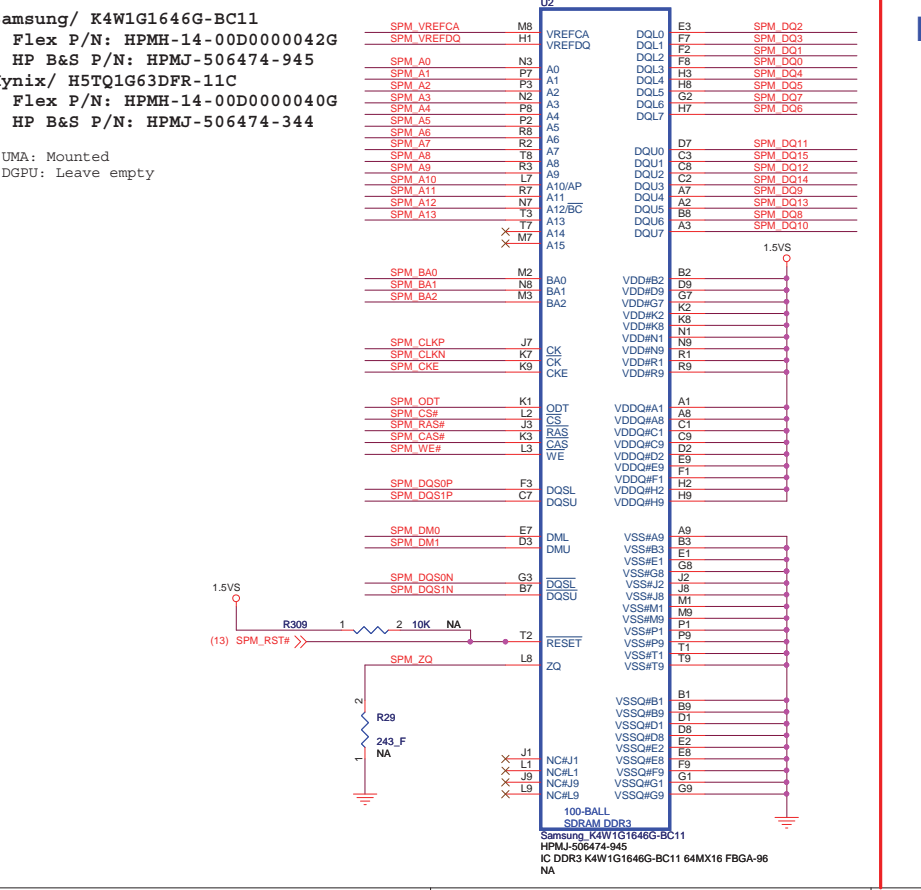
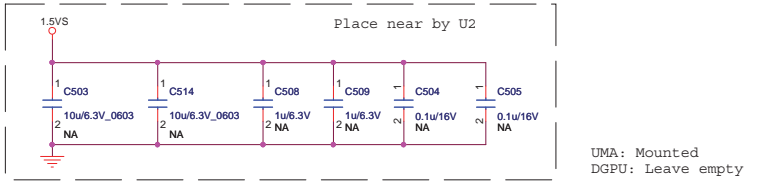
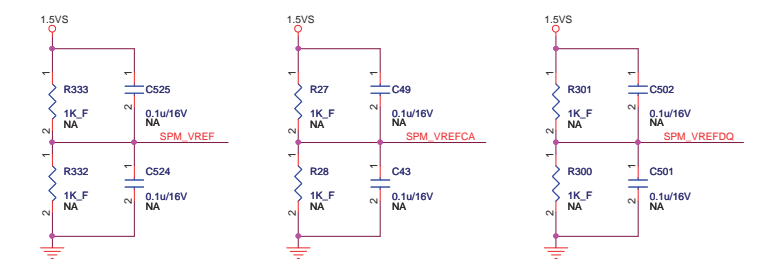
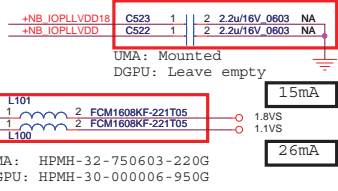
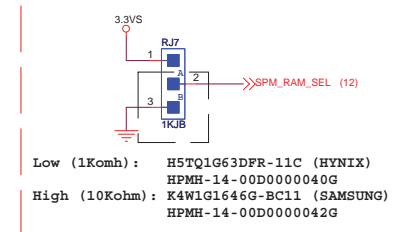
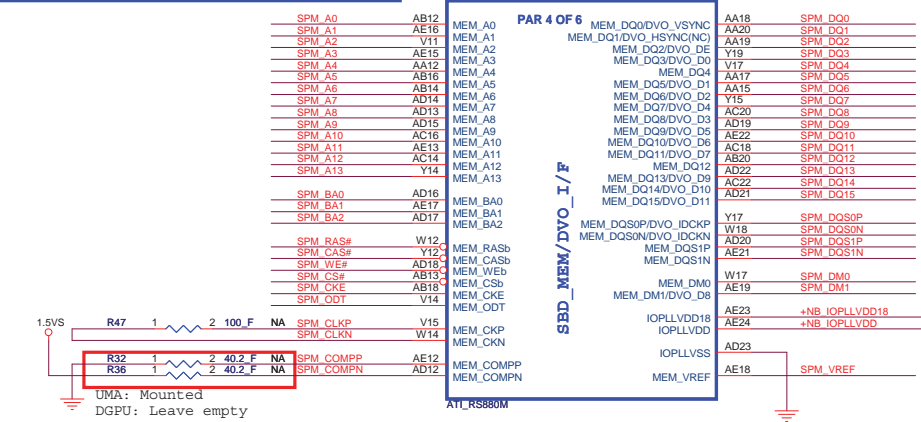
FLEXComputing

Project Name: H510UA1 Title: RS880M - LVDS/ PM I/F

Size: Document Number: HPMH-40GAB6300-D Rev: D

Date: Thursday, December 30, 2010 Sheet: 8 of 51

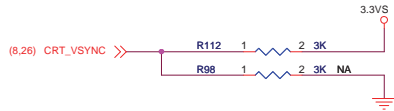
NB Side Port/ Strapping



RS880M HW STRAPS

The strap values are latched into internal registers after the assertion of the POWERGOOD signal to the RS880M

STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.
DAC_VSYNC (RS880.Pin B11)
1 = Disable (default)
0 = Enable

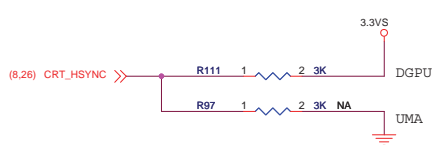


DFT_GPIO1: LOAD_EEPROM_STRAPS

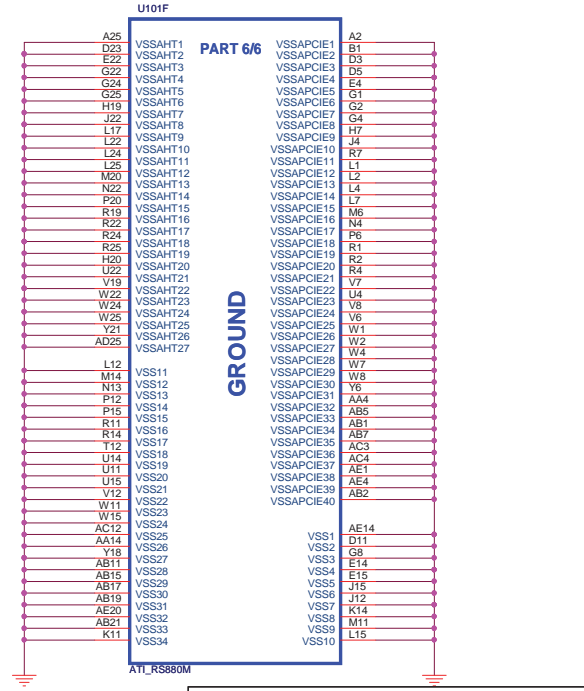
Selects Loading of STRAPS from EEPROM.
SUS_STAT# (RS880.Pin D12)
1 = Bypass the loading of EEPROM straps and use Hardware Default Values
0 = I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880: Enable Side Port Memory

Selects if Memory SIDE PORT is available or not
DAC_HSYNC (RS880.Pin A11)
1 : Disable (default)
0 : Enable
Register Readback of strap:
NB_CLKCFG:CLK_TOP_SPARE_D[1]



NB GND



FLEX Computing

Project Name: H510UA1 Title: RS880M - Side Port/ Strap/ GND

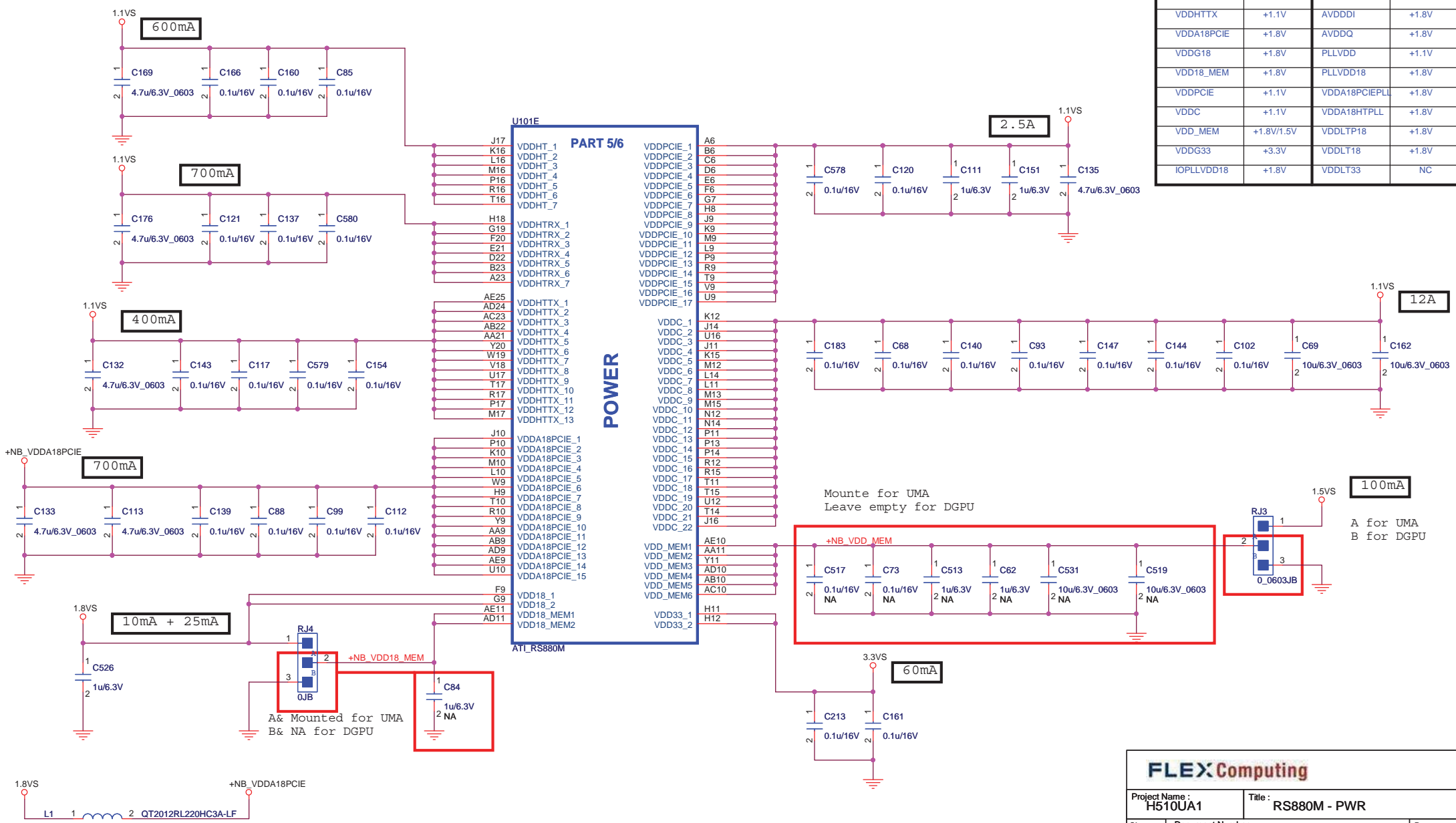
Size: Document Number: HPMH-40GAB6300-D Rev: D

Date: Thursday, December 30, 2010 Sheet: 9 of 51

NB PWR

RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.1V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC

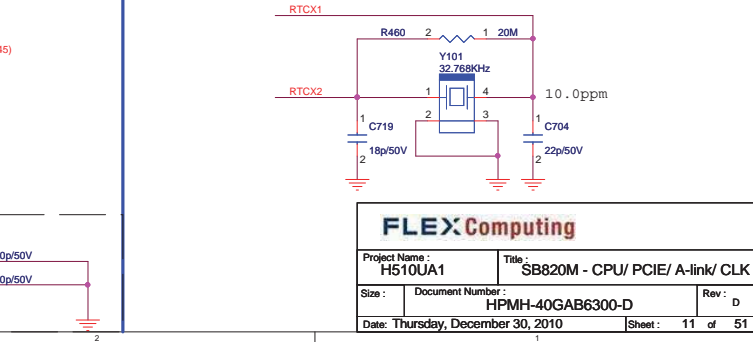
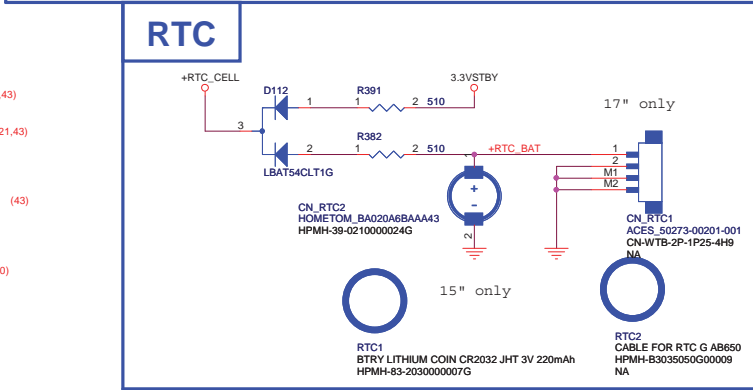
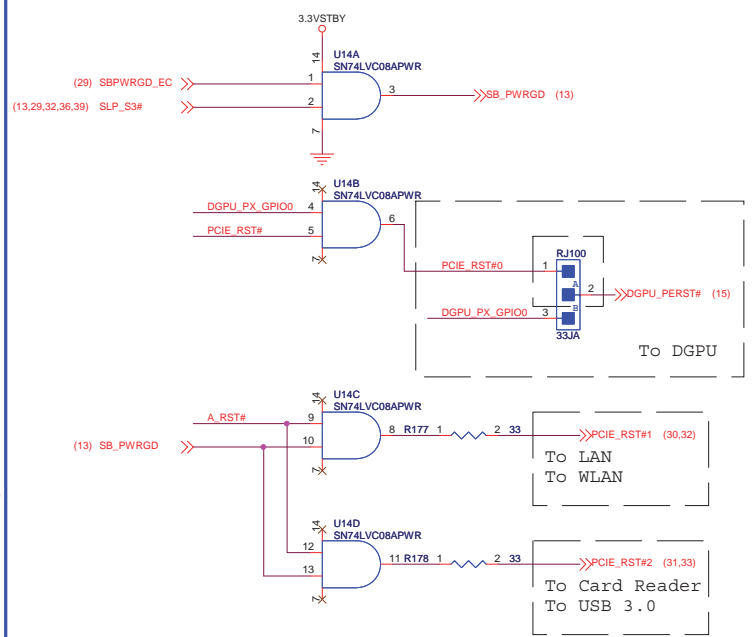
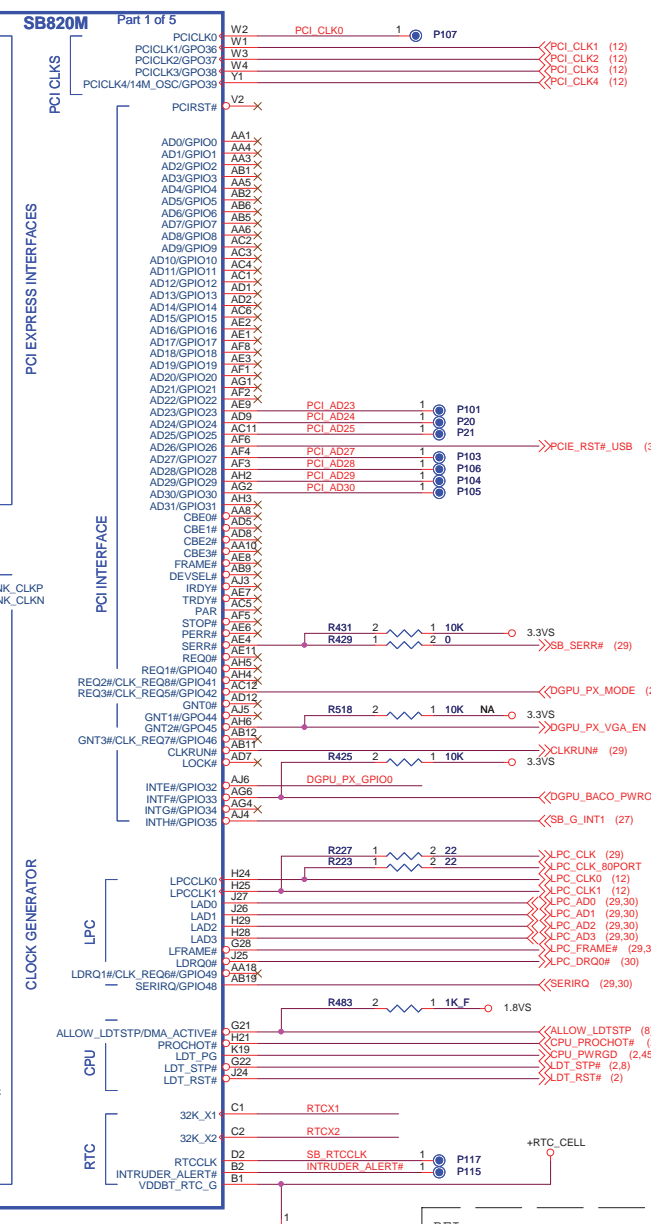
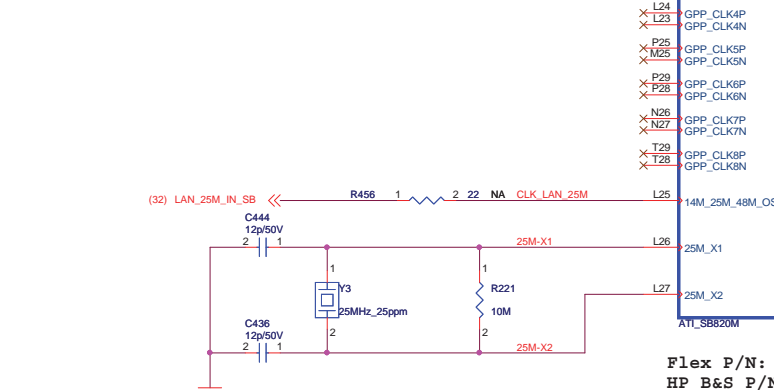
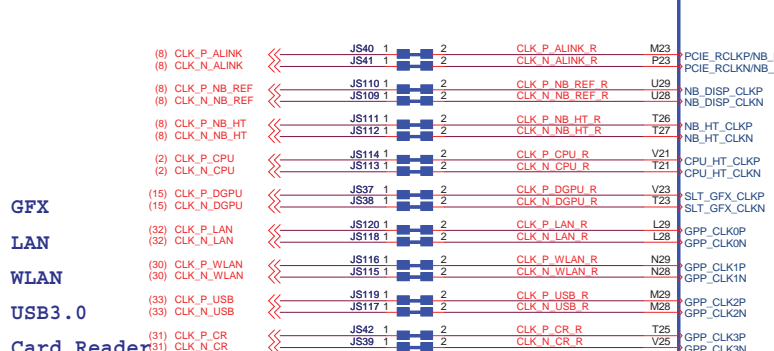
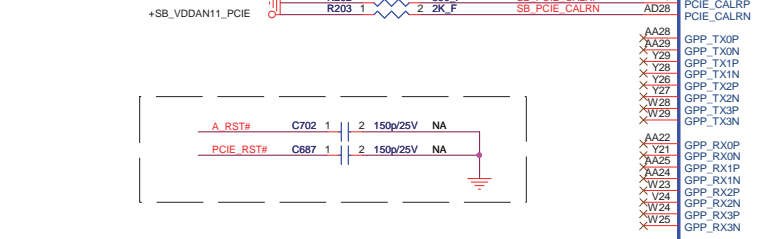
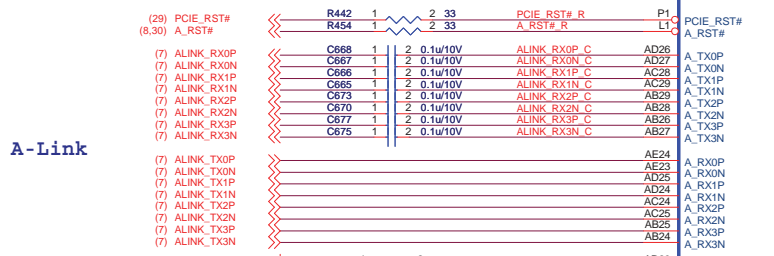


A for UMA
B for DGPU

FLEX Computing

Project Name : H510UA1	Title : RS880M - PWR
Size : Document Number : HPMH-40GAB6300-D	Rev : D
Date : Thursday, December 30, 2010	Sheet : 10 of 51

SB PCI-E/ CPU/ Alink/ CLK I/F



Flex P/N: HPMH-10-0010000106G
 HP B&S P/N: HPMJ-590825-002

FLEX Computing

Project Name: H510UA1 Title: SB820M - CPU/ PCIE/ A-link/ CLK

Size: Document Number: HPMH-40GAB6300-D Rev: D

Date: Thursday, December 30, 2010 Sheet: 11 of 51

SB820M Debug Straps

PciIIByp (PCI AD27)

Bypass PCI PLL
(Used in functional test at tester):
L: Bypass internal PLL clock
H: Use internal PLL generated PLL CLK (Internal Pull-Up of 15Kohm)

ILAAutorunEnB (PCI AD26)

ILA Auto run Enable
L: ILA Auto run enable
H: ILA Auto run disable (Internal Pull-Up of 15Kohm)

FCCIkByP (PCI AD25)

Bypass FC CLK
L: Bypass internal FC CLK (Used in functional test at tester)
H: Use internal FC CLK

I2CROMEn (PCI AD24)

I2C ROM Enable. Load the setting for A-Link Express/ PLL/ music control from I2C ROM

L: Getting the value from I2C EPROM
H: Disable I2C ROM
(Internal Pull-Up of 15Kohm)

PCI_ROM_BOOT (PCI AD23)

Bootting from PCI memory
L: Route ROM fetch tp PCI bus on the very first boot. Use ROMTYPE to determine the ROM type on the subsequent boots.
H: Use ROMTYPE straps to determine the ROM type
(Internal Pull-Up of 15Kohm)

PCIe EEPROM Data/ Clock (PCI_REQ3/PCI_GNT3)

PCIe EEPROM Data/ Clock
Connected to PCIe EEPROM SDA/ SCL pin or provided test point access for lad use.

SB820M H/W STRAPS

Type I are captured on RSMRST#
Type II are captured on PWRGD#.

ECEnableStrap (LPCCLK0)

Embedded Controller (EC):
L: Disable
H: Enable



CLKGEN (LPCCLK1)

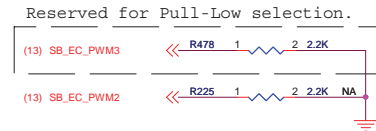
Define Clock Generator:
L: External clock mode
H: Internal clock mode



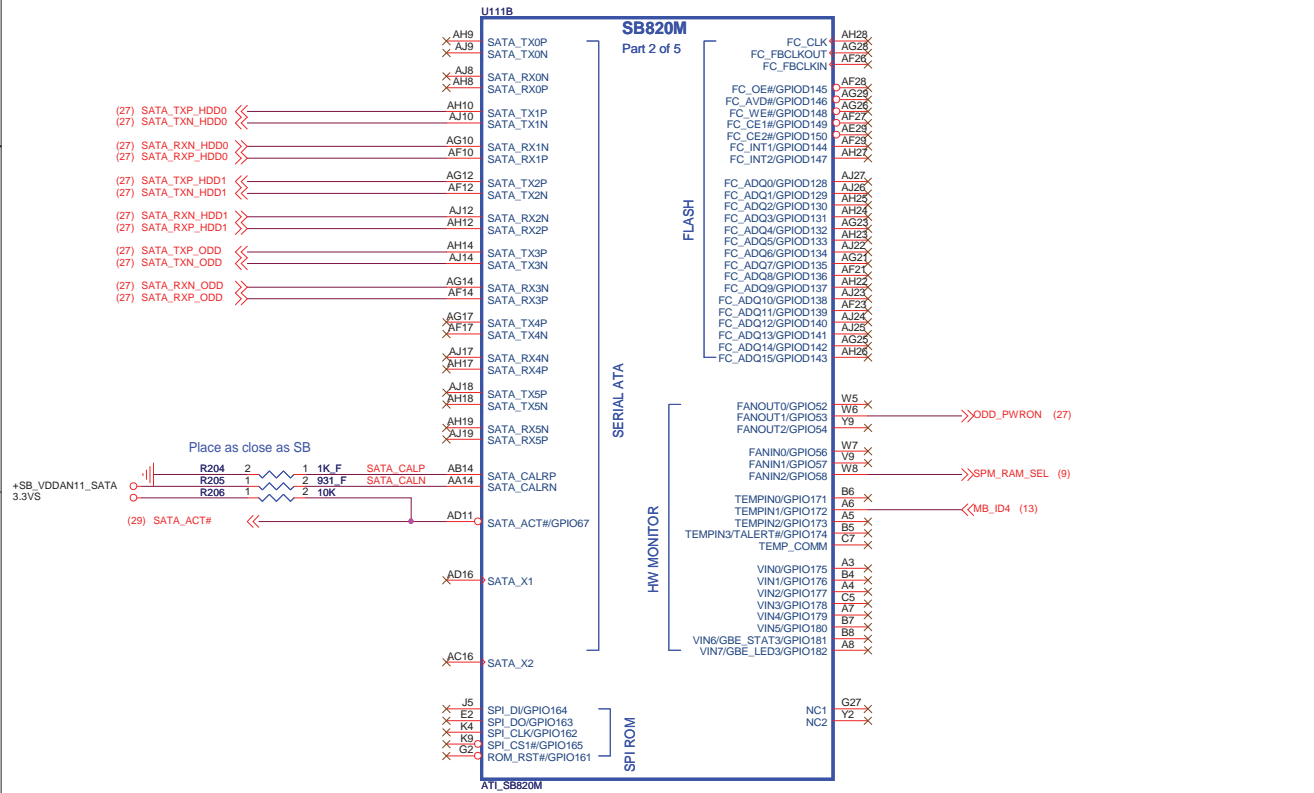
ROMTYPE_1&0 (EC_PWM3& EC_PWM2)

ROMTYPE_1 EC_PWM3	ROMTYPE_0 EC_PWM2	ROM type
0	0	FWH
0	1	LPC& PMC ROM
1	0	SPI
1	1	Reserve

Default Pull-High Pull-Low --> 2.2Kohm



SB SATA/ SPI/ STRAP



BIF_GEN2_COMPLIANCE_Strap (PCI CLK1)

Set PCIe to Gen II mode:
SB820M: Only provision for Pull down is required, not install by default.



BootFailTmrEn (PCI CLK2)

Watchdog function:
L: Disable BootFailtmr function
H: Enable BootFailtmr function



DefaulStrapMode (PCI CLK3)

Default Debug Straps:
L: Disable Debug Straps
H: Select external Debug Straps



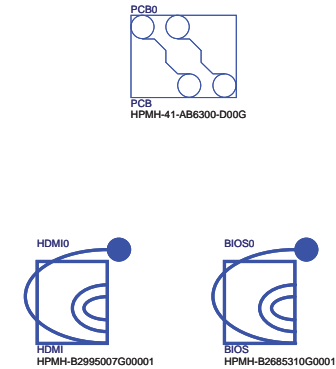
CPUCIkSel (PCI CLK4)

CPU/ NB HT Clock Selection:
L: Reserved
H: Required setting for integrated clock mode



CoreSpeedMode (AZ_SDOUT)

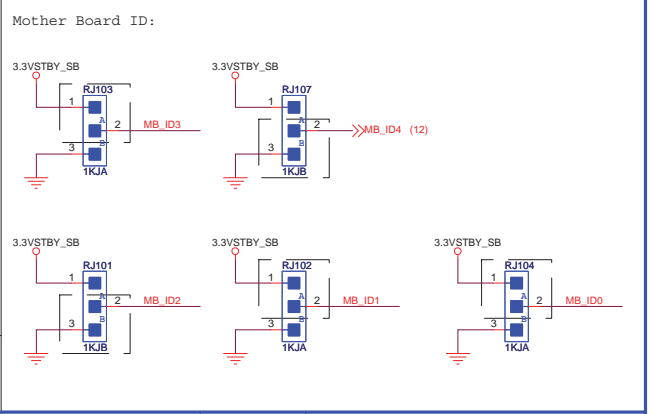
Slow down core clock for low power mobile platform:
L: Performance Mode
H: Low Power Mode



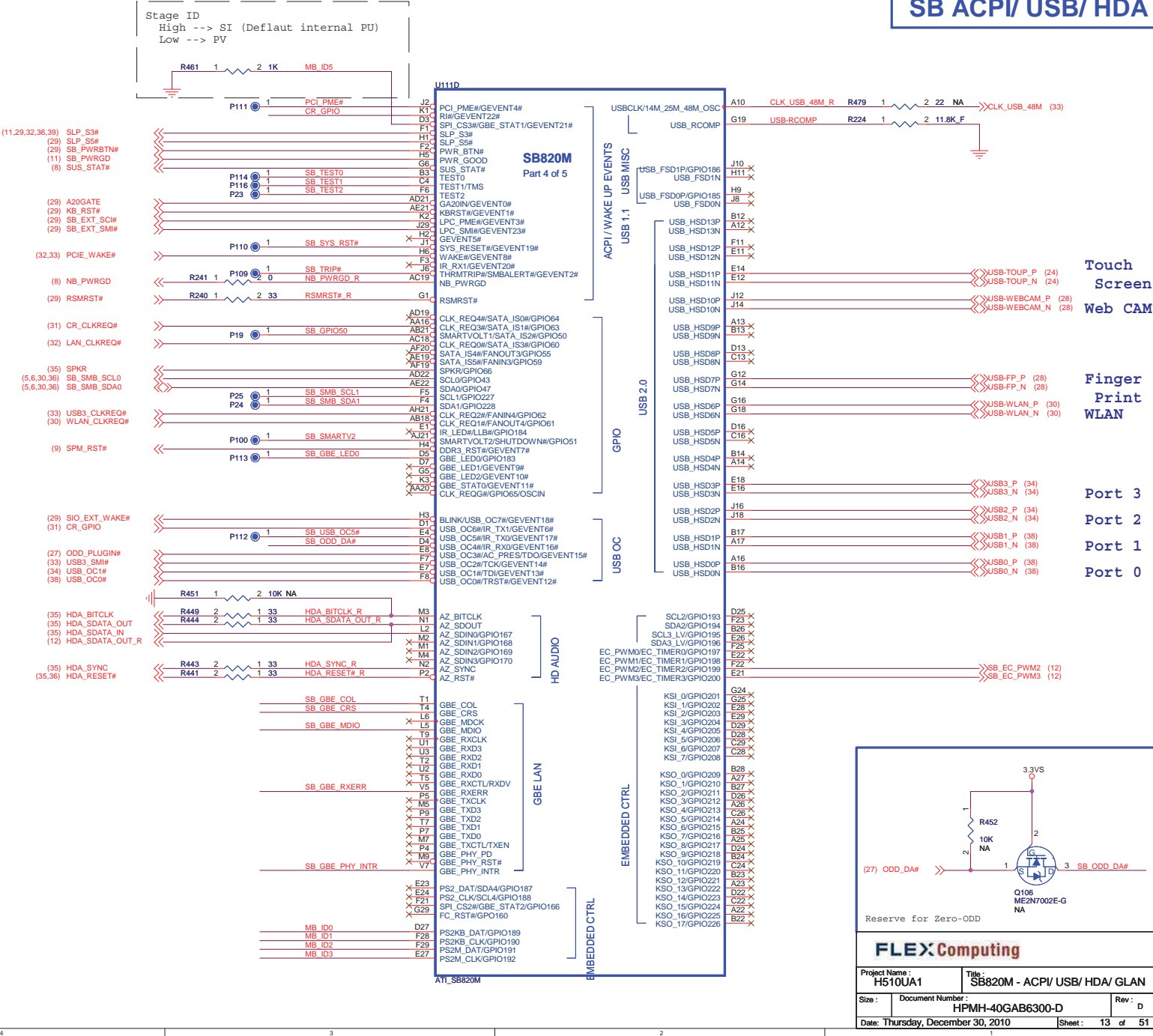
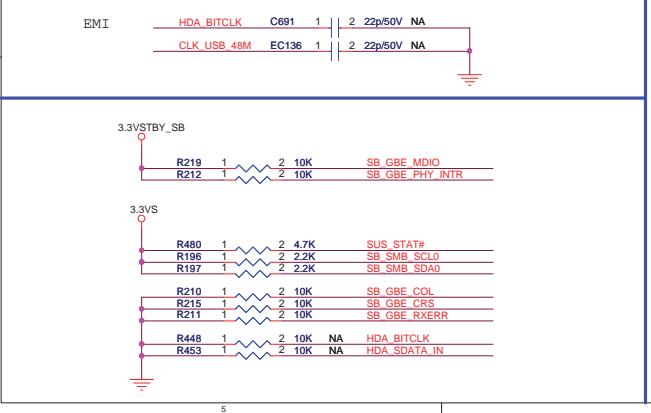
Type I : LPCCCLK0, EC_PWM3& EC_PWM2
Type II : the rest of strapping

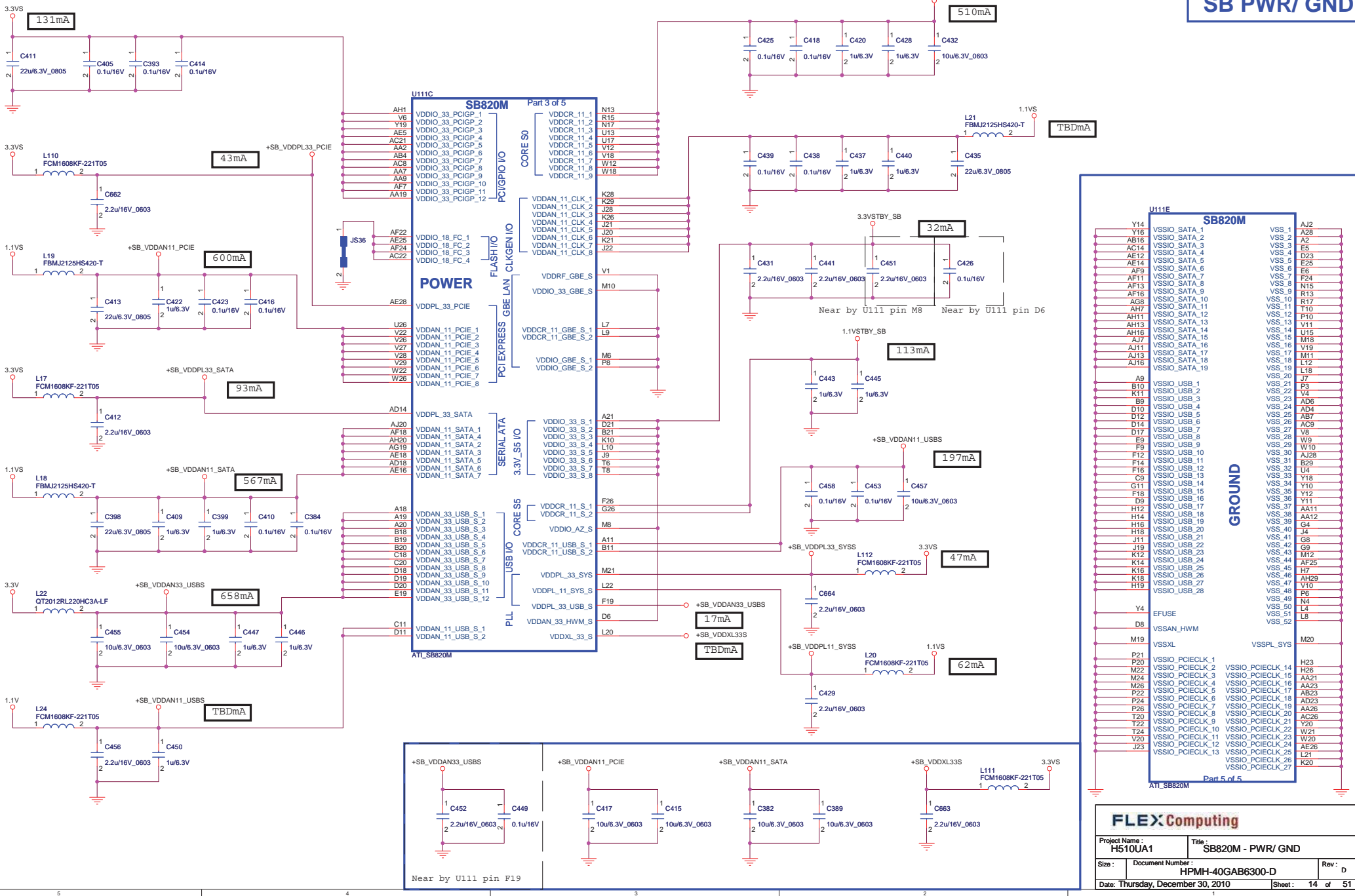
FLEX Computing

Project Name : H510UA1	Title : SB820M - SATA/ SPI/ Strap
Size :	Document Number : HPMH-40GAB6300-D
Date : Thursday, December 30, 2010	Rev : D
	Sheet : 12 of 51



ID4	ID3	ID2	ID1	ID0	Board ID	Board ID
0	0	1	1	0	0x366A	Kelly 1.x UMA (IMR)
0	0	1	1	1	0x366B	Kelly 1.x Seymour XT (IMR)
0	1	0	0	0	0x366C	Kelly 1.x Whistler Pro (IMR)
0	1	0	0	1	0x1649	Kelly 1.x UMA
0	1	0	1	0	0x164A	Kelly 1.x Seymour XT
0	1	0	1	1	0x164B	Kelly 1.x Whistler Pro
0	1	1	0	0	0x164C	Young 1.x UMA
0	1	1	0	1	0x164D	Young 1.x Seymour XT
0	1	1	1	0	0x164E	Young 1.x Whistler Pro





FLEXComputing

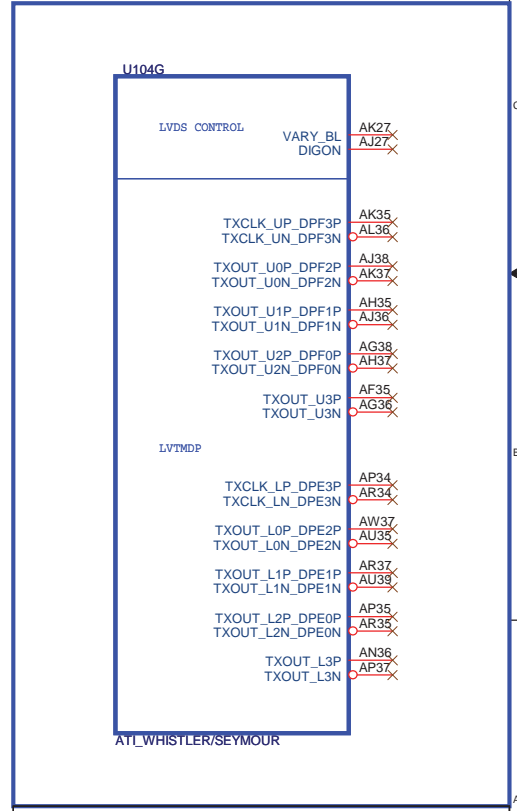
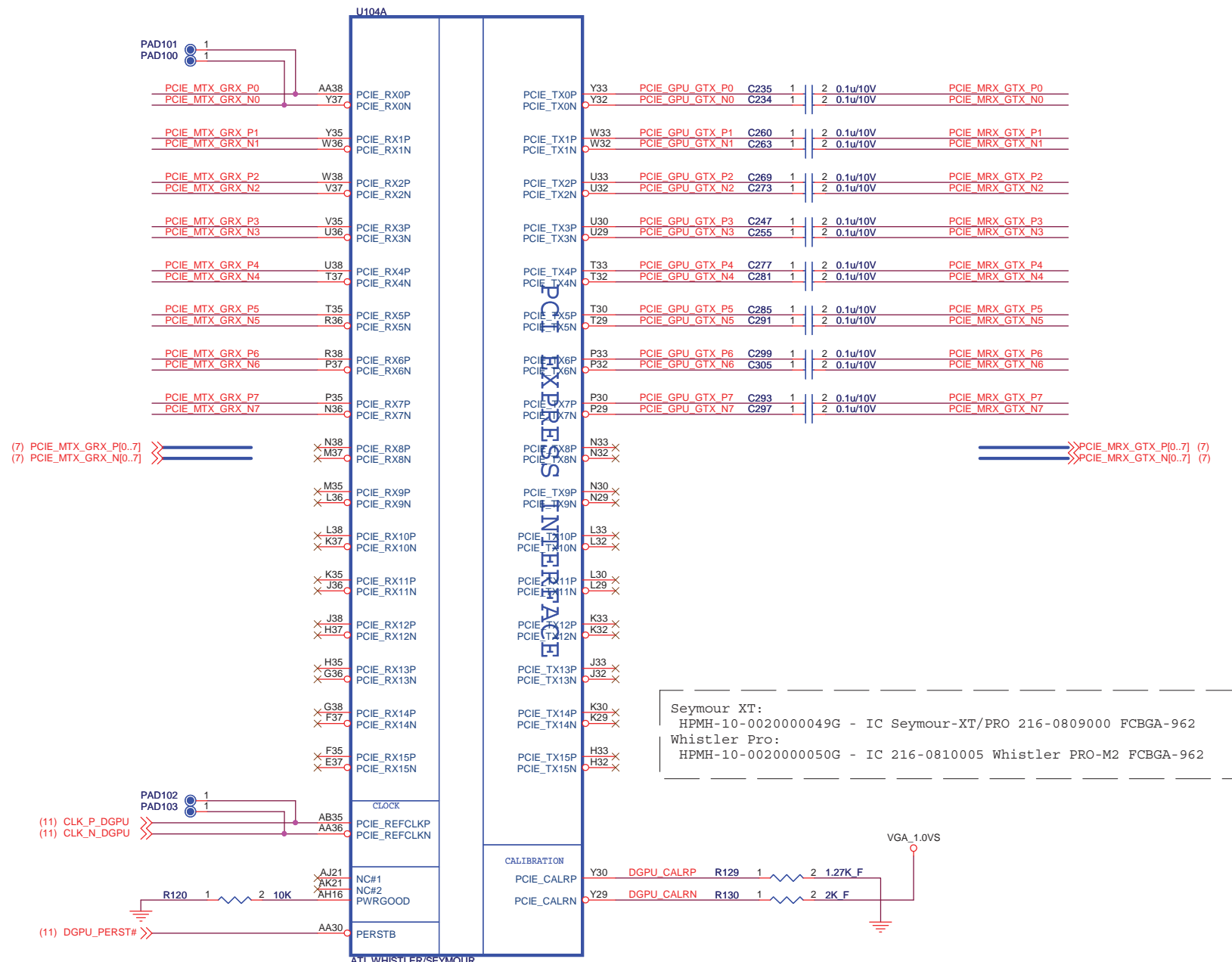
Project Name: H510UA1 Title: SB820M - PWR/ GND

Size: Document Number: HPMH-40GAB6300-D Rev: D

Date: Thursday, December 30, 2010 Sheet: 14 of 51

DGPU PCIE/ LVDS

Seymour
 Flex P/N: HPMH-10-002000049G
 HP B&S P/N: HPMJ-633843-001
 Whistler
 Flex P/N: HPMH-10-002000050G
 HP B&S P/N: HPMJ-628114-001

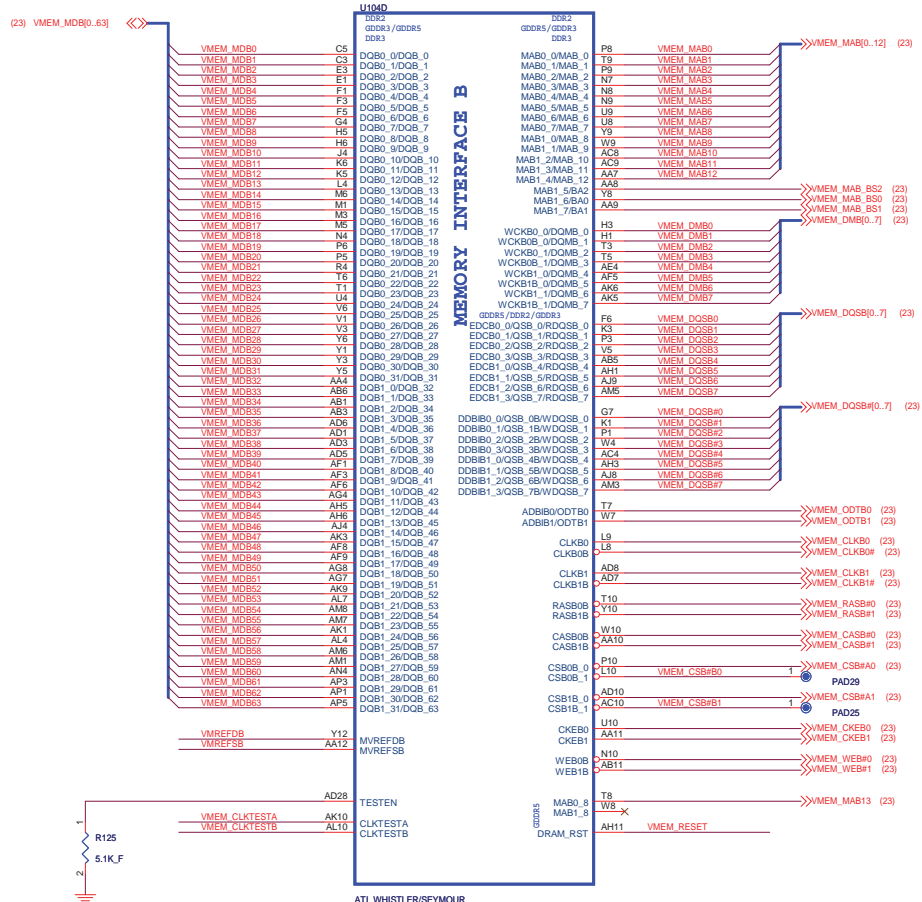
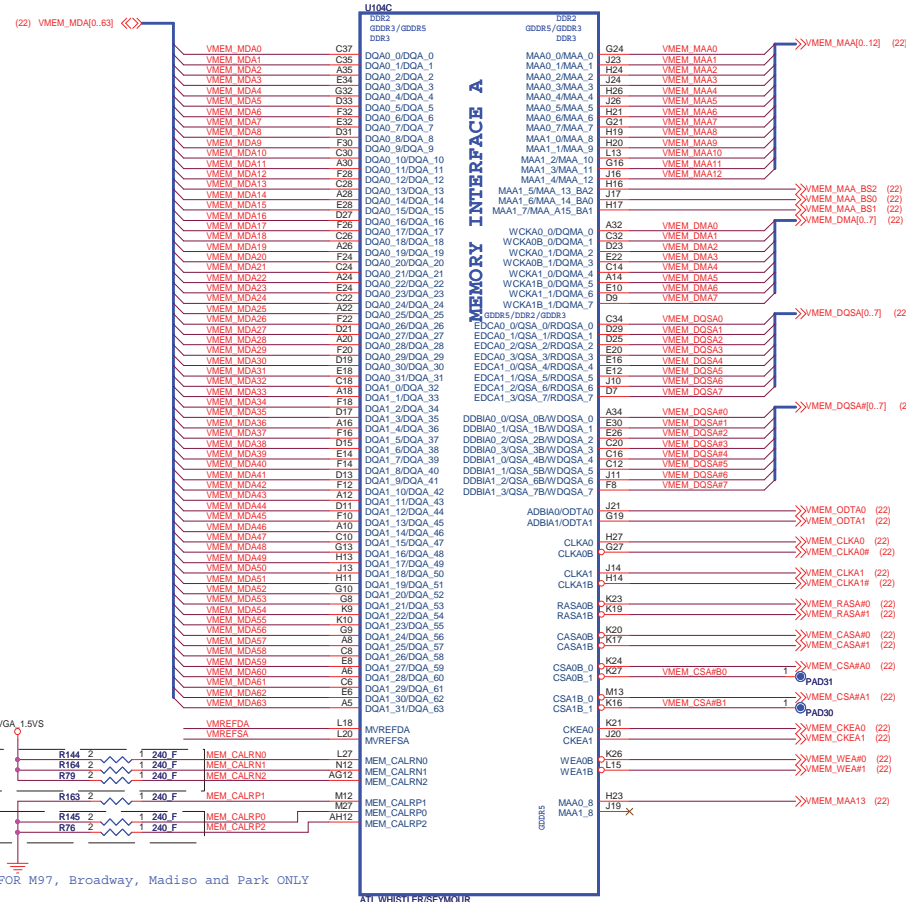


Seymour XT:
 HPMH-10-002000049G - IC Seymour-XT/PRO 216-0809000 FCBGA-962
 Whistler Pro:
 HPMH-10-002000050G - IC 216-0810005 Whistler PRO-M2 FCBGA-962

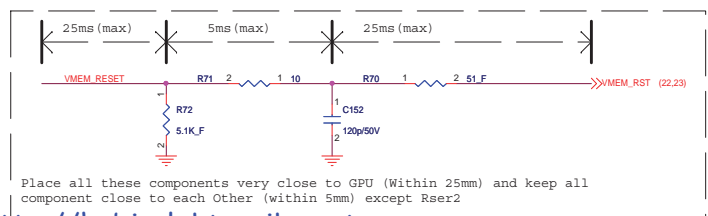
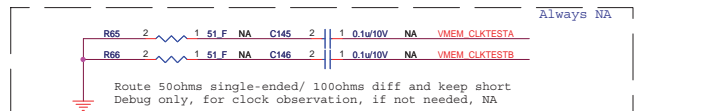
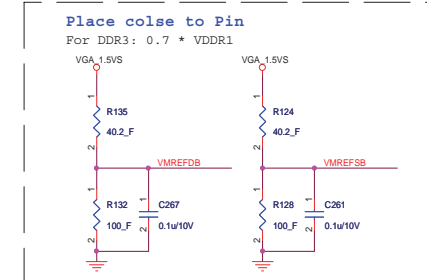
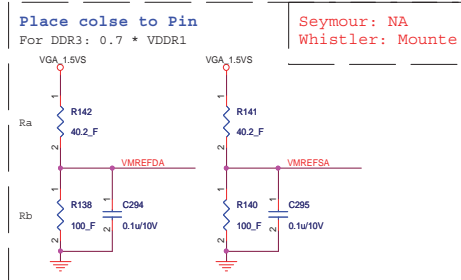
PWRGOOD
 For Broadway, Madison and Park the PWRGOOD ball must be connected to ground

FLEXComputing

Project Name : H510UA1	Title : DGPU - PCI-E/ LVDS I/F
Size : Document Number : HPMH-40GAB6300-D	Rev : D
Date : Thursday, December 30, 2010	Sheet : 15 of 51



DIVIDER RESISTORS	DDR3 / GDDR3
MVREF TO 1.5V (Ra)	40.2R
MVREF TO GND (Rb)	100R



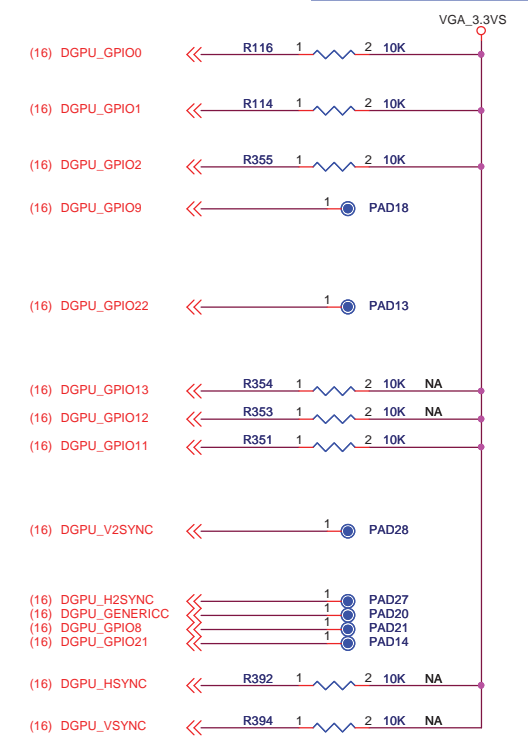
Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2

FLEX Computing

Project Name: H510QA1	Title: DGPU - VRAM I/F
Size: _____	Document Number: HPMH-40GAB6300-D
Date: Thursday, December 30, 2010	Rev: D
Sheet: 17 of 51	

DGPU STRAP

CONFIGURATION STRAPS				
STRAPS	PIN	DESCRIPTION	ASIC Deault	Status
TX_PWRS_ENB	GPIO0	Transmitter (Tx) power savings enable 0: 50% Tx output swing (DEFAULT) 1: Full Tx output swing	All Internal Pull Down	Mounted
TX_DEEMPH	GPIO1	PCI Express transmitter deemphasis enable. 0: Tx de-emphasis disabled (DEFAULT) 1: Tx de-emphasis enabled		Mounted
RESERVED	GPIO2	0 : PCIe device as 2.5 GT/s capable (DEFAULT) 1 : PCIe device as 5.0 GT/s capable		Mounted
VGA_DIS	GPIO9	VGA disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space): 0 : VGA Controller capacity enabled (DEFAULT) 1 : The device will not be recognized as the system's VGA controller		NA
BIOS_ROM_EN	GPIO_22_ROMCSB	0 - Disable external BIOS ROM device (DEFAULT) 1 - Enable external BIOS ROM device		NA
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	BIOS_ROM_EN = 1, Config[2:0] defines the ROM type. BIOS_ROM_EN = 0, Config[2:0] defines the primary memory aperture size. Size of the primary memory apertures CONFIG[2:0] 128 MB 000 256 MB 001 64MB 010 32MB 011		NA NA Mounted
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS L: Ignore VIP Device Strap (DEFAULT) H: Enable VIP Device Strap		NA
RSVD RSVD RSVD RSVD	H2SYNC GENERICC GPIO8 GPIO21_BB_EN			NA NA NA NA
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI		NA NA



Signal	Seymour/Whistler	Robson/ Park/ Medison/ Capilano/ Broadway
Ball AJ21 on M2 Ball AG13 on S3	SWAPLOCKA SwaplockA/ B signals can be optionally used on a multi-GPU design with multiple display outputs to allow all displays in a group (group A or group B) to update at the same time and have synchronous left/ right stereo timing. Genlock of the GPUs is also needed, either via a genlock system, or by feeding all GPUs with the same reference clock. Also connecting SwaplockB is preferred, but not required. SwaplockA/ B are open drain, 3.3V signals. If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AJ21 is NC on M2 packages Ball AG13 is R2SET on S3 package
Ball AK21 on M2 Ball H12 on S3	SWAPLOCKB - see above On a multi-gpu design, SwaplockB from all GPUs are connected together with an external pull-up resistor (10K Ohms). If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AK21 is NC on M2 packages Ball AH12 is DAC2 Output - on S3 package

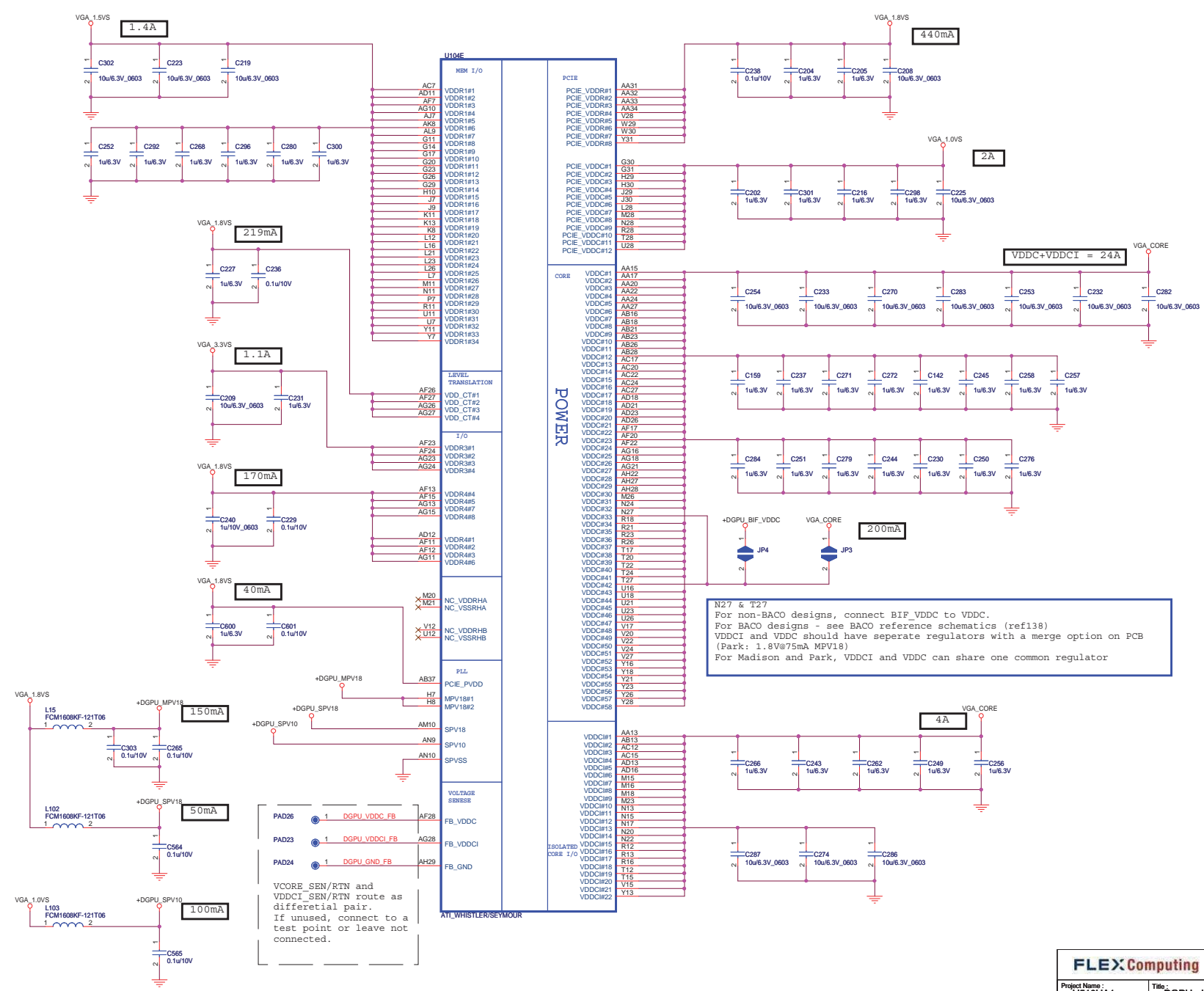
Signal	Seymour/Whistler	Robson/ Park/ Medison/ Capilano/ Broadway
Ball AC32 on M2	NC	DAC2 Output-C on M2 package
Ball AA29 on M2	NC	R2SET on M2 package
Ball AD32 on M2	NC	DAC2 Output- Y
Ball AG33 on M2	NC	A2VDD
Ball AD33 on M2	NC	A2VDDQ
Ball AF33 on M2	TSVSSQ	A2VSSQ
Ball AG33, AG32 on M2	NC	VDD2DI/VSS2DI
H2SYNC	GENLK_CLK (3.3V): Reference clock input (3.3V) for pixel PLL received from frame-lock/gen-lock interface	H2SYNC
V2SYNC	GENLK_VSYNC (3.3V): Frame timing indicator. Output to frame-lock/genlock interface	V2SYNC

FLEX Computing

Project Name : H510UA1 Title : DGPU - Strap

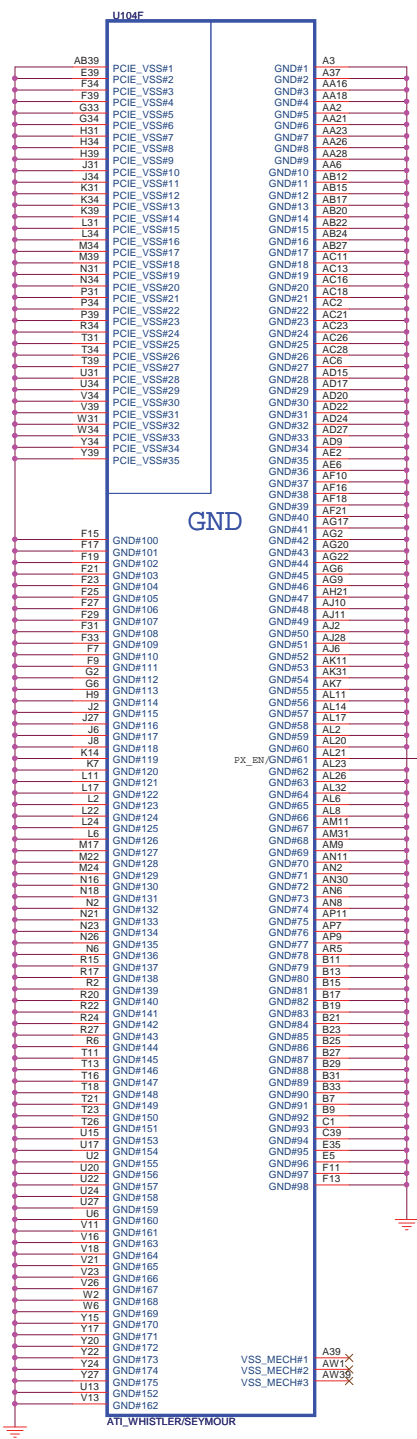
Size : Document Number : HPMH-40GAB6300-D Rev : D

Date : Thursday, December 30, 2010 Sheet : 18 of 51



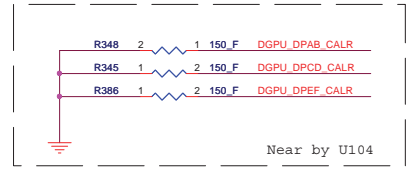
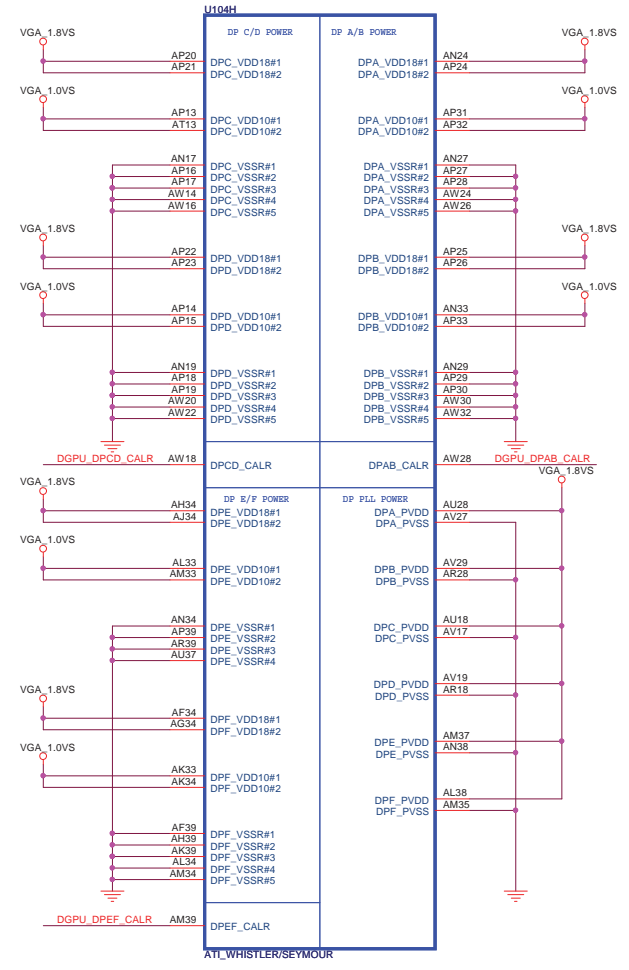
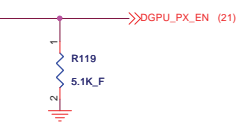
N27 & T27
 For non-BACO designs, connect BIF_VDDC to VDDC.
 For BACO designs - see BACO reference schematics (ref138)
 VDDCI and VDDC should have separate regulators with a merge option on PCB
 (Park: 1.8V@75mA MPV18)
 For Madison and Park, VDDCI and VDDC can share one common regulator

VCORE_SEN/RIN and VDDCI_SEN/RIN route as differential pair. If unused, connect to a test point or leave not connected.



BACO design options as Apps Note Seymour/ Whistler/ Robson supported Park/ Madison/ Capilano/ Broadway not Applicable

For PX_EN, refer to the BACO reference schematics for detail.
PX_EN is used to control discrete GPU regulators for PowerXpress (Switchable graphics) BACO mode. A pull-down resistor is required. Leave signal unconnected if not used.



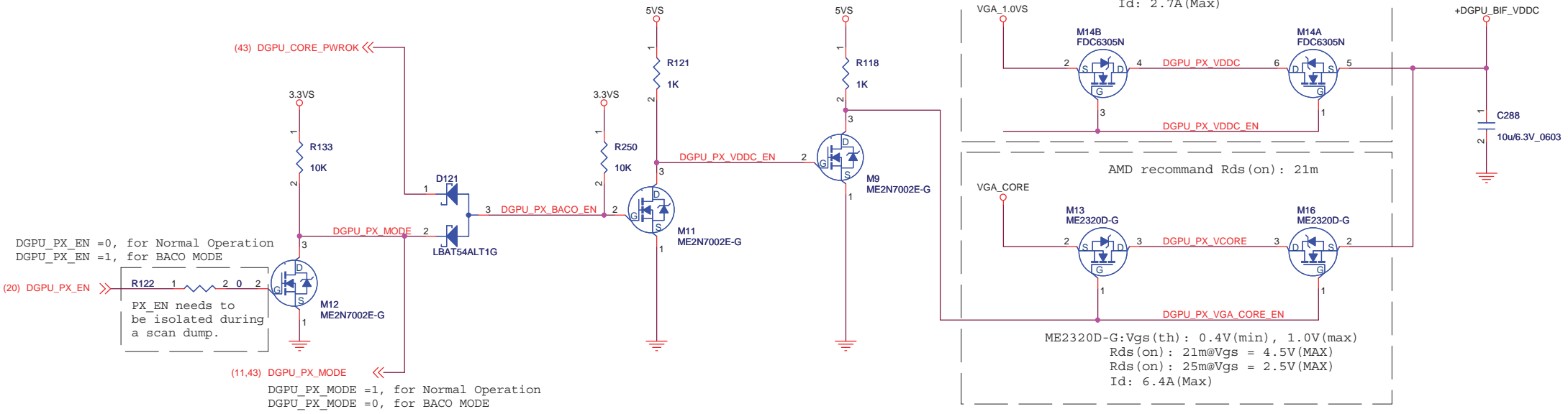
FLEX Computing

Project Name: H510UA1 Title: DGPU - Display PWR/ GND

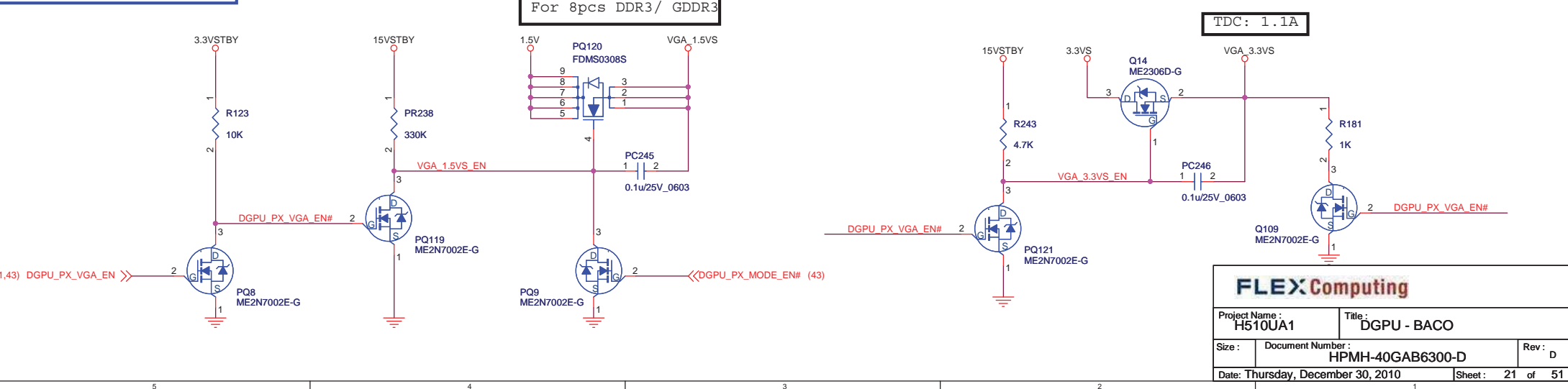
Size: Document Number: HPMH-40GAB6300-D Rev: D

Date: Thursday, December 30, 2010 Sheet: 20 of 51

DGPU BACO



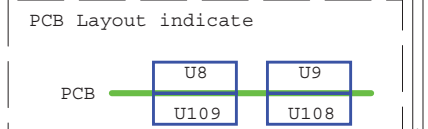
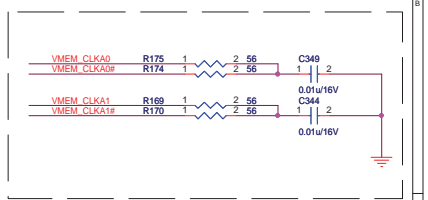
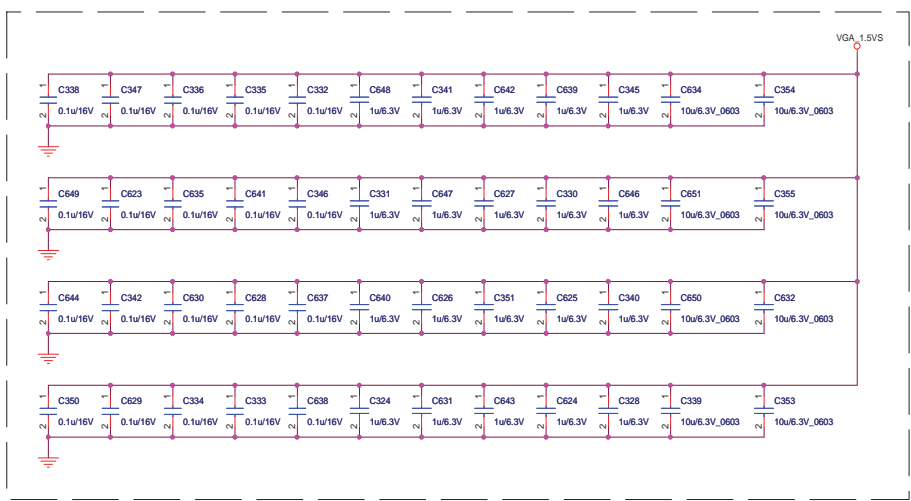
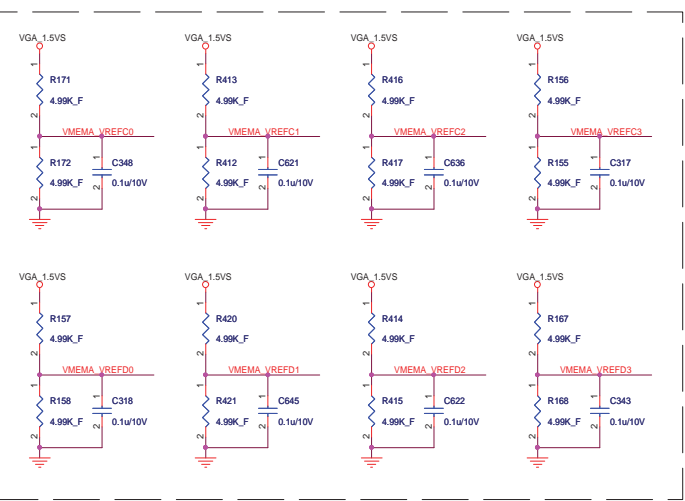
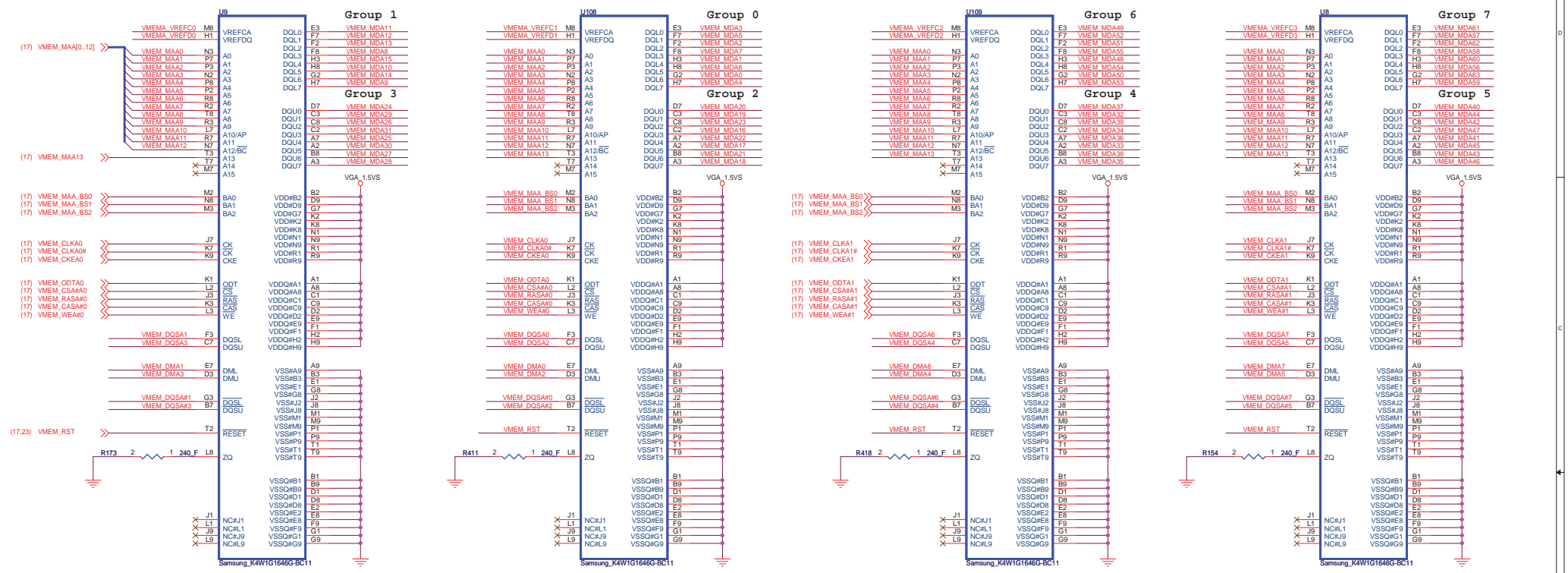
DGPU PWRSW



DGPU VRAM Channel - A

Samsung/ K4W1G1646G-BC11
 Flex P/N: HPMH-14-00D0000042G
 HP B&S P/N: HPMJ-506474-945
 Hynix/ H5TQ1G63DFR-11C
 Flex P/N: HPMH-14-00D0000040G
 HP B&S P/N: HPMJ-506474-344

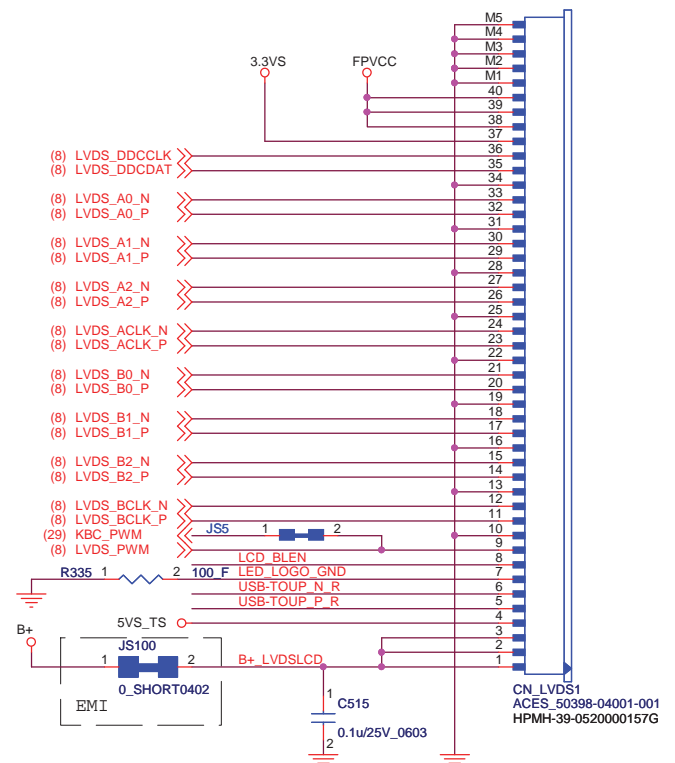
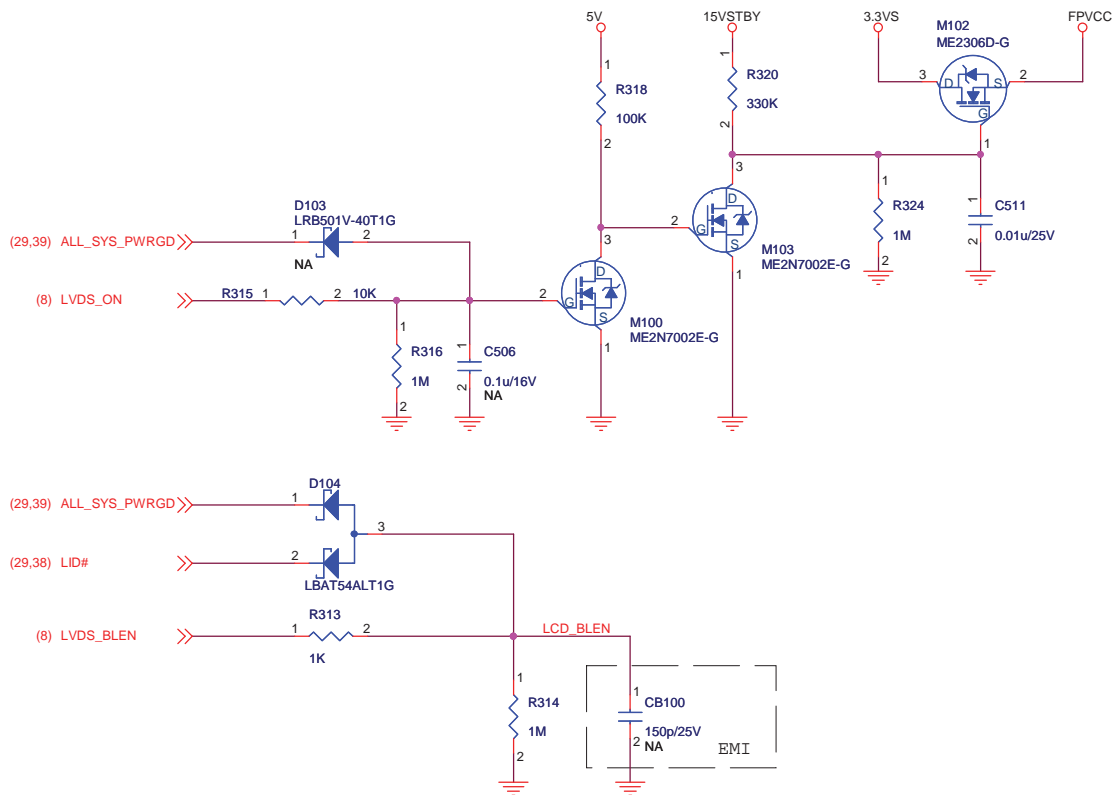
(17) VMEM_MDA0_63
 (17) VMEM_MDA0_7
 (17) VMEM_DQSA0_7
 (17) VMEM_DQSA0_7



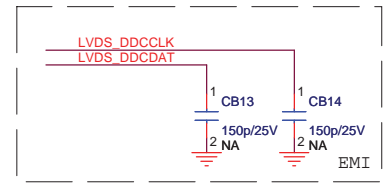
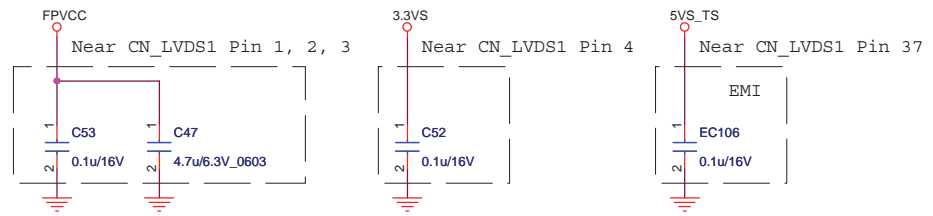
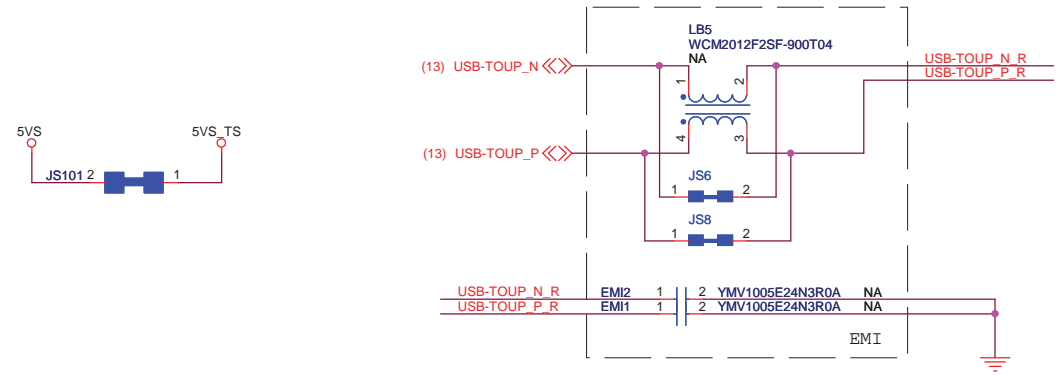
FLEX Computing

Project Name: H510UA1	Title: DGPU - VRAM Channel - A
Size:	Document Number: HPMH-40GAB6300-D
Date: Thursday, December 30, 2010	Rev: D
Sheet: 22 of 51	

LVDS

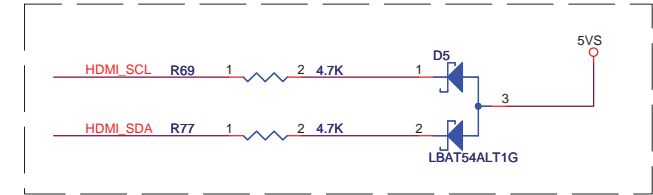
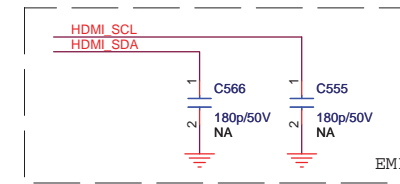
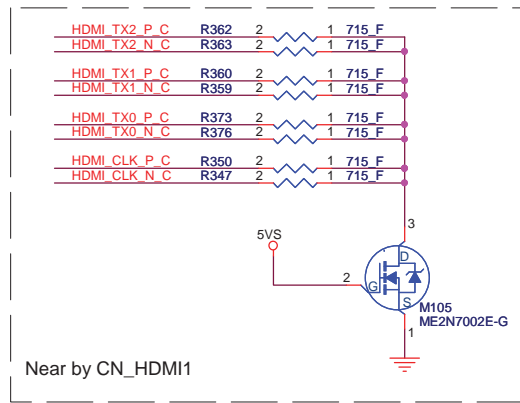
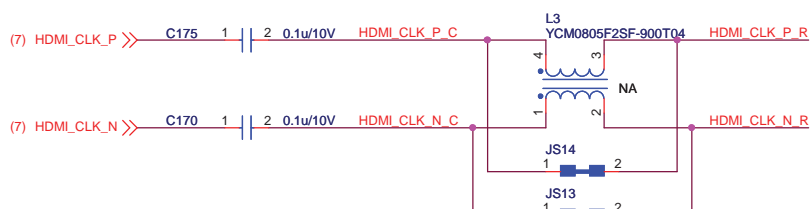
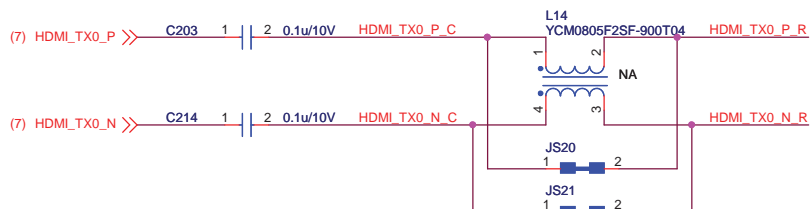
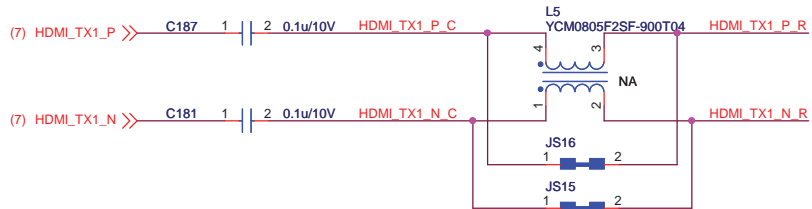
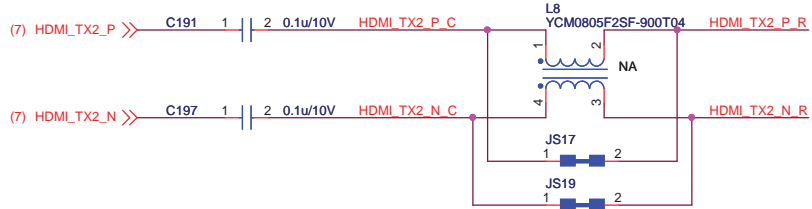


Touch Screen

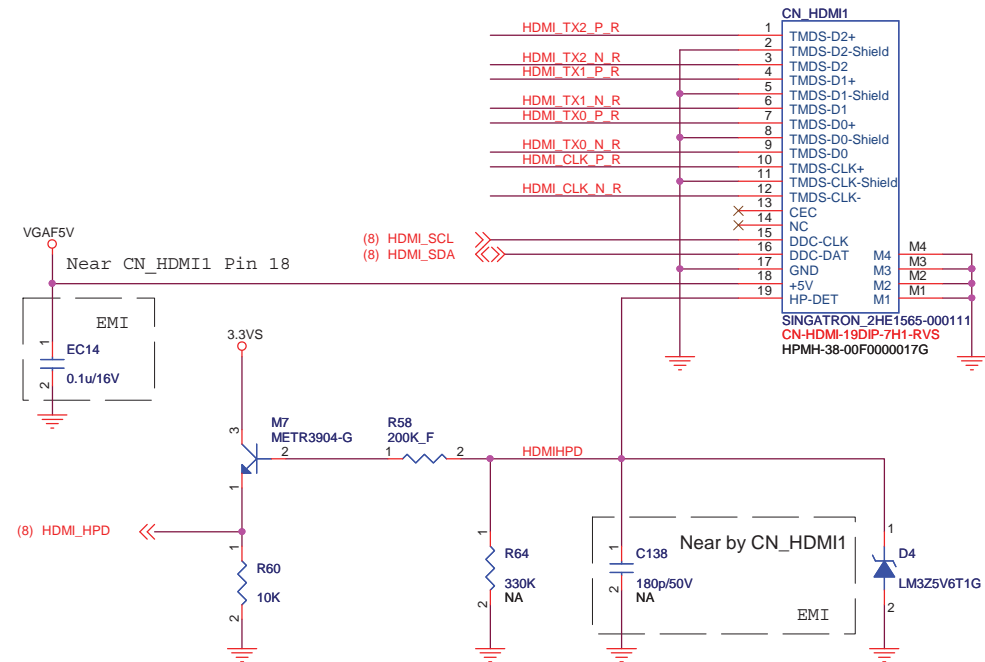


FLEX Computing	
Project Name : H510UA1	Title : LVDS/ Touch Screen I/F
Size :	Document Number : HPMH-40GAB6300-D
Date : Thursday, December 30, 2010	Rev : D
Sheet : 24 of 51	

HDMI



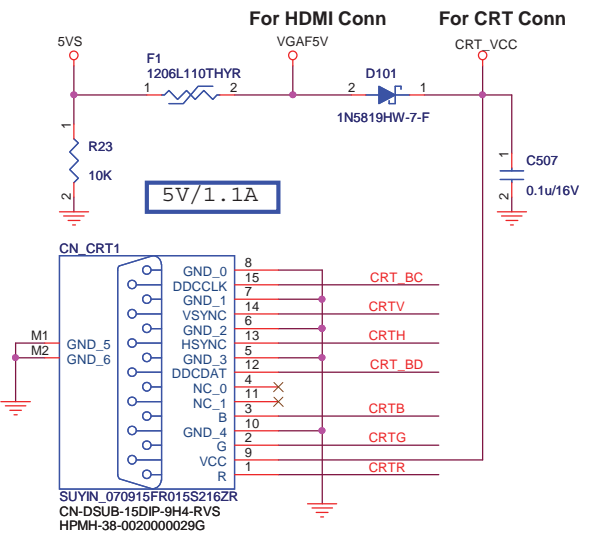
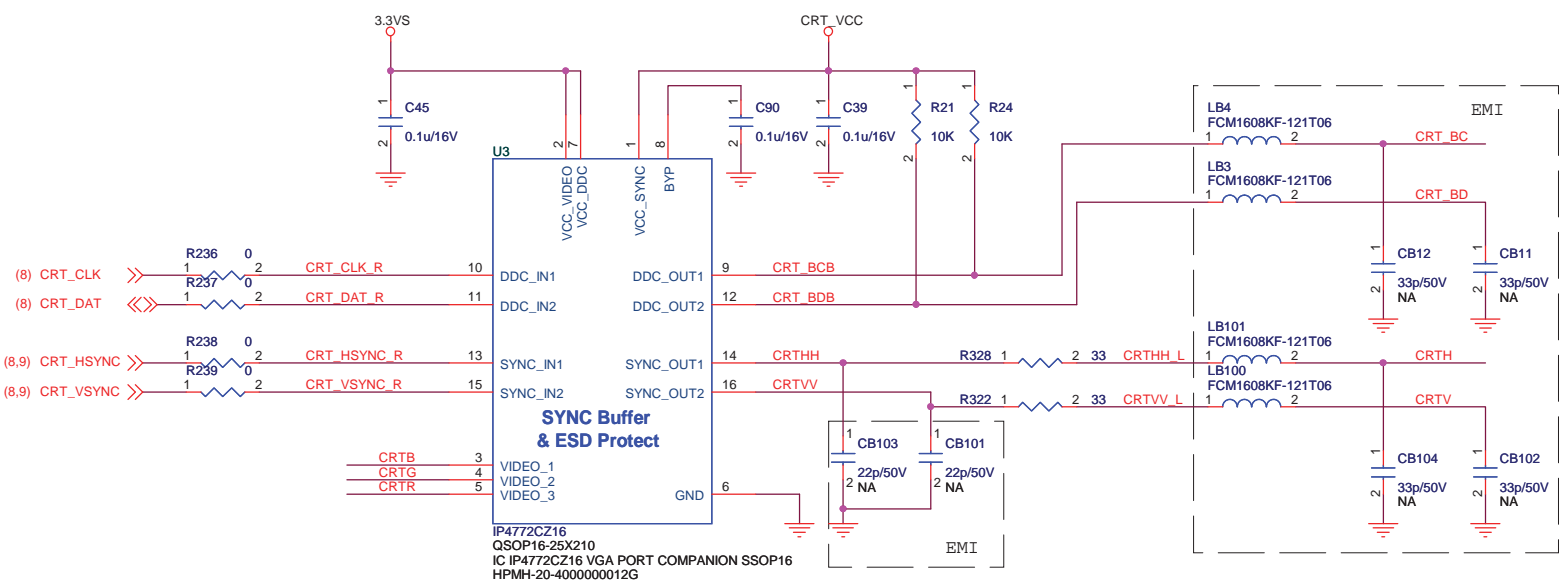
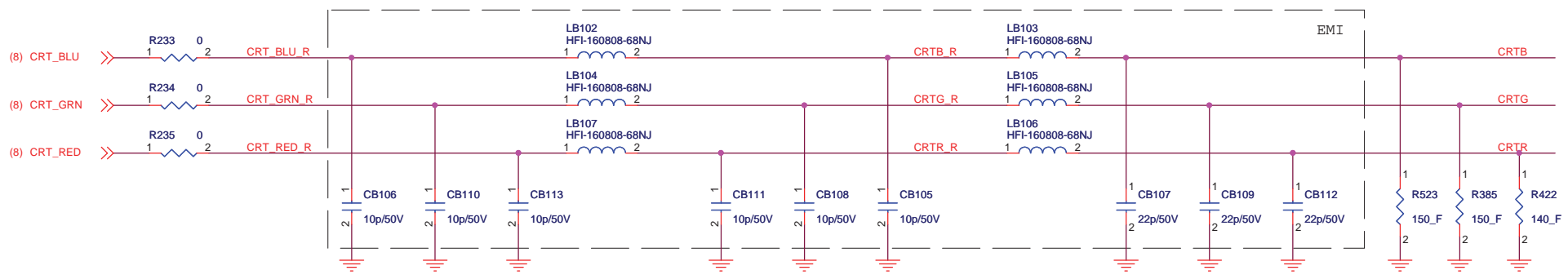
Near by CN_HDMI1



FLEXComputing

Project Name : H510UA1		Title : HDMI I/F	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D	
Date : Thursday, December 30, 2010		Sheet : 25 of 51	

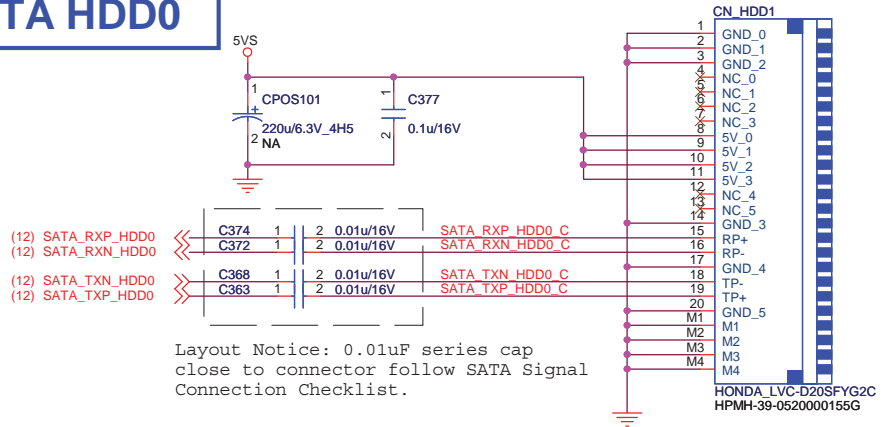
CRT



FLEX Computing

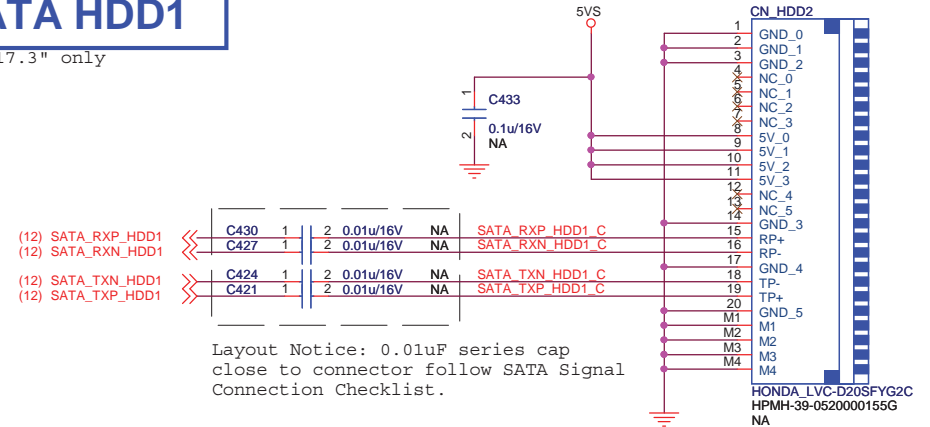
Project Name: H510UA1	Title: D-sub I/F
Size:	Document Number: HPMH-40GAB6300-D
Date: Thursday, December 30, 2010	Rev: D
Sheet: 26 of 51	

SATA HDD0

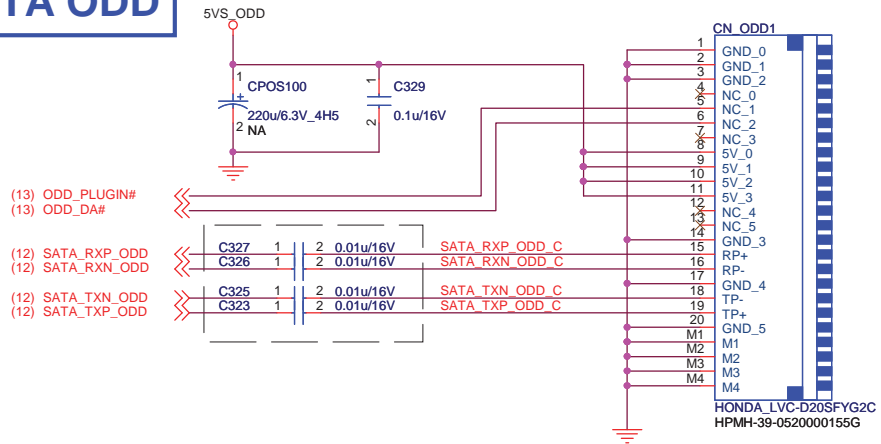


SATA HDD1

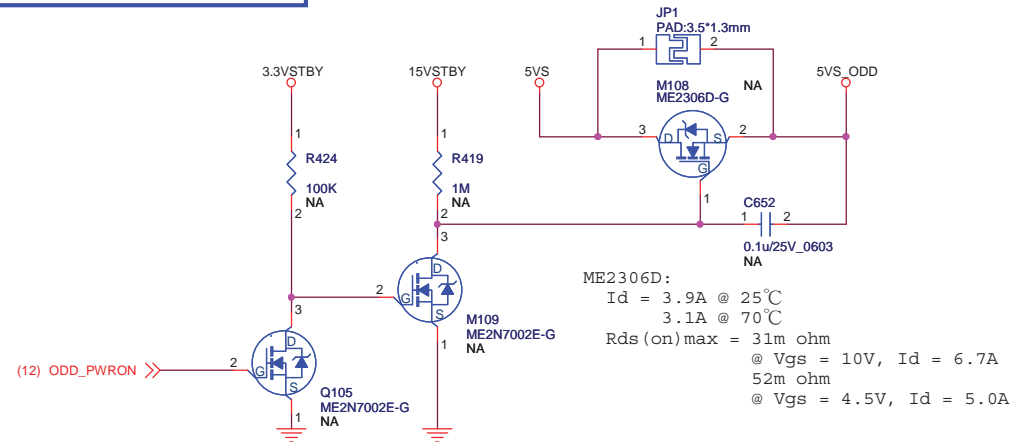
For 17.3" only



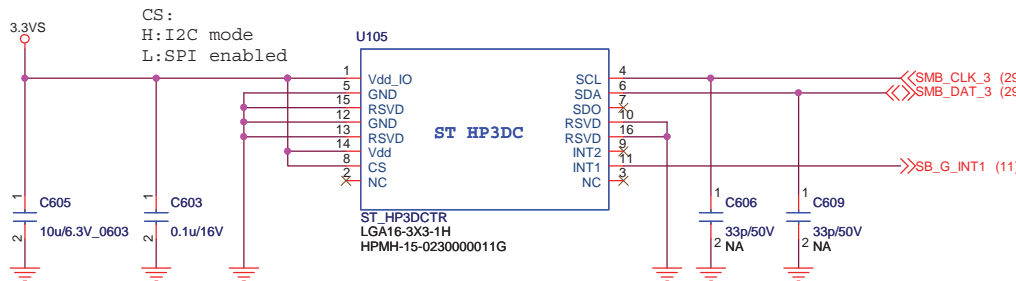
SATA ODD



ODD Zero PWR



G-Sensor



G-SENSOR - ST HP3DC

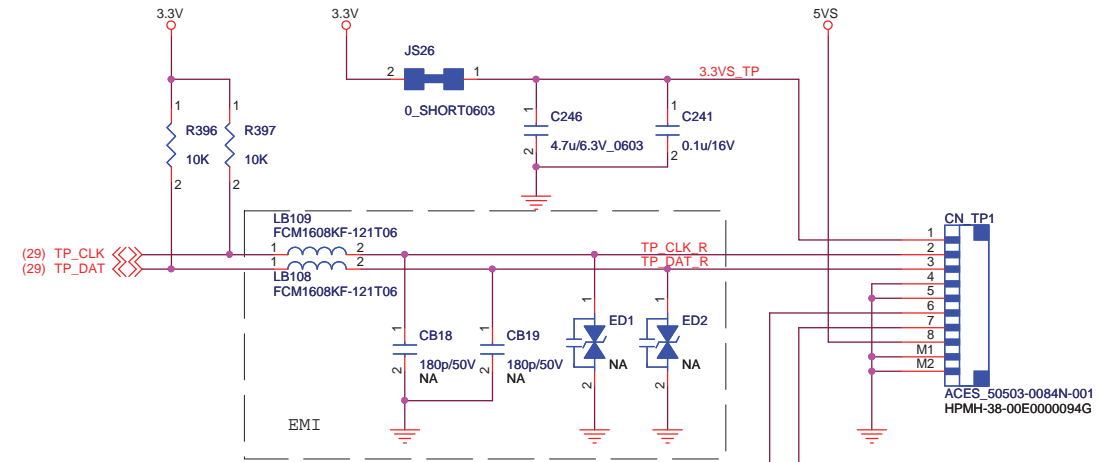
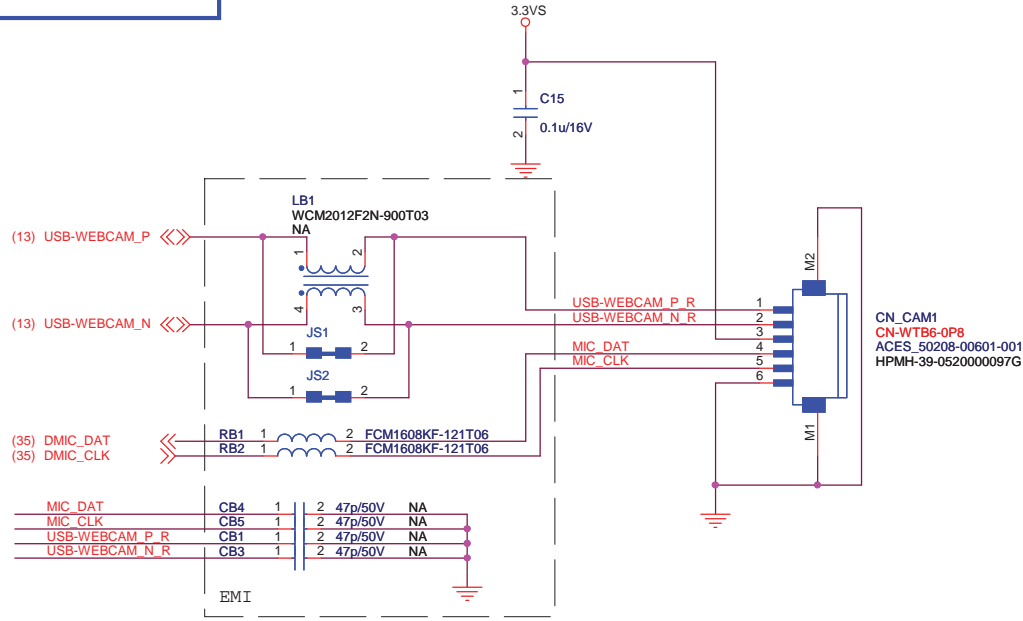
3.3VS
 ADDR: 0001100x(30h) - SDO PD
 ADDR: 0011101x(32h) - SDO NC
 SINK: ?mA@VOL=0.33V (MAX)

FLEXComputing

Project Name: H510UA1		Title: HDD/ ODD/ Zero PWR/ G-sensor	
Size:	Document Number: HPMH-40GAB6300-D	Rev:	D
Date: Thursday, December 30, 2010		Sheet: 27 of 51	

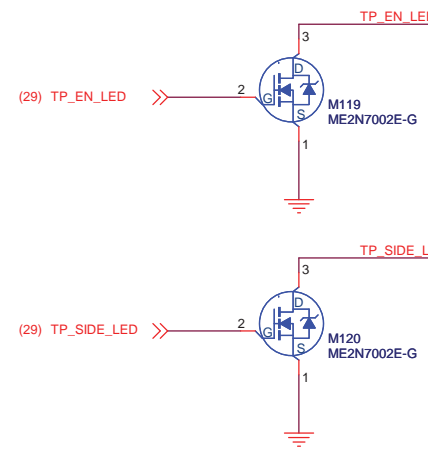
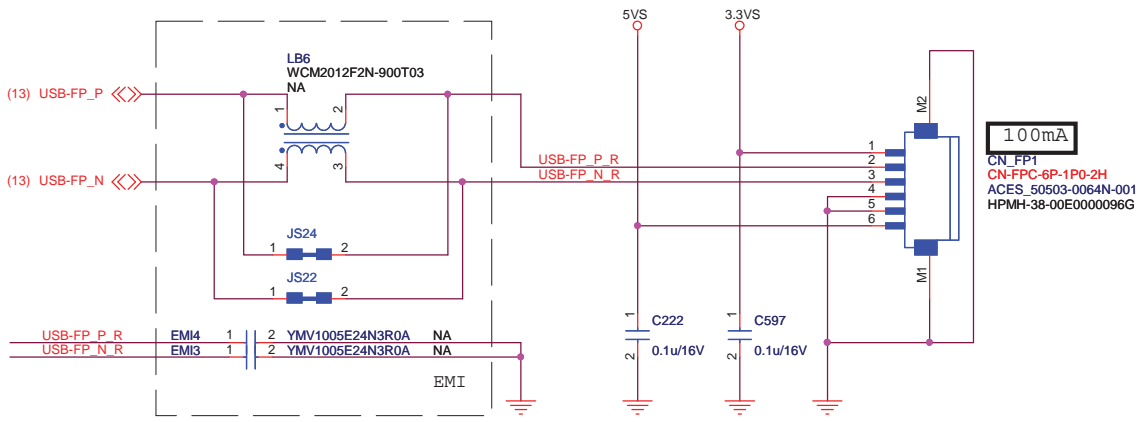
Web CAM

T/P



Finger Printer

Remve Finger Printer copenents for IMR

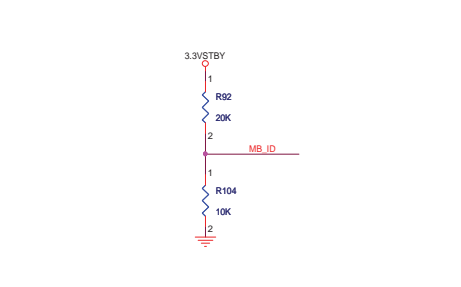
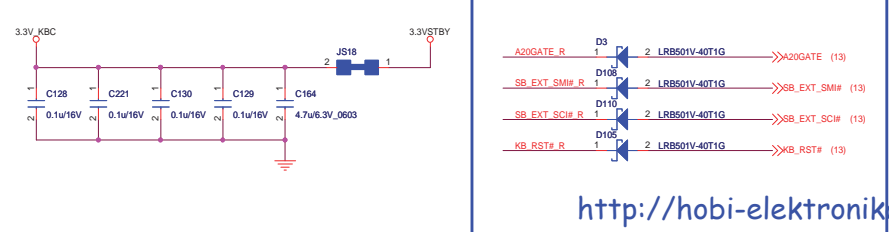
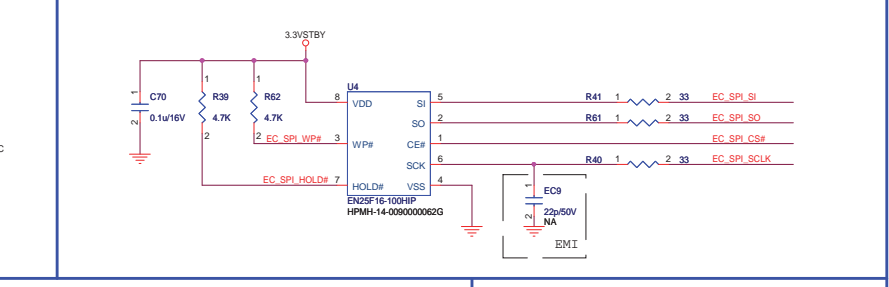
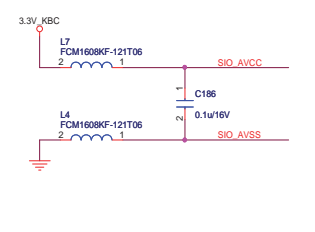
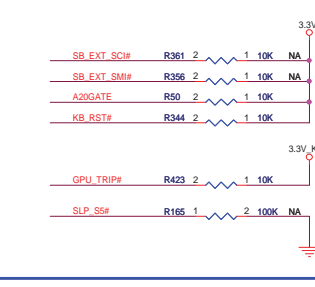
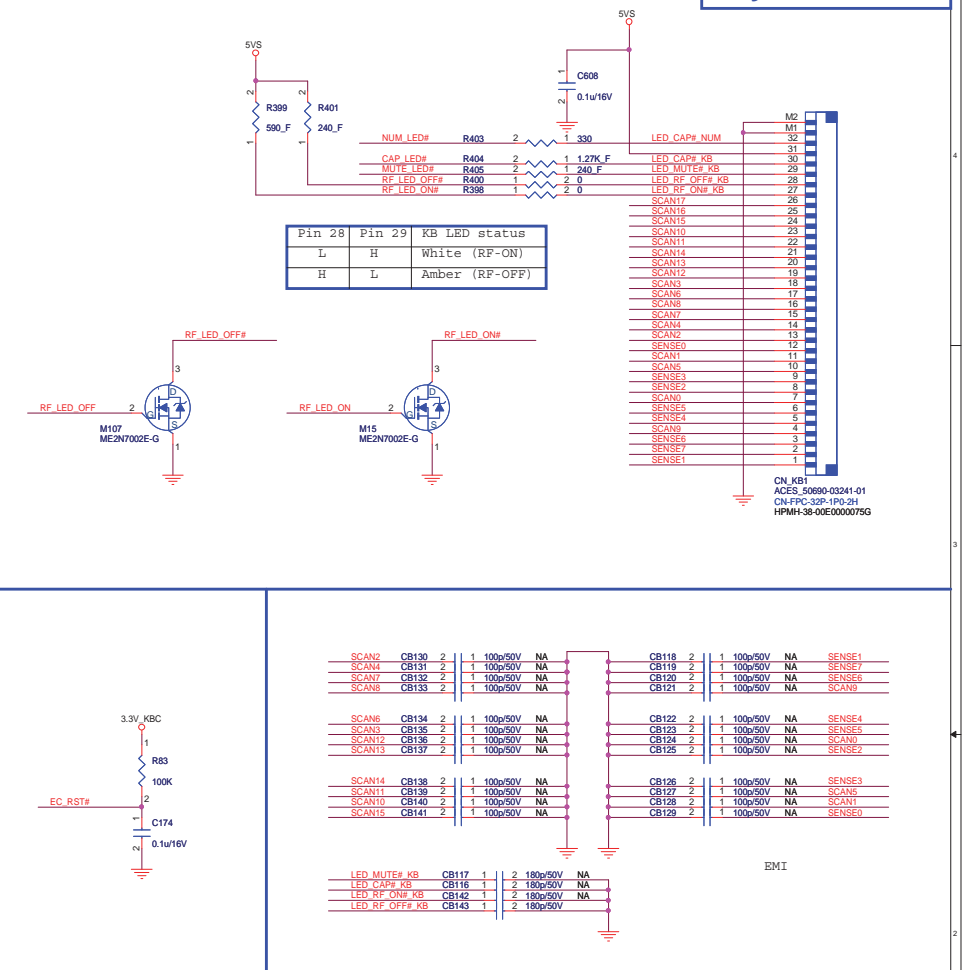
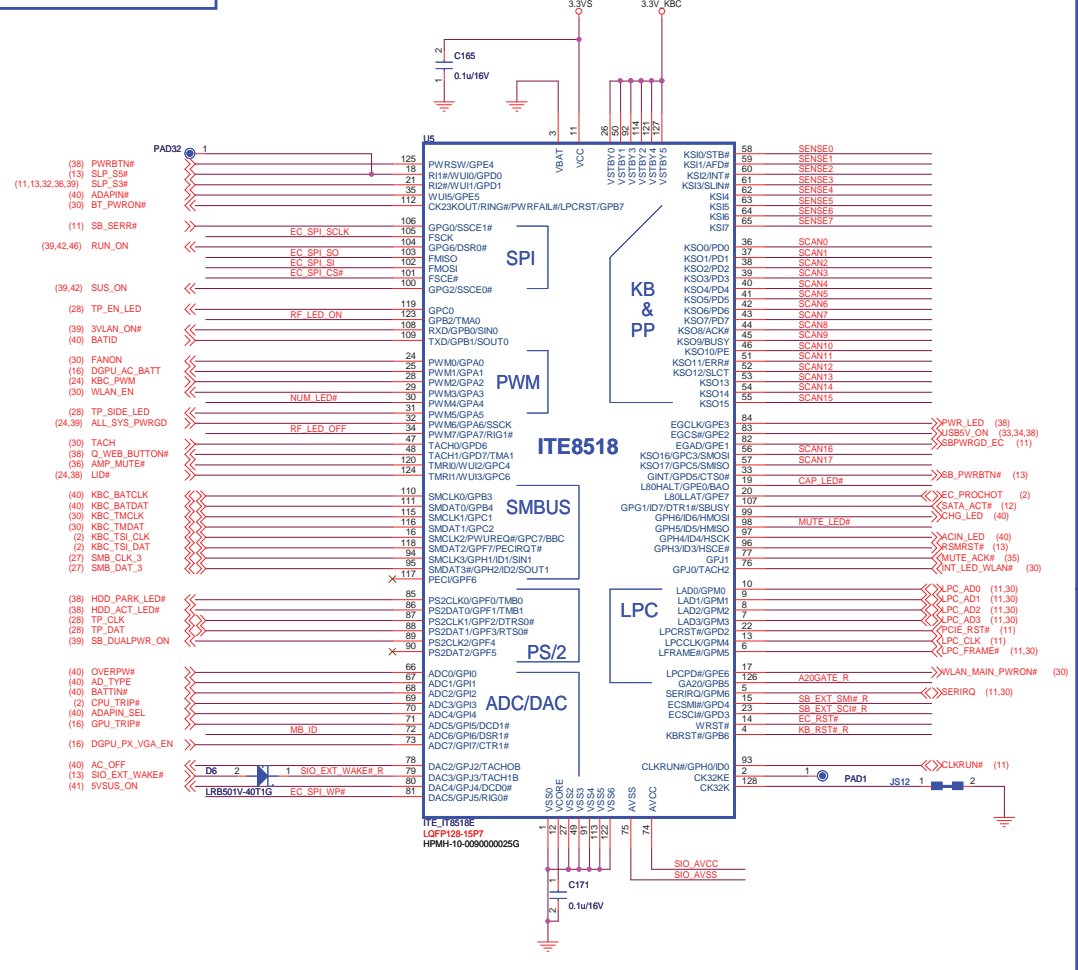


FLEX Computing

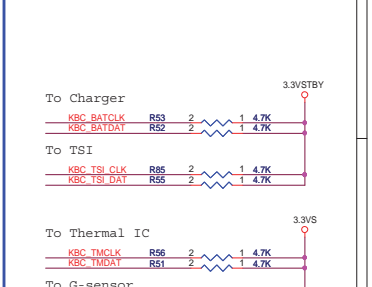
Project Name : H510UA1	Title : WebCAM/ BT/ FP/ Touch Screen
Size : Document Number : HPMH-40GAB6300-D	Rev : D
Date : Thursday, December 30, 2010	Sheet : 28 of 51

EC/ ITE8518E

Keyboard Conn



MB-ID	INTEL-DI	R92: 10K -- HPMH-30-301036-990G
3.3V	INTEL-DI	R104: NA
2.2V	INTEL-UI	R92: 10K -- HPMH-30-301036-990G
		R104: 20K -- HPMH-30-102036-990G
1.1V	AMD-DA	R92: 20K -- HPMH-30-102036-990G
		R104: 10K -- HPMH-30-301036-990G
GND	AMD-UA	R92: NA
		R104: 10K -- HPMH-30-301036-990G



FLEX Computing

Project Name: H510QA1 | Title: EC/ ITE8518E

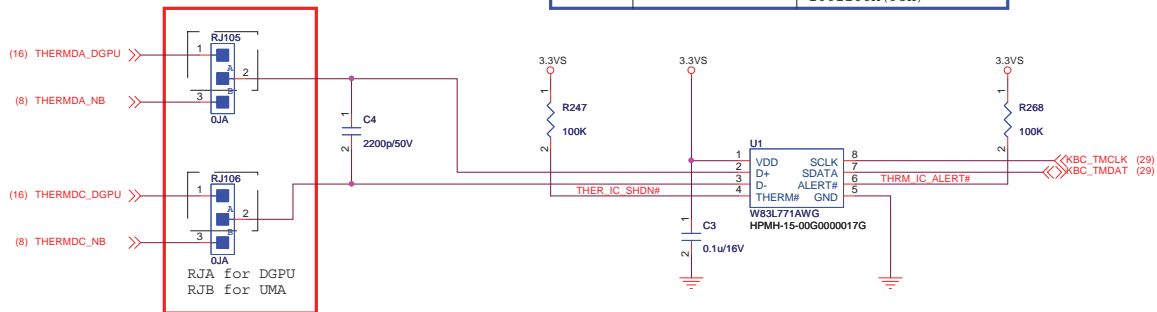
Size: | Document Number: HPMH-40GAB6300-D | Rev: D

Date: Thursday, December 30, 2010 | Sheet: 29 of 51

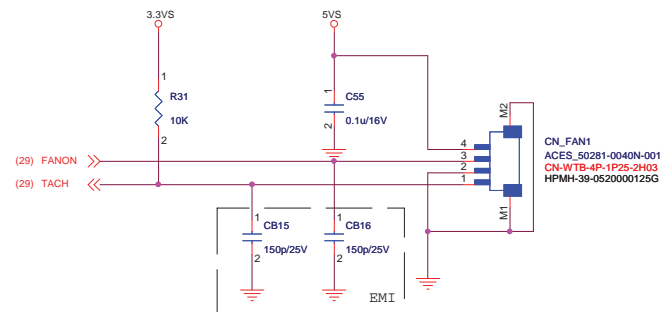
Thermal Sensor

THERMAL IC FOR CPU or DGPU

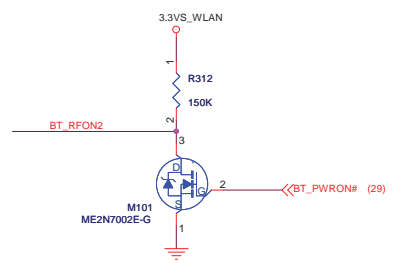
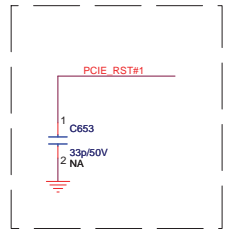
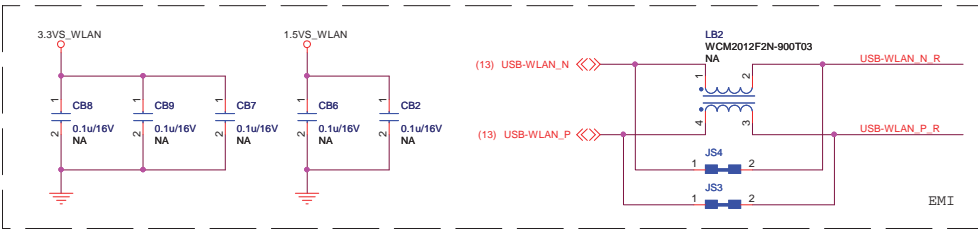
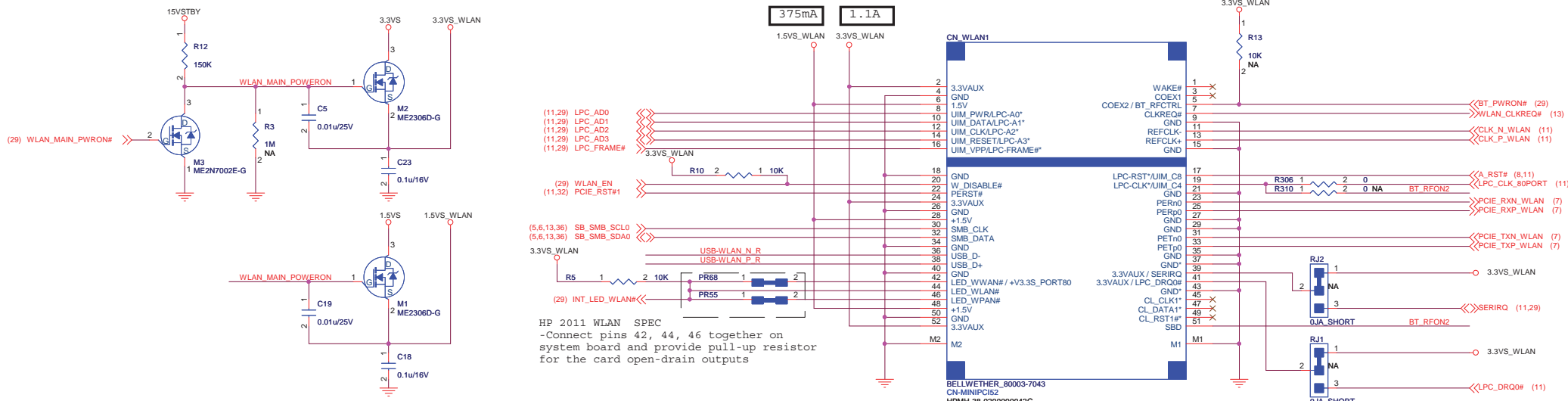
WINBOND	W83L771AWG	HPMH-15-00G0000017G 1001100x(98h)
TI	TMP431ADGKR	HPMH-15-0500000005G 1001100x(98h)



FAN



Mini PCI-E - WLAN (Half)



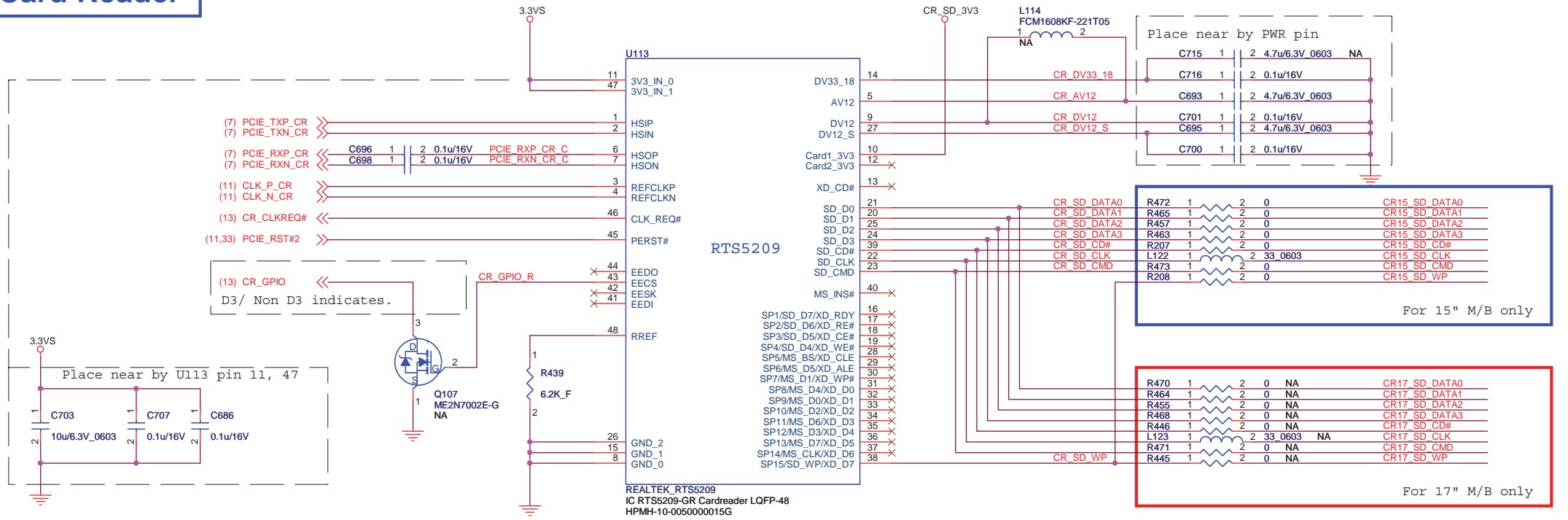
FLEX Computing

Project Name: H510UA1 Title: Thermal/ FAN/ WLAN/ HP-Logo

Size: Document Number: HPMH-40GAB6300-D Rev: D

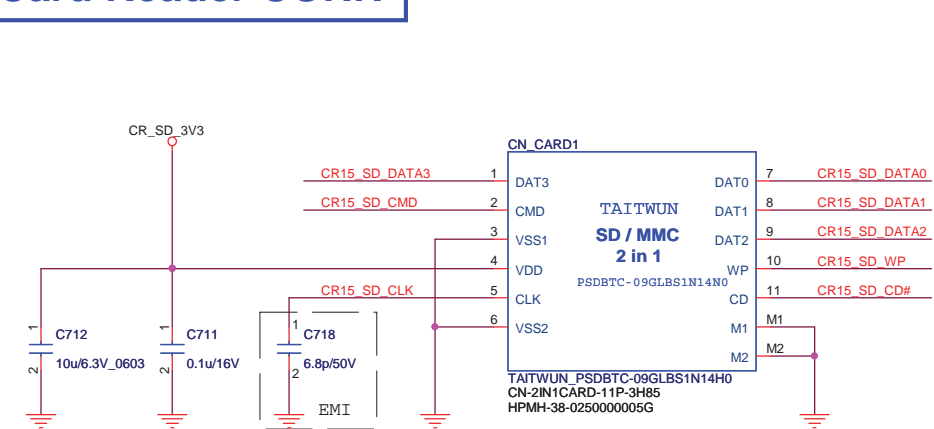
Date: Tuesday, January 11, 2011 Sheet: 30 of 51

Card Reader



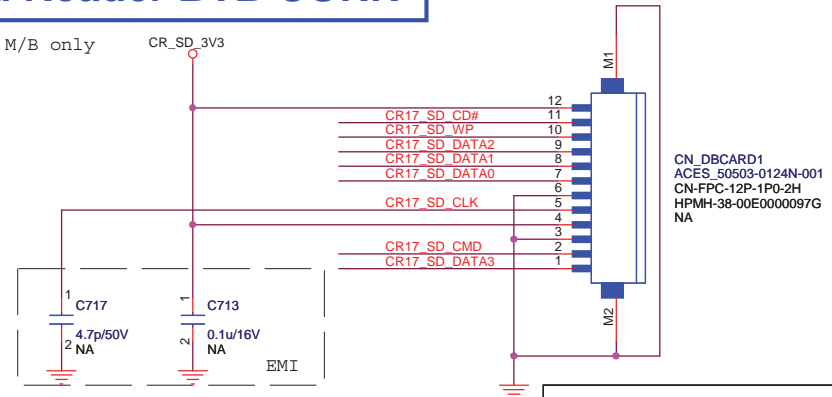
Card Reader CONN

For 15" M/B only



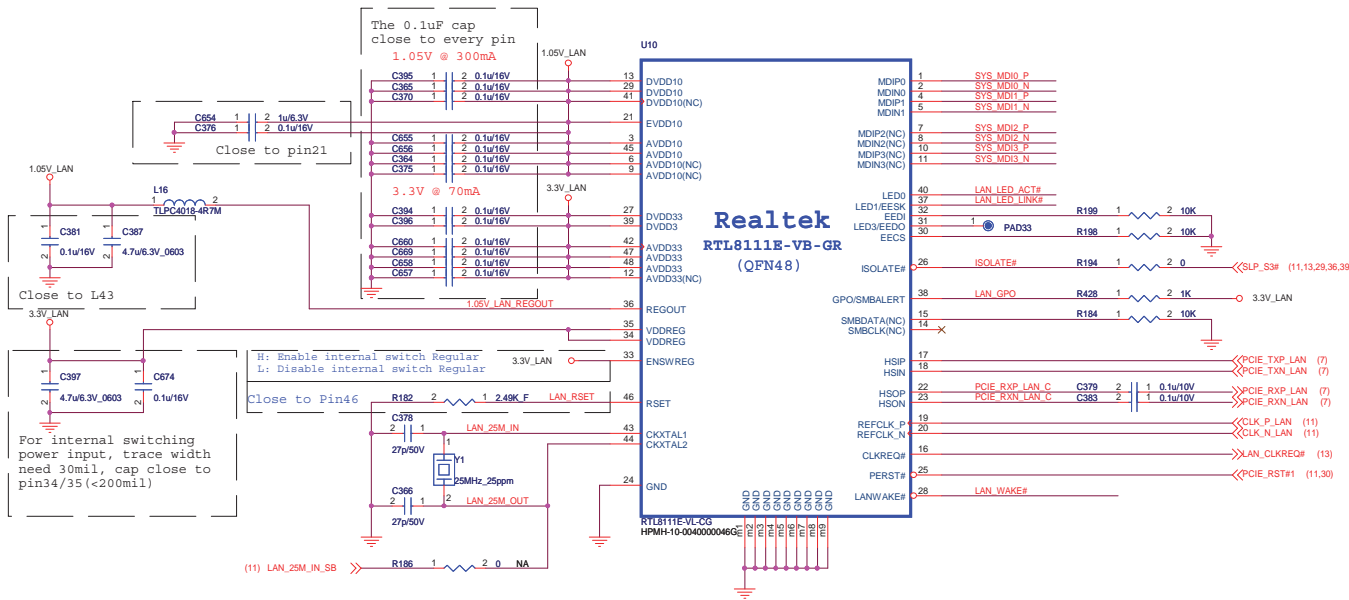
Card Reader BTB CONN

For 17" M/B only



FLEX Computing

Project Name: H510UA1		Title: Card Reader -- Realtek RTS5209	
Size:	Document Number: HPMH-40GAB6300-D	Rev:	D
Date: Thursday, December 30, 2010		Sheet: 31 of 51	

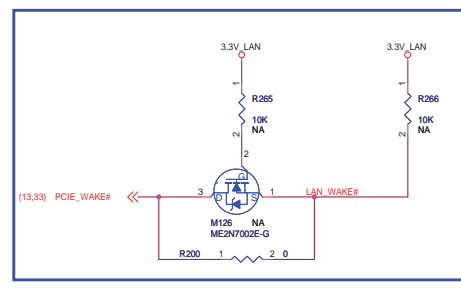


Mini-spec requirements:
 10/100/1000 :
 - Link :White
 - Activity :Amber/Yellow

RTL8111E

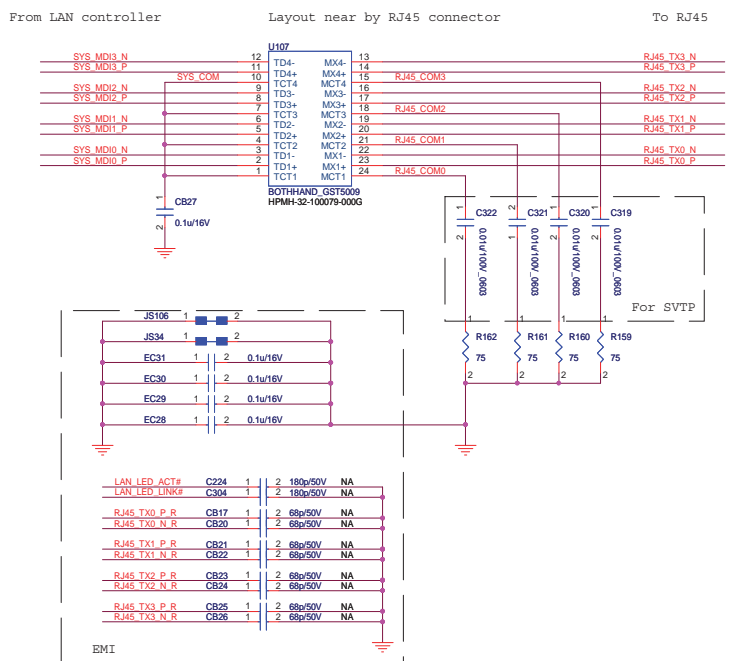
LEDS1-0	00	01	10	11
LED0	ACT ALL	LINK ALL	LINK10 /ACT ALL	LINK10 /ACT10
LED1	LINK100	LINK100	LINK100 /ACT100	LINK100 /ACT100
LED3	LINK1000	LINK1000	LINK1000 /ACT1000	LINK1000 /ACT1000

LEDS1-0s initial value comes from the EEPROM if there is no EEPROM, the default value is 11

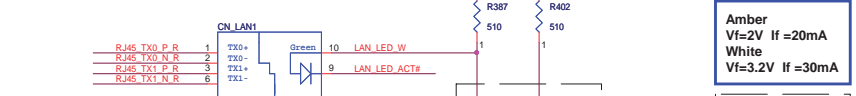
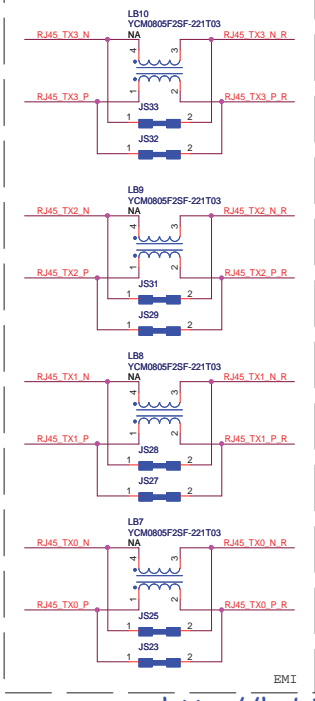


Transformer

Transformer :
 Gbit P/N: 32-100079-000G (GST5009)
 10/100 P/N: 32-000000009G (TST1284)



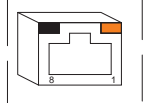
RJ45



Amber
 Vf=2V If=20mA
 White
 Vf=3.2V If=30mA

Reference:
 RJ45 Phone Jack
 Pin define:

1	TXD+0
2	TXD-0
3	TXD+1
4	TXD-2
5	TXD-2
6	TXD-1
7	TXD+3
8	TXD-3

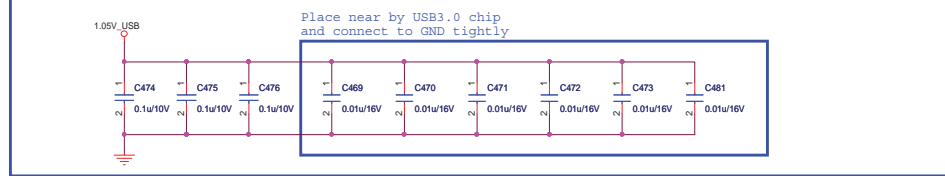
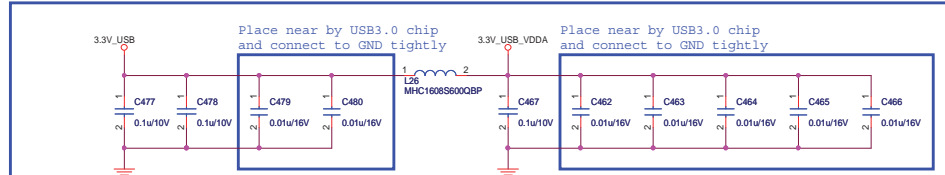
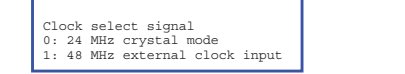
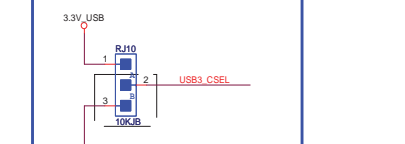
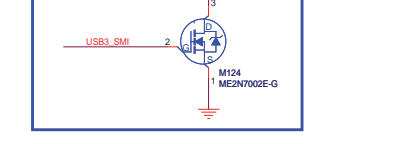
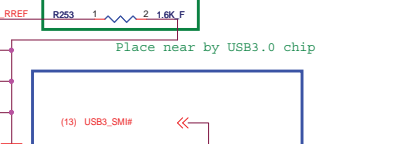
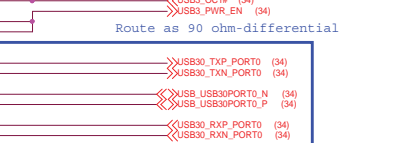
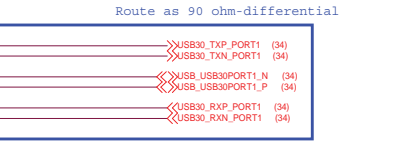
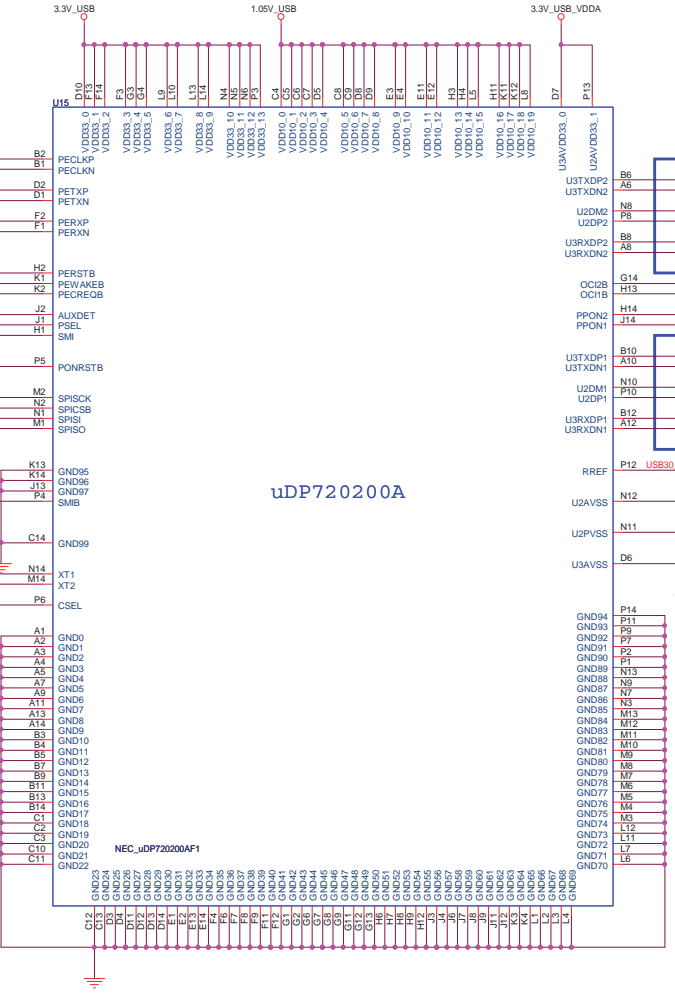
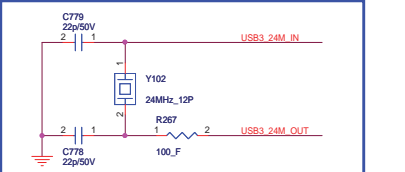
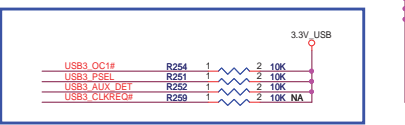
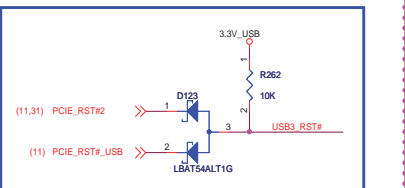
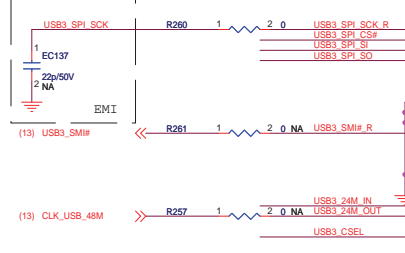
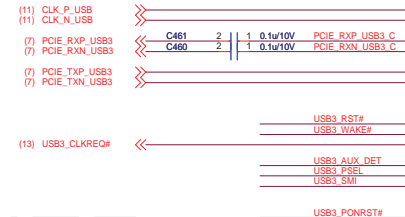
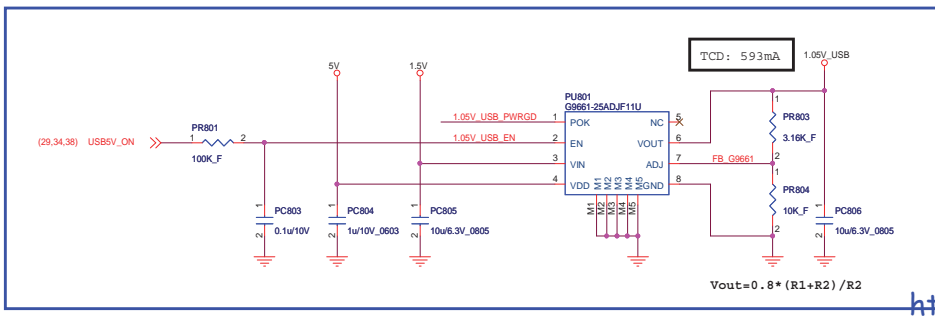
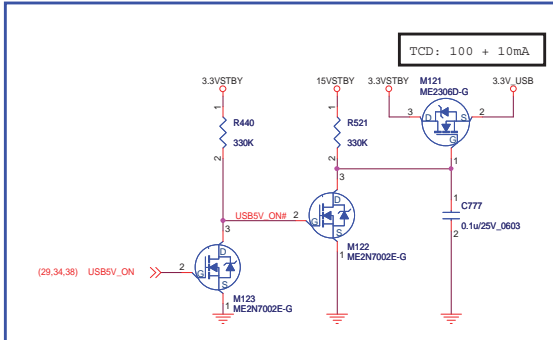
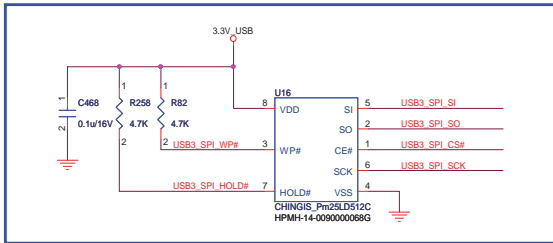
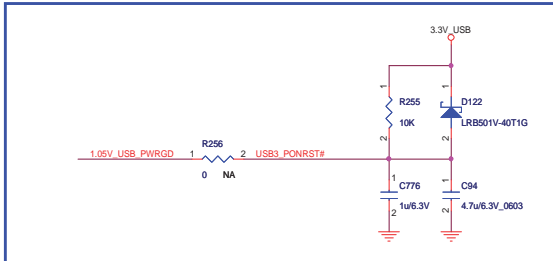
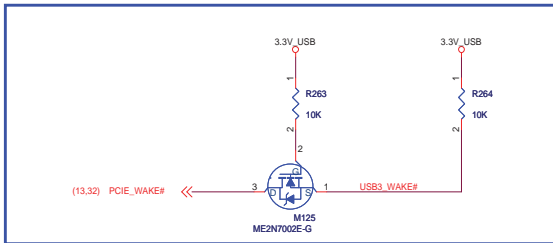


SVTP_v4.03 - 2.6 - Ethernet Checklist - Rev C.x1s

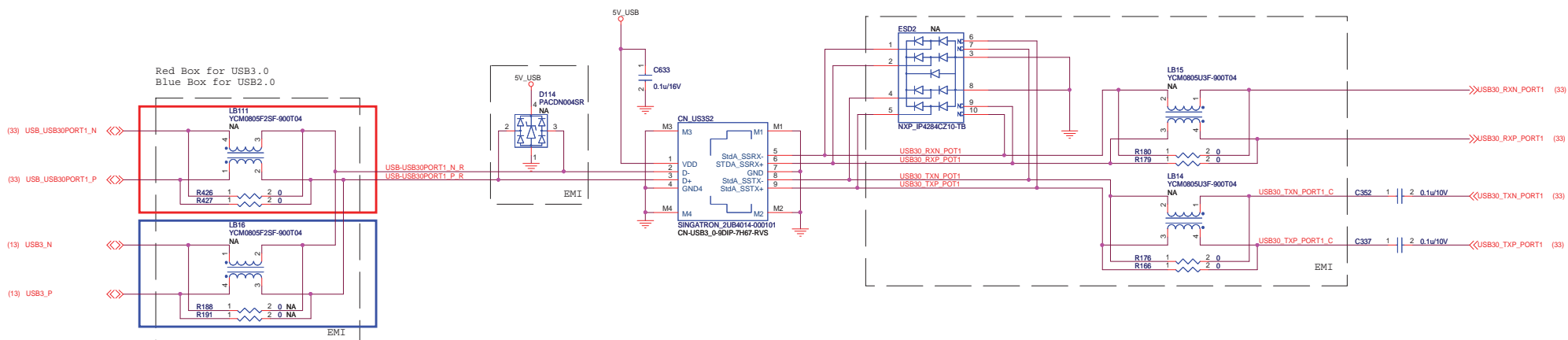
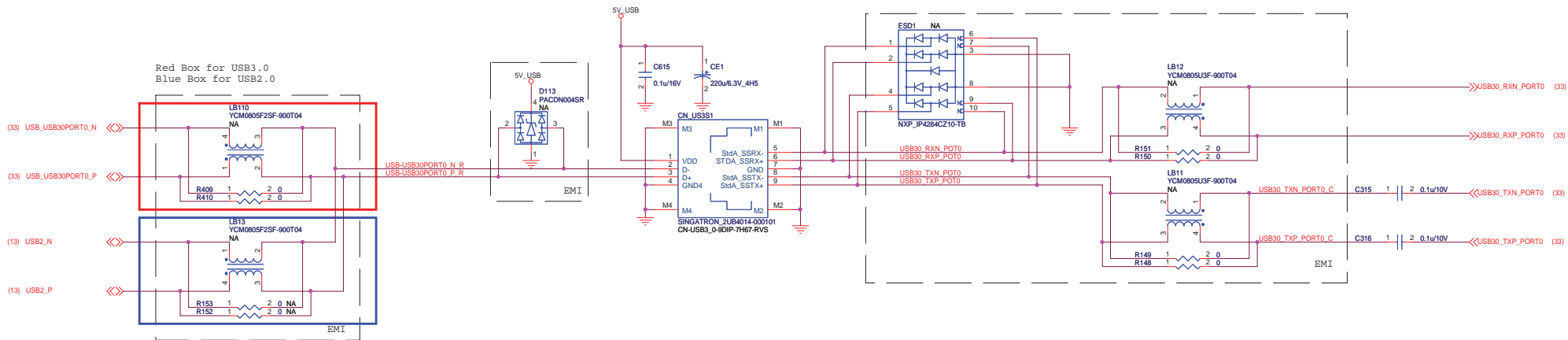
- Ch.3.1.4.4
Some older cheap RJ-45s only populate pins 1,2,3,6. 10/100 requires the other 4 pins for grounding. Gigabit Ethernet requires all 8 pins for data signals.
- Ch.3.1.4.13
Resistance from RJ-45 shell to any other chassis ground point (ohms) less than 1 ohm
- Ch.3.1.4.14 & Ch.3.1.4.15
Protection against non-standard power-over-Ethernet (PoE)
Resistance between pins 1,3 (TXD0P, TXD1P) and pins 4,7 (TXD2P, TXD3P) of the RJ-45 greater than 58K ohms.

USB3.0 Controller

Leave empty for IMR

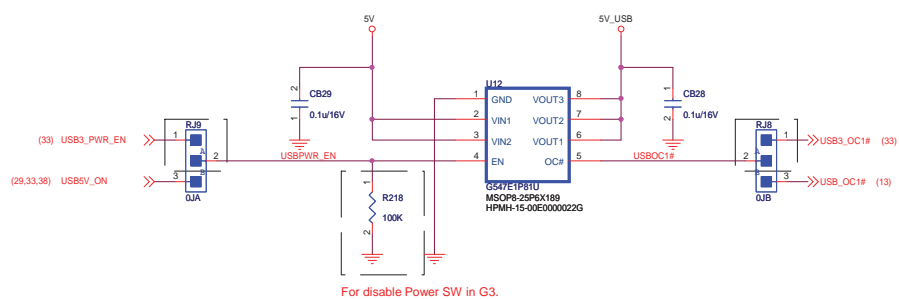


USB 3.0/ 2.0



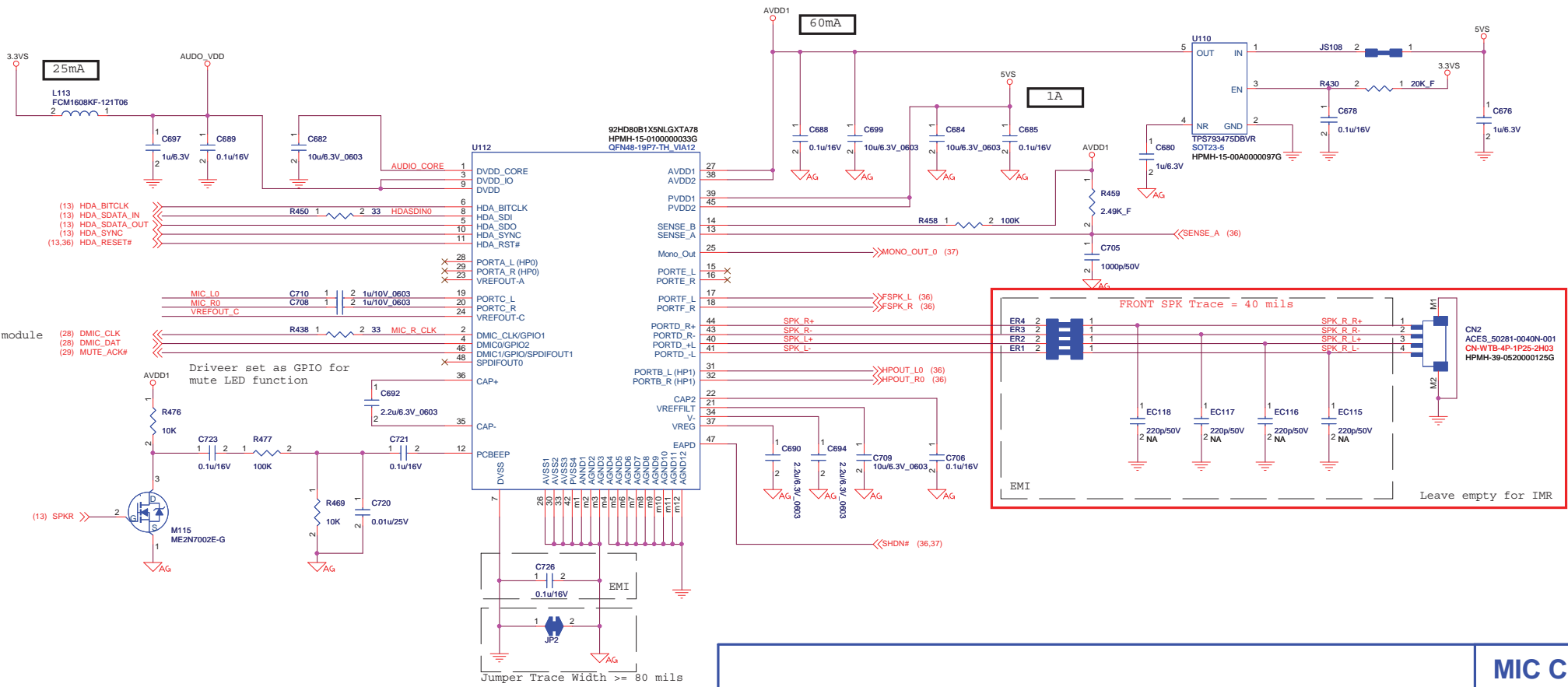
USB PWR SW

USB 3.0: RJ8& RJ9 mounted A, B.
 USB 2.0: RJ8& RJ9 mounted B, B.



- USB3.0 Conn:
- HPMH-38-0040000065G -- CONN USB 3.0 9P 2UB4014-000101 SINGATRON
 - HPMH-38-0040000067G -- CONN USB 3.0 9PIN TARA7-9Y5391 ACON
 - HPMH-38-0040000068G -- CONN USB 3.0 9P USBF-D9F1-ANR1-00 E-CONN
 - HPMH-38-0040000088G -- CONN USB3.0 1-1932354-1 9P H:7.4mm
- USB2.0 Conn:
- HPMH-38-0040000066G -- CONN USB 2.0 4P 2UB4015-000111 SINGATRON
 - HPMH-38-0040000070G -- CONN USB 2.0 4PIN UARBS-4K5986 ACON
 - HPMH-38-0040000071G -- CONN USB 2.0 4P USBF-D4F1-ANR1-CA E-CONN

Audio CODEC



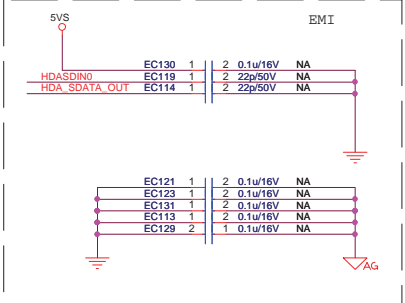
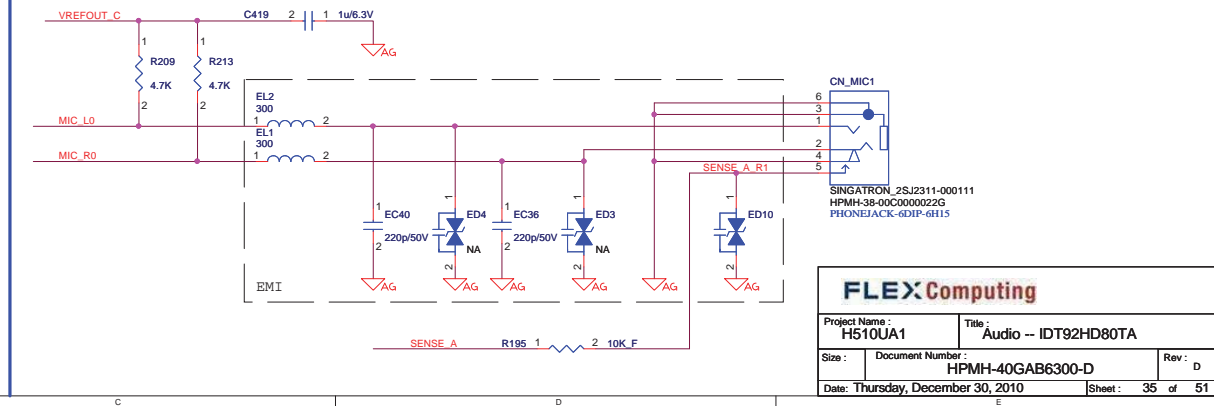
To WebCAM module

(28) DMIC_CLK
(28) DMIC_DAT
(29) MUTE_ACK#

Driver set as GPIO for mute LED function

(13) SPKR

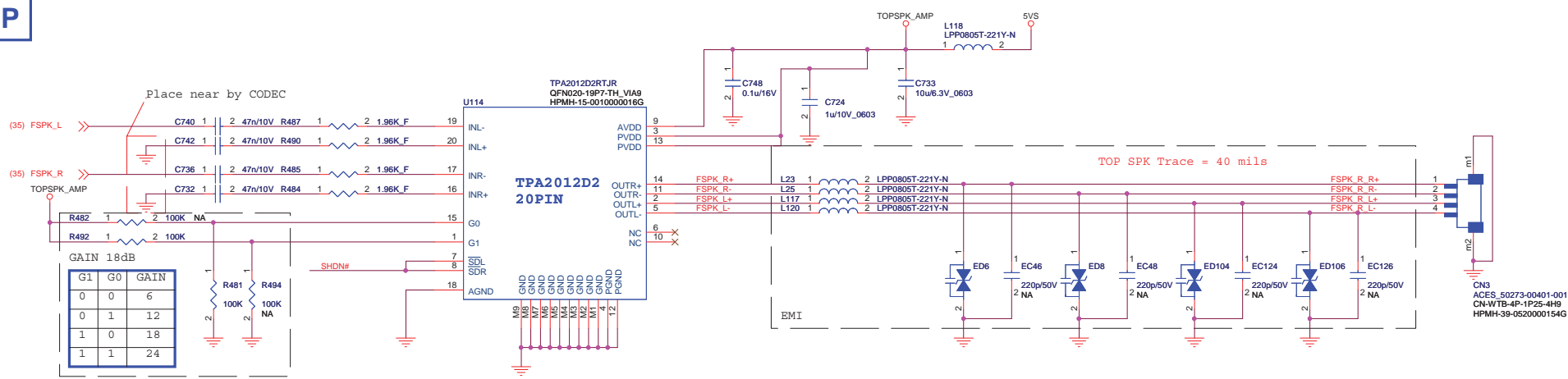
MIC CONN



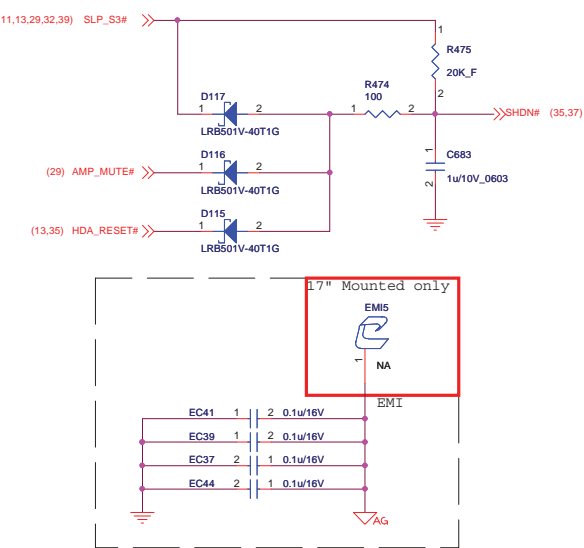
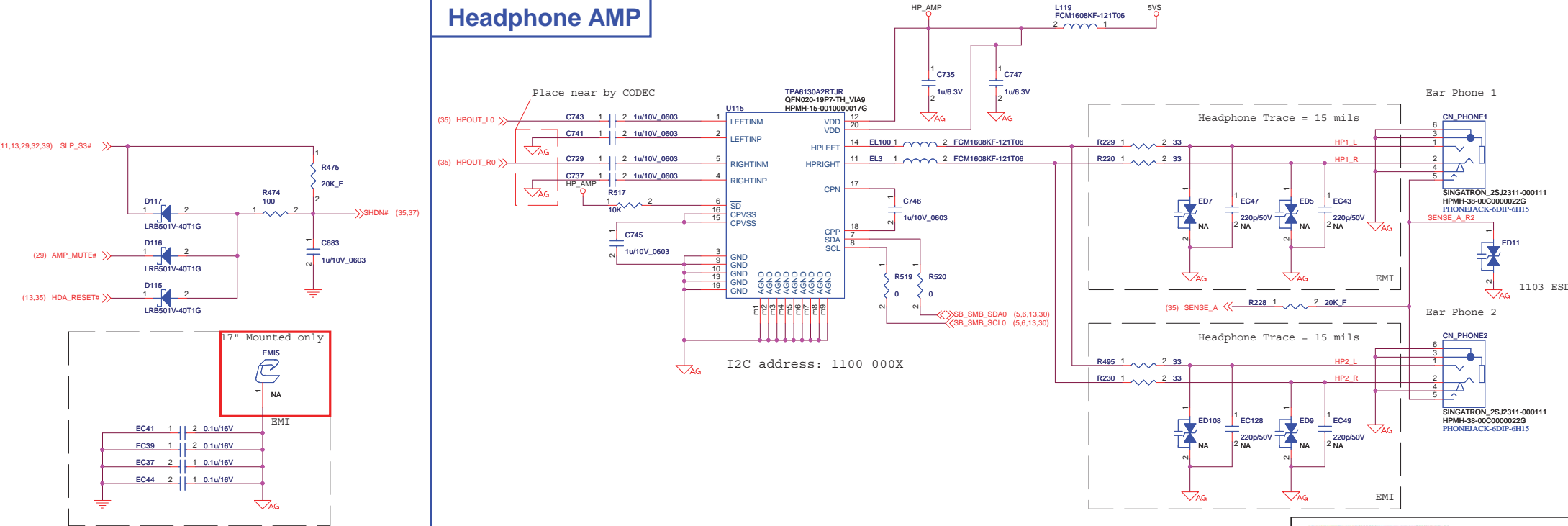
FLEX Computing

Project Name: H510UA1	Title: Audio -- IDT92HD80TA
Size: Document Number: HPMH-40GAB6300-D	Rev: D
Date: Thursday, December 30, 2010	
Sheet: 35 of 51	

FRONT SPK AMP



Headphone AMP



FLEXComputing

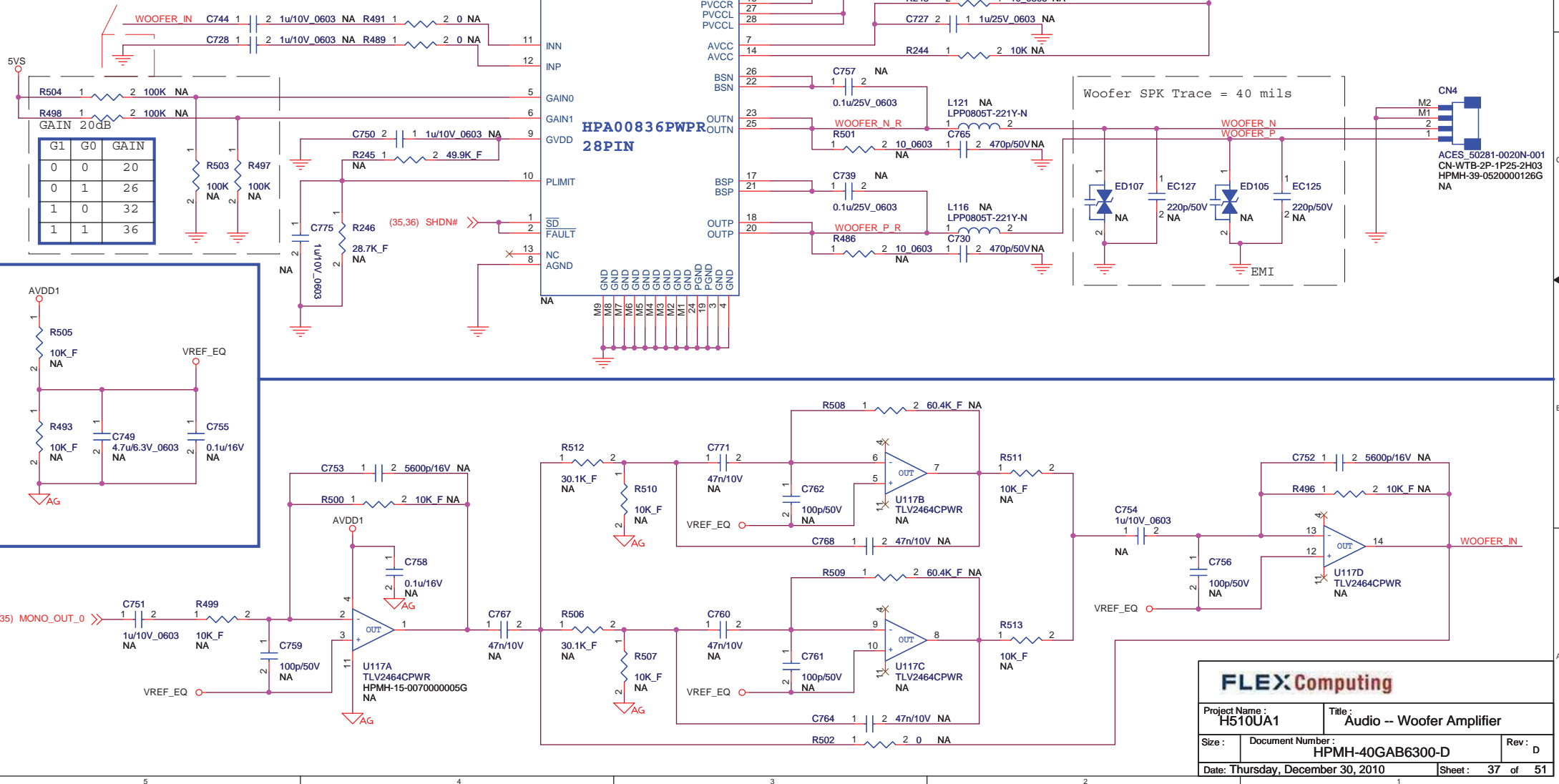
Project Name: H510UA1 Title: Audio -- Speaker/ Amplifier

Size: Document Number: HPMH-40GAB6300-D Rev: D

Date: Thursday, December 30, 2010 Sheet: 36 of 51

Woofers AMP

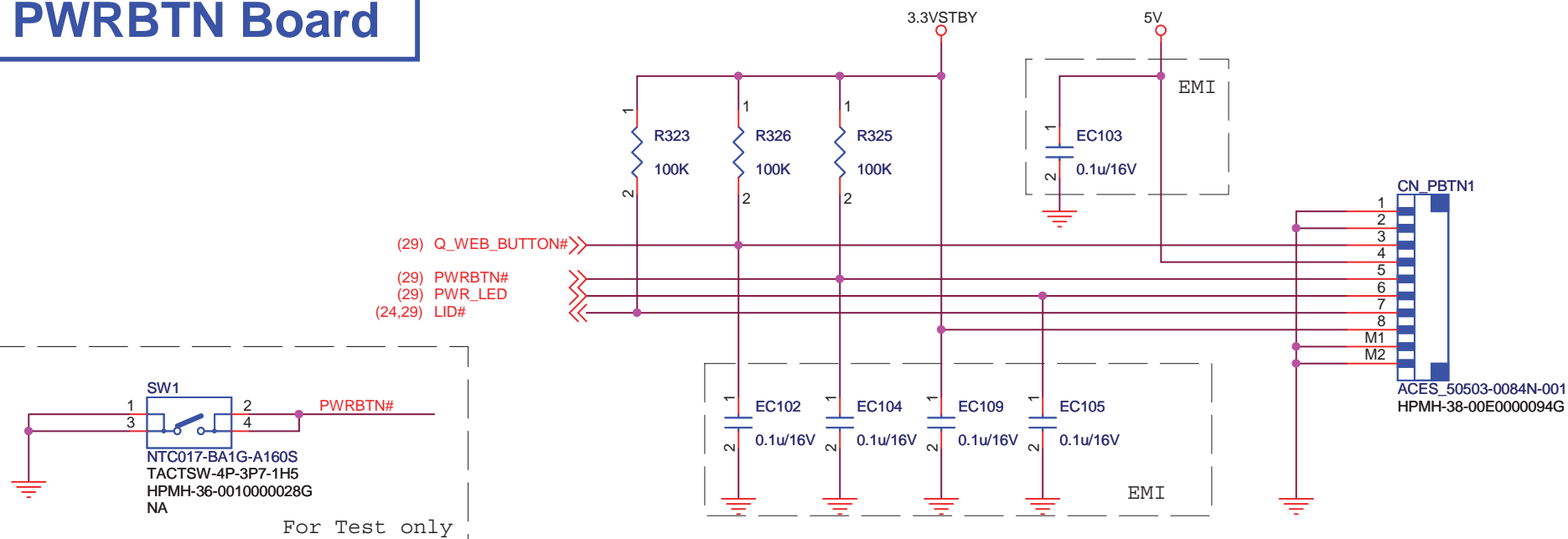
Place near by CODEC



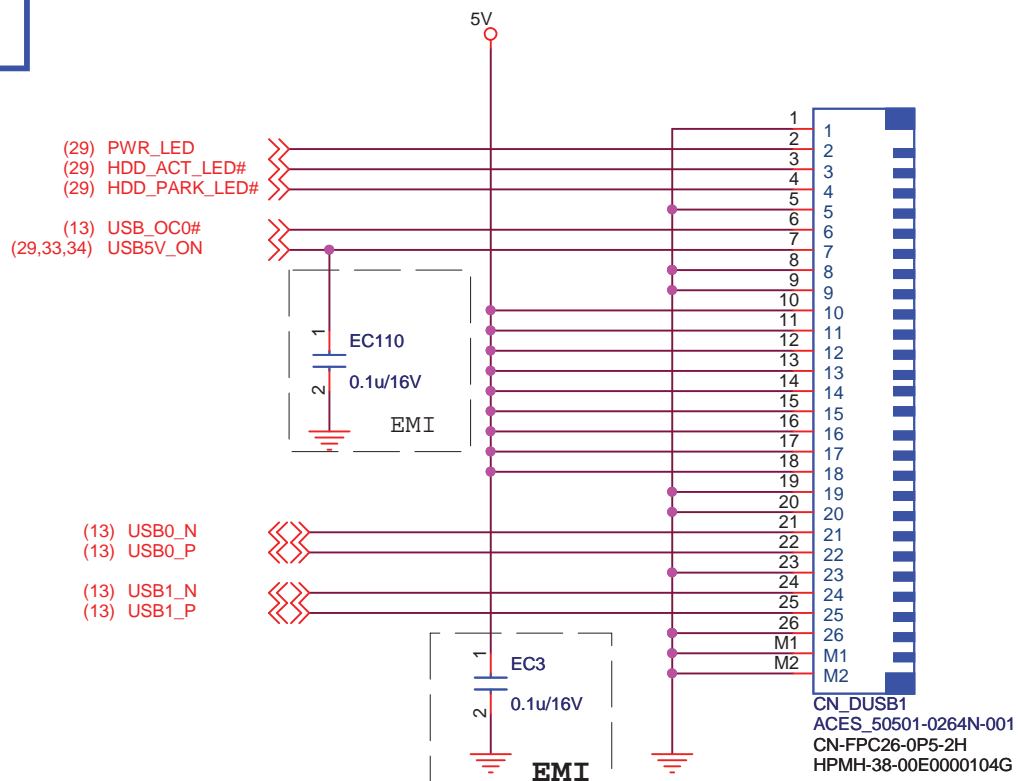
FLEX Computing

Project Name: H510UA1	Title: Audio -- Woofer Amplifier	
Size:	Document Number: HPMH-40GAB6300-D	Rev: D
Date: Thursday, December 30, 2010		Sheet: 37 of 51

PWRBTN Board



USB Board



FLEX Computing

Project Name :
H510UA1

Title :
Daughter Board Connector

Size :

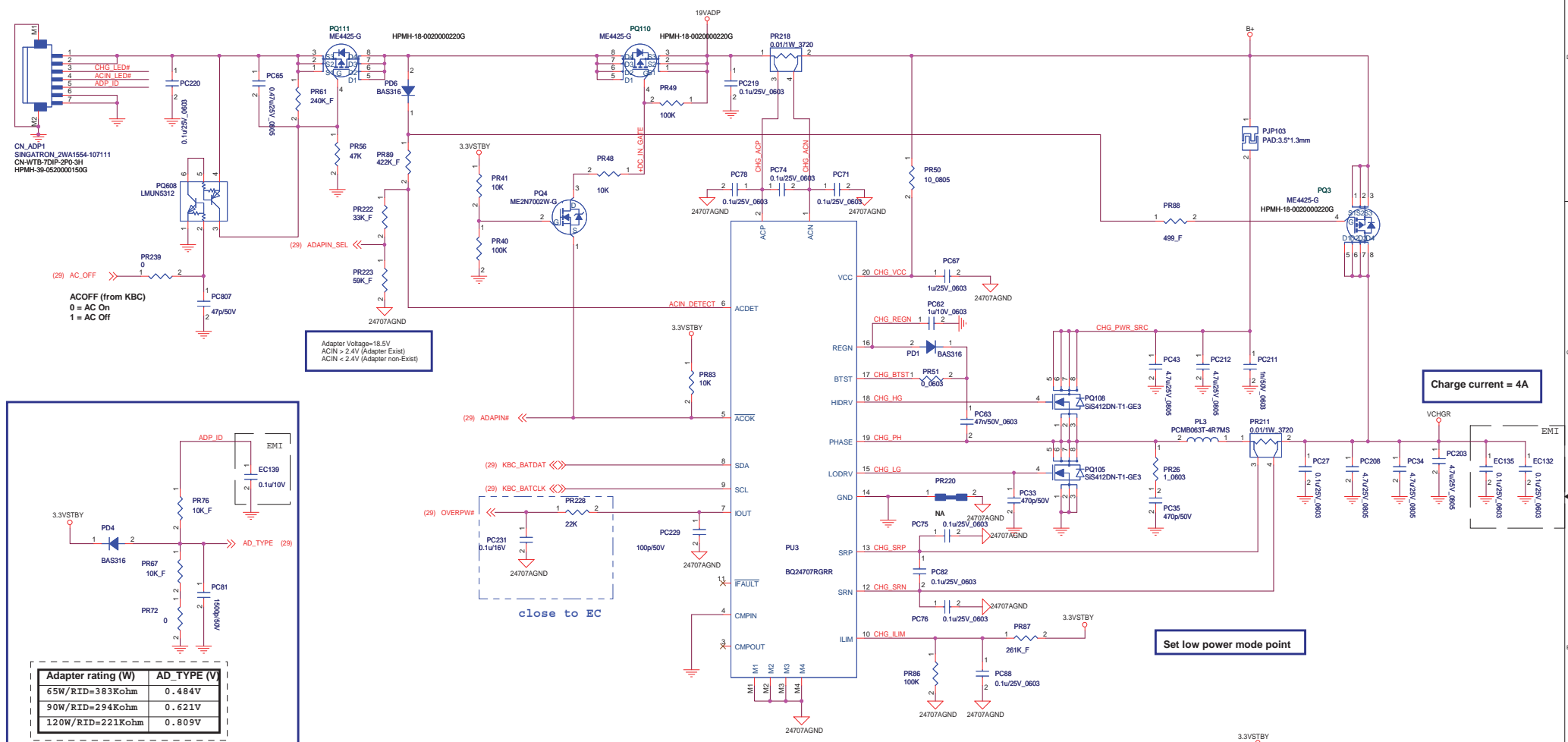
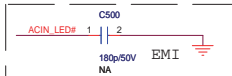
Document Number :
HPMH-40GAB6300-D

Rev :
D

Date: Thursday, December 30, 2010

Sheet : 38 of 51

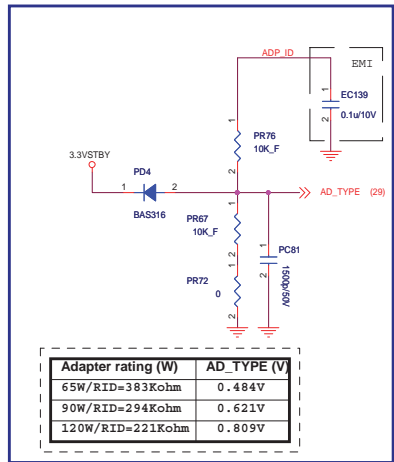
Charger



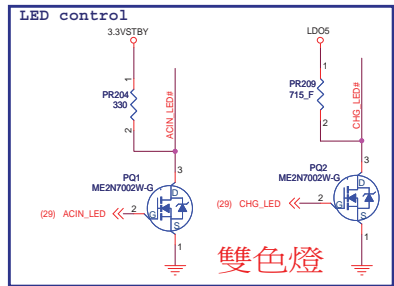
Adapter Voltage=18.5V
 ACIN > 2.4V (Adapter Exist)
 ACIN < 2.4V (Adapter non-Exist)

Charge current = 4A

Set low power mode point

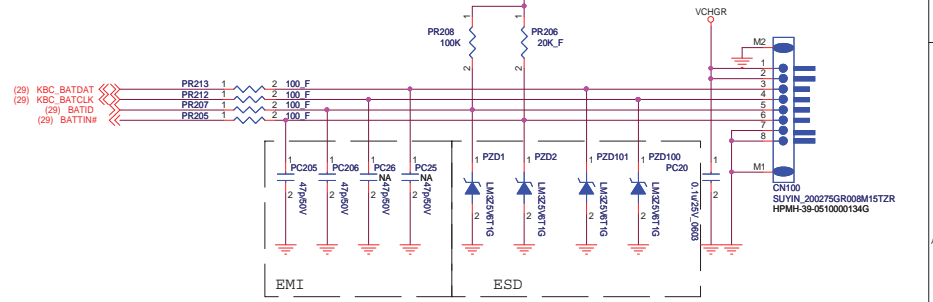


Adapter rating (W)	AD_TYPE (V)
65W/RID=383Kohm	0.484V
90W/RID=294Kohm	0.621V
120W/RID=221Kohm	0.809V



雙色燈

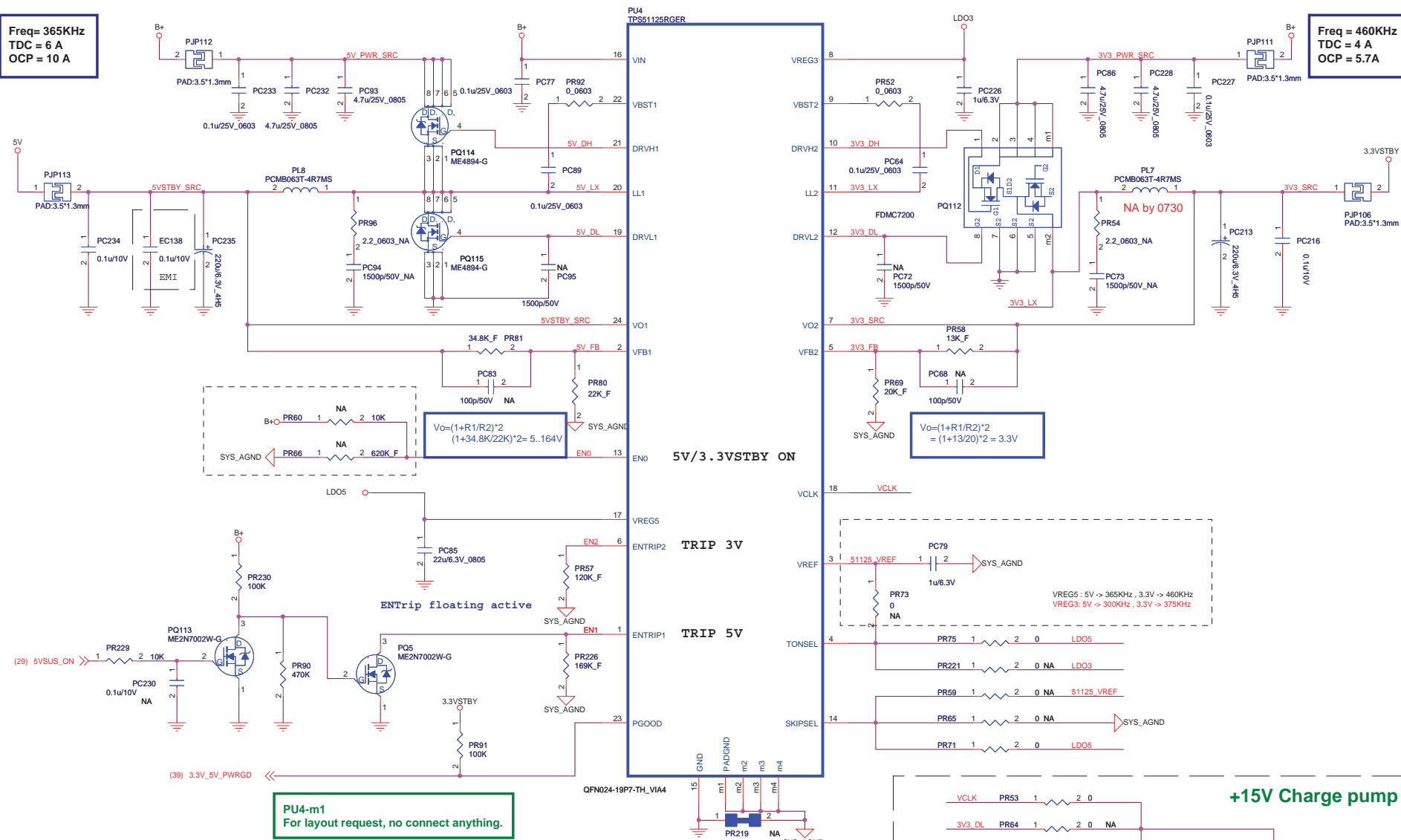
AirLine Combo	AC available	Charge
2.032V > ADAPIN_SEL > 1.542V	V	X
ADAPIN_SEL > 2.032V	V	V
1.542V > ADAPIN_SEL	X	X



5V / 3.3VSTBY

Freq= 365KHz
TDC = 6 A
OCP = 10 A

Freq = 460KHz
TDC = 4 A
OCP = 5.7 A



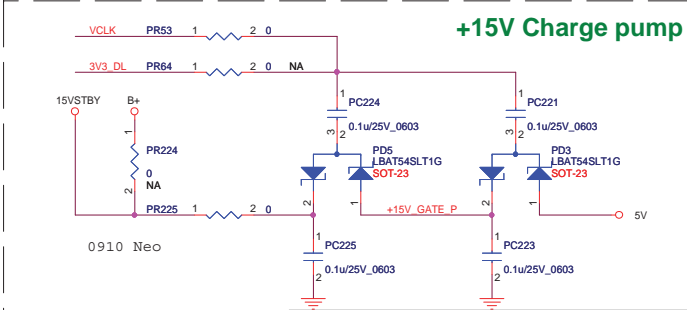
$$V_o = \frac{(1+R1/R2) \cdot 2}{(1+34.8K/22K)} \cdot 2 = 5.164V$$

$$V_o = \frac{(1+R1/R2) \cdot 2}{(1+13/20)} \cdot 2 = 3.3V$$

VREG5 : 5V -> 365KHz , 3.3V -> 460KHz
VREG3 : 5V -> 300KHz , 3.3V -> 375KHz

Table 3. Enabling State

EN0	ENTRIP1	ENTRIP2	VREF	VREG5	VREG3	CH1	CH2	VCLK
GND	Don't Care	Don't Care	Off	Off	Off	Off	Off	Off
R to GND	Off	Off	On	On	On	Off	Off	Off
R to GND	Off	On	On	On	On	Off	On	Off
R to GND	On	On	On	On	On	On	On	Off
Open	Off	Off	On	On	On	Off	Off	Off
Open	On	Off	On	On	On	On	Off	On
Open	Off	On	On	On	On	Off	On	Off
Open	On	On	On	On	On	On	On	On



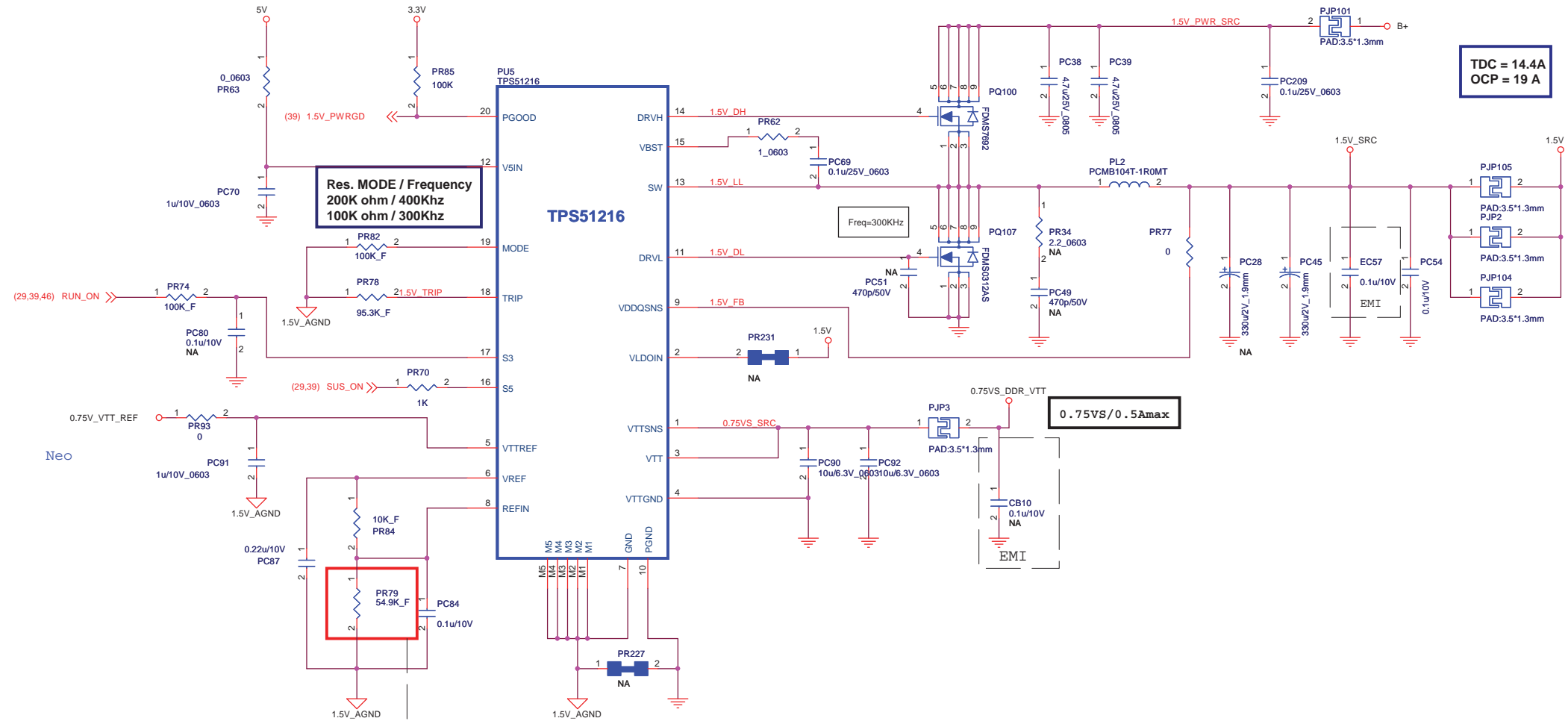
FLEXComputing

Project Name : H510UA1 Title : PWR -- 3V/ 5V (TPS51125)

Size : Document Number : HPMH-40GAB6300-D Rev : D

Date : Thursday, December 30, 2010 Sheet : 41 of 51

1.5V



TDC = 14.4A
OCP = 19A

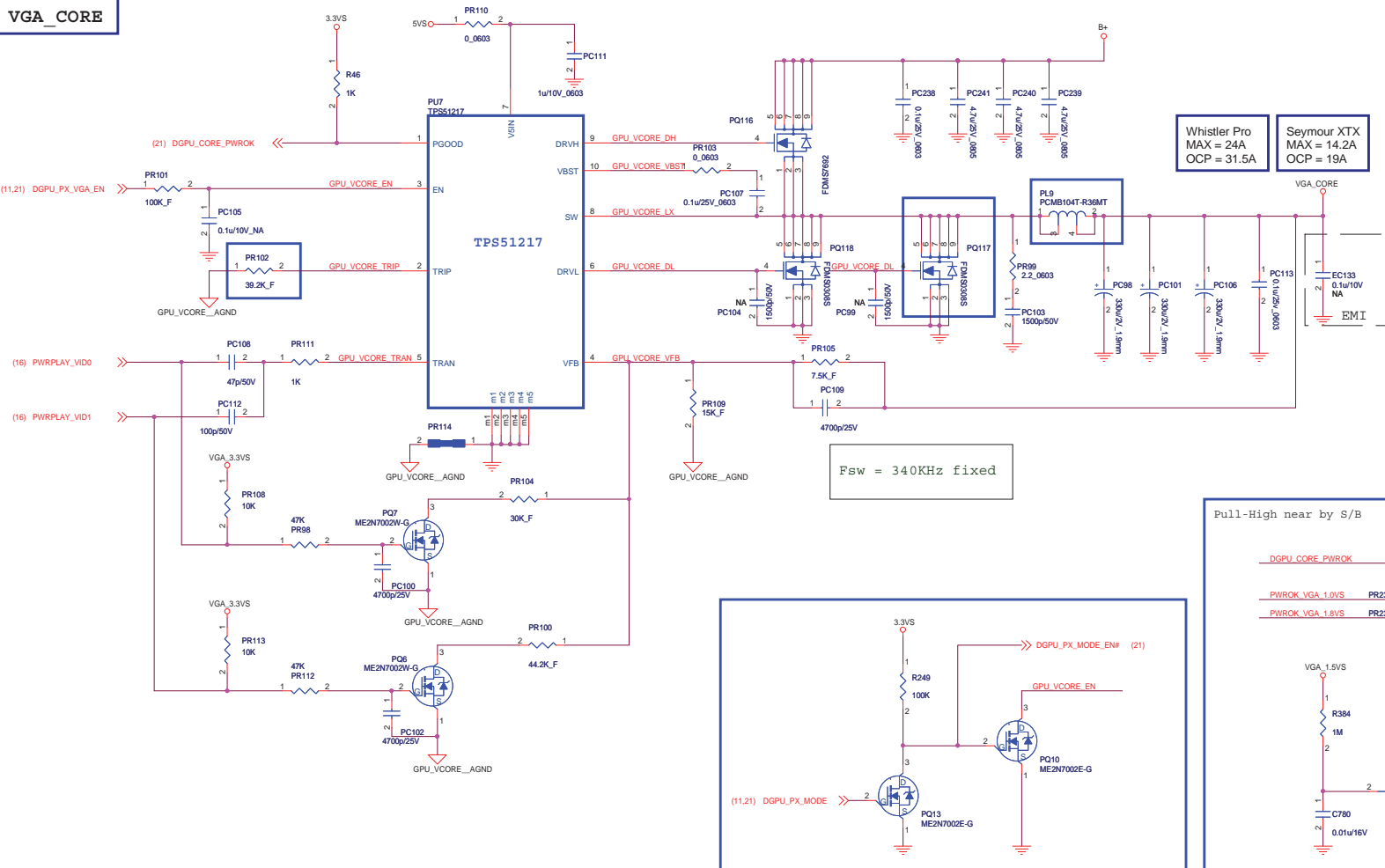
0.75VS/0.5Amax

	UMA	Discret
PR79	49.9K ohm 1% HPMH-30-149921-990G	54.9K ohm 1% HPMH-30-154921-990G

Table 1. S3 and S5 Control Table

STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3	L	H	1	0 (high-Z)
S4/S5	L	L	0 (discharge)	0 (discharge)

VGA_CORE



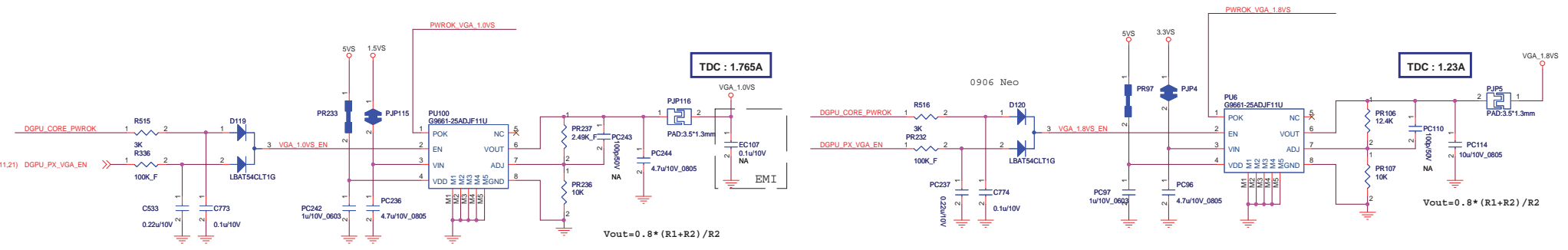
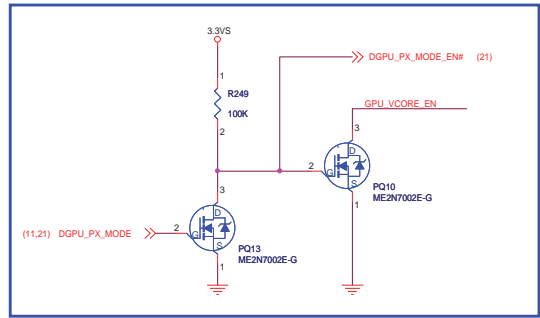
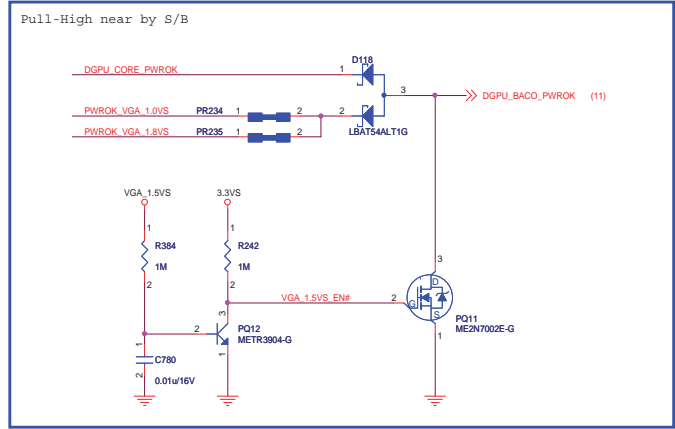
Whistler Pro VID table

VID1	VID0 [N/A]	VGA_CORE (V)
0	-	0.9
1	-	1.0

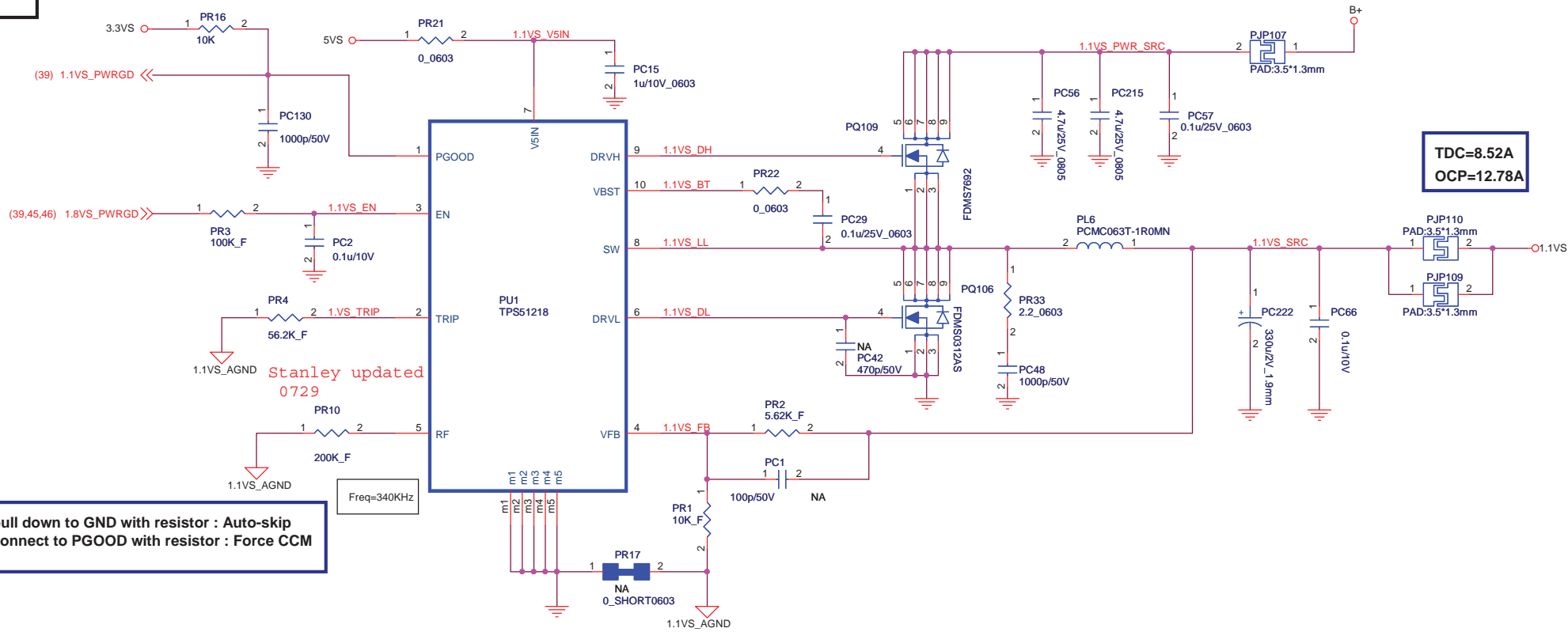
Seymour XTX VID table

VID1	VID0	VGA_CORE (V)
0	0	0.9
0	1	1.05
1	0	1.0
1	1	1.15

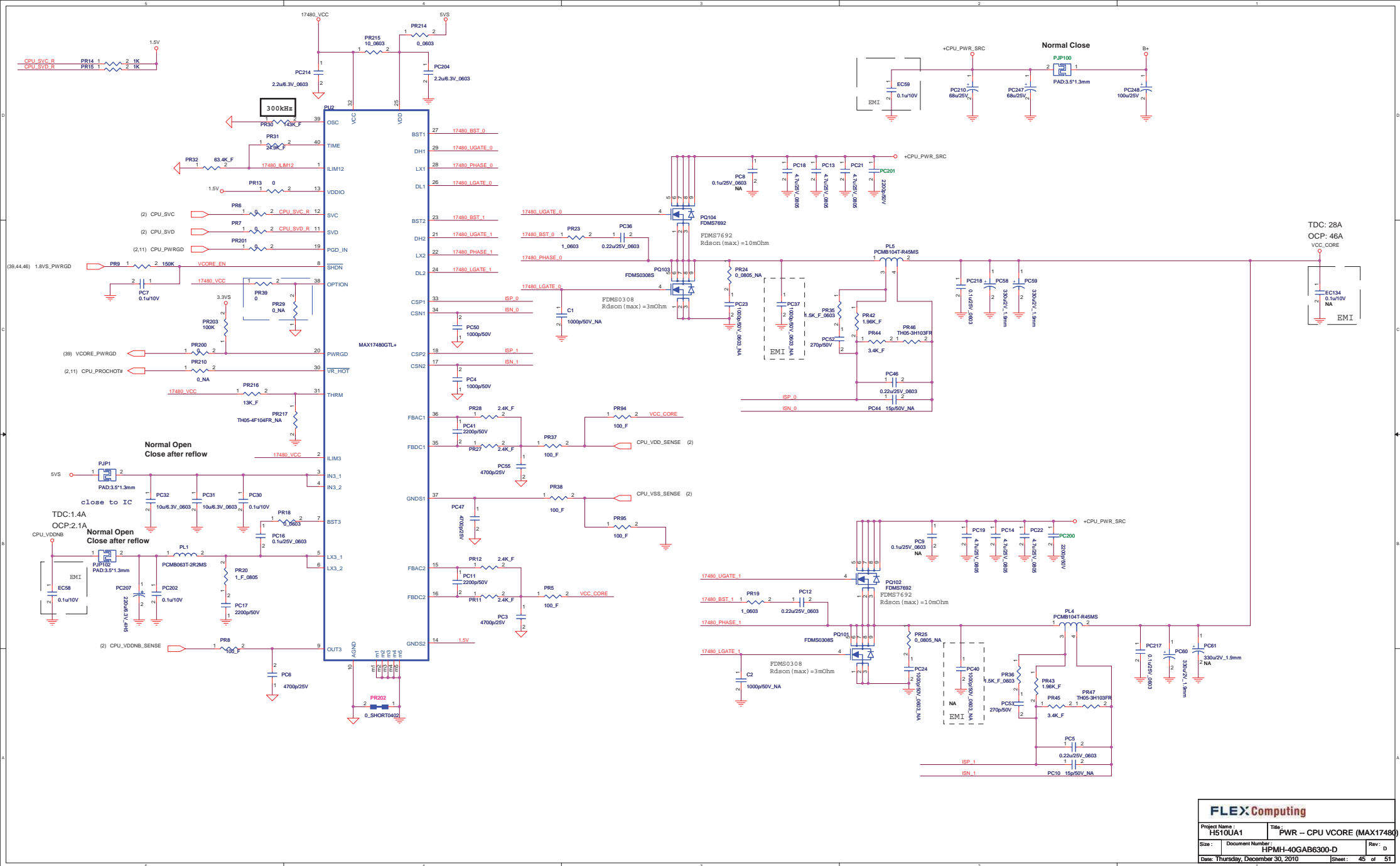
	Whistler	Seymour
PR102	39.2K ohm 1% HPMH-30-139221-990G	49.9K ohm 1% HPMH-30-149921-990G
PL9	0.36uH HPMH-32-4000000254G	1.0uH HPMH-32-4000000245G
PR104	NA	Mounted
PR98	NA	Mounted
PR108	NA	Mounted
PQ7	NA	Mounted
PQ100	NA	Mounted
PQ117	Mounted	NA
PC241	Mounted	NA



1.1VS

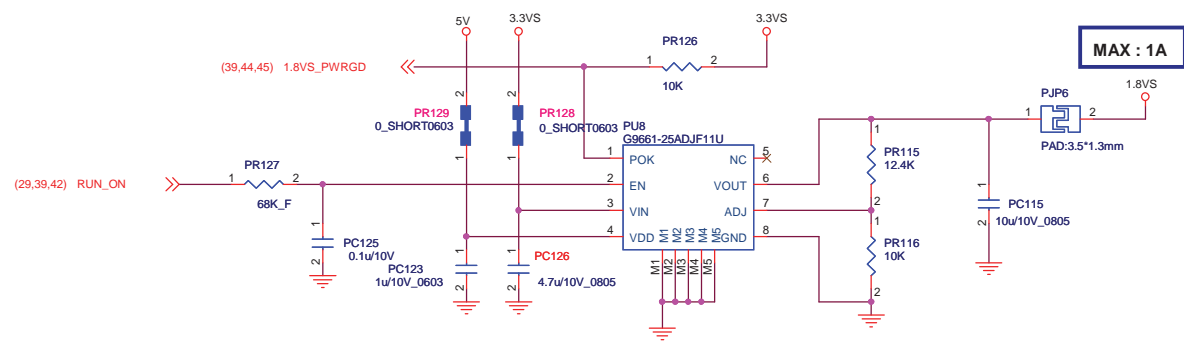


FLEX Computing		
Project Name : H510UA1	Title : PWR -- 1.1VS (TPS51218)	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet: 44	of 51



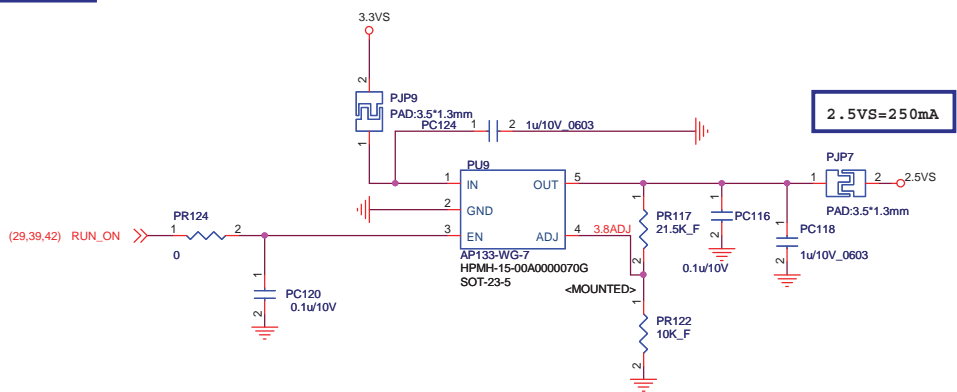
FLEX:Computing			
Project Name : H510UA1		Title : PWR -- CPU VCORE (MAX17480)	
Size :	Document Number :	HPMH-40GAB6300-D	Rev : D
Date : Thursday, December 30, 2010			Sheet : 45 of 51

1.8VS



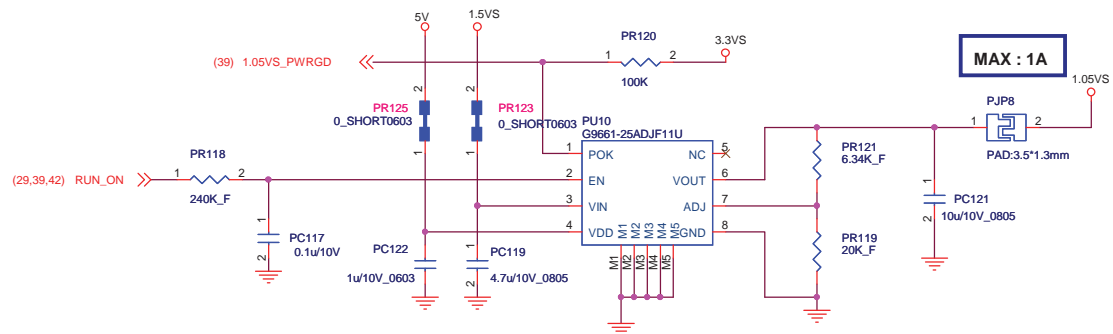
MAX : 1A

2.5VS

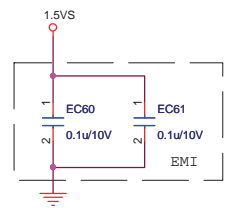


2.5VS=250mA

1.05VS



MAX : 1A

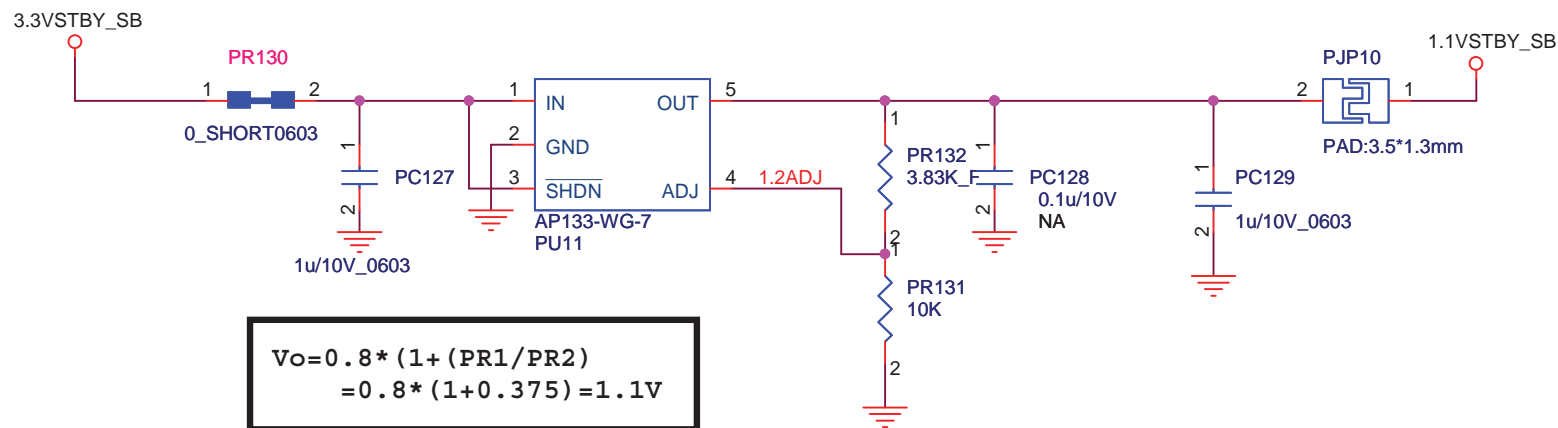


AP133:
 Low dropout: 350mV at 300mA
 EN logic low: <0.4V
 EN logic high: >1.4V
 Thermal shutdown: 145°C

FLEX Computing	
Project Name : H510UA1	Title : PWR -- 1.8VS/ 1.05VS/ 2.5VS
Size :	Document Number : HPMH-40GAB6300-D
Date : Thursday, December 30, 2010	Rev : D
Sheet : 46	of 51

1.1VSTBY

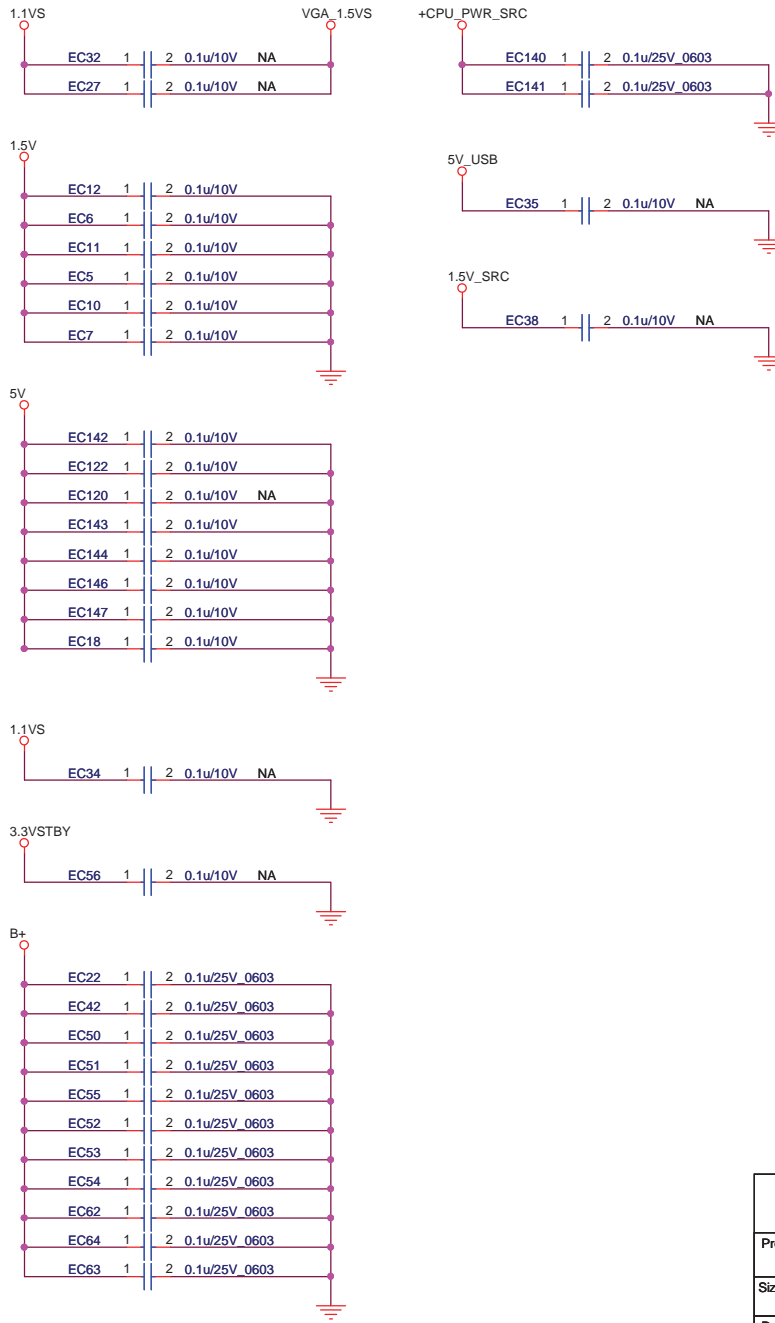
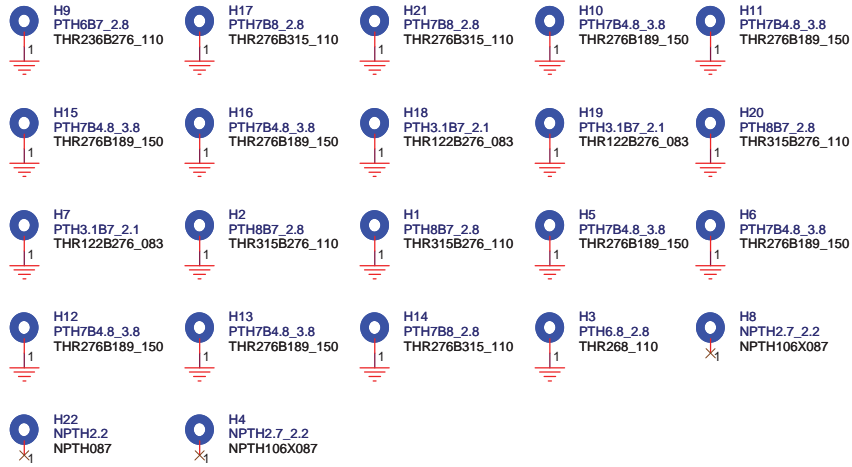
1.1V_DUAL=250mA



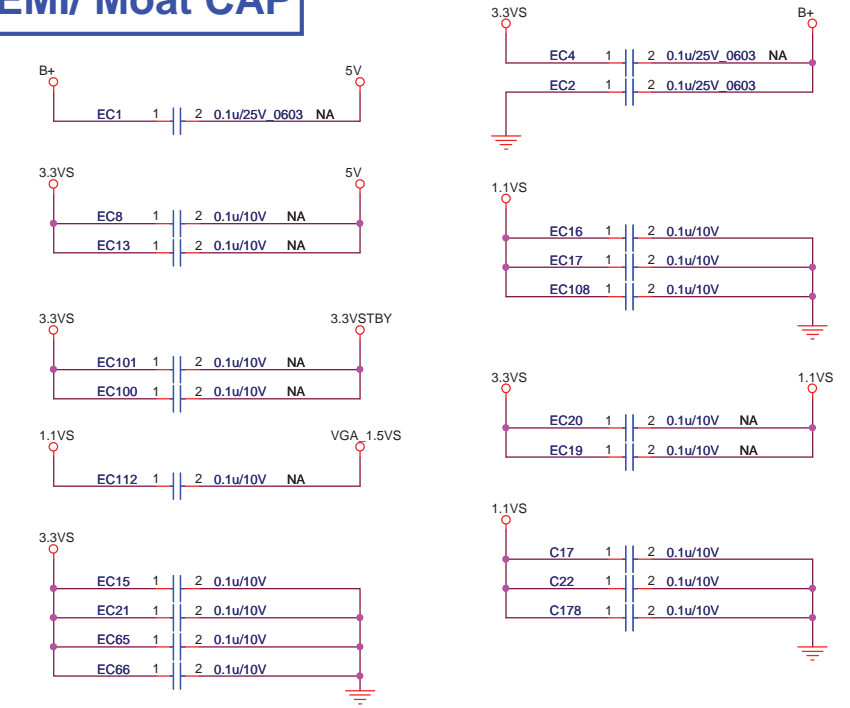
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Project Name : H510UA1		Title : PWR -- 1.1VSTBY_SB (AP133)	
Size :	Document Number : HPMH-40GAB6300-D		Rev : D
Date: Thursday, December 30, 2010		Sheet : 47 of 51	

Screw Hole



EMI/ Moat CAP



FID

- FID1 FIDUCIAL CAD-016
 NC, NO CONNECT TO ANY.
- FID2 FIDUCIAL CAD-016
 NC, NO CONNECT TO ANY.
- FID3 FIDUCIAL CAD-016
 NC, NO CONNECT TO ANY.
- FID4 FIDUCIAL CAD-016
 NC, NO CONNECT TO ANY.
- FID5 FIDUCIAL CAD-016
 NC, NO CONNECT TO ANY.
- FID6 FIDUCIAL CAD-016
 NC, NO CONNECT TO ANY.
- FID7 FIDUCIAL CAD-016
 NC, NO CONNECT TO ANY.
- FID8 FIDUCIAL CAD-016
 NC, NO CONNECT TO ANY.

FLEX Computing

Project Name : H510UA1	Title : Screw Hole/ EMI/ Unused
Size : HPMH-40GAB6300-D	Rev : D
Date : Thursday, December 30, 2010	Sheet : 48 of 51

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
1	Rev. A Schematic released	Rev. A Schematic released	A			A0	DB
2	Modify F1 to smaller package	Modify F1 to smaller package	B	26	Modify F1 package to "FUSE-3L4X1W8X1H".	B0	SI
3	Add resistor for CPU test point resistor.	Add resistor for CPU test point resistor.	B	2	Add R514 for 80.6 ohm.	B0	SI
4	Add thermal sensor for NB thermal diode	Prevent N/B thermal break down	B	8, 30	Add RJ105, RJ106 and C772 to seperate DGPU& NB thermal signal.	B0	SI
5	Add DGPU CRT DDC source	Add DGPU CRT DDC channel for DDC6	B	16	Add U104 DDC channel test PAD (P27, P26) of pin AJ30, AJ31 (DDC6)	B0	SI
6	Modify CRT damping components.	Improve re-work performance	B	26	Modify JS102, JS103, JS104, JS7, JS9, JS10, JS11 to R233, R234, R235, R236, R237, R238, R239	B0	SI
7	Shift LAN transformer pin signal	Correct LAN transformer pin-out	B	32	Shift U107 pin-out to meet transformer spec	B0	SI
8	Update LAN 25M net-name	Correct LAN 25M for reserved signal.	B	32	Modify LAN 25M clock from S/B and named "LAN_25M_IN_SB"	B0	SI
9	Modify USB3.0 clock request signal	Modify USB3.0 clock request signal	B	33	Delete D7 for USB 3.0 clock request work properly	B0	SI
10	Reduce CPU/ DGPU screw hole size	To meet BGA& Screw hole keeping 3mm.	B	48	Reduce H5, H6, H12, H3 (CPU), H10, H11, H15, H16 (DGPU) to 7B4.8_3.8 mm	B0	SI
11	Prevent leakage current& fine-tune PWR seq	Prevent leakage current& fine-tune PWR seq	B	34, 39, 44, 45, 46	1. Modify R423 pin 1 to 3.3VSTBY 2. Leave C25 as empty for 1.1V seq 3. Modify R44 to 200K ohm 1% for 3.3VSTBY_SB seq. 4. Add R240, R241 for waveform improve 5. Add R519, R520 to Audio SM bus reserved. 6. Modify PR118 to 240Kohm 1% for 1.05VS seq. 7. Modify PR126 to 10Kohm for 1.8VS seq. 8. Modify PR9 to 150Kohm 1% for VCORE seq. 9. Modify PR3 to 100Kohm 1% for 1.1VS seq. 10. Del R82	B0	SI
12	Remove un-used circuit	Remove function by HP requirement	B		Remove Blue tooth& Keyboard bakclight circuit	B0	SI
13	Add KBC External Wake up event	Add KBC External Wake up event	B	13, 29	Add D6 and make link "SIO_EXT_WAKE#" from U5 pin 117 to U111 pin H3.	B0	SI
14	Modify components by ME/ height limitation	Modify components by ME/ height limitation	B	11, 28, 35, 37	1. Modify CN_RTC1 to ACES - "50273-0020N", CN2 to ACES - "50273-0020N", CN4 to ACES - "50281-00201", CN LVDS1 to ACES "50398-04001" 2. Add M119, M120 for TP EN LED& TP Sidelight LED sinker.	B0	SI
15	Modify DGPU power sequence& BACO circuit	To meet DGPU power sequence& BACO required.	B	11, 21, 43	1. Modify U111 pin AH6 as "DGPU_PX_VGA_EN" 2. Modify PR238 to 620K ohm 1%. 3. Add R243, Q14, PQ121, PC246 for VGA 3.3VS gating circuit. 4. Modify VGA 1.5VS enable signal from DGPU_PX_EN to DGPU_PX_VGA_EN. 5. Delete D6 and connect DGPU_PX_MODE to BACO circuit as enable 6. Add D118, D119, D120, PR240, R249, R515, R516, C773, C774, PC130, PQ10, PQ11, PQ12, PQ13 for VGA PWR Seq. 7. Add JP3, JP4 for BACO mode reserved. 8. Add D121, R250, PQ9, PQ11, PQ12, R242 for DGPU BACO PWROK seq. 9. Modify DGPU_PERST# from DGPU_PX_GPIO0 and PCIE_RST# combined. Or shorted by RJ100B from DGPU_GPIO0. 10. Modify entire 3.3VS of DGPU to VGA 3.3VS. 11. Update PCIE_RST#0 reset source.	B0	SI
16	DFB update	DFB update improvement (Factory)	B	26	Modify D101 to 1N5819HW-7-F.	B0	SI
17	X'tal accuracy modify	X'tal accuracy modify	B	11	1. Modify C704, C719 to 27pF for 32.768M Hz	B0	SI
18	Seperate PCI_WAKE# from different power source	Seperate PCI_WAKE# from different power source	B	11	Add D123, R200 and pull-high to 3.3V_LAN	B0	SI
19	Add transistor for LED sinker	Add transistor for LED sinker	B	28	Add M119& M120 for LED power sinker.	B0	SI
20	Update thermal circuit	Update thermal circuit	B	30	1. Add RJ105, RJ106, R247 for DGPU& NB thermal diode switch circuit. 2. Delete R23, R25, R30, R37, R38, R42, R43, C94, D1, D2, M5, M6, Q9.	B0	SI
21	Update USB3.0 solution to NEC	Update USB3.0 solution to NEC by HP required.	B	33	Modify USB3.0 solution to NEC uDP720200	B0	SI
22	Audio circuit modify (Kevin.Yeh)	Audio circuit modify	B	36, 37	1. Modify R484, R485, R487& R490 to 1.96K ohm 1% 2. Add R517 (10K ohm) and pull-high to "HP_AMP". 3. Add R244, R245, R246, R248, C727, C775 for B+ break down issue.	B0	SI
23	Power circuit modify (Eva.Chao)	Power circuit modify	B	40, 42, 44, 45	1. Modify PR50, PC67 from 1206 to 0805& 0603 package. 2. Modify PC45, PC207 to 220uF/ 6.3V. 3. Leave PC22, PC45& PC61 empty. 4. Add PQ608, PR239 for AC-off funtion. 5. Modify PL8 to PCMC063T-3R3MN 6. Leave PR64 empty and PR53 mouted for charge-pump states. 7. Modify PR102 to 30.1K ohm 1%. 8. Modify PR16 to 10K ohm and Add PC130 for 1.1VS PWRGD signal quality 9. Modify PC222 for double pulse issue.	B0	SI

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
24	Prevent GPU ACAVIN leakage current	Prevent GPU ACAVIN leakage current	C	16	Add R352& D7 to prevent GPU ACAVIN leakage current.	C0	PV
25	Update USB3.0 circuit	Update USB3.0 circuit	C	33, 34	1. Add R263, R264& M125 for USB3.0 Wake up event. 2. Add R262& D123 for USB3.0 reset timing issue. 3. Modify L26 to package 0603 for parts lead time issue. 4. Correct Analog& Digital power source 5. Add R261 for SMI BOM option 6. Delete M17 and update power switch circuit. 7. Update U16 footprint	C0	PV
26	KBC SLP_S5# signal setting	KBC SLP_S5# signal setting	C	29	Add R165 to setting SLP_S5# GND level	C0	PV
27	Logo LED broken issue	Logo LED module didn't have current limit resistor	C	24	Add R335 for Logo LED current limit	C0	PV
28	Zero power ODD function removal	Zero power ODD function removal	C	27	Leave C652, M108, M109, Q105, Q106, R419, R424& R452 empty for Zero Power ODD function removal.	C0	PV
29	EEPROM WP#	Add EEPROM WP# from EC	C	29	Add EC pin 81 as EEPROM WP# signal for EEPROM Write Protection.	C0	PV
30	NEC USB3.0 device disappear issue	Fine-tune NEC USB3.0 power up seq	C	33	1. Add C94 for NEC uPD700200A global reset timing fine-tune 2. Add R259 as empty for CLKREQ external pull-high	C0	PV
31	GPU thermal trip normal operation status	Set GPU thermal trip normal operation status	C	2, 29	1. Add R423 for GPU thermal trip normal operation status 2. Add Q108 for CPU processor hot	C0	PV
32	Hall sensor sense issue	Hall sensor can't work fine	C	28, 38	Modify SW100, C510 to D/B and modify CN_PBTN1 to 8 pin to meet M.E. modify	C0	PV
33	PX mode GPU thermal sensor fail	EC can't check GPU thermal status	C	2, 21, 29 30	1. Remove Q101, R303 remove CPU thermal alert. 2. Add R268 pull-high at alert of thermal sensor. 3. Connect DGPU PX_VGA_EN to EC for PX mode indicates. 4. Add Q109, R181 for thermal sensor leakage issue	C0	PV
34	Stage ID indicate	Indicate SI/ PV stage for SW	C	12	Add R461 for Stage ID (Default internal PU: H-SI, L-PV)	C0	PV
35	Power seq fine-tune	Power seq fine-tune	C	33, 43	1. Modify PR801 to 100K_F for USB3.0 chip power seq 2. Modify R336, PR232 to 100K_F for VGA power seq	C0	PV
36	Power circuit modify (Staley Chiu)	Power circuit modify	C	41, 43, 44, 45, 46	1. PL8 change to 4R7 2. Leave PR66 as empty 3. PR81/ PR81 change to 22K/ 34.8K for USB port load issue 4. PR79 change to 54.9k for VRAM load issue 5. PR104 change to 30K for AMD VID Updated 6. PR100 change to 44.2k for AMD VID Updated 7. Modify MAX/OCF current text 8. Update VID table 9. PC114 change to 10u/10v0805 for Phase/Gain 10. PC222 change to 330u/2v for double pulse 11. PC60 change to Panasonic source (use the same source with others) 12. Add PC247, PC248/ 68uF/25V for closing acoustic noise 13. PC115 change to 10u/10v0805 for Phase/Gain 14. PC121 change to 10u/10v0805 for Phase/Gain 15. Delete PJP114	C0	PV
37	RFI solution (Hank Tsai)	RFI solution	C	11	Modify C442, C448 to 10pF as mounted.	C0	PV
38	EMI solution (PV - Benson Ni)	Update EMI solution	C	30, 37, 38, 39, 40, 41, 42, 45, 46, 48	1. Modify CB15, CB16 as mounted. 2. Modify EC37, EC39, EC41, EC44 as mounted. 3. Modify EC102, EC104, EC105 as mounted. 4. Add EC110/ 0.1uF bypass caps. Between USB conn pin7 (USB5V_ON) and GND. 5. Add EC139/ 0.1uF bypass caps. Between CN_ADP1 pin 5 and GND. 6. Modify C500 as mounted. 7. Add EC138/ 0.1uF bypass caps. between 5VSTBY_SRC and GND. 8. Add EC57/ 0.1uF bypass caps. between 1.5V_SRC and GND. 9. Add EC45/ 0.1uF bypass caps. between CPU_VDDNB and GND. 10. Add EC59/ 0.1uF bypass caps. between +CPU_PWR_SRC and GND. 11. Add EC60, EC61/ 0.1uF bypass caps. between 1.5VS and GND. 12. Modify EC5, EC6, EC7, EC10, EC11, EC12, EC108, EC122 as mounted. 13. Add EC62, EC63, EC64/ 0.1uF bypass caps. between B+ and GND. 14. Add EC65/ 0.1uF bypass caps. between 3.3VS and GND. 15. Delete EC111, EC25, EC23, EC24, EC26, EC33, EC35, EC109, EC110, EC45, EC38.	C0	PV
39	ESD solution (PV - Stone Wang)	Update ESD solution	C	35, 36	1. EL1, EL2 from Bead 120ohm change to the Resistor 300ohm. 2. EC36, EC40 change to mounted. 3. Add a Varistor ED10 between CN_MIC1 pin5 and Net AGND. 4. ED3, ED4 change to 0603 Varistors. 5. Add a Varistor ED11 between CN_PHONE1 pin5 and Net AGND. 6. ED6, ED8, ED104, ED106 change to 0603 Varistors. 7. ED5, ED7, ED9, ED108 change to 0603 Varistors and keep them as empty	C0	PV

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Project Name:
H510UA1Title:
History - 2Size: Document Number:
HPMH-40GAB6300-D

Rev: D

Date: Thursday, December 30, 2010

Sheet: 50 of 51

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
40	RTC accuracy update (BOM)	RTC accuracy update	D	11	Modify C704& C719 to 22pF and 18pF.	D0	MV
41	Prevent adaptor level fail (Power)	Prevent adaptor level fail	D	40	Modify PR89 to 422Kohm 1%	D0	MV
42	Prevent leakage current from CRT	Prevent leakage current from CRT	D	26	Add R23 as 10Kohm to prevent leakage current from CRT	D0	MV
43	Fine-tune LED brightness (BOM)	Fine-tune LED brightness by HP ID	D	29	1. Modify R399 to 590ohm 1% for RF on LED 2. Modify R401 to 240ohm 1% for RF off LED 3. Modify R404 to 1.27Kohm 1% for CAP lock LED 4. Modify R405 to 240ohm 1% for MUTE LED 5. Modify PR209 to 715ohm 1% for Charger LED	D0	MV
44	S5 wake-up event leakage issue (BOM)	Prevent leakage current from pull-high resistor	D	29	Leave R356, R361 as empty to prevent it.	D0	MV
45	DFX report improvement	Meet Factory DFX checking	D	45	Modify PJP100 to Normal close footprint	D0	MV
46	EMI solution improvement	EMI solution improvement	D	48	1. Modify EC15 from between 3.3VS& 5V to 3.3VS& GND 2. Modify EC18 from between 3.3VS& 5V to 5V& GND 3. Modify EC2 from between 3.3VS& B+ to B+& GND 4. Add EC35, EC38, EC66, EC140, EC141, EC142, EC143, EC144, EC146, EC147, EC148	D0	MV