AT5 BLOCK DIAGRAM

01

04-- 0402 footprint
06-- 0603 footprint
08-- 0805 footprint
12-- 1206 footprint
F-- 1% tolerance

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

CPU Merom
478P (uPGA)/35W
PAG 3,4

CPU THERMAL SENSOR
PAG 5

14.318MHz

CLOCK GEN
ICS9LPRS355AGLFT
64pinsTSSOP
PAG 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

NORTH BRIDGE
Crestline
PAG 7,8,9,10,11,12

DDRII-SODIMM1 PAG 13,14 — DDRII 533,667 MHz
DDRII-SODIMM2 PAG 13,14 — DDRII 533,667 MHz

PCI-Express 16X
NVDIA G3-64 for 15.4"
NVDIA G3-128 for 17"
820p FCBGA PAG 15,16,17,18,19,20

Option for 17" only
HDMI CON PAG 26

TV_OUT
CRT_OUT
CRT/S-VIDEO PAG 25

LVDS(2 Channel)
Panel Connector 15" / 17" PAG 26

Cable Docking PAG 38
- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

DMI LINK

NBSRCCLK, NBSRCCLK#

SOUTH BRIDGE
ICH-8M
PAG 21,22,23,24

USB2.0
5 — **Bluetooth** PAG 35
0,1,2 — **USB2.0 I/O Ports X3** PAG 32
3 — **Camera X1** PAG 32
4,6,7 — **Mini PCI-E Card x1**
Express Card x1
Cable Docking x1

Option for 17" only
SATA - HDD PAG 35 — *SATA2*
SATA - HDD PAG 32 — *SATA0 150MB*
PATA- CD-ROM PAG 32 — *PATA (66/100/133)*

PCI BUS / 33MHz
PCI-E
Azalia

Mini PCI-E Card
PCI Express Mini Card (Wireless LAN/WAN)
PAG 39

LAN
Realtek PCIE-LAN
RTL8101E/8111B
10/100/GagaLAN
PAG 33,34

Express Card
(NEW CARD)
PAG 35

RICOH
RICOH 832
PAG 27,28

Realtek
ALC 268
PAG 29

Two-element microphone PAG 29
Audio Jacks (Phone/ MIC) PAG 29

LPC

ENE KBC
KB3920 Bx
KB3926 Bx
PAG 37,48

Keyboard Touch Pad PAG 36
CIR PAG 36
Capacitive Sense SW PAG 36

X-Bus

FAN PAG 38
Flash PAG 37
SPI PAG 37

AUDIO Amplifier PAG 30
Jack to Speaker PAG 30

MDC DAA
SI3080
PAG 31
MODEM RJ 11 PAG 33

SIM CARD PAG 32
RJ45 PAG 33
IEEE1394 CONN PAG 28
Memory CardReader PAG 27

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

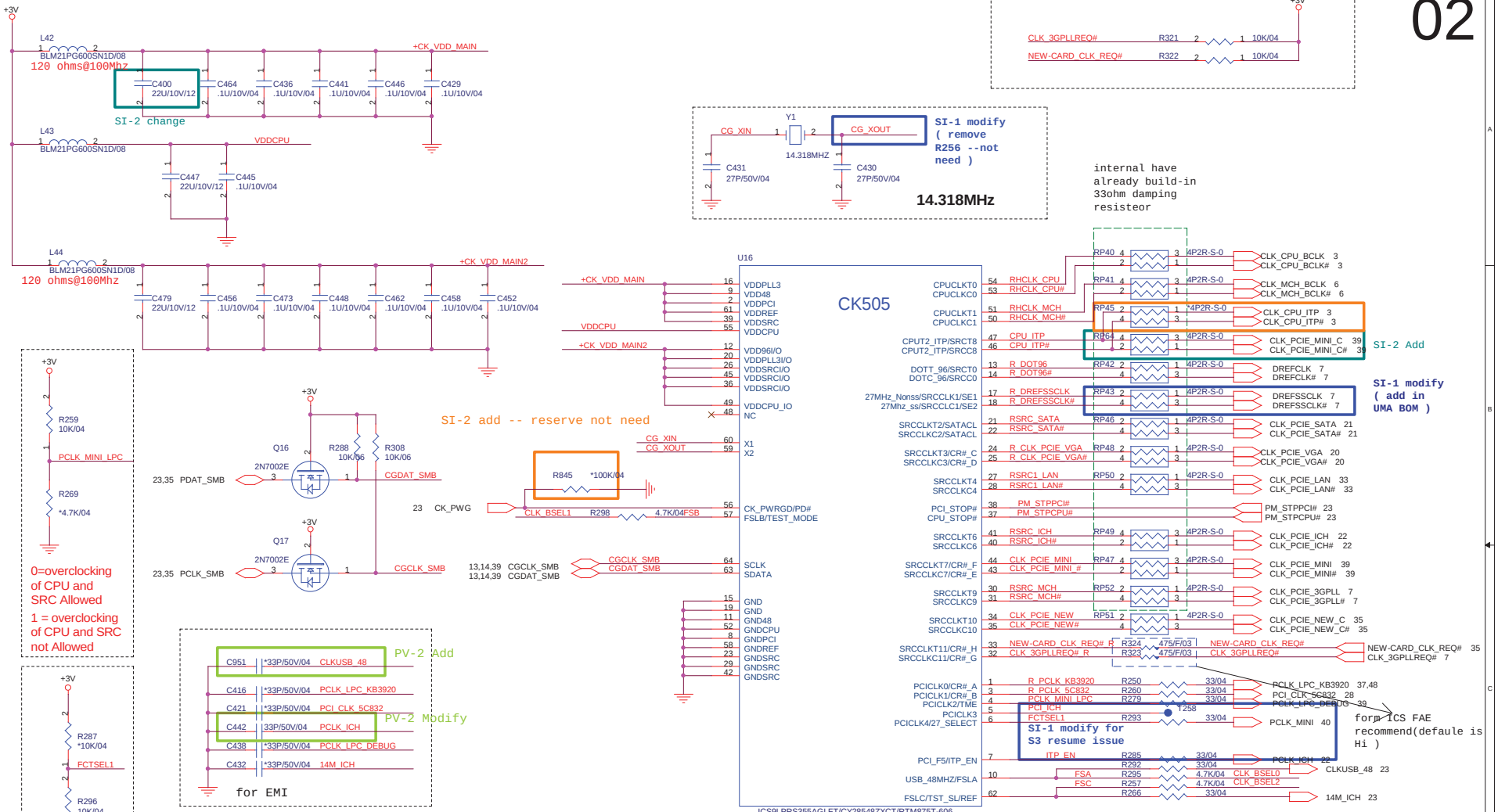
SYSTEM CHARGER(MAX8724) PAG 41
SYSTEM POWER MAX8778 PAG 42
DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAG 46
VCCP +1.5V AND GMCH 1.05V(MAX8717) PAG 43
VGACORE(1.025V)MAX1992 PAG 45
CPU CORE MAX8771 PAG 44

NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Monday, March 19, 2007 Sheet 1 of 48



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

GCLK_SEL = FCTSEL1

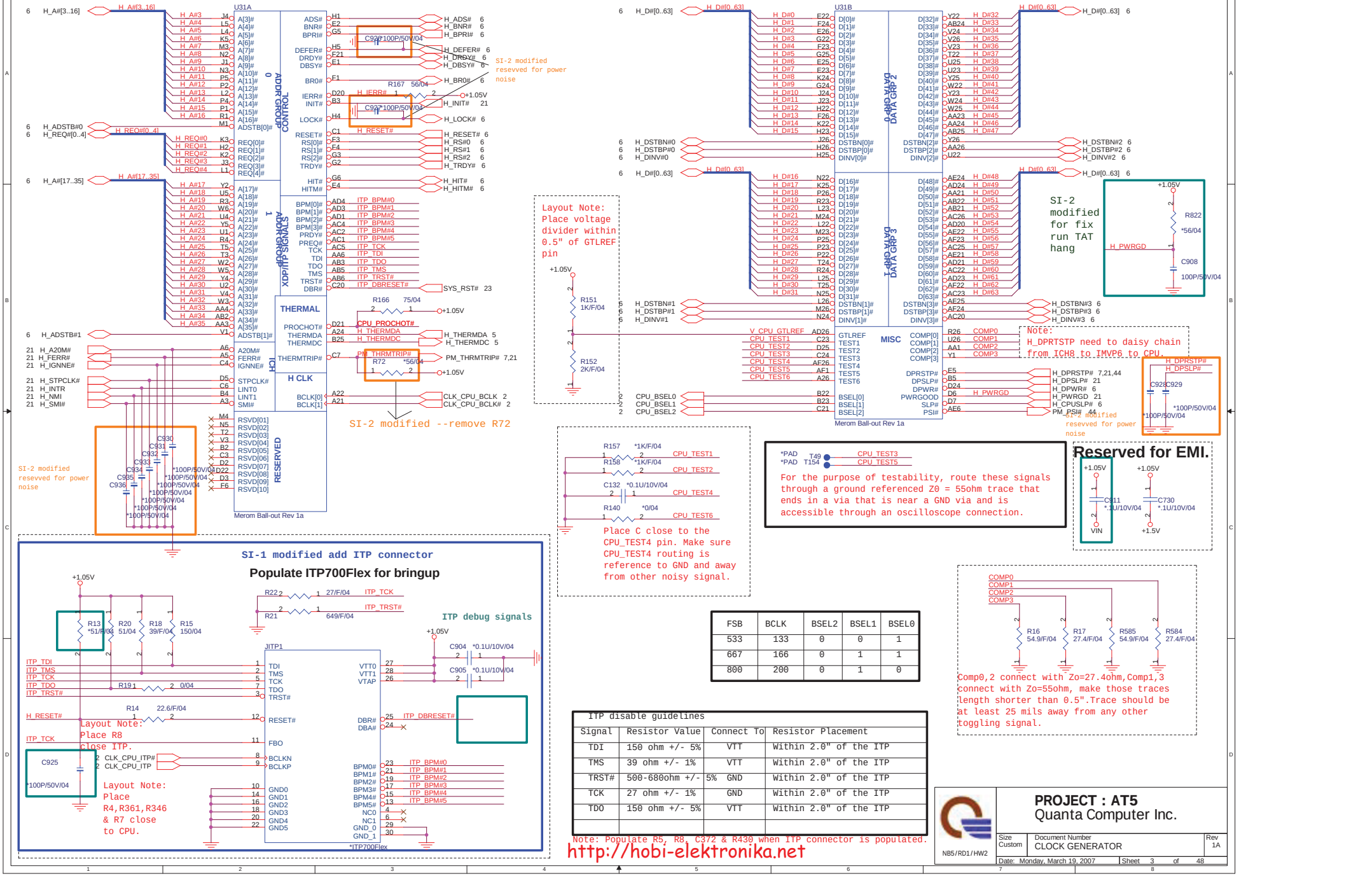
FCTSEL1 (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

PROJECT : AT5
Quanta Computer Inc.

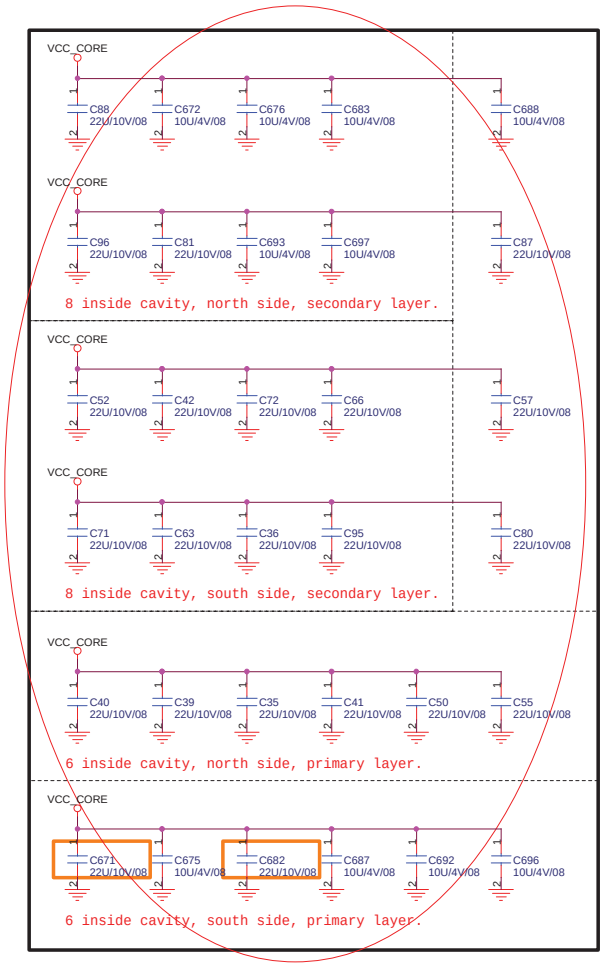
NB5/RD1/HW2

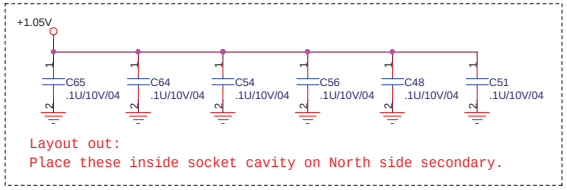
Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

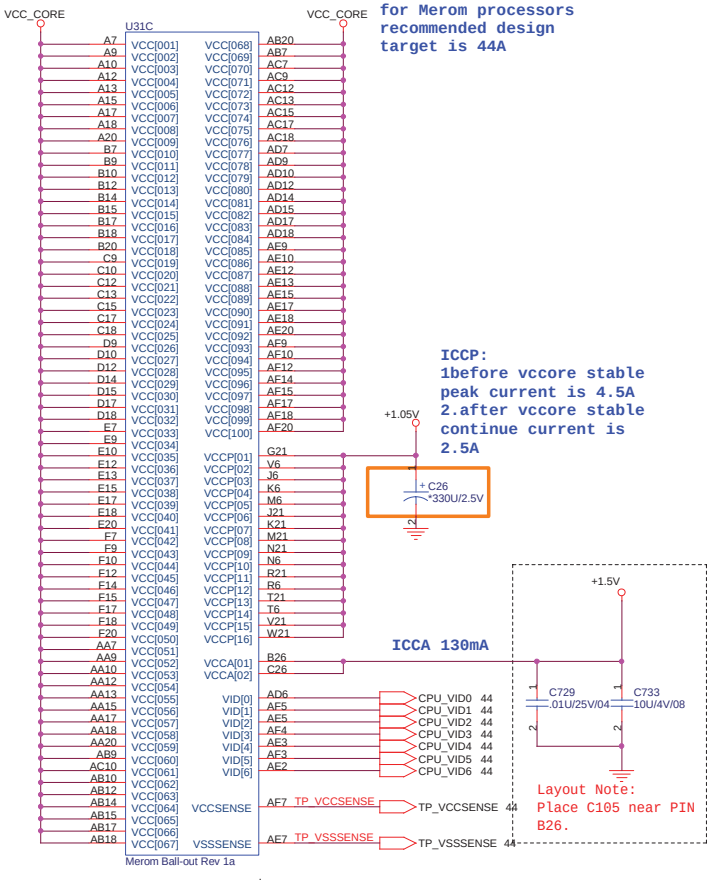
Date: Monday, March 19, 2007 | Sheet 2 of 48

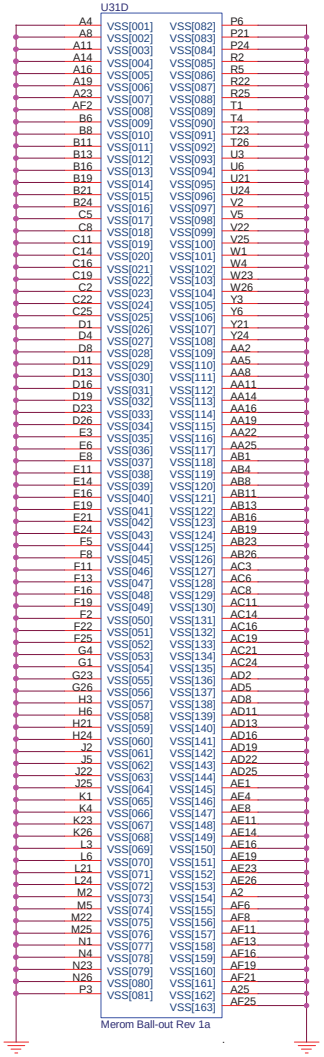


FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

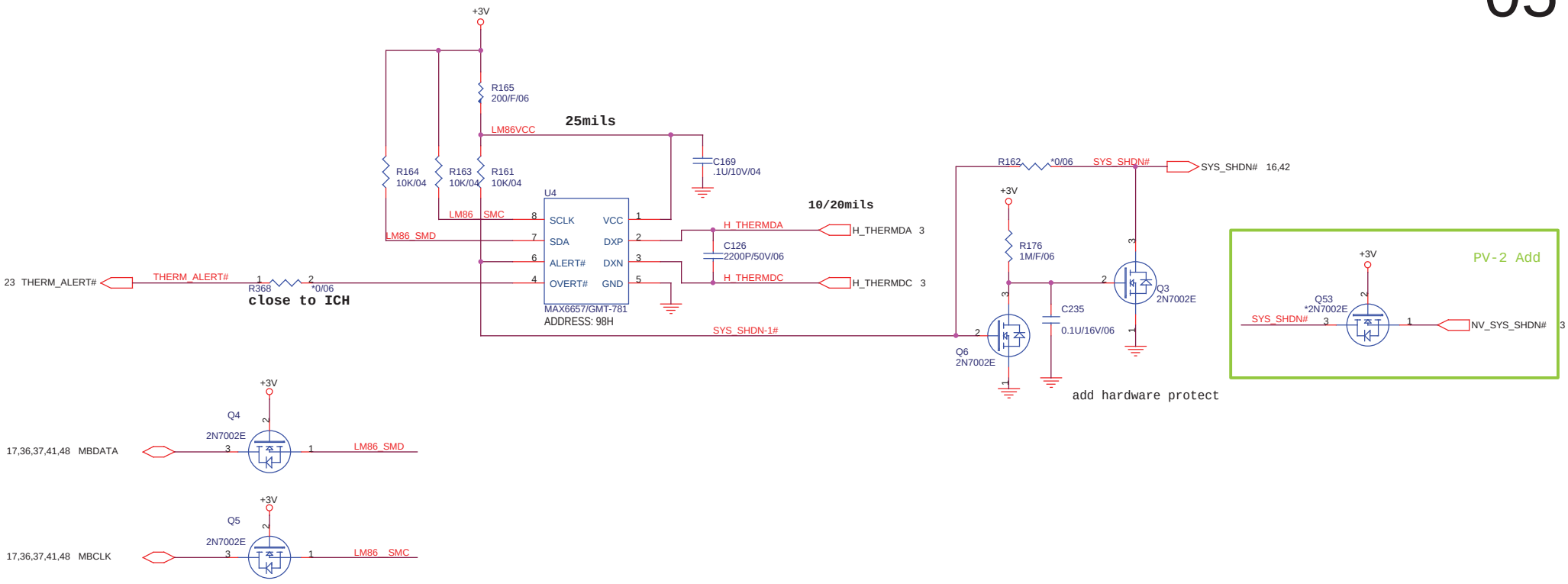




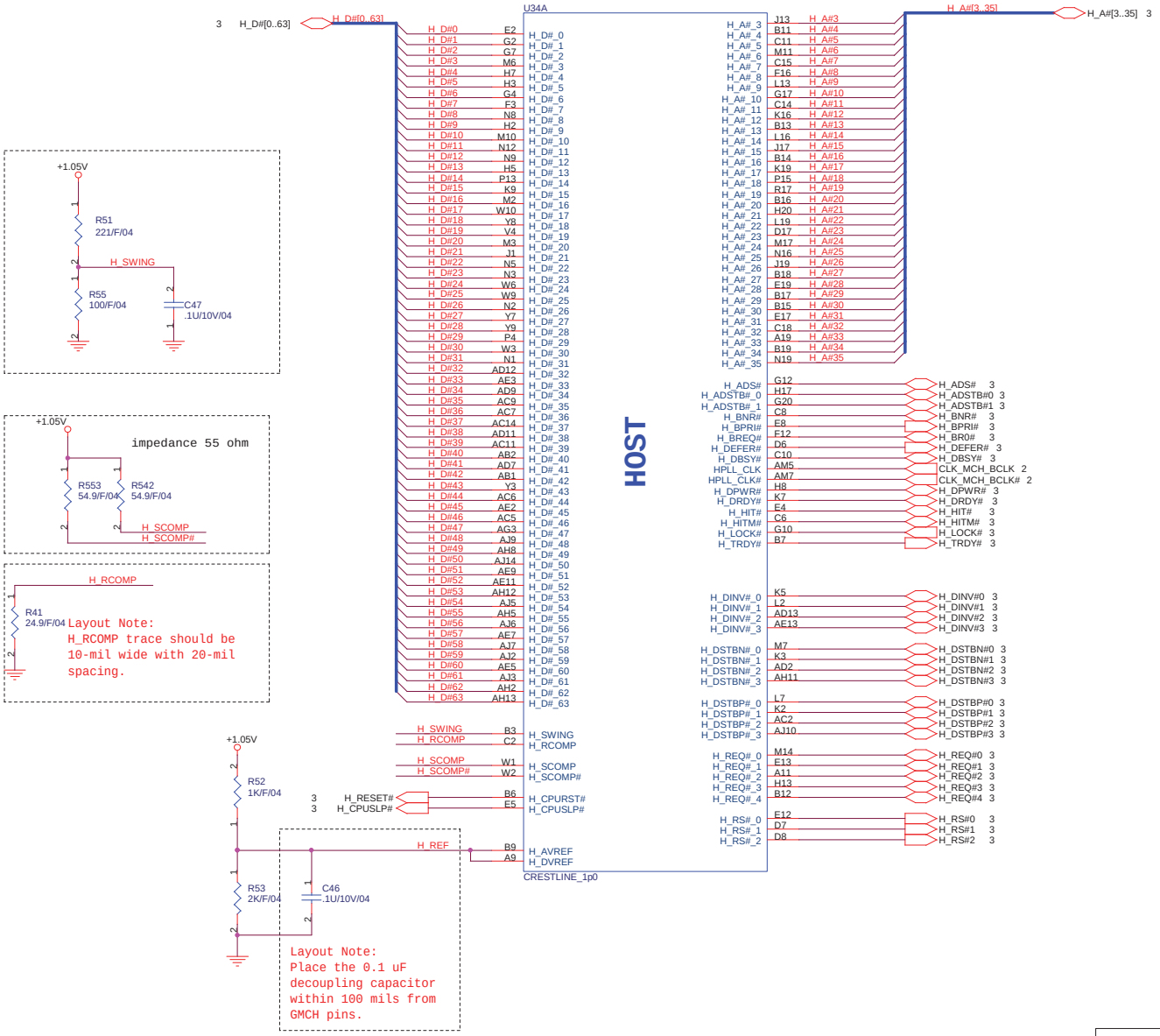




NB5/RD1/HW2	**PROJECT : AT5** Quanta Computer Inc.	
Size: Custom	Document Number: Merom Processor (POWER)	Rev: 1A
Date: Monday, March 19, 2007	Sheet 4 of 48	



NB5/RD1/HW2	**PROJECT : AT5** Quanta Computer Inc.	
	Size: B — Document Number: THERMAL LM86	Rev: 1A
	Date: Monday, March 19, 2007 — Sheet 5 of 48	



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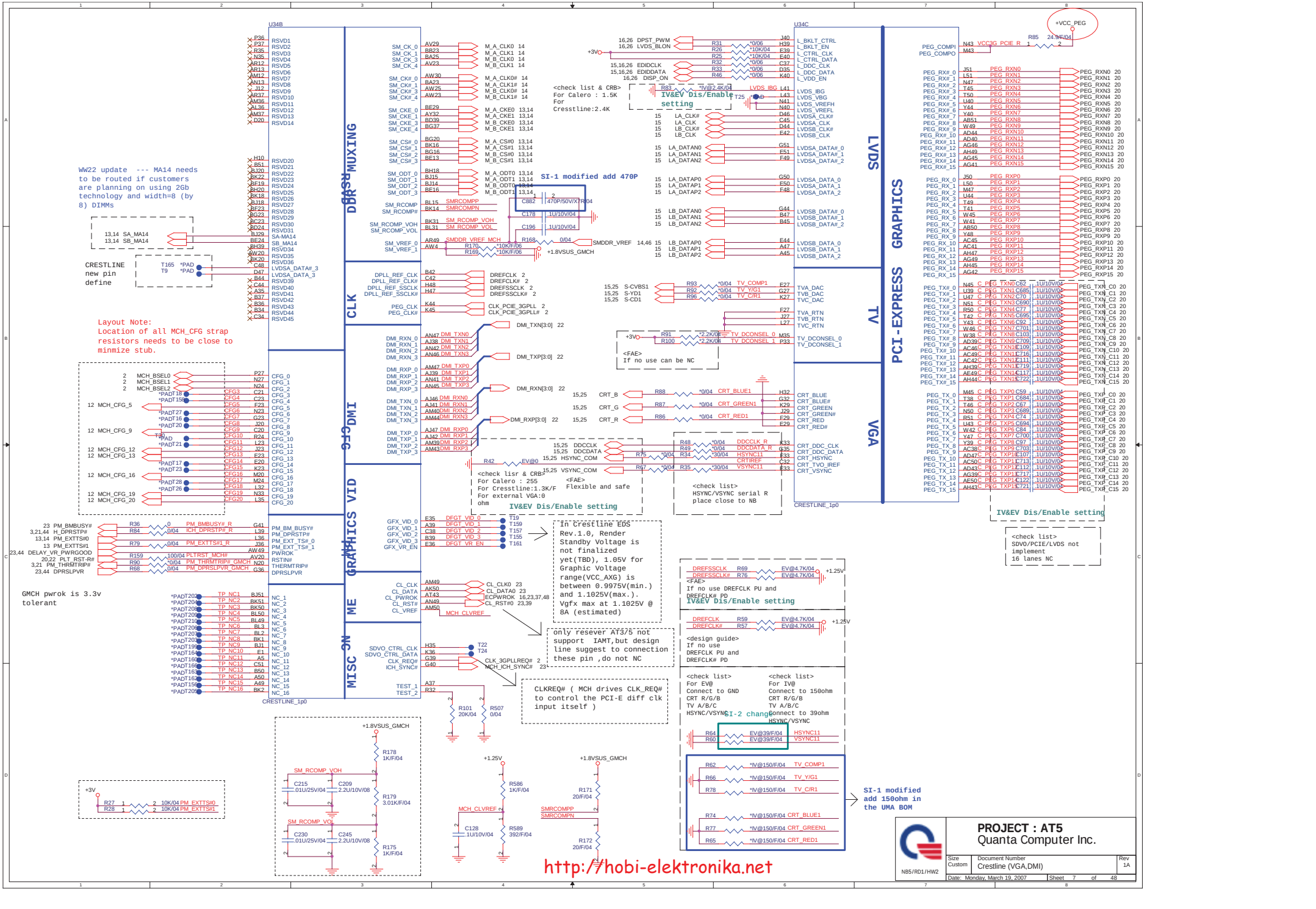
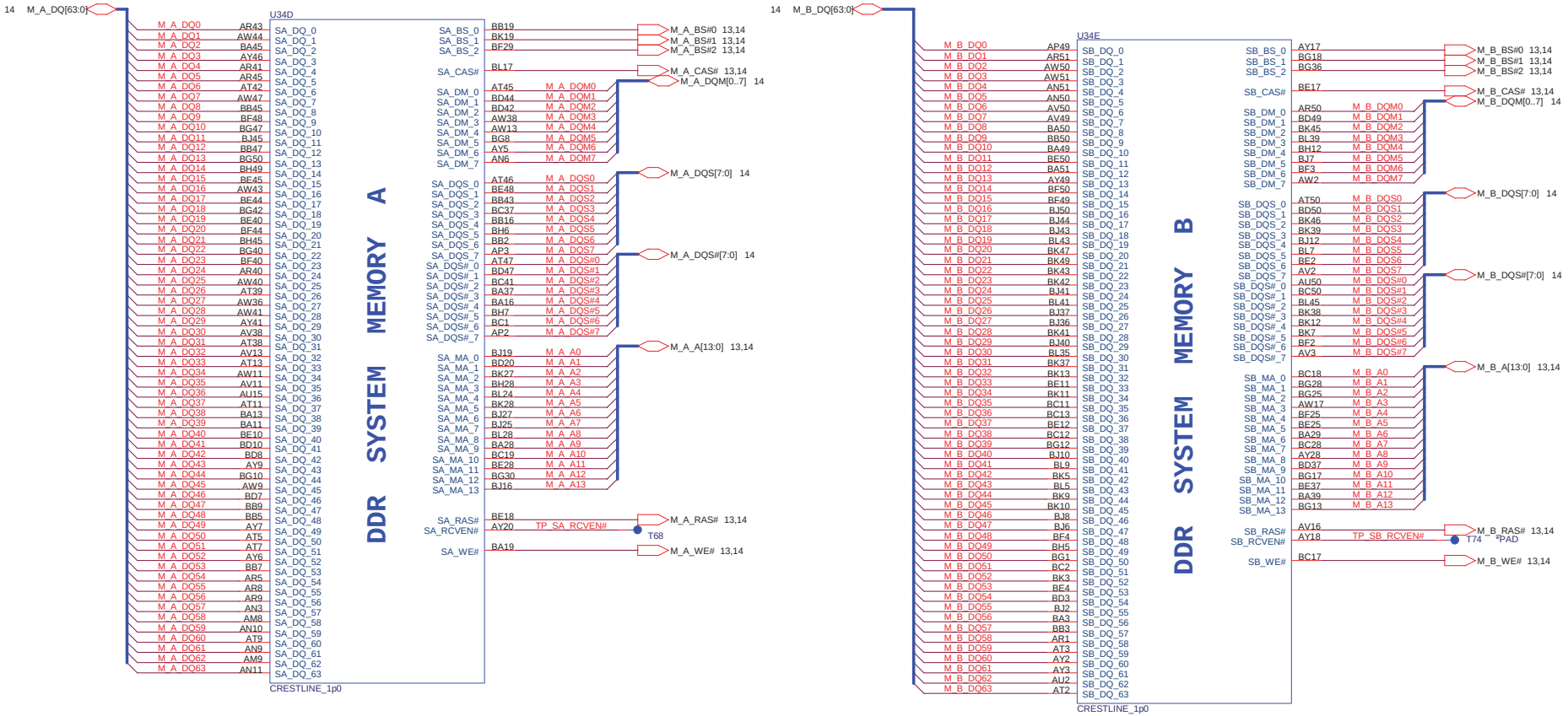
PROJECT : AT5 Quanta Computer Inc.		
Size: Custom	Document Number: Crestline (HOST)	Rev: 1A
NB5/RD1/HW2	Date: Monday, March 19, 2007	Sheet 6 of 48


U34B
U34C
DDR MUXING
CLK
DMI
GRAPHICS VID
GRAPHICS VID
MISC
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
WW22 update --- MA14 needs to be routed if customers are planning on using 2Gb technology and width=8 (by 8) DIMMs
CRESTLINE new pin define
Layout Note: Location of all MCH_CFG strap resistors needs to be close to minmize stub.
SI-1 modified add 470P
IV&EV Dis/Enable setting
GMCH pwrok is 3.3v tolerant
In crestline EDS Rev.1.0, Render Standby Voltage is not finalized yet(TBD), 1.05V for Graphic Voltage range(VCC_AXG) is between 0.9975V(min.) and 1.1025V(max.). Vgfx max at 1.1025V @ 8A (estimated)
only resever AT3/5 not support IAMT,but design line suggest to connection these pin ,do not NC
CLKREQ# (MCH drives CLK_REQ# to control the PCI-E diff clk input itself)
SI-2 change
SI-1 modified add 150ohm in the UMA BOM
CRESTLINE_1p0
http://hobi-elektronika.net
PROJECT : AT5
Quanta Computer Inc.
Crestline (VGA,DMI)
Monday, March 19, 2007

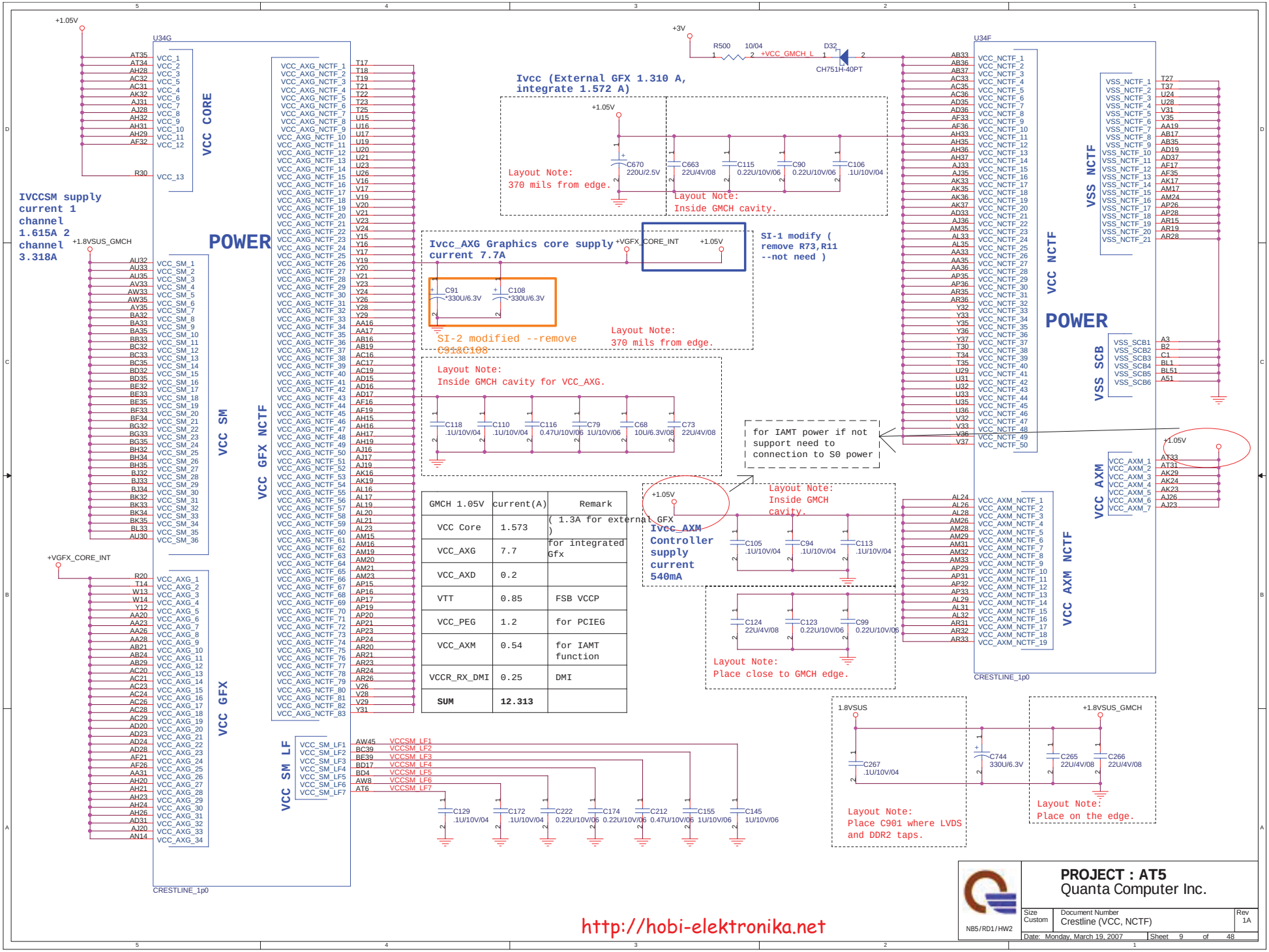


NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (DDR)	1A

Date: Monday, March 19, 2007 | Sheet 8 of 48



GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

PROJECT : AT5		
Quanta Computer Inc.		
Size: Custom	Document Number: Crestline (VCC, NCTF)	Rev: 1A
NB5/RD1/HW2	Date: Monday, March 19, 2007	Sheet 9 of 48

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

IV&EV Dis/Enable setting

<FAE>
INT VGA disable
VCCSYNC connect
to GND

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

SI-1 modify
(NET name
wrong)

FB_120ohm+-25%_100mHz
_200mA_0.2ohm DC

50mA
150mA
80mA
80mA
10uH+-20%_100mA

0.1Caps should be
placed 200 mils
with in its pins.

10mA
100mA
Ivcca_PEG_BG
supply current
100mA

POWER

CRESTLINE_1p0

Ivcc_VTT FSB
supply
current
0.85A

Place on the edge.

Reserved L81 pad for
inductor.

Place caps close
to VCC_AXD.

Ivcc_DMI supply
current 100mA

200mA

100mA

1uH+-20%_300mA

Ivcc_PEG
supply current
1.2A

SI-1 modified change

Ivcc_RX_DMI
supply current
250mA

250mA

150mA

SI-2
modified
for WW44
request

SI-2 add for UMA to
fix TV-out noise

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

22nF & 0.1uF for
VCC_TVDACA:C_R should
be placed with in 250
mils from Crestline.

IV&EV Dis/Enable setting

FB_220ohm+-25%_100MHz
_2A_0.1ohm DC

100mA

+3V_VCC_HV

D1
CH751H-40HPT_NC

40 mil
wide

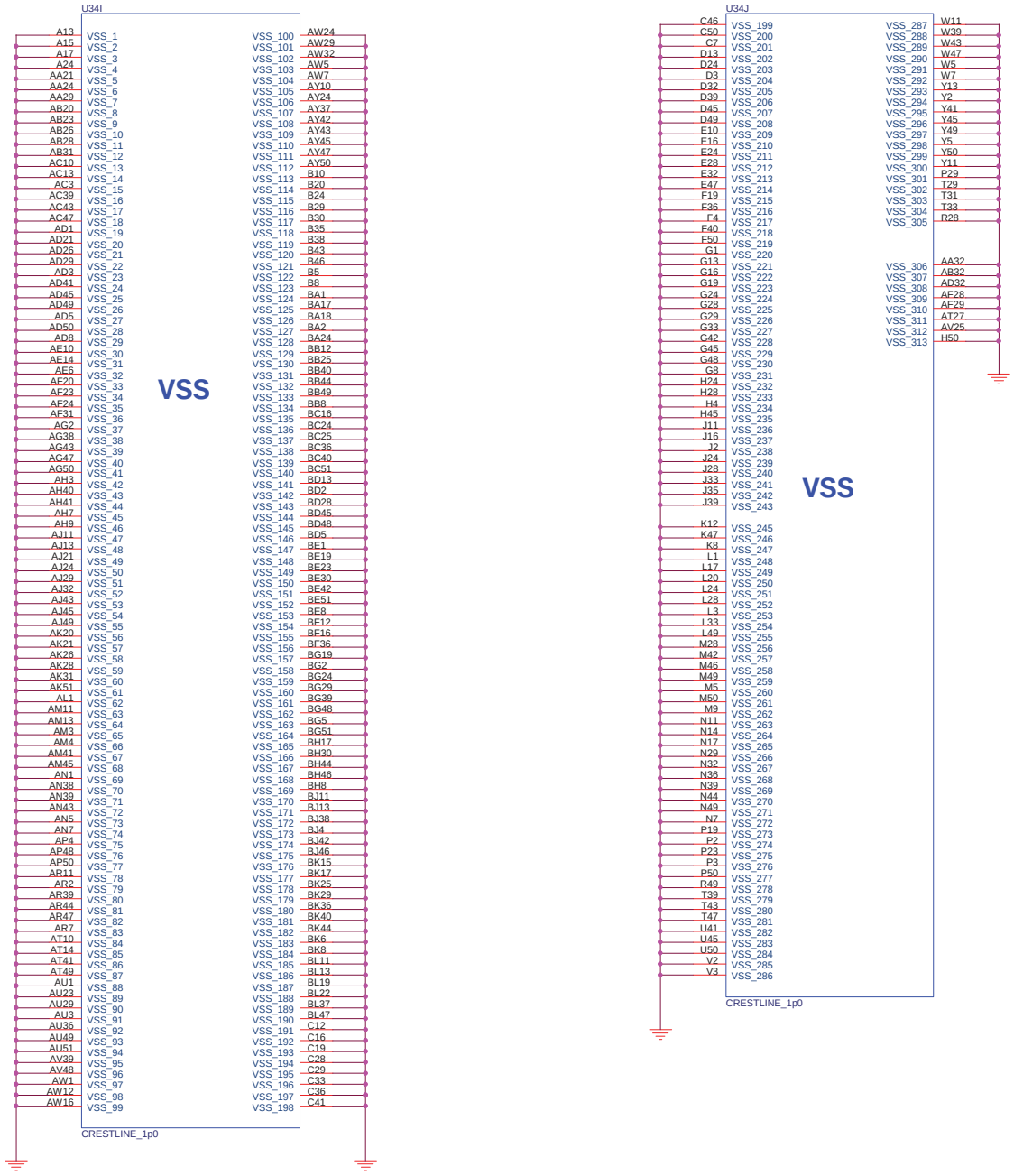
Place caps close
to VCC_AXF

PROJECT : AT5
Quanta Computer Inc.

N85/RD1/HW2

Size: Custom | Document Number: Crestline (POWER) | Rev: 1A

Date: Monday, March 19, 2007 | Sheet 10 of 48



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NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (VSS)	1A

Date: Monday, March 19, 2007 Sheet 11 of 48

Strap table

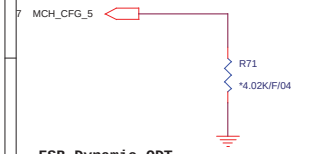
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

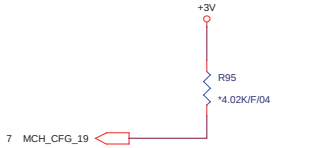
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

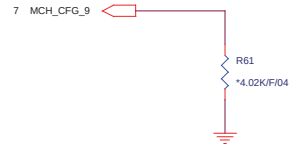


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

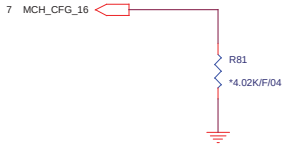


SDVO Present

Strap define at External DVI control page

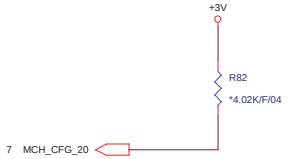
FSB Dynamic ODT

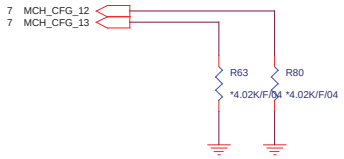
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- GMCH STRAP-3(6 of 6)	1A

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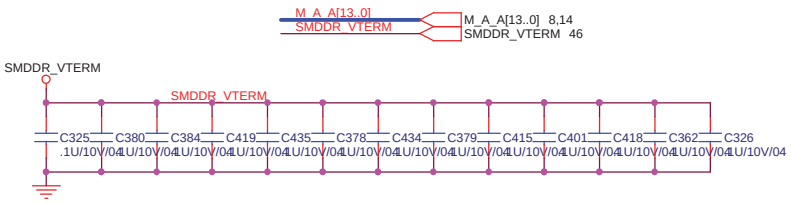
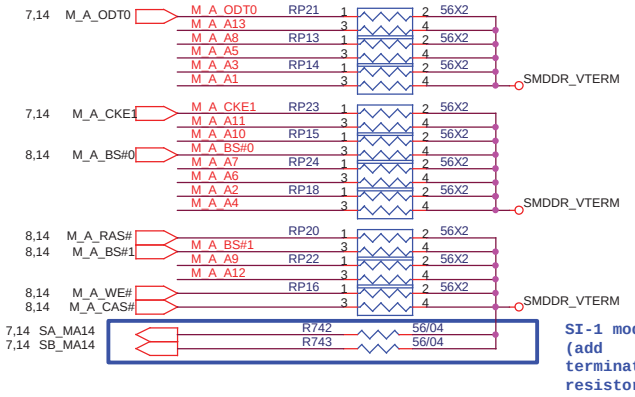
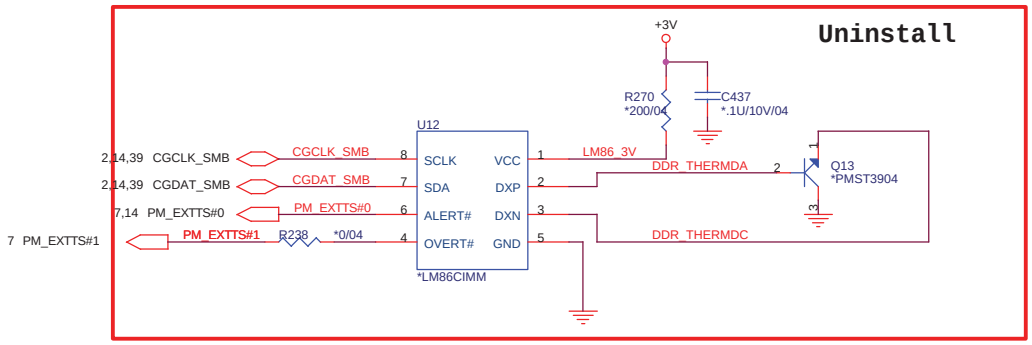
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

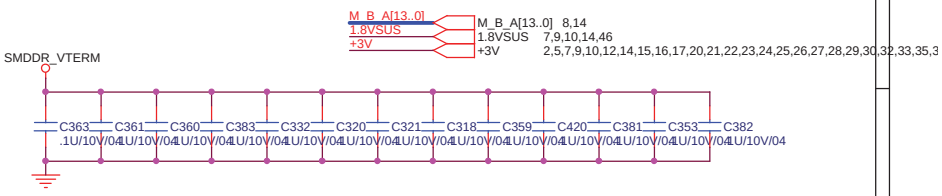




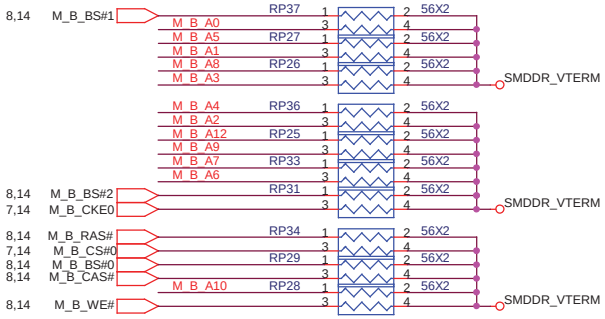
SI-1 modify (add terminater resistor)

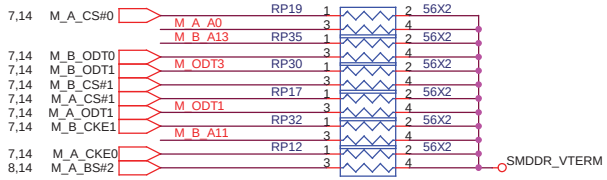


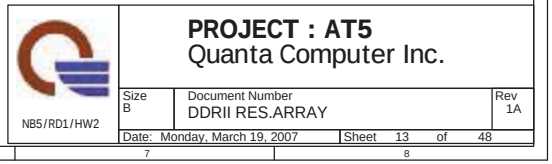
DDRII B CHANNEL

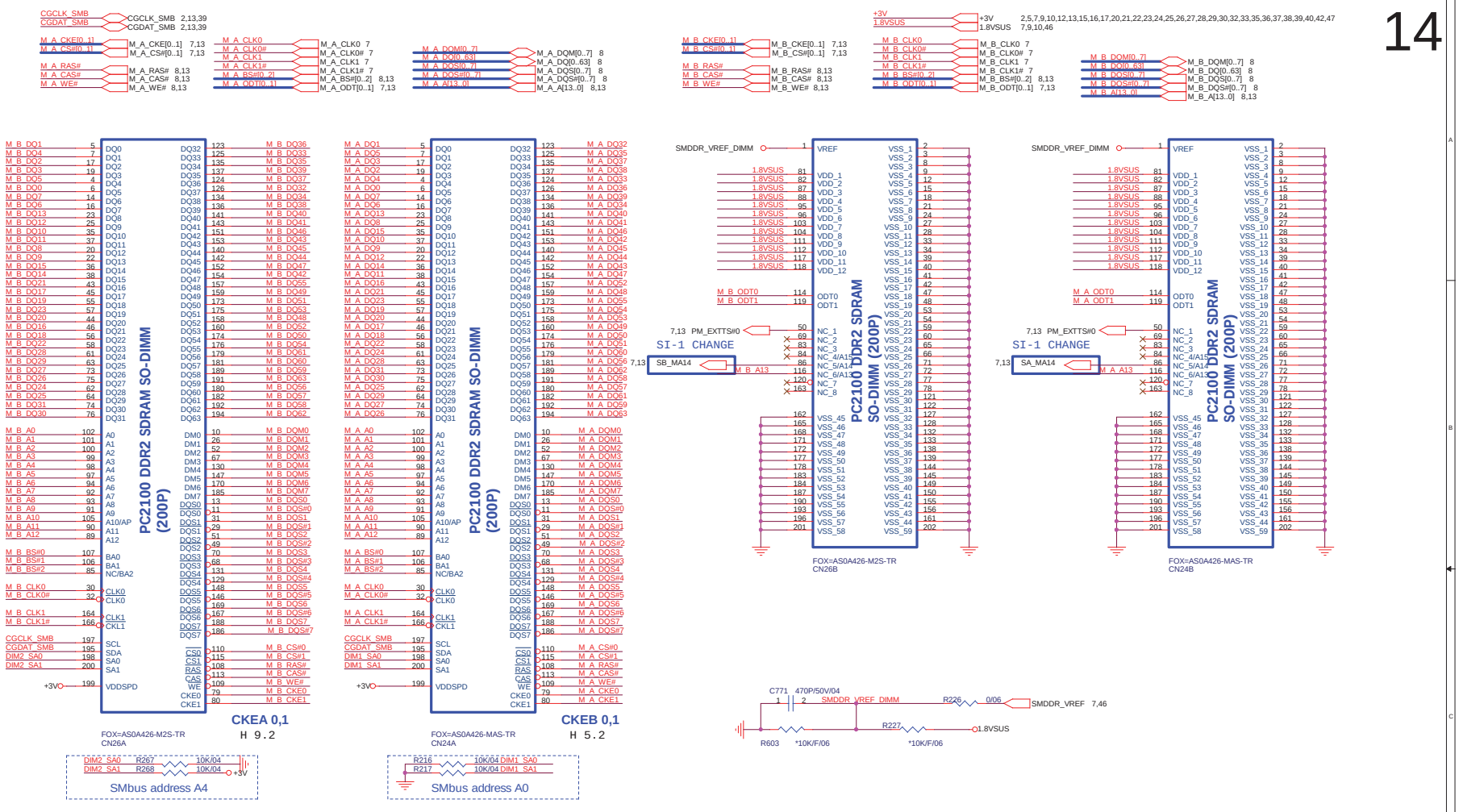


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

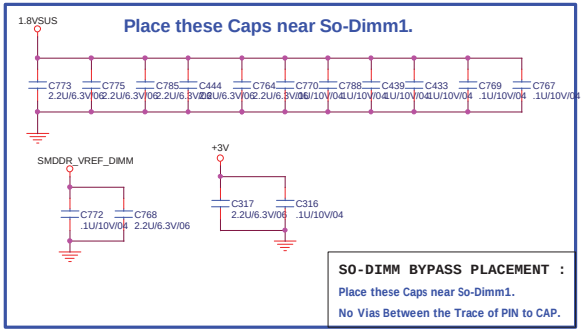








Place these Caps near So-Dimm1.

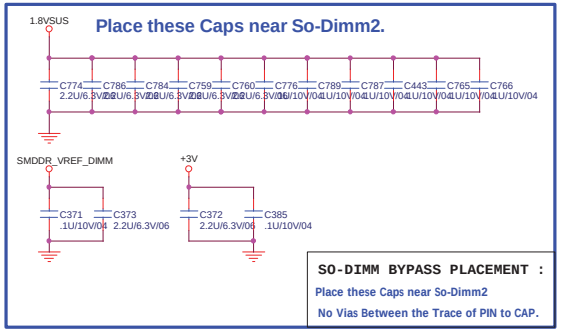


SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm2.

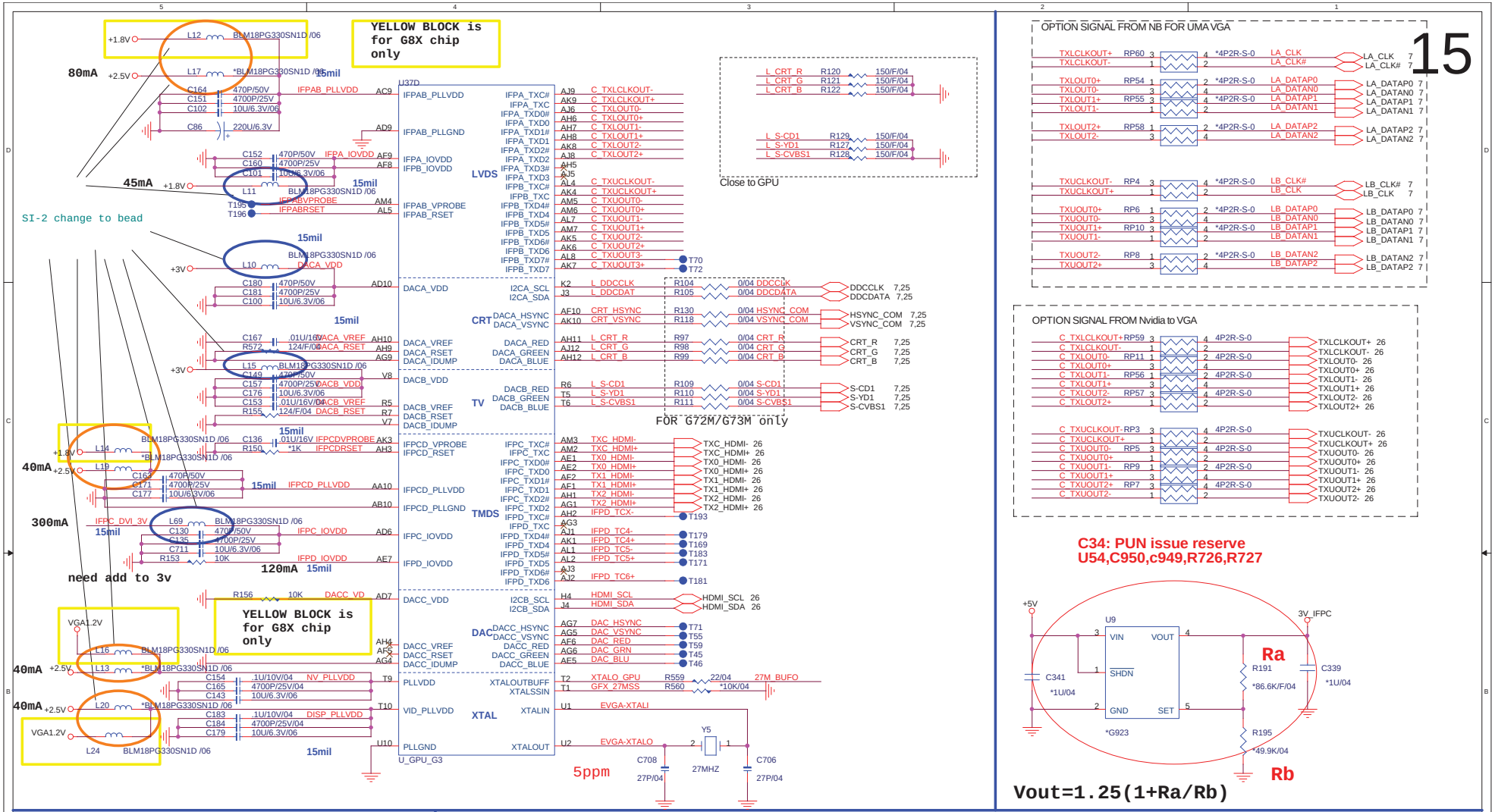


SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm2

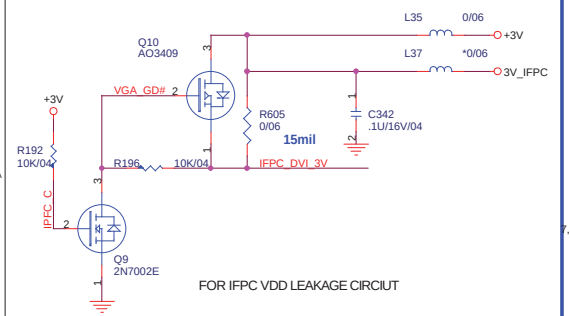
No Vias Between the Trace of PIN to CAP.

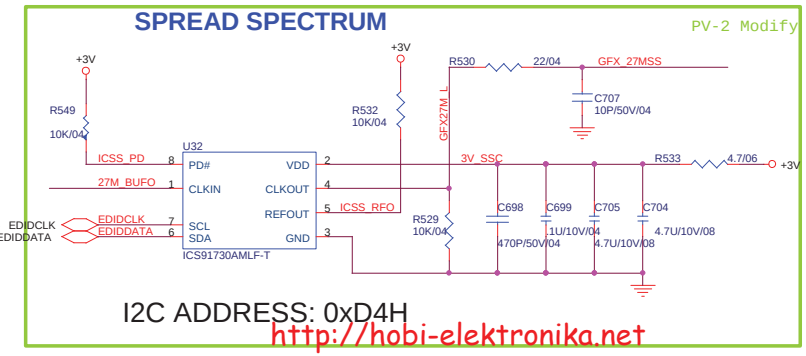
N8S/RD1/HW2	**PROJECT : AT5** Quanta Computer Inc.	
Size Custom	Document Number DDRII SO-DIMM(200P)	Rev 1A
Date: Monday, March 19, 2007	Sheet 14 of 48	



C34: PUN issue reserve
U54,C950,c949,R726,R727

Vout=1.25(1+Ra/Rb)

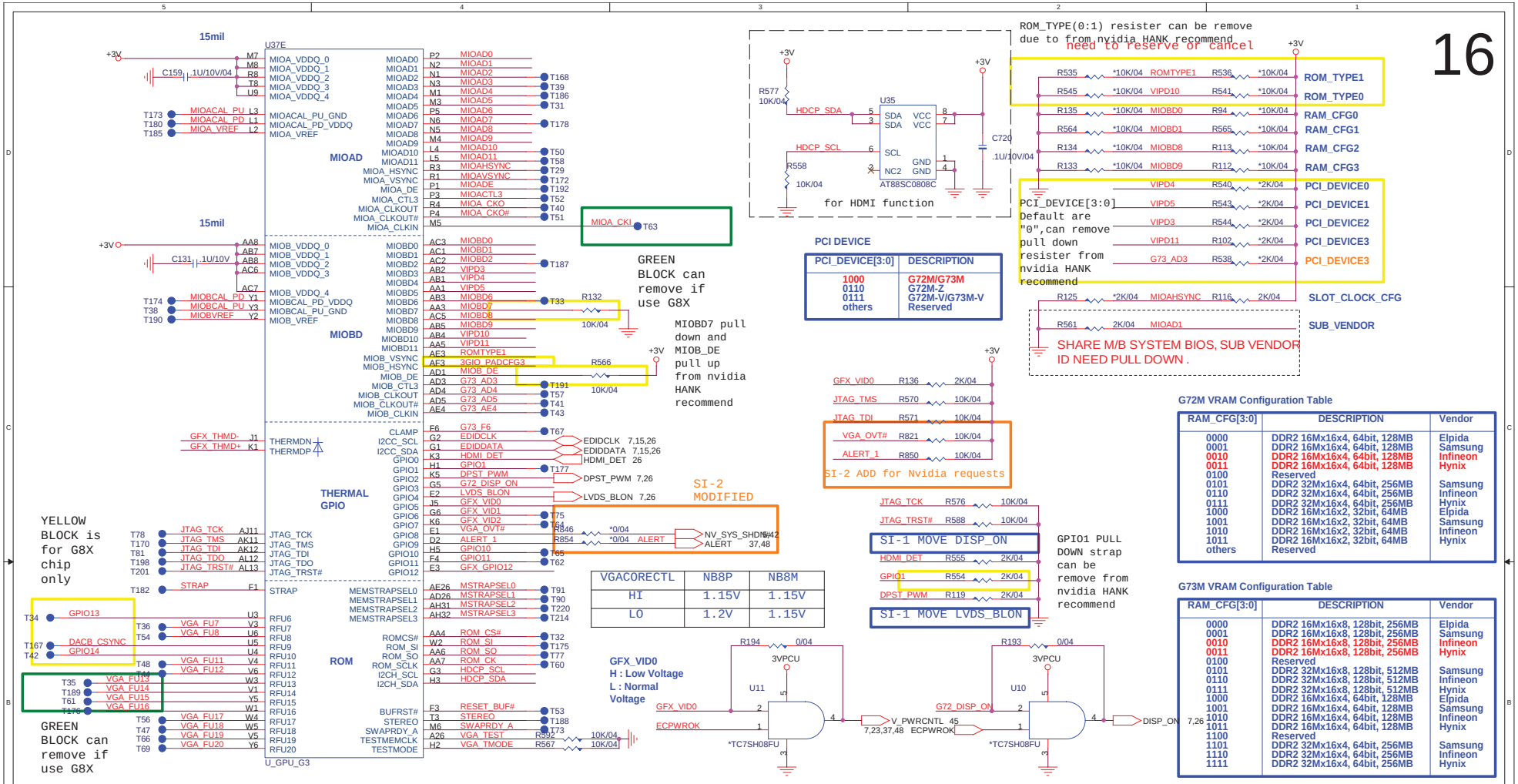




NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M (LVDS/DVI/CRT/TV)	1A
Date: Monday, March 19, 2007	Sheet 15 of 48	



http://hobi-elektronika.net

PROJECT : AT5	Quanta Computer Inc.
NB5/RD1/HW2	Size: Custom; Document Number: NVG73M (ROM/GPIO/STRAP); Rev: 1A
	Date: Monday, March 19, 2007; Sheet 16 of 48

Channel C is available on G73M only

U37B

VMA_DQ0 N27 … VMA_DQ63 AE28 — FBAD0 … FBAD63

VMA_DM0 M29 … VMA_DM7 AG30 — FBADQM0 … FBADQM7

VMA_WDQS0 L28 … VMA_WDQS7 AH30 — FBADQS_WP0 … FBADQS_WP7

VMA_RDQS0 M28 … VMA_RDQS7 AH29 — FBADQS_RN0 … FBADQS_RN7

FBA

FBVDD_0 … FBVDD_19 — A12, A15, A18, A21, A24, A27, A3, A30, A6, A9, AA32, AD32, AG32, AK32, C32, F32, J32, M32, R32, V32

C309 … C289 .1U/10V/04 … 10U/4V/06 — +1.8V

PLACE NEAR GPU

FBVDDQ_0 … FBVDDQ_23 — AA25, AA26, AB26, G11, G12, G15, G18, G21, G22, H11, H12, H21, H22, L25, L26, M25, M26, R25, R26, V25, V26

C763 … C305 .1U/10V/04 … 10U/4V/06 — +1.8V

PLACE NEAR GPU

C783 220U

FBA_CMD0 … FBA_CMD26 — P32, U27, P31, U30, Y31, W32, W31, T32, V27, T28, T31, U32, W29, W30, T27, V28, V30, U31, R27, V29, T30, W28, R29, R30, P29, U28, Y32

VMA_MA3 … VMA_MA13, VMA_BA0, VMA_BA1, VMA_BA2, VMA_CS0#, VMA_WE#, VMA_CAS#, VMA_CKE, VMA_ODT, VMA_CLK0, VMA_CLK0#, VMA_CLK1, VMA_CLK1#

T219, T215

FBA_CLK0 … FBA_CLK1# — P28, R28, Y27, AA27

RFU2 Y30 — FBA_CMD27 — T218

RFU3 AC26 — G73_AC26 — T86

FBA_DEBUG AC27 — VMA_DEBUG — T87

FBA_REFCLK D32 — VMA_REFCK — T217

FBA_REFCLK# D31 — VMA_REFCK# — T216

GREEN BLOCK can remove if use G8X

C313 4.7U/10V/06

C261 .1U/10V

L27 BLM18PG221SN1D/06 VGA1.2V

H_PLLVDD

FBA_PLLVDD G23

FBA_PLLAVDD G25 — 15mil — FBA_PLLAVDD — L33 BLM18PG330SN1D/06 VGA1.2V

FBA_PLLGND G24

C328 4.7U/10V/06 C286 .1U/10V

C315 470P/50V/04 C322 4700P/25V/04 For EMI

+1.8V R604 *1K/04 FB_VREF1 E32 — R602 *1K/04 C762 *.1U/10V/04 — *U_GPU_G3

15mil

G72: Stuff these parts
G73M : NC

VREF = FBVDDQ * Rbot/(Rtop + Rbot)

U37C

VMC_DQ0 B7 … VMC_DQ63 E19 — FBCD0 … FBCD63

VMC_DM0 A4 … VMC_DM7 E20 — FBCDQM0 … FBCDQM7

VMC_WDQS0 C5 … VMC_WDQS7 F20 — FBCDQS_WP0 … FBCDQS_WP7

VMC_RDQS0 C6 … VMC_RDQS7 F21 — FBCDQS_RN0 … FBCDQS_RN7

FBC

FBVTT_0 … FBVTT_17 — AA23, AB23, H16, H17, J10, J23, J24, J9, K11, K12, K21, K22, K24, K9, L23, M23, T25, U25

C287 … C251 .1U/10V/04 … 10U/4V/06 — +1.8V

PLACE NEAR GPU

FBC_CMD0 … FBC_CMD26 — C13, A16, A13, B17, B20, A19, B19, B14, E16, A14, C15, B16, F17, C19, D15, C17, A17, C16, D14, F16, C14, C18, E14, B13, E15, F15, A20

VMC_MA3, VMC_MA0, VMC_MA2, VMC_MA1, VMC_MA3H, VMC_MA4H, VMC_MA5H, VMC_BA2, VMC_CS0#, VMC_WE#, VMC_BA0, VMC_CKE, VMC_ODT, VMC_MA2H, VMC_MA12, VMC_RAS#, VMC_MA11, VMC_MA10, VMC_BA1, VMC_MA8, VMC_MA9, VMC_MA6, VMC_MA5, VMC_MA7, VMC_MA4, VMC_CAS#, VMC_MA13

T83, T212

FBC_CLK0 … FBC_CLK1# — E13, F13, F18, E17

VMC_CLK0, VMC_CLK0#, VMC_CLK1, VMC_CLK1#

RFU4 C20 — FBC_CMD27 — T211

RFU5 D1 — G73_D1 — T184

FBC_DEBUG F12 — VMC_DEBUG

I2C_DAT B1 — I2C_DAT — R137 0/04 — I2CS_SDA

I2C_CLK C1 — I2C_CLK — R117 0/04 — I2CS_SCL

+3V +3V R131 2.2K/04 R103 2.2K/04

YELLOW BLOCK is for G8X chip only

FBC_PLLVDD G8 — G73_G8 — T76

FBC_PLLAVDD G10 — FBC_PLLAVDD — 15mil — L23 — VGA1.2V

FBC_PLLGND G9

C731 470P/50V/04 C727 4700P/25V/04 C162 BLM18PG330SN1D/06 4.7U/10V/06

FBCAL_PD_VDDQ K26 — FBCAL_PD — R185 40.2/F/06 — +1.8V

FBCAL_PU_GND H26 — FBCAL_PU — R187 40/F/04

FBCAL_TERM_GND J26 — FBCAL_TERM — R186 40.2/F/04

FB_VREF2 A28 — FB_VREF2 — 15mil — T213

F_VREF2 filter can be remove from nvidia HANK recommend
G70,G71: Stuff these parts
G72M,G73M : NC

*U_GPU_G3

18 VMA_DQ[63..0]
18 VMA_DM[7..0]
18 VMA_WDQS[7..0]
18 VMA_RDQS[7..0]

19 VMC_DQ[63..0]
19 VMC_DM[7..0]
19 VMC_WDQS[7..0]
19 VMC_RDQS[7..0]

VMA_ODT — R832 0/04 — VMA_ODT_R — VMA_ODT_R 18
VMA_DEBUG — R831 *0/04

R598 10K/04

G72M/G73M: STUFF
UMA:NC

VMC_ODT — R830 0/04 — VMC_ODT_R — VMC_ODT_R 19
VMC_DEBUG — R829 *0/04

R174 10K/04

G72M/G73M: STUFF
UMA:NC

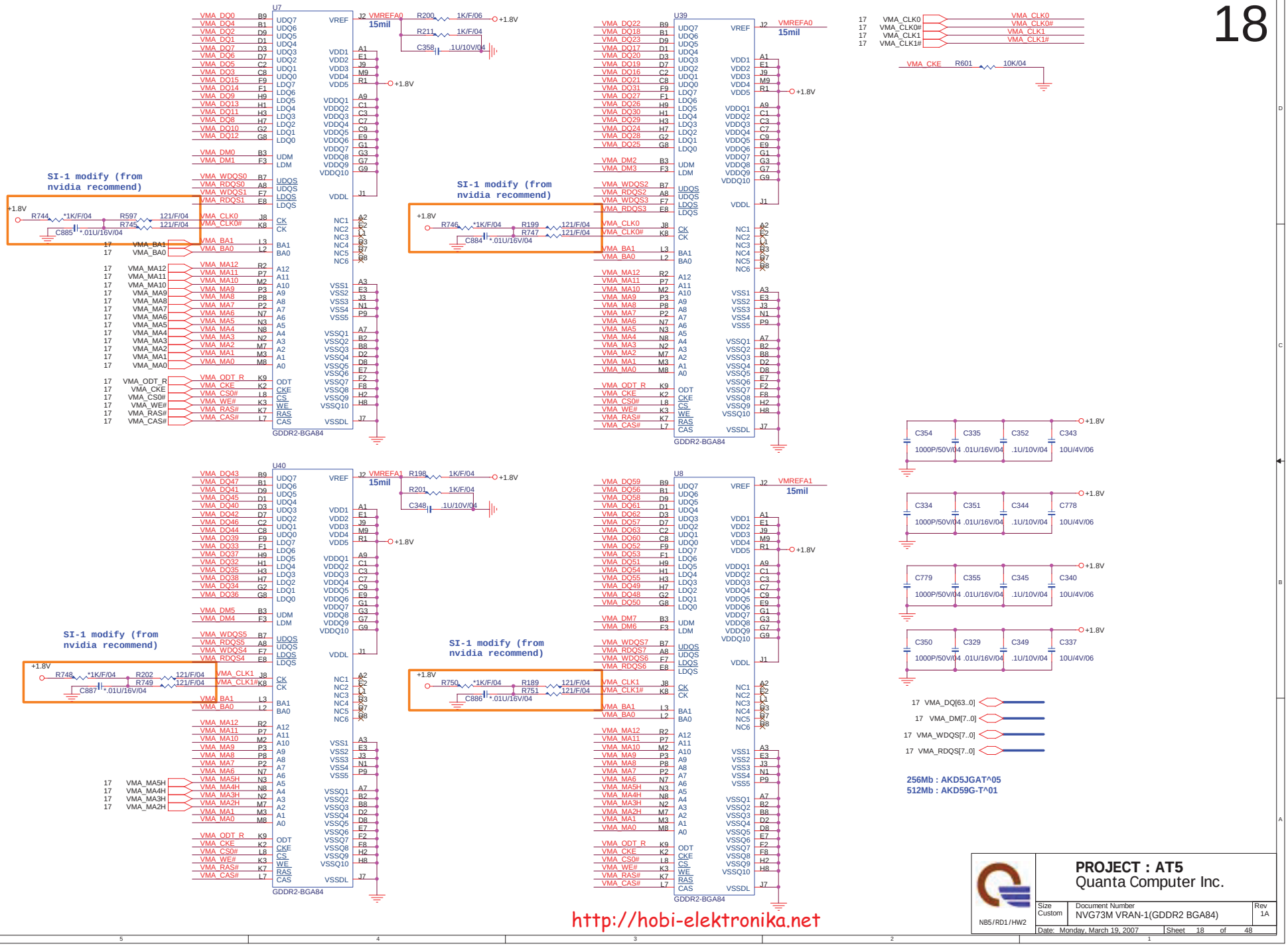
+3V Q51 2N7002E — MBDATA 5,36,37,41,48 — I2CS_SDA

+3V Q52 2N7002E — MBCLK 5,36,37,41,48 — I2CS_SCL

SI-2 modified for G8X thermal sensor

YELLOW BLOCK is for G8X chip only

PROJECT : AT5	Quanta Computer Inc.
NB5/RD1/HW2	
Size: Custom	Document Number: NVG73M (MEM I/F)
Rev: 1A	
Date: Monday, March 19, 2007	Sheet 17 of 48


U7
U39
U40
U8
GDDR2-BGA84
SI-1 modify (from nvidia recommend)
VMREFA0
VMREFA1
15mil
+1.8V
VMA_CLK0
VMA_CLK0#
VMA_CLK1
VMA_CLK1#
VMA_CKE
R601 10K/04
C354 C335 C352 C343
C334 C351 C344 C778
C779 C355 C345 C340
C350 C329 C349 C337
1000P/50V/04 .01U/16V/04 .1U/10V/04 10U/4V/06
17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]
256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01
http://hobi-elektronika.net
PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number NVG73M VRAN-1(GDDR2 BGA84)
Rev 1A
Date: Monday, March 19, 2007
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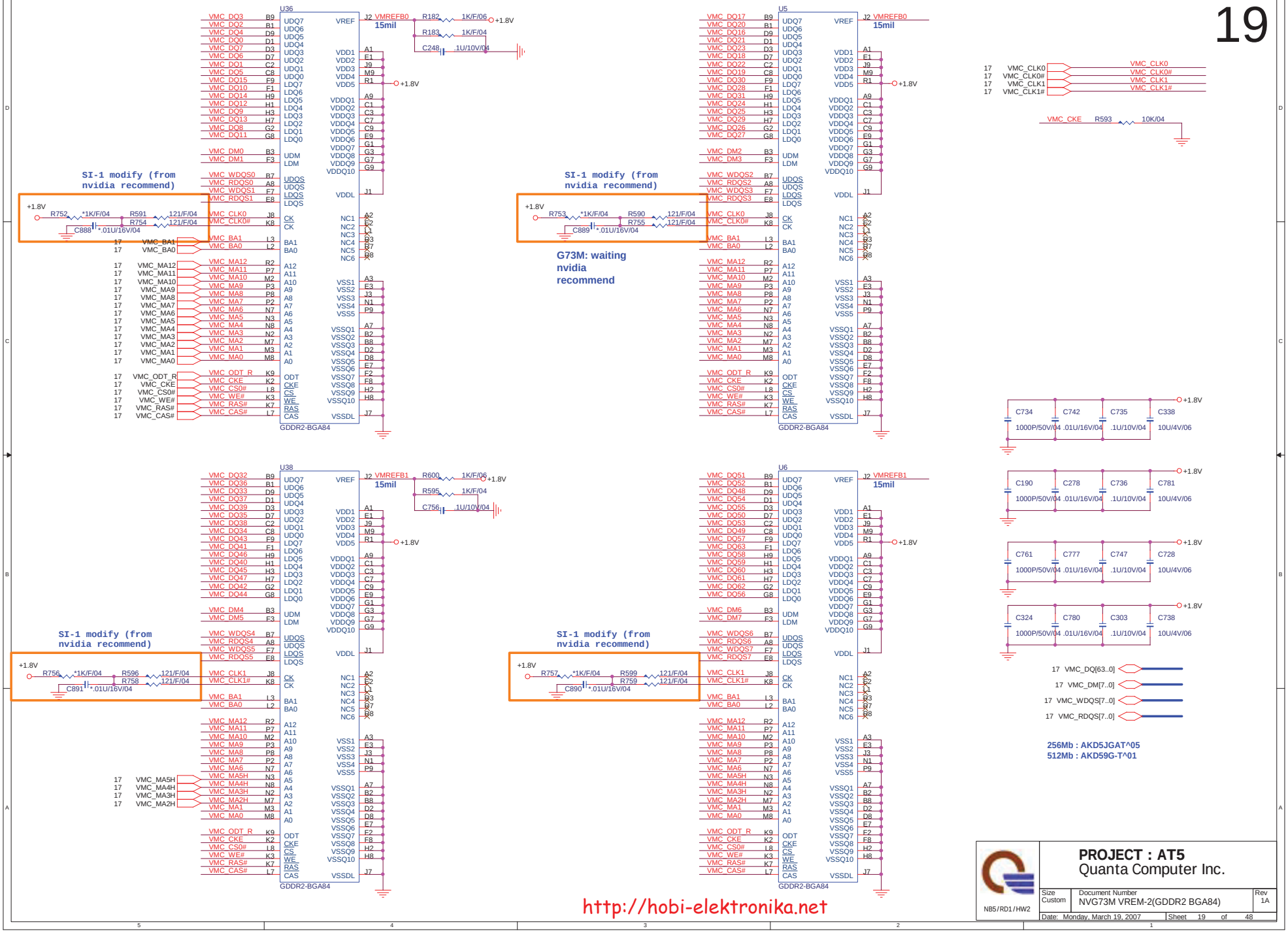
U36
U5
U38
U6
GDDR2-BGA84
SI-1 modify (from nvidia recommend)
G73M: waiting nvidia recommend
15mil
VMREFB0
VMREFB1
+1.8V
R752 *1K/F/04
R591 121/F/04
R754 121/F/04
C888 *.01U/16V/04
R753 *1K/F/04
R590 121/F/04
R755 121/F/04
C889 *.01U/16V/04
R756 *1K/F/04
R596 121/F/04
R758 121/F/04
C891 *.01U/16V/04
R757 *1K/F/04
R599 121/F/04
R759 121/F/04
C890 *.01U/16V/04
R182 1K/F/06
R183 1K/F/04
C248 .1U/10V/04
R600 1K/F/06
R595 1K/F/04
C756 .1U/10V/04
VMC_CLK0
VMC_CLK0#
VMC_CLK1
VMC_CLK1#
VMC_CKE R593 10K/04
C734 1000P/50V/04
C742 .01U/16V/04
C735 .1U/10V/04
C338 10U/4V/06
C190 1000P/50V/04
C278 .01U/16V/04
C736 .1U/10V/04
C781 10U/4V/06
C761 1000P/50V/04
C777 .01U/16V/04
C747 .1U/10V/04
C728 10U/4V/06
C324 1000P/50V/04
C780 .01U/16V/04
C303 .1U/10V/04
C738 10U/4V/06
VMC_DQ[63..0]
VMC_DM[7..0]
VMC_WDQS[7..0]
VMC_RDQS[7..0]
256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01
http://hobi-elektronika.net
PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number NVG73M VREM-2(GDDR2 BGA84)
Rev 1A
Date: Monday, March 19, 2007
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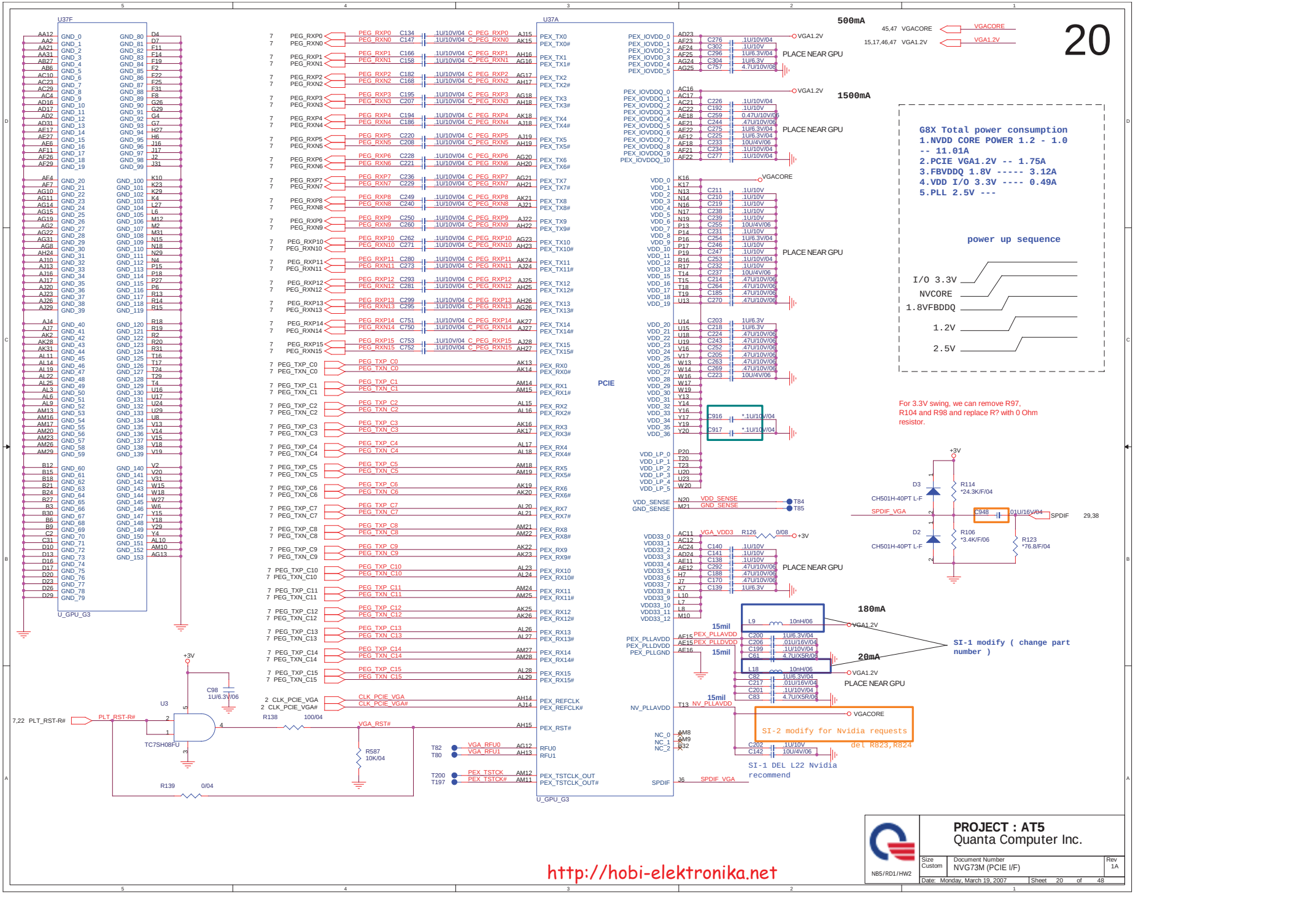
20
500mA
1500mA
180mA
20mA
U37F
U37A
U_GPU_G3
PCIE
PLACE NEAR GPU
VGA1.2V
VGACORE
G8X Total power consumption
1.NVDD CORE POWER 1.2 - 1.0 -- 11.01A
2.PCIE VGA1.2V -- 1.75A
3.FBVDDQ 1.8V ----- 3.12A
4.VDD I/O 3.3V ---- 0.49A
5.PLL 2.5V ---
power up sequence
I/O 3.3V
NVCORE
1.8VFBDDQ
1.2V
2.5V
For 3.3V swing, we can remove R97, R104 and R98 and replace R? with 0 Ohm resistor.
SI-1 modify (change part number)
SI-2 modify for Nvidia requests
del R823,R824
SI-1 DEL L22 Nvidia recommend
U3
TC7SH08FU
PLT_RST-R#
VGA_RST#
http://hobi-elektronika.net
PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number NVG73M (PCIE I/F)
Rev 1A
Date: Monday, March 19, 2007
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RTC

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF

Place near to Mini-door

VCCRTC, 3VPCU, D41 CH500H-40, D42 CH500H-40, C804 1U/16V/06, R638 20K/06, R635 1K/06, R637 1M/F/06, C811 1U/16V/06, G2 *SHORT_PAD1

C820 15P/50V/04, C817 15P/50V/04, Y6 32.768KHZ, R663 10M/06, CLK_32KX1, CLK_32KX2

BT1 BAT_CONN, CN30 *CWY020-B0G1Z

SI-2-1 modified (change to battery con)

5VPCU, 20MIL, 20MIL, R625 *1.2K/06, R628 *1K/06, Q42 *MMBT3904, R626 *4.7K/06, R629 *15K/06

add RTC Bat rechargeable circuit

U42A

RTCX1, RTCX2, RTCRST#, INTRUDER#, INTVRMEN, LAN100_SLP, GLAN_CLK, LAN_RSTSYNC, LAN_RXD0, LAN_RXD1, LAN_RXD2, LAN_TXD0, LAN_TXD1, LAN_TXD2, GLAN_DOCK#/GPIO13, GLAN_COMPI, GLAN_COMPO, HDA_BIT_CLK, HDA_SYNC, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDOUT, HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO34, SATALED#, SATA0RXN, SATA0RXP, SATA0TXN, SATA0TXP, SATA1RXN, SATA1RXP, SATA1TXN, SATA1TXP, SATA2RXN, SATA2RXP, SATA2TXN, SATA2TXP, SATA_CLKN, SATA_CLKP, SATARBIAS#, SATARBIAS

RTC, LPC, LAN / GLAN, CPU, IHDA, SATA, IDE

FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, FWH4/LFRAME#, LDRQ0#, LDRQ1#/GPIO23, A20GATE, A20M#, DPRSTP#, DPSLP#, FERR#, CPUPWRGD/GPIO49, IGNNE#, INIT#, INTR, RCIN#, NMI, SMI#, STPCLK#, THRMTRIP#, TP8

DD0–DD15, DA0–DA2, DCS1#, DCS3#, DIOR#, DIOW#, DDACK#, IDEIRQ, IORDY, DDREQ

ICH8M REV 1.0

SI-1 modified

CKL:1n ~ 20nF

Place within 500 mils of ICH7

25mils/15mils

SI-2 add for fix ESD issue

Should be 2" close ICH7

*SFI0603-050E101NP/06

intel check list define to stuff 33ohm

SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

R443 332K/F/06, R417 *0, R444 332K/F/06, R414 *0, R644 *1K/06, R428 *1K

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M HOST(1/4)	1A

NB5/RD1/HW2

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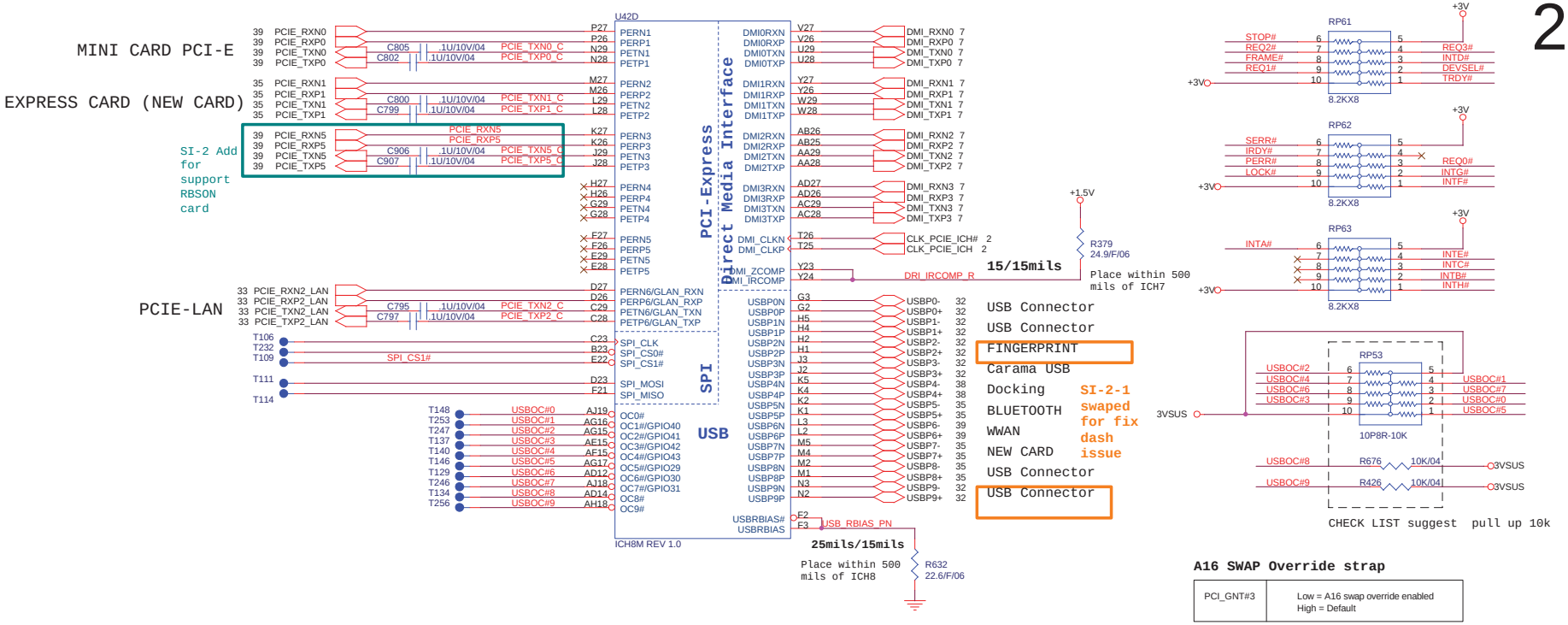
MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

SI-2 Add for support RBSON card

PCIE-LAN



A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

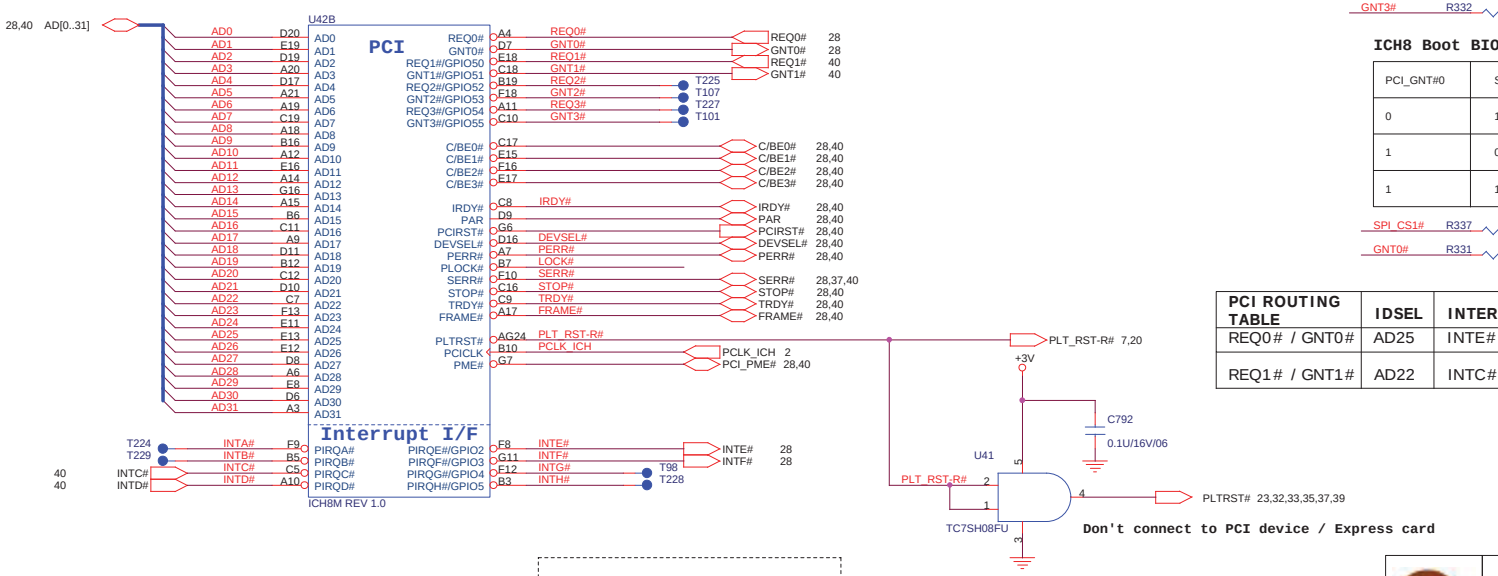
GNT3# R332 *1K

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R337 *1K

GNT0# R331 *1K



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PCLK_ICH R328 *0 C484 *33P/50V

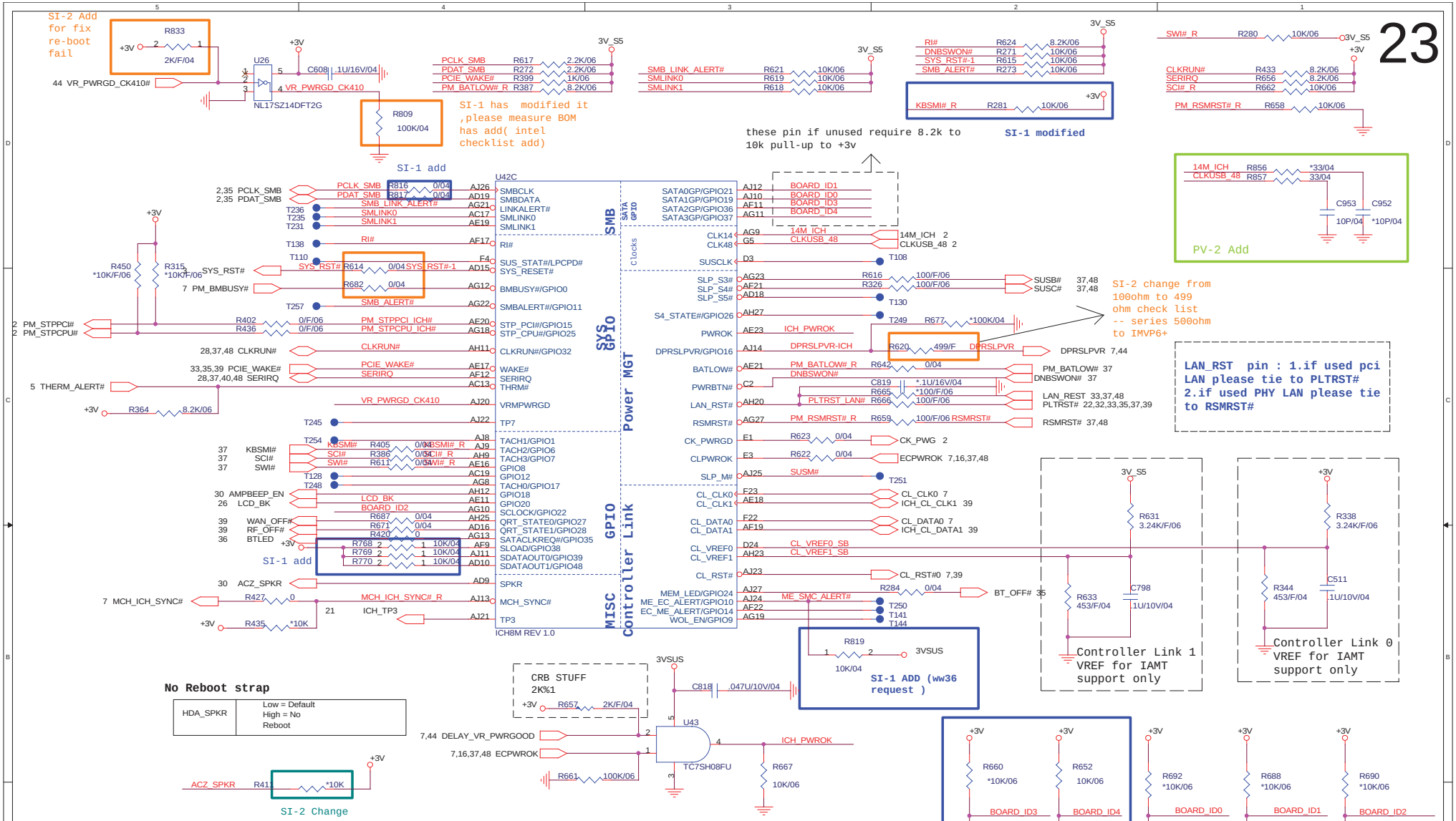
for EMI request

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M M PCI E(2/4)	1A

NB5/RD1/HW2

Date: Monday, March 19, 2007 Sheet 22 of 48



Board ID	15 " PAV UMA 965GM (0:0:0)	15" PRE UMA 965GM (0:0:1)	15″PAV Discrete 965PM+G86MV+128M (0:1:0)	17″ PAV Discrete 965PM+G86MV+128M (0:1:1)	17″ PAV Discrete 965PM+G84MV+256M (1:0:0)	17″ PAV UMA 965GM (1:0:1)
ID0	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff
ID1	R448 Stuff	R448 Stuff	R688 Stuff	R688 Stuff	R448 Stuff	R448 Stuff
ID2	R689 Stuff	R689 Stuff	R689 Stuff	R689 Stuff	R690 Stuff	R690 Stuff

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M GPIO(3/4)	1A

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NB5/RD1/HW2

1.5V_A 1.5A
1.5V_B 675mA
VCC1.05 1.13A

V5REF 1mA
V5REF_SUS 1mA
VCCSATAPLL 47mA
VCCUSBPLL 10mA
VCCGLAN3.3 1mA
VCCGLLAN_PLL --23mA
VCCGLAN1.5 80mA
VCCGLAN3.3 18mA
VCCDMIPLL 23mA
VCC_DMI 50mA
VCPU_IO 1mA
VCC3.3 278mA
VCCHDA 32mA
VCC_SUSHDA 32mA
VCC_SUS3.3 177mA
VCCL3.3 18mA - 64mA (S3)

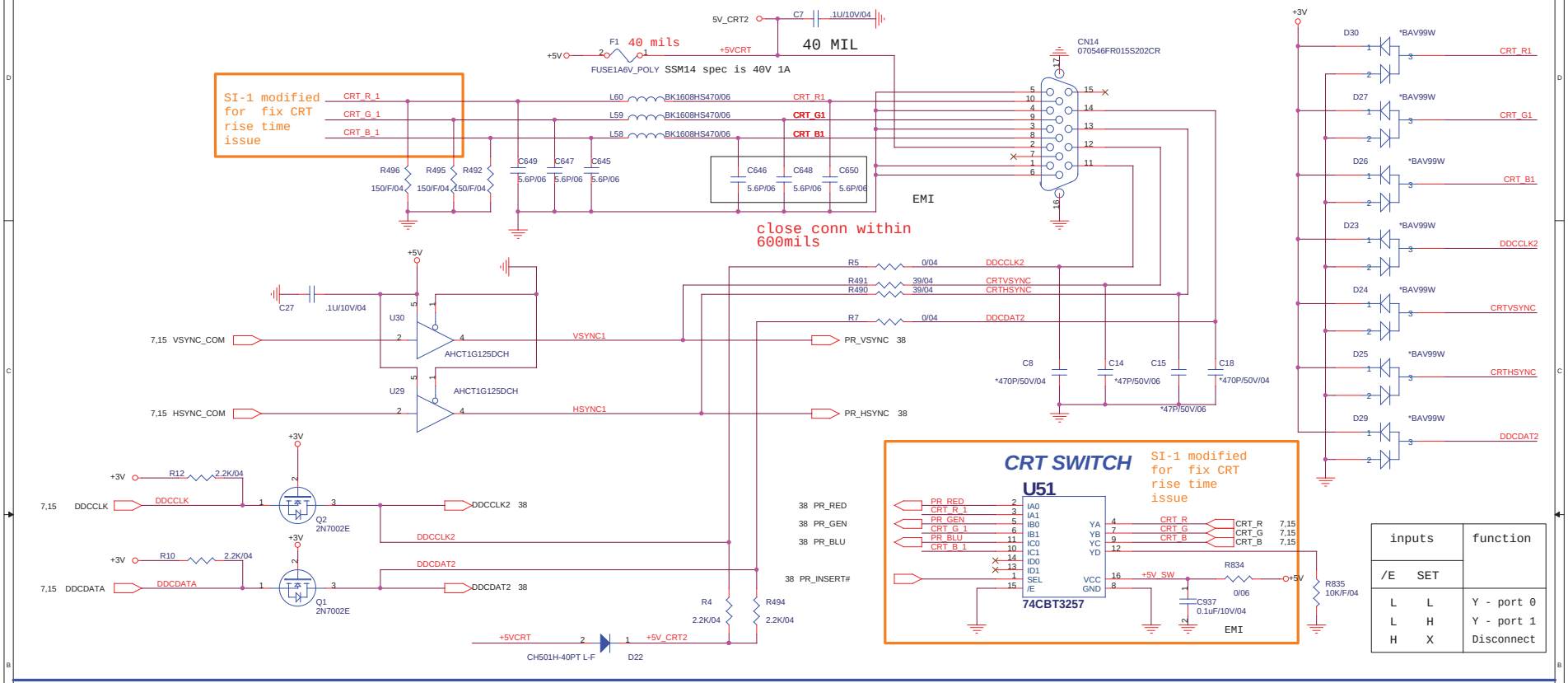
SI-2 modified (remove R374)

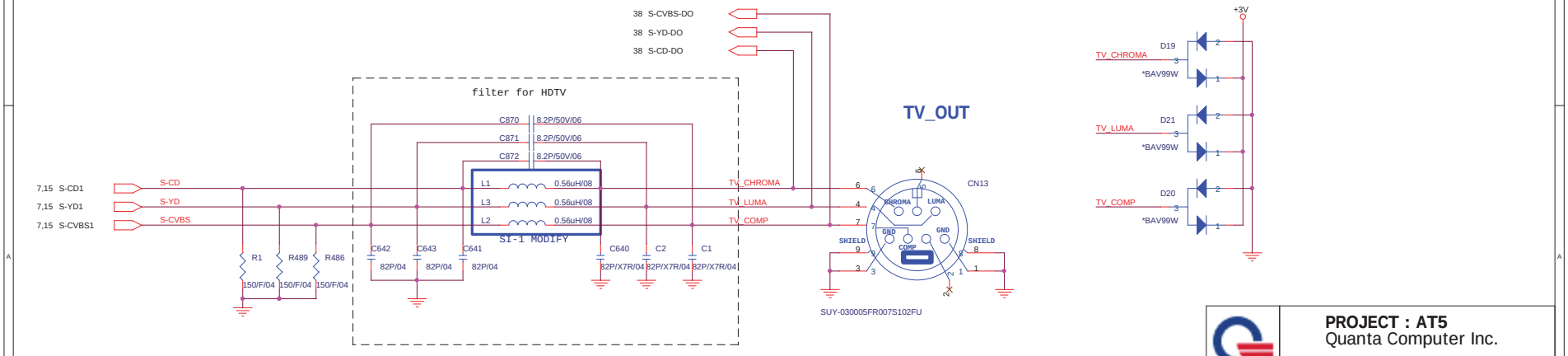
Can be connect to +3V_S5 or +1.5V_S5

Can be connect to +3V or +1.5V

PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size: Custom
Document Number: ICH7-M POWER(4/4)
Rev: 1A
Date: Monday, March 19, 2007
Sheet 24 of 48

CRT PORT





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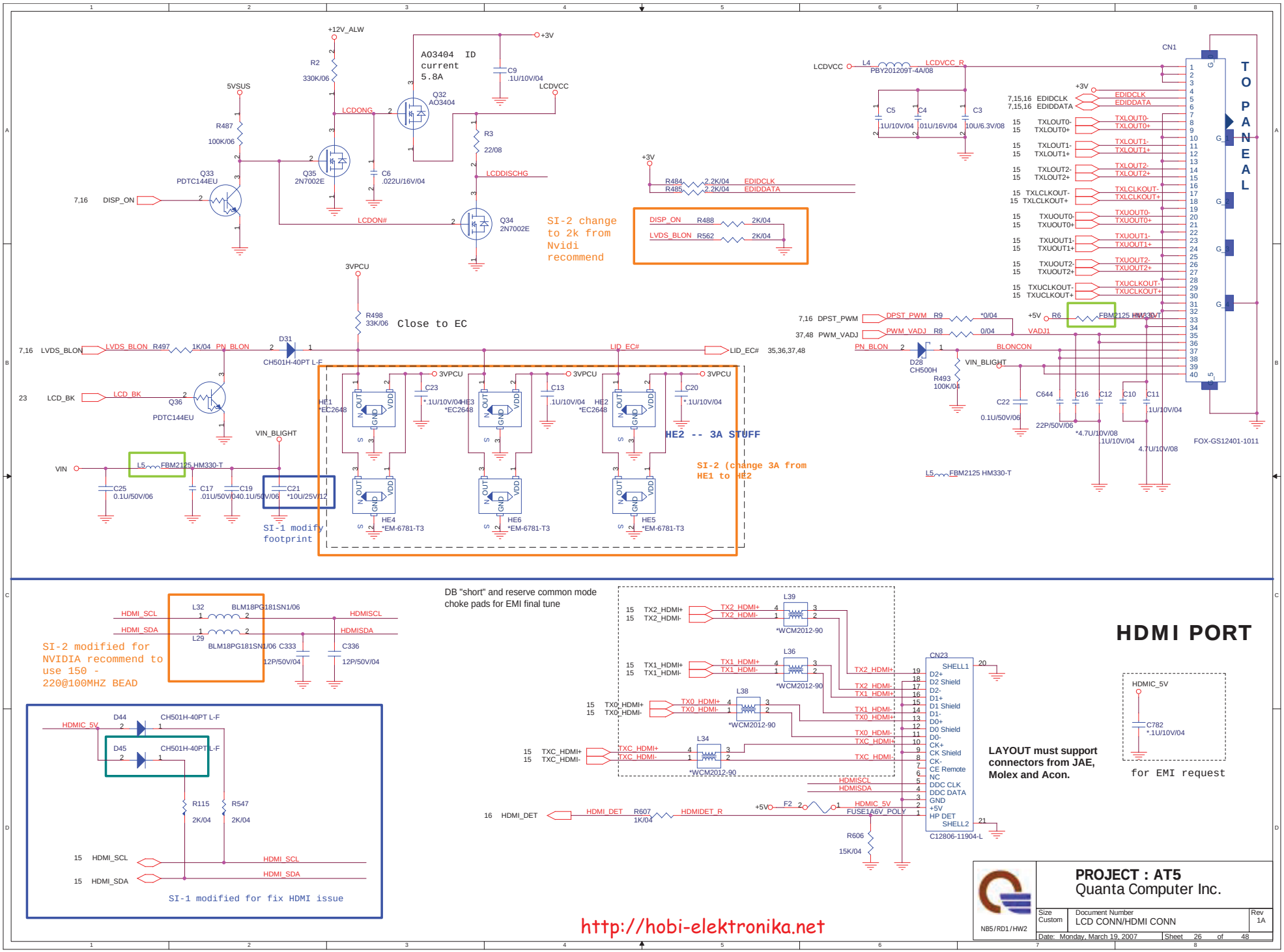
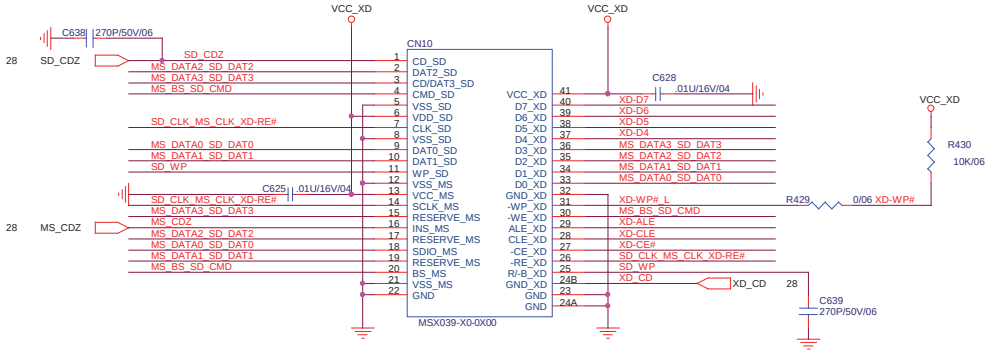
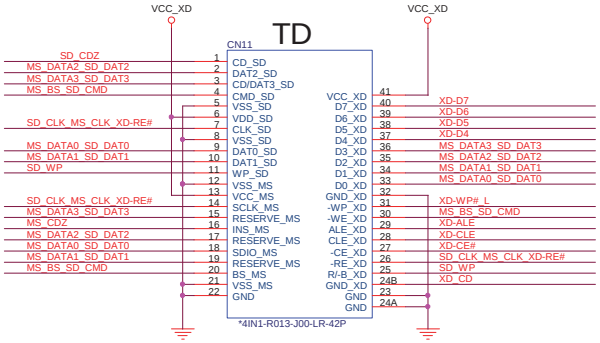
NB5/RD1/HW2	**PROJECT : AT5** Quanta Computer Inc.
Size: Custom	Document Number: CRT/TV_OUT — Rev: 1A
Date: Monday, March 19, 2007	Sheet 25 of 48


+12V_ALW
R2
330K/06
AO3404 ID current 5.8A
+3V
C9 .1U/10V/04
LCDVCC
5VSUS
R487
100K/06
LCDONG
Q32 AO3404
R3
22/08
LCDDISCHG
Q33 PDTC144EU
7,16 DISP_ON
Q35 2N7002E
C6 .022U/16V/04
LCDON#
Q34 2N7002E
SI-2 change to 2k from Nvidi recommend
+3V
R484 2.2K/04 EDIDCLK
R485 2.2K/04 EDIDDATA
DISP_ON R488 2K/04
LVDS_BLON R562 2K/04
LCDVCC
L4 PBY201209T-4A/08
LCDVCC_R
C5 1U/10V/04
C4 .01U/16V/04
C3 10U/6.3V/08
CN1
TO PANEAL
7,15,16 EDIDCLK
7,15,16 EDIDDATA
15 TXLOUT0-
15 TXLOUT0+
15 TXLOUT1-
15 TXLOUT1+
15 TXLOUT2-
15 TXLOUT2+
15 TXLCLKOUT-
15 TXLCLKOUT+
15 TXUOUT0-
15 TXUOUT0+
15 TXUOUT1-
15 TXUOUT1+
15 TXUOUT2-
15 TXUOUT2+
15 TXUCLKOUT-
15 TXUCLKOUT+
FOX-GS12401-1011
3VPCU
R498 33K/06
Close to EC
7,16 LVDS_BLON
LVDS_BLON R497 1K/04 PN_BLON
D31 CH501H-40PT L-F
LID_EC#
LID_EC# 35,36,37,48
23 LCD_BK
LCD_BK
Q36 PDTC144EU
VIN_BLIGHT
VIN
L5 FBM2125 HM330-T
C25 0.1U/50V/06
C17 .01U/50V/04
C19 .1U/50V/06
C21 *10U/25V/12
HE1 *EC2648
HE3 *EC2648
HE2 *EC2648
HE4 *EM-6781-T3
HE6 *EM-6781-T3
HE5 *EM-6781-T3
C23 *.1U/10V/04
C13 .1U/10V/04
C20 *.1U/10V/04
HE2 -- 3A STUFF
SI-2 (change 3A from HE1 to HE2
SI-1 modify footprint
7,16 DPST_PWM
DPST_PWM R9 *0/04
37,48 PWM_VADJ
PWM_VADJ R8 0/04
+5V
R6 FBM2125 HM330-T
VADJ1
PN_BLON
D28 CH500H
BLONCON
R493 100K/04
C22 0.1U/50V/06
C644 22P/50V/06
C16 *4.7U/10V/08
C12 .1U/10V/04
C10
C11 4.7U/10V/08
L5 FBM2125 HM330-T
HDMI_SCL
HDMI_SDA
L32 BLM18PG181SN1/06
L29 BLM18PG181SN1/06
C333 12P/50V/04
C336 12P/50V/04
HDMISCL
HDMISDA
SI-2 modified for NVIDIA recommend to use 150 - 220@100MHZ BEAD
DB "short" and reserve common mode choke pads for EMI final tune
L39
L36
L38
L34
*WCM2012-90
15 TX2_HDMI+
15 TX2_HDMI-
15 TX1_HDMI+
15 TX1_HDMI-
15 TX0_HDMI+
15 TX0_HDMI-
15 TXC_HDMI+
15 TXC_HDMI-
CN23
SHELL1
SHELL2
C12806-11904-L
D2+
D2 Shield
D2-
D1+
D1 Shield
D1-
D0+
D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
HDMIC_5V
C782 *.1U/10V/04
for EMI request
HDMI PORT
LAYOUT must support connectors from JAE, Molex and Acon.
D44 CH501H-40PT L-F
D45 CH501H-40PT L-F
R115 2K/04
R547 2K/04
15 HDMI_SCL
15 HDMI_SDA
SI-1 modified for fix HDMI issue
16 HDMI_DET
R607 1K/04
HDMIDET_R
+5V
F2 FUSE1A6V_POLY
R606 15K/04
http://hobi-elektronika.net
NB5/RD1/HW2
PROJECT : AT5
Quanta Computer Inc.
Size Custom
Document Number LCD CONN/HDMI CONN
Rev 1A
Date: Monday, March 19, 2007
Sheet 26 of 48

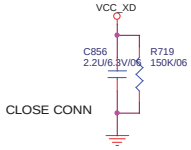
5 IN1 CARD READER
XD,MMC/SD,MS/MSP

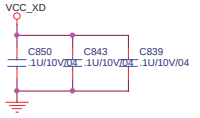


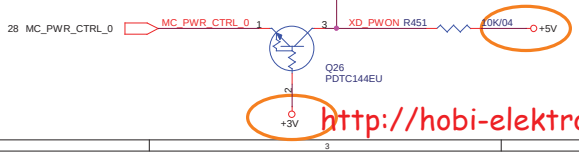
TD

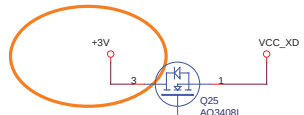


bom create 2'nd source

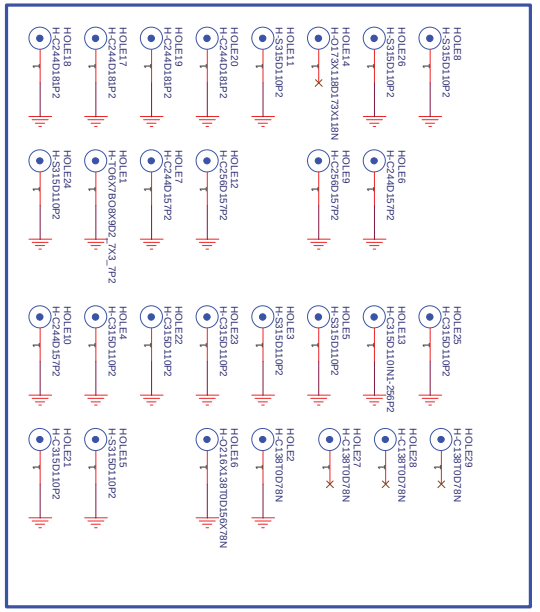




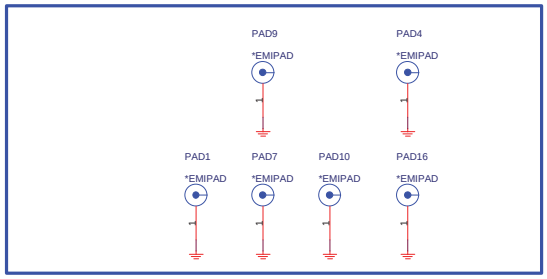




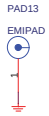
SCREW HOLE



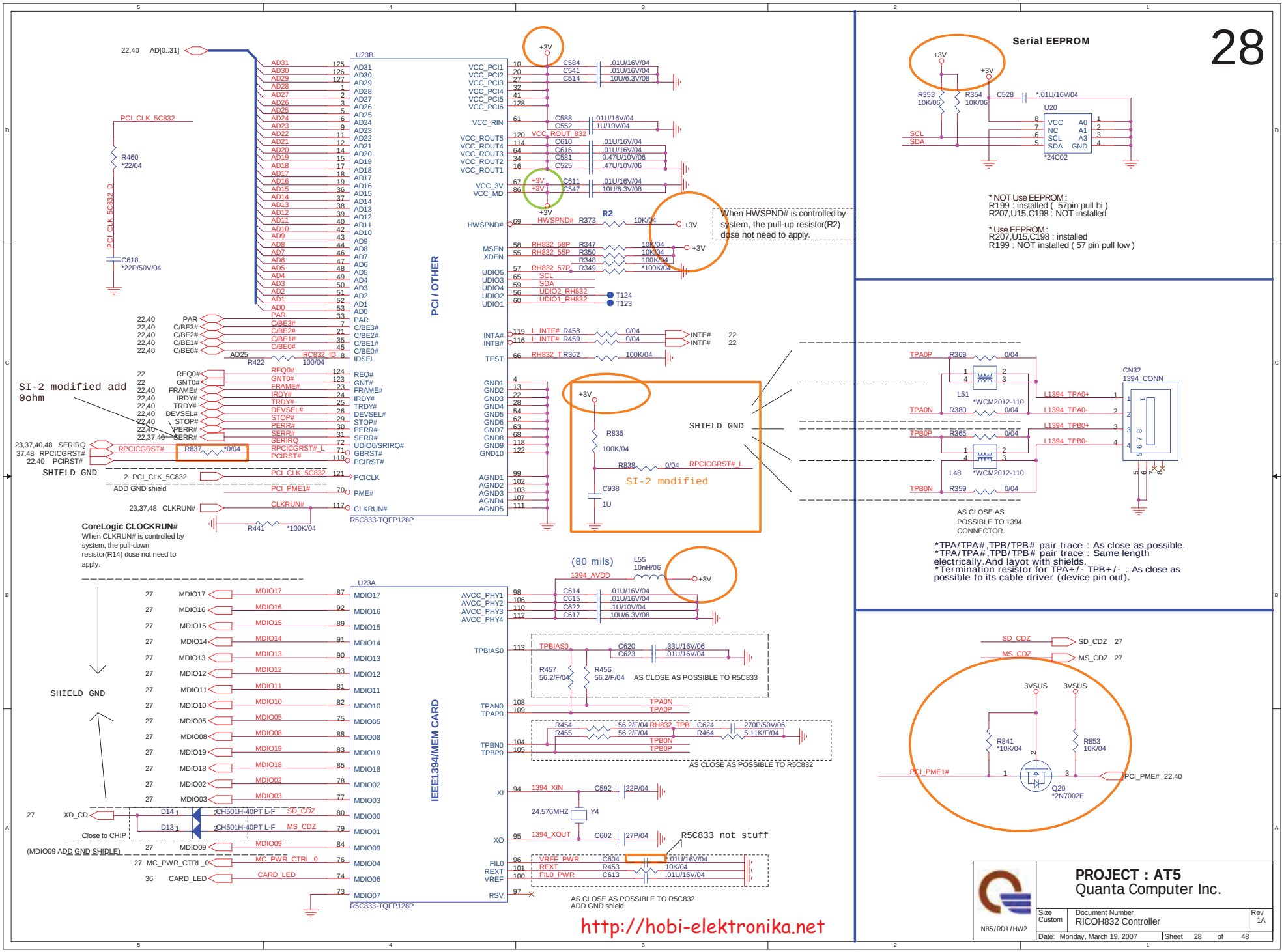
EMI PAD



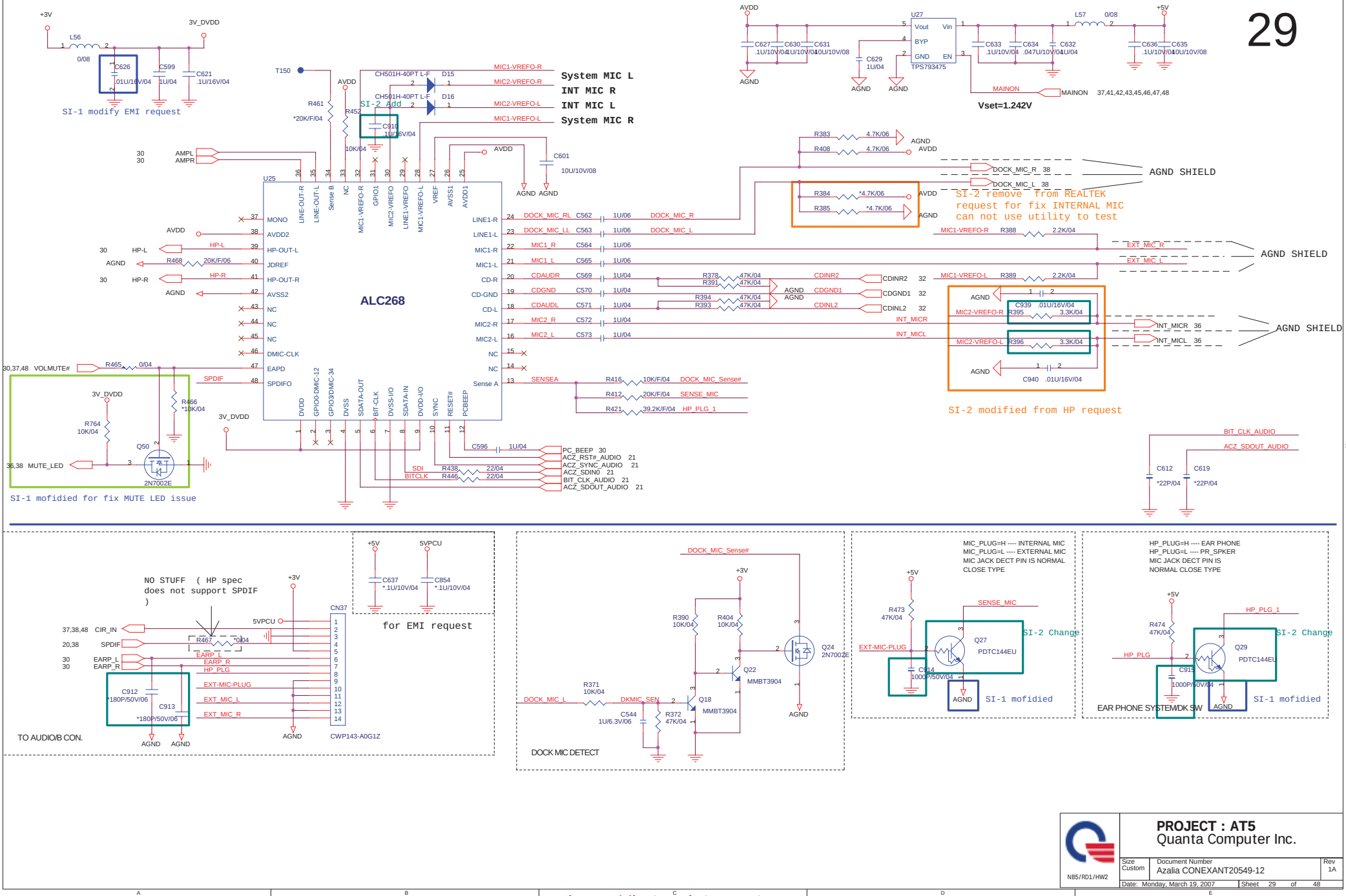
moden cable sprig



NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.		
	Size: Custom	Document Number: CARD READER/HOLE	Rev: 1A
	Date: Monday, March 19, 2007	Sheet 27 of 48	



PROJECT :	AT5
	Quanta Computer Inc.
Size	Custom
Document Number	RICOH832 Controller
Rev	1A
NB5/RD1/HW2	
Date:	Monday, March 19, 2007
Sheet	28 of 48



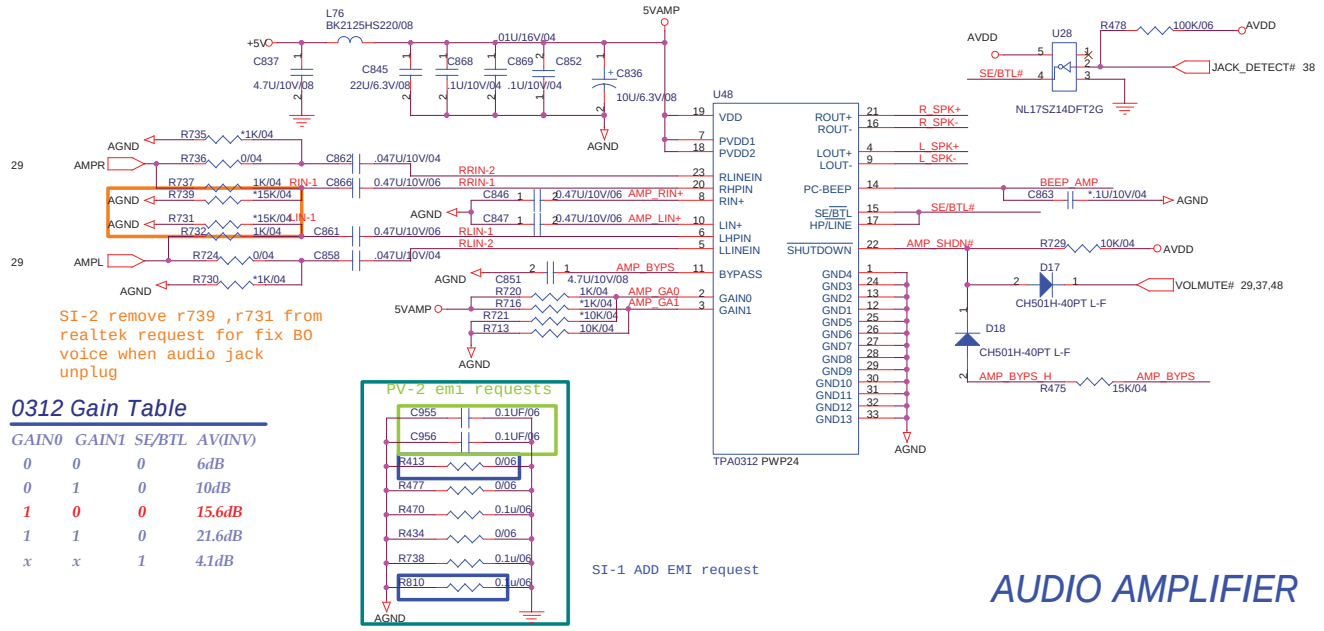
PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia CONEXANT20549-12	1A

N85/RD1/HW2

Date: Monday, March 19, 2007 Sheet 29 of 48

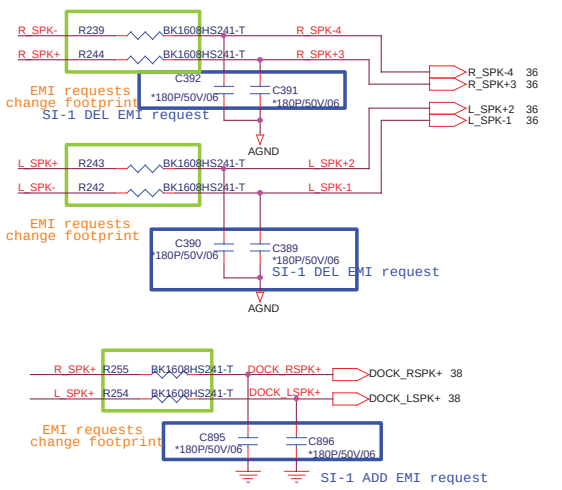
AUDIO AMPLIFIER



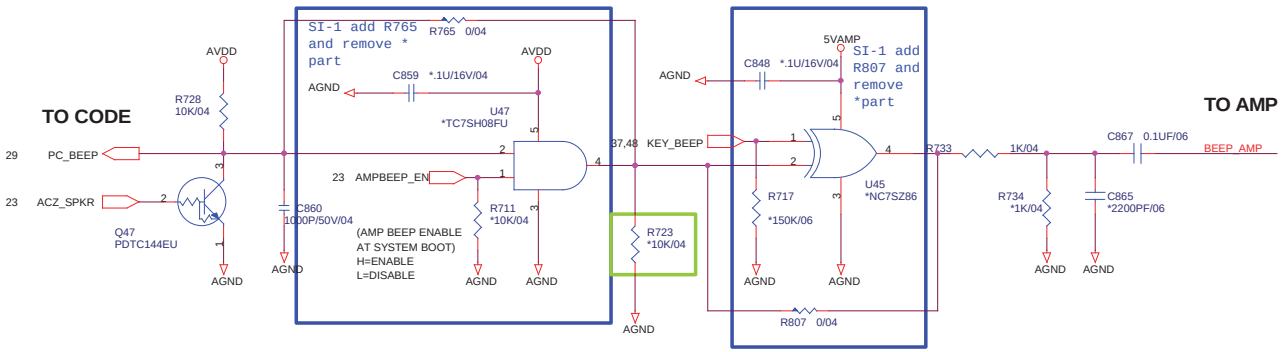
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	**0**	**0**	**15.6dB**
1	1	0	21.6dB
x	x	1	4.1dB

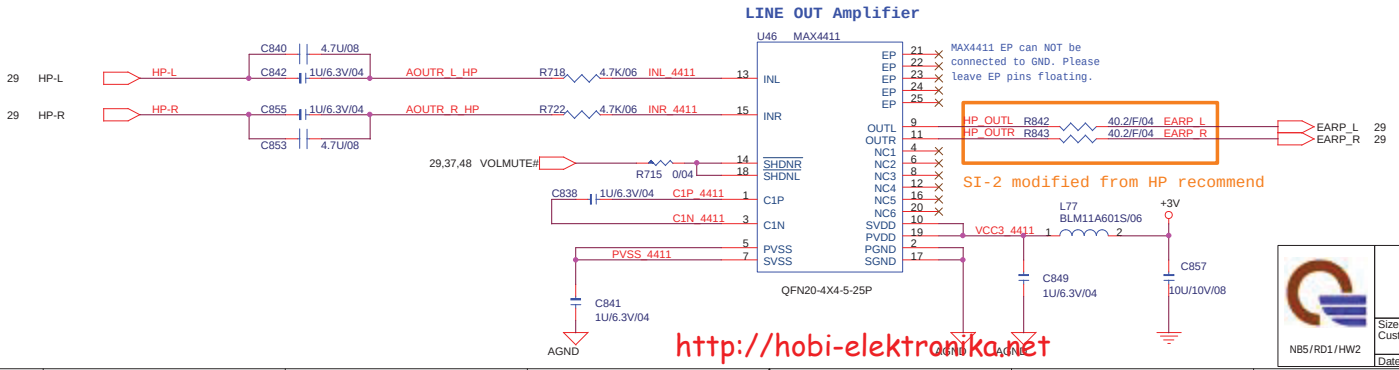
INT. SPEAKER



PCSPK BEEP



LINE OUT Amplifier

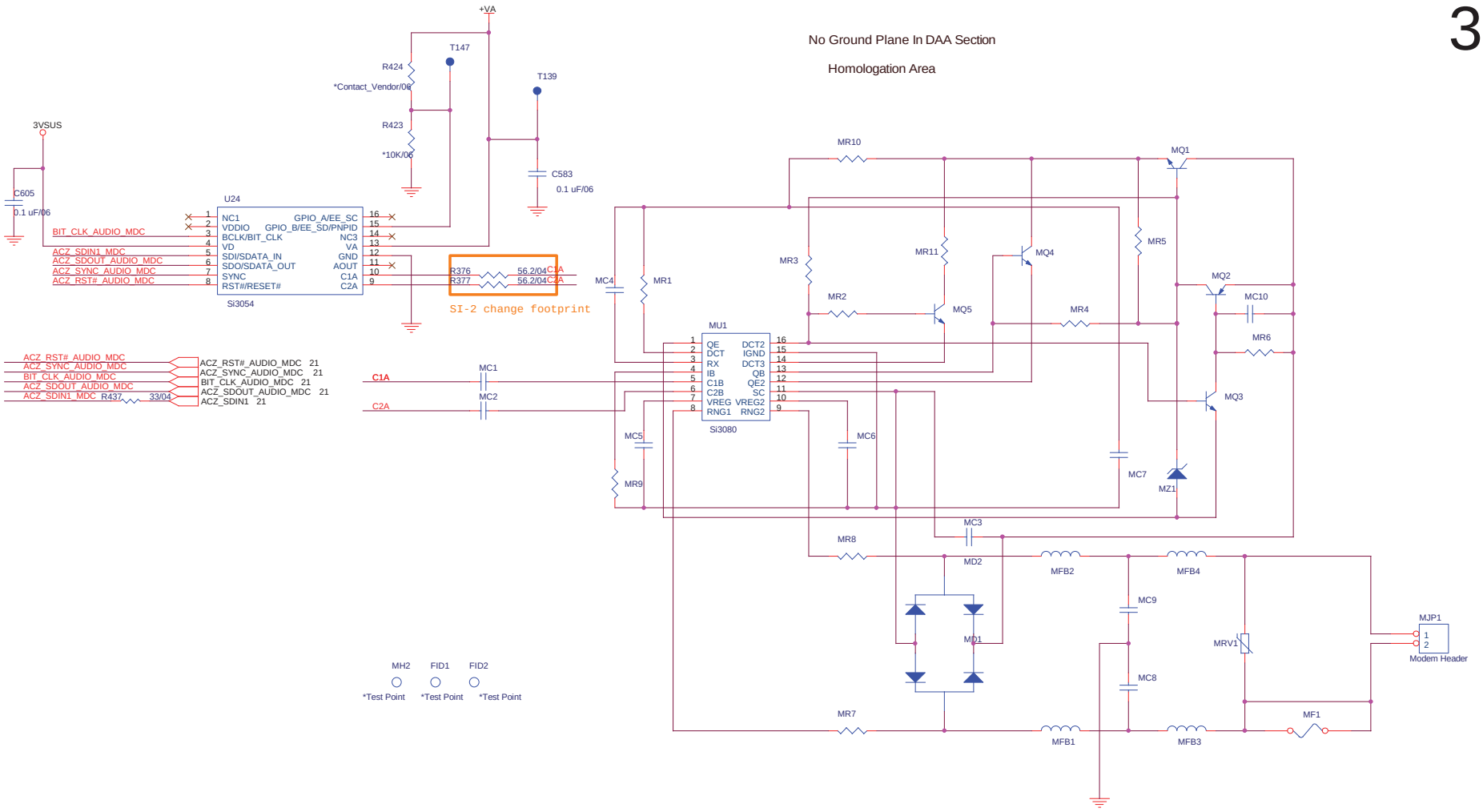


PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	JACK/AMP_TAP0312	1A

NB5/RD1/HW2

Date: Monday, March 19, 2007 Sheet 30 of 48



DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL

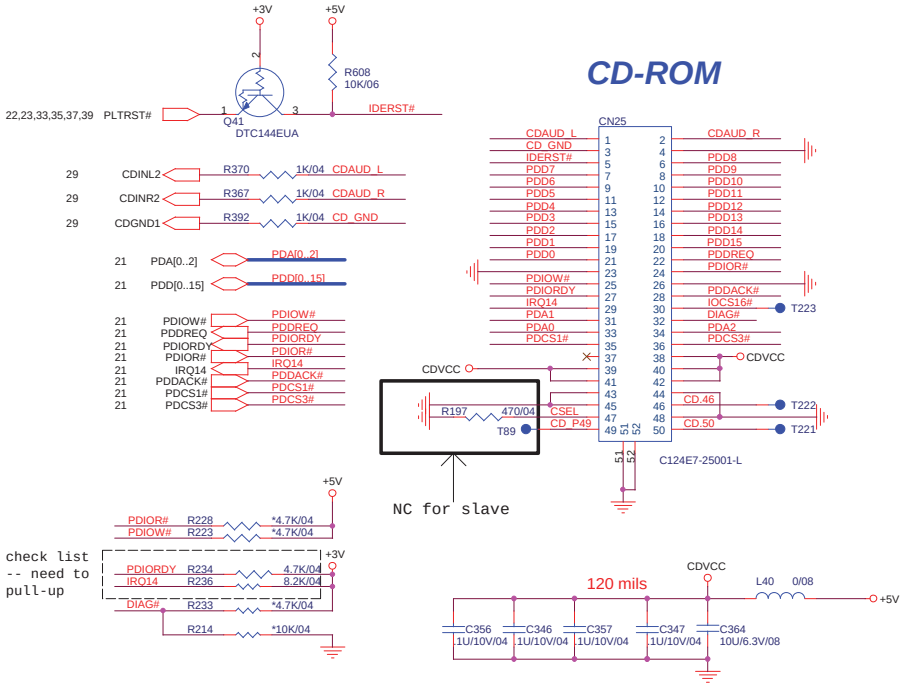
NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

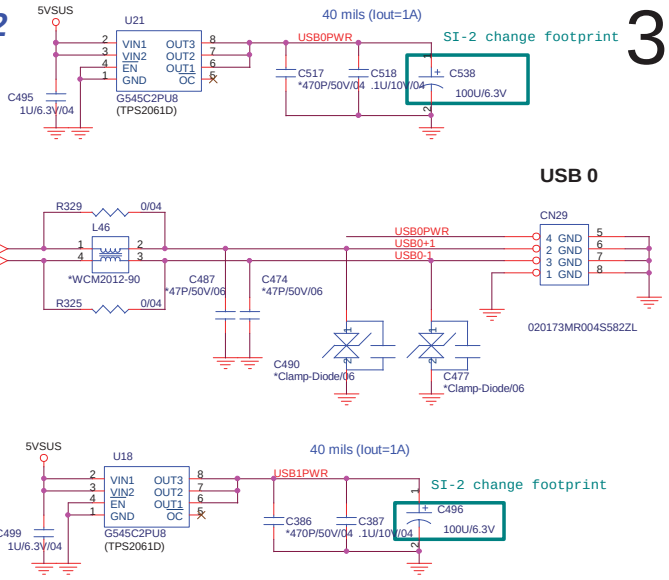
Size	Document Number	Rev
Custom	MODEM(DAA)	1A

Date: Monday, March 19, 2007 Sheet 31 of 48

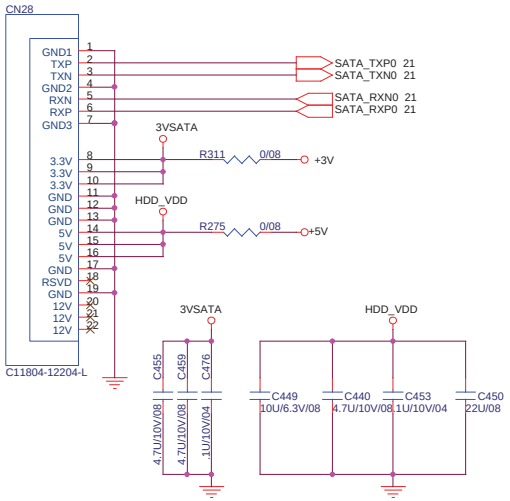
CD-ROM



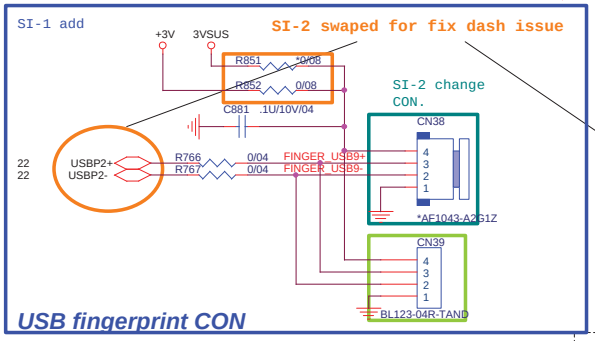
USBX2



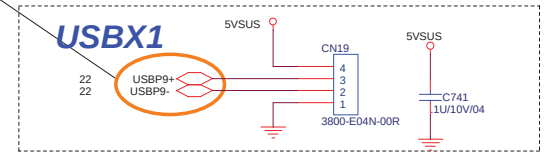
SATA_1 CONNECTOR



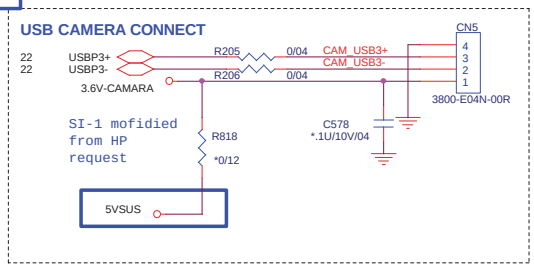
USB fingerprint CON

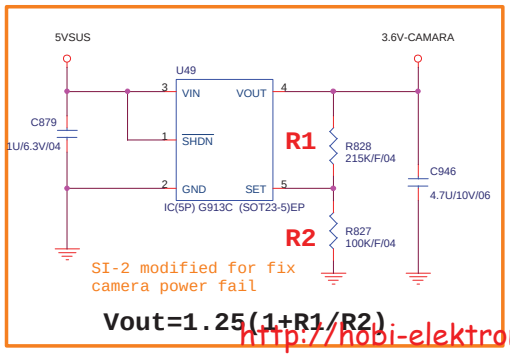


USBX1



USB CAMERA CONNECT





NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

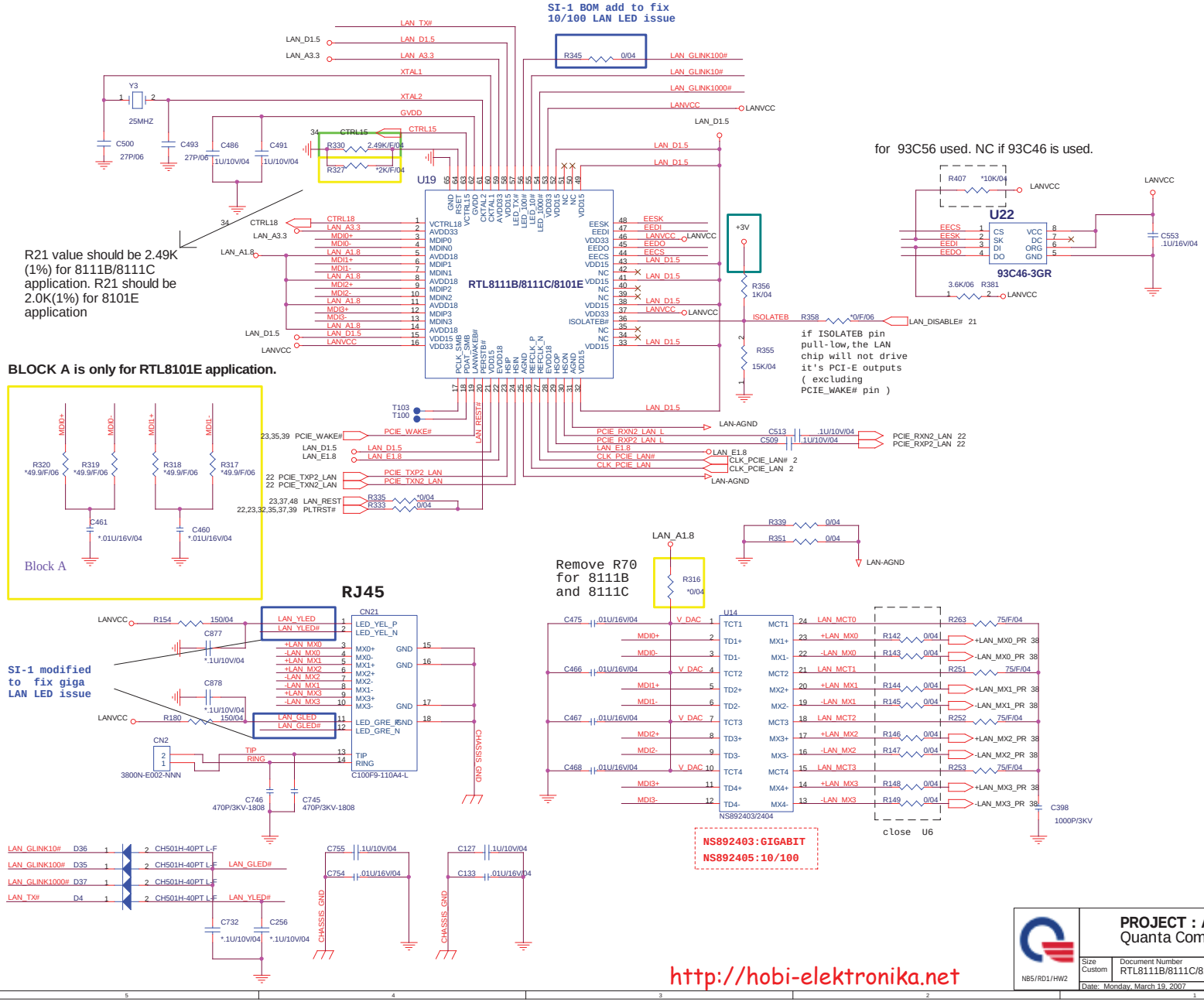
Size	Document Number	Rev
Custom	SATA HDD/CD-ROM/USBX3	1A
Date: Monday, March 19, 2007	Sheet 32 of 48	

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)

giga LAN part number AJ081110006

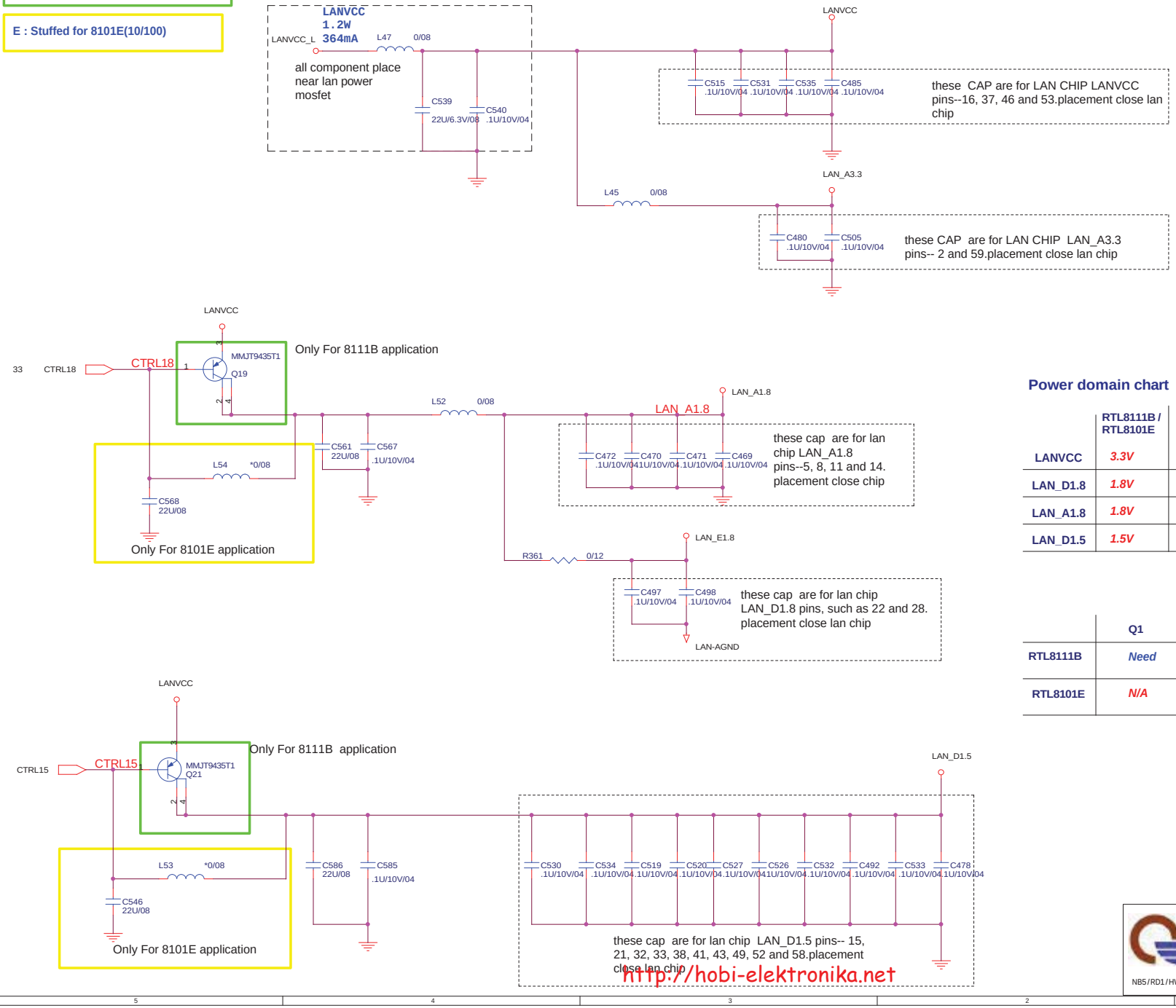
SI-1 BOM add to fix
10/100 LAN LED issue



PROJECT : AT5 Quanta Computer Inc.			
Size: Custom	Document Number: RTL8111B/8111C/8101E		Rev: 1A
NB5/RD1/HW2	Date: Monday, March 19, 2007	Sheet 33 of 48	

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B / RTL8101E
LANVCC	3.3V
LAN_D1.8	1.8V
LAN_A1.8	1.8V
LAN_D1.5	1.5V

	Q1	Q3
RTL8111B	Need	Need
RTL8101E	N/A	N/A

NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
A3	LAN POWER	1A

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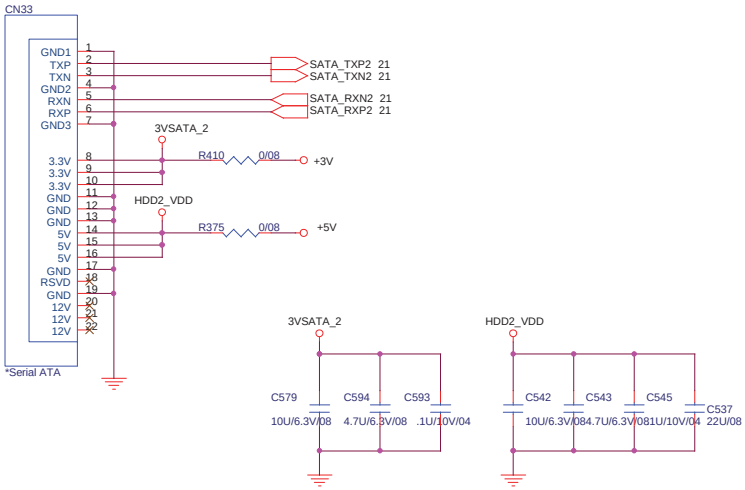
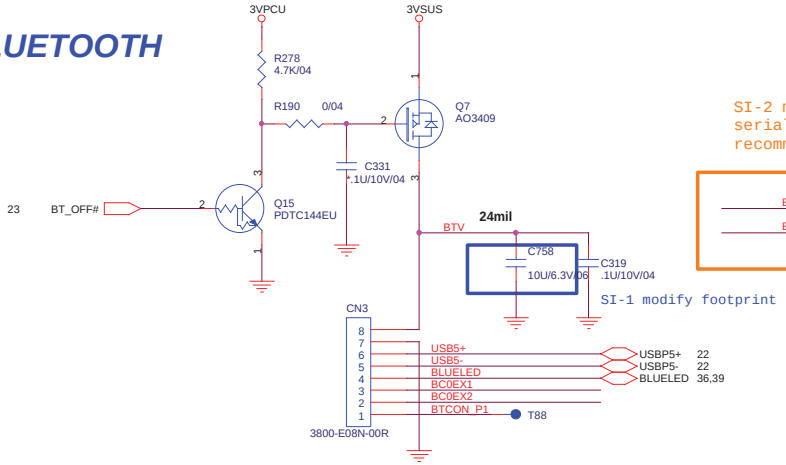
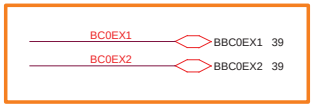
SATA_2 CONNECTOR
For 17"W Second HDD



BLUETOOTH

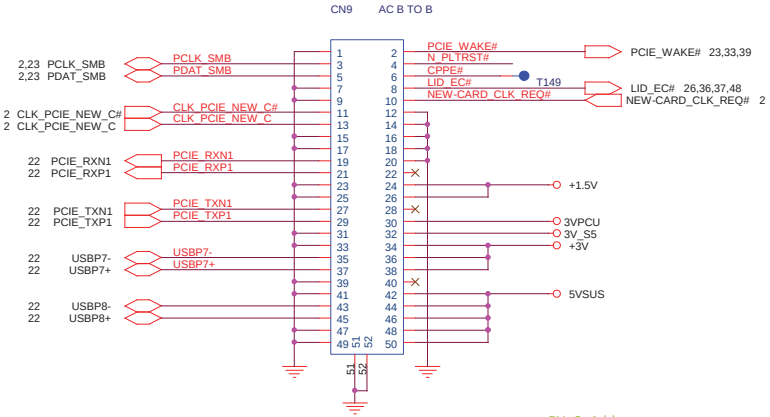


SI-2 modified (remove serial resistors) from HP recommend

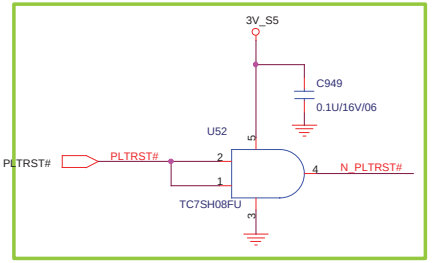


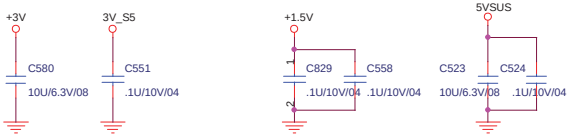
SI-1 modify footprint

NEWCARD



PV-2 Add



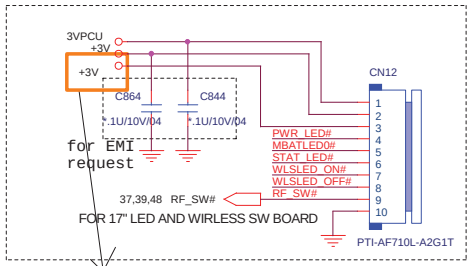


NB5/RD1/HW2

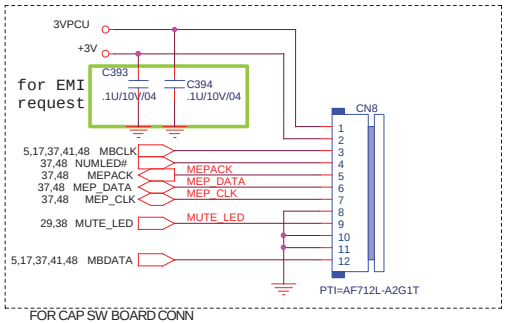
PROJECT : AT5
Quanta Computer Inc.

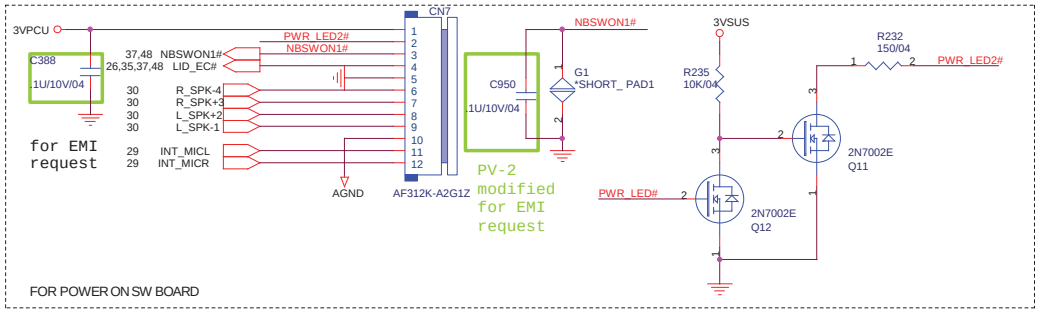
Size	Document Number	Rev
Custom	NEW CARD/BT	1A

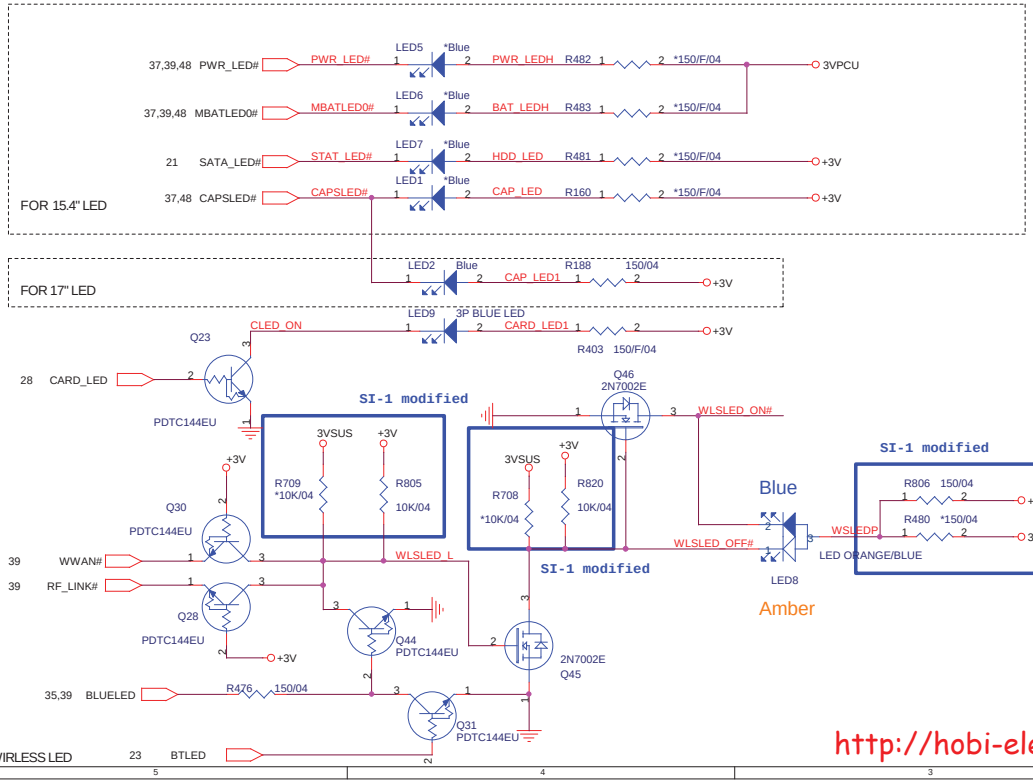
Date: Monday, March 19, 2007 Sheet 35 of 48

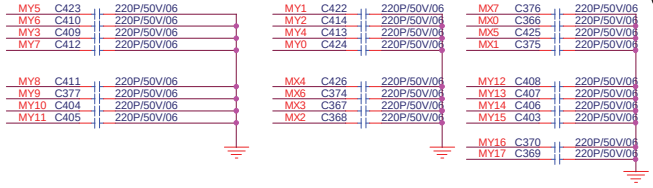


SI-2 modified for fix s3 not support wirless LED

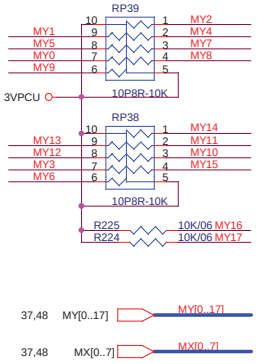


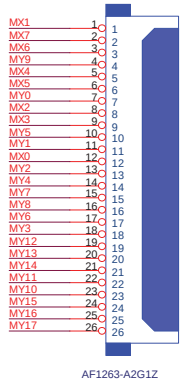


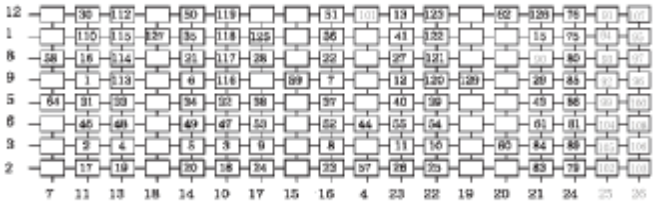




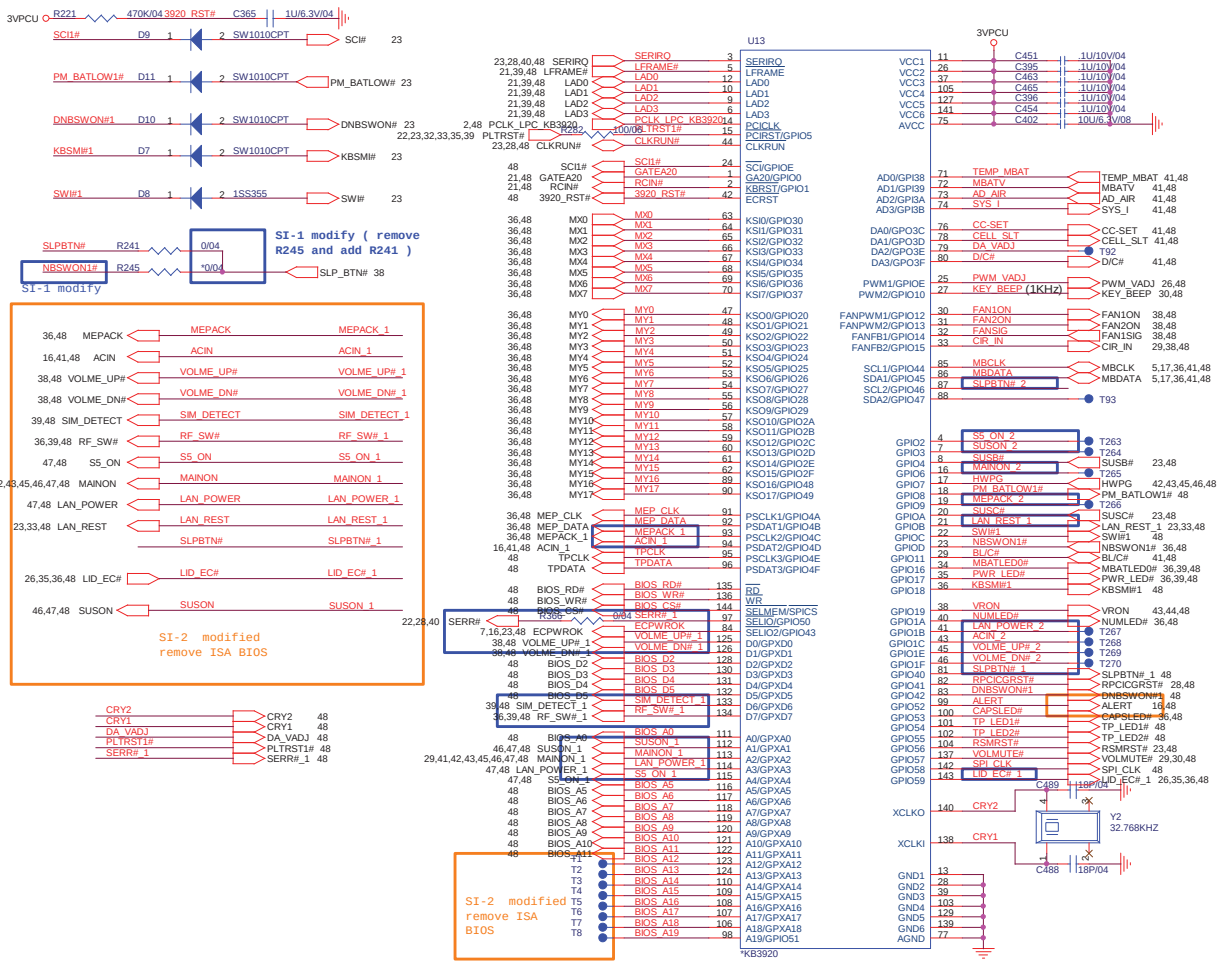
KEYBOARD PULL-UP







NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.		
	Size: Custom	Document Number: LED/KEYBOARD/SW	Rev: 1A
	Date: Monday, March 19, 2007	Sheet 36 of 48	



STRAP PIN

MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode

SI-1 DEL R209,R210,R218,R219,R220

MY2 R208 *10K/04

MY3 R212 *0/04

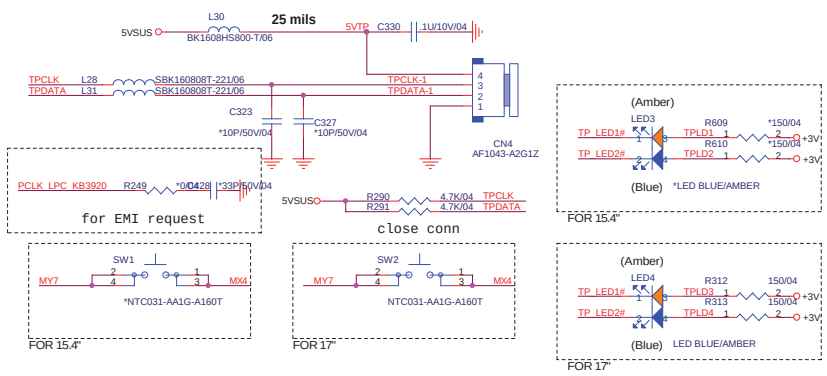
All hardware straps default internal pull-up, so don't need pull-UP outside. A TEST need try --andrew ????

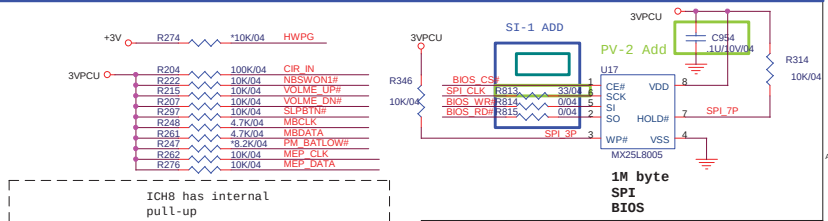
SELECT KBC TPYE

PIN NAME	USE KBC3920	USE KBC3926
MY2	R208	REMOVE R208
BIOS_A0	REMOVE R808	R808

SI-2 modified remove ISA BIOS

TOUCH PAD CONNECTOR





PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB3920/ROM/TP	1A

N85/RD1/HW2

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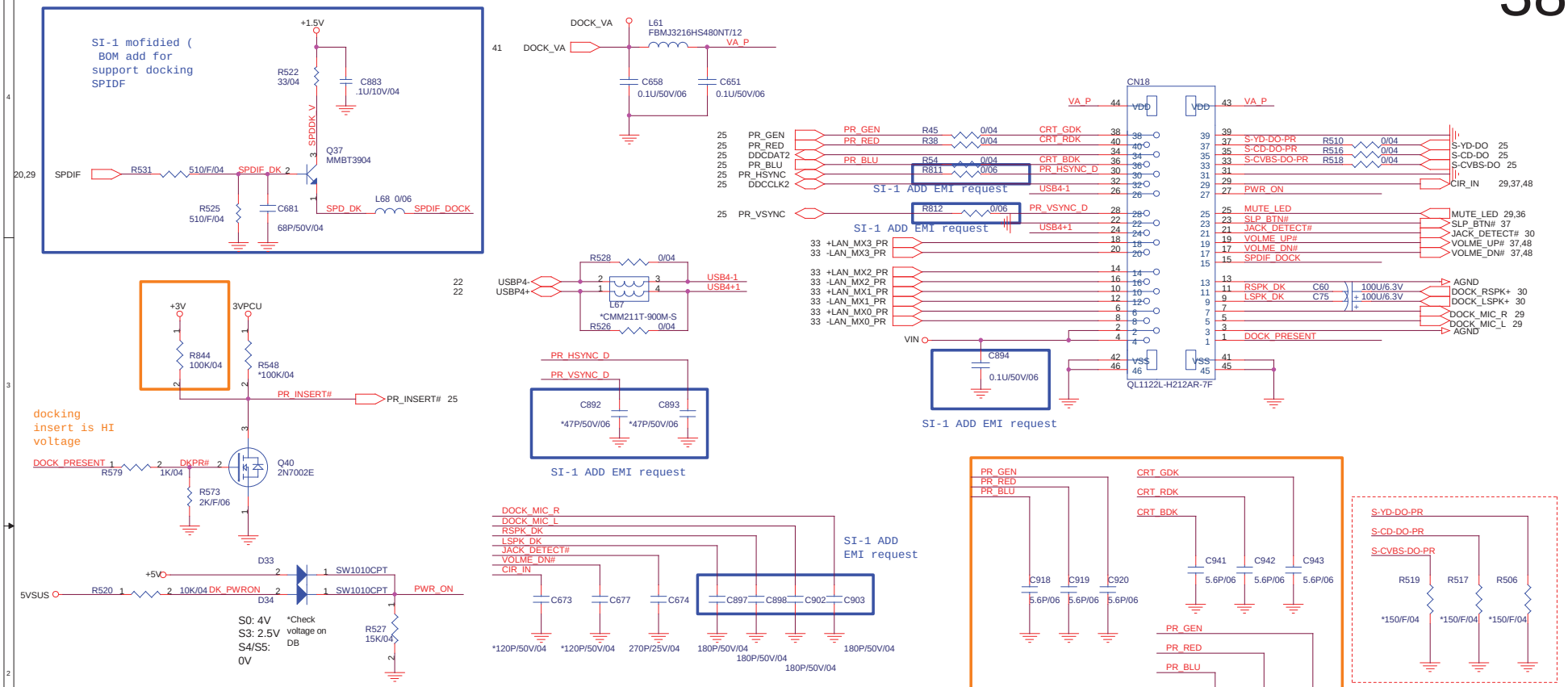
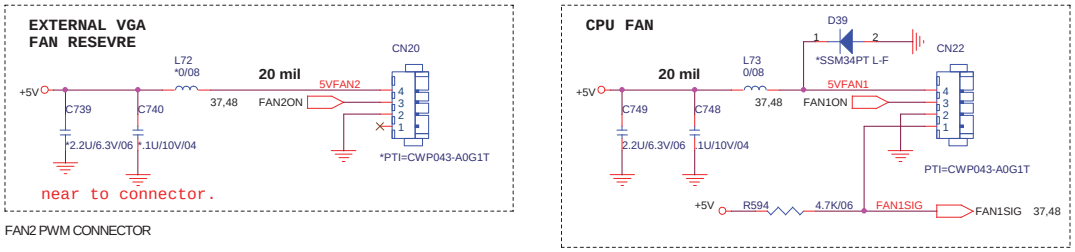
CABLE DOCK

support 6A 200mils
CX000480005



FAN

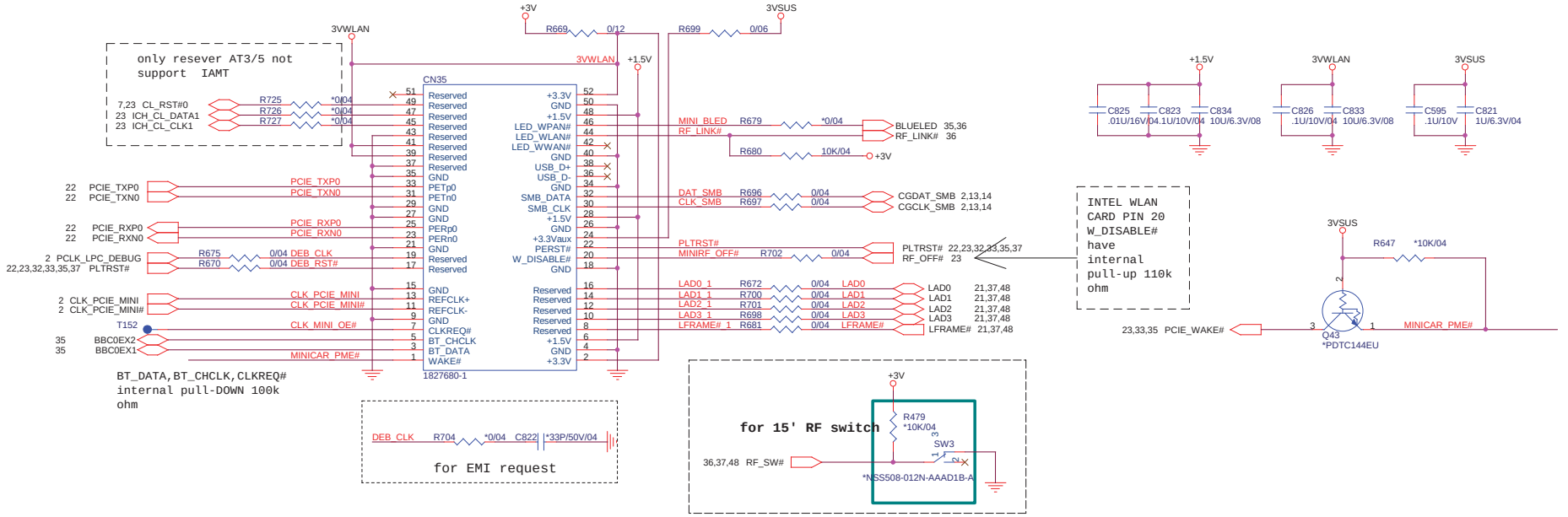


FAN2 PWM CONNECTOR

FAN1 PWM CONNECTOR

NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
Size: Custom	Document Number: CABLE DOCKING/FAN	Rev: 1A
Date: Monday, March 19, 2007	Sheet 38 of 48	

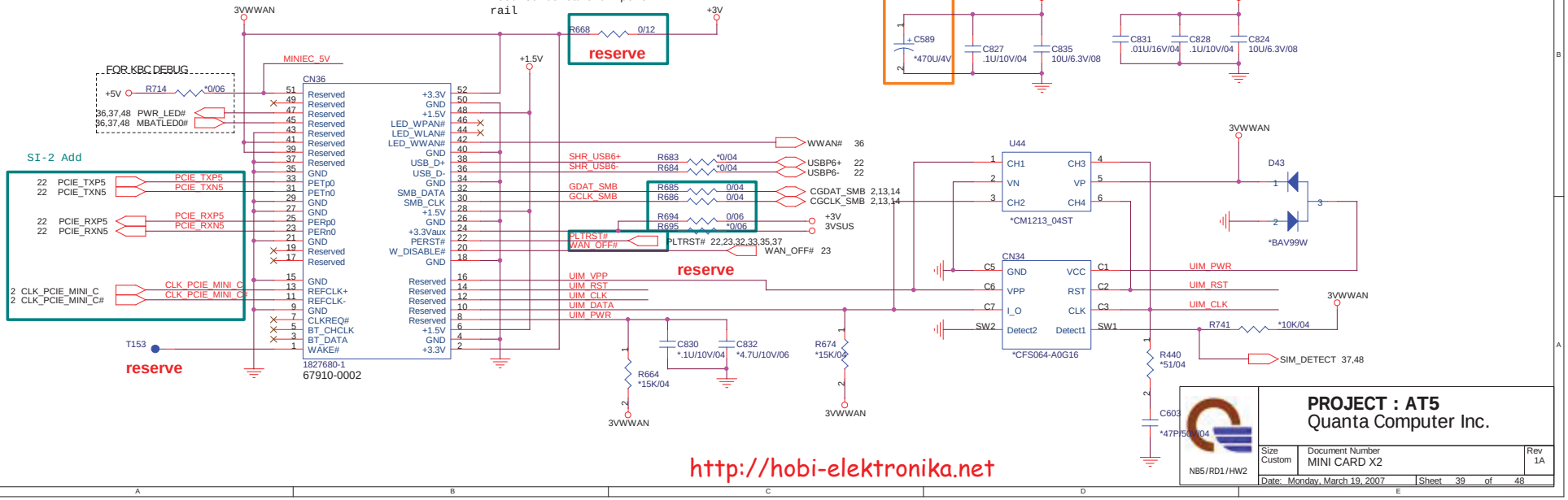
Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2
WWAN(W/SIM)

WWAN -- have 2.8A 7W power consumption
power pin 24.39.41
GND pin 37,43
need to be careful power rail

SI-2 modified (BOM remove C589)



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PROJECT : AT5
Quanta Computer Inc.

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Custom	MINI CARD X2	1A
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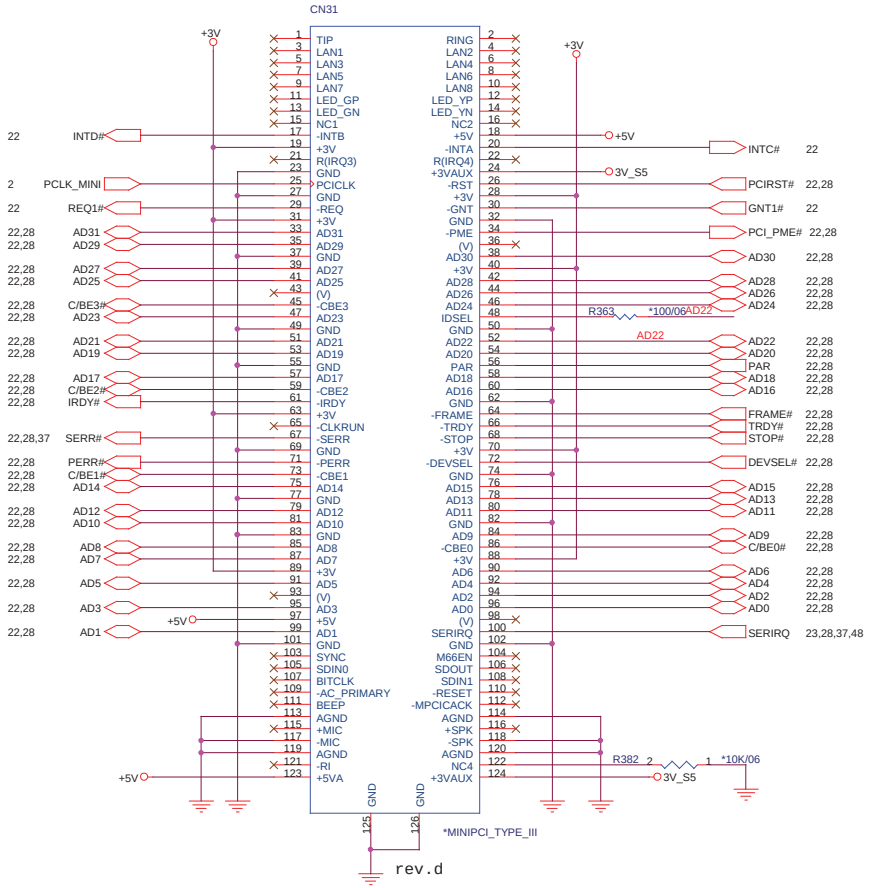
NB5/RD1/HW2

MINI PCI TYPE III SLOT

INTC#, INTD#
REQ1#/GNT1#
D_ID : AD22



NB5/RD1/HW2	**PROJECT : AT5** Quanta Computer Inc.		
	Size: Custom	Document Number: MINI PCI TYPE III SLOT	Rev: 1A
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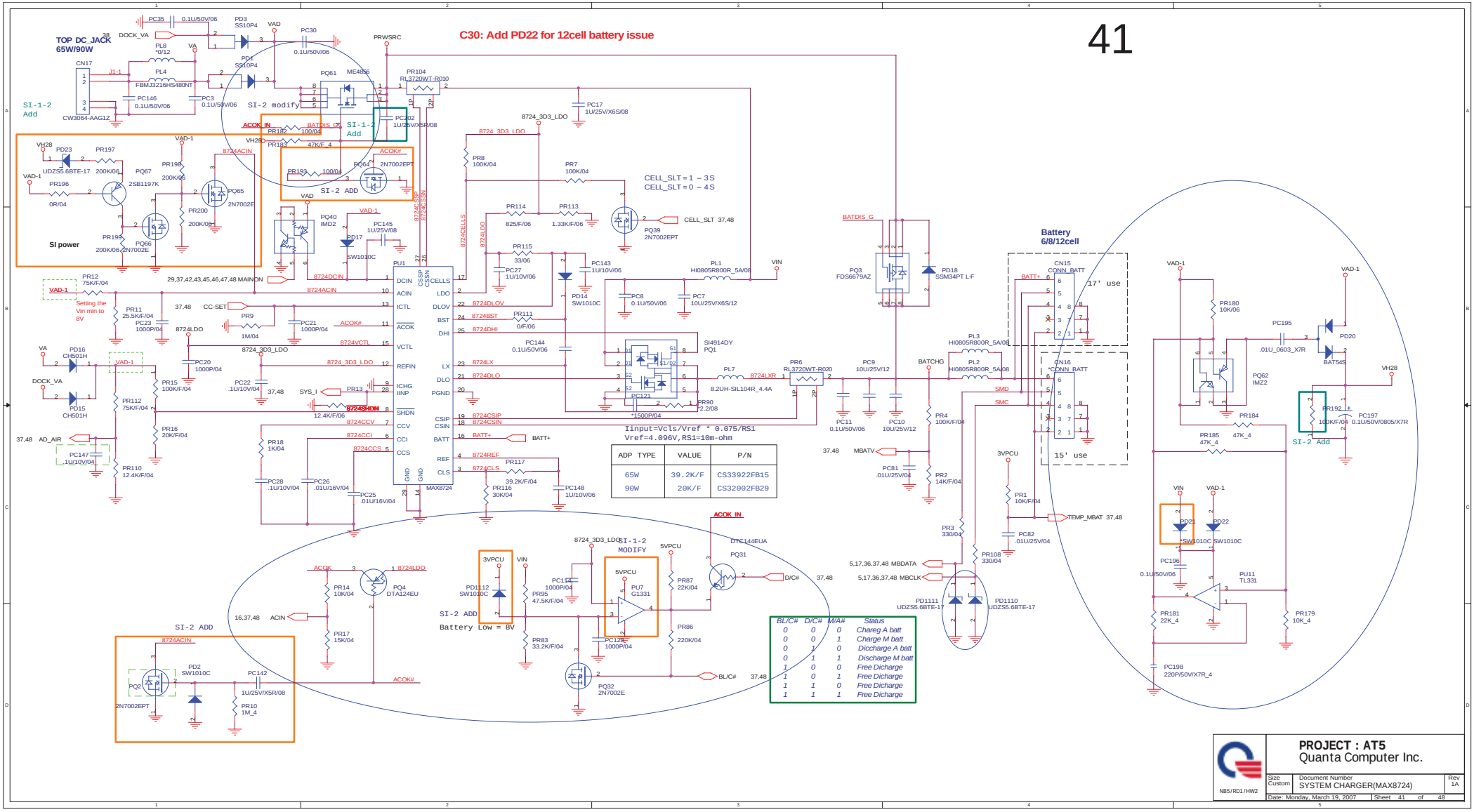

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SYSTEM CHARGER(MAX8724)	1A

N85/RD1/HW2

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DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

5 Volt +/- 5%
Countinue current:8A
Peak current:11A
OCP minimum 13A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

Rds(on) 13m ohm

Rds(on) 15m ohm

Max Power Consumption 1.6W

For G73 Only

SI-1 MODIFY

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Quanta Computer Inc.		
N85/RD1/HW2	Size: Custom	Document Number: 3v/5v
	Rev: 1A	
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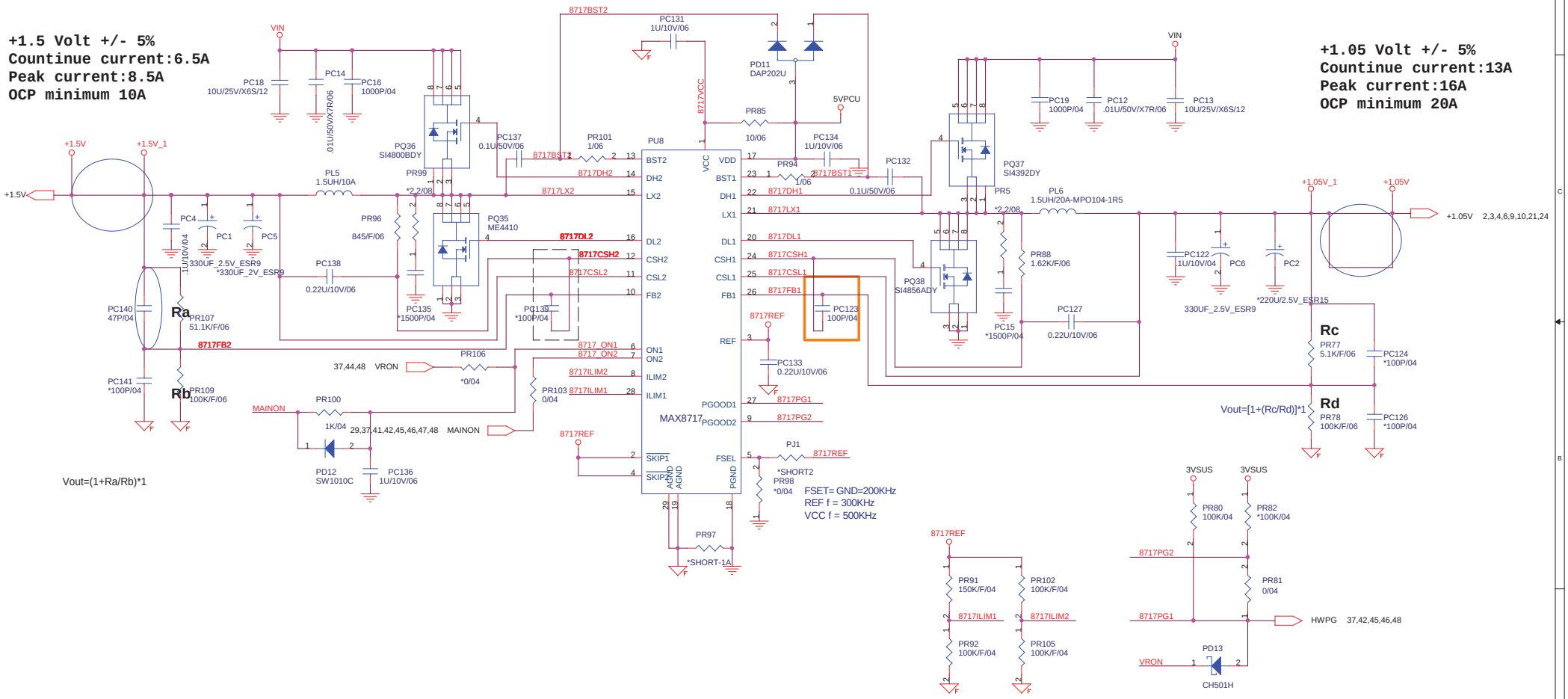
+1.5 Volt +/- 5%
Countinue current:6.5A
Peak current:8.5A
OCP minimum 10A

+1.05 Volt +/- 5%
Countinue current:13A
Peak current:16A
OCP minimum 20A



Vout=(1+Ra/Rb)*1

NB5/RD1/HW2	**PROJECT : AT5** Quanta Computer Inc.	
Size: Custom	Document Number: +-1.5V &VCCP+1.05V(MAX8743)	Rev: 1A
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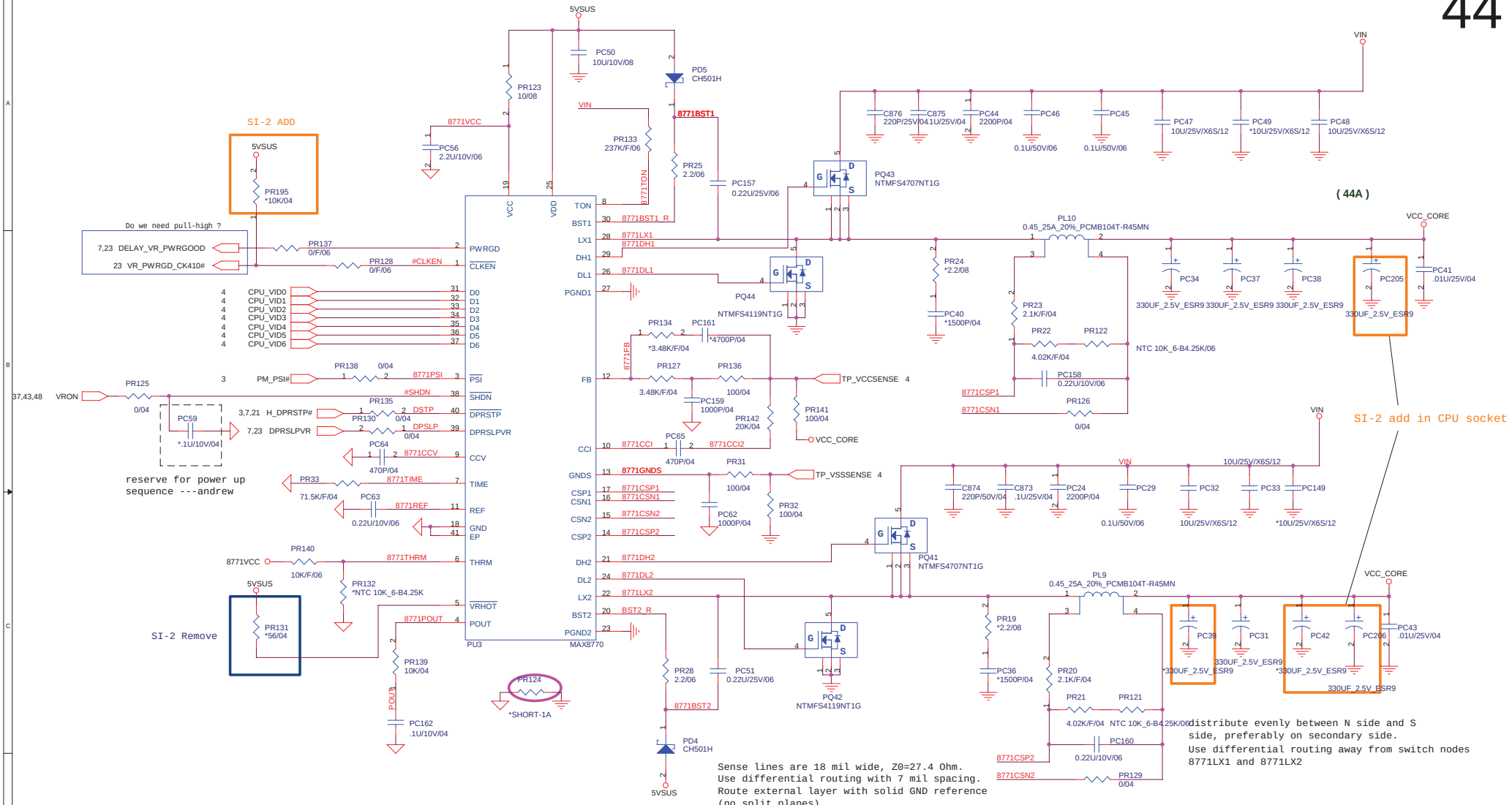

NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
Size: Custom	Document Number: CPU_CORE(MAX8771)	Rev: 1A
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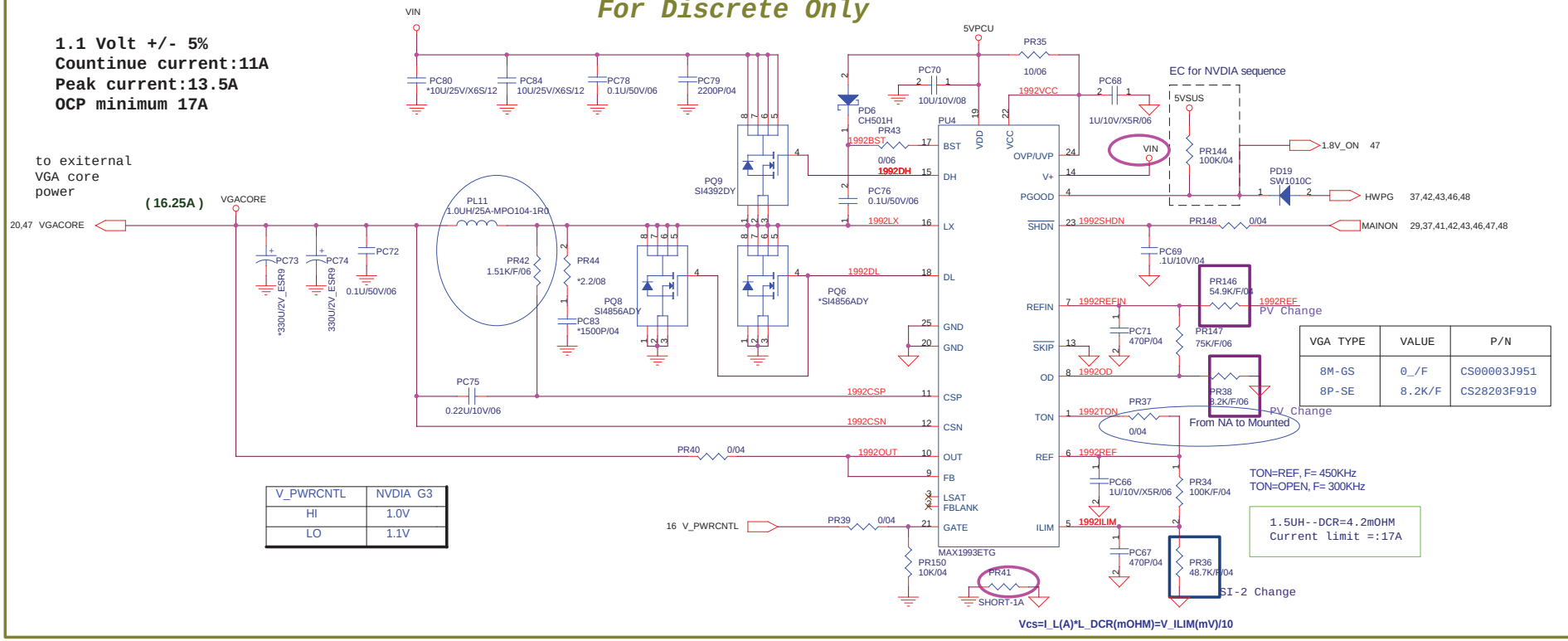
For Discrete Only

1.1 Volt +/- 5%
Countinue current:11A
Peak current:13.5A
OCP minimum 17A

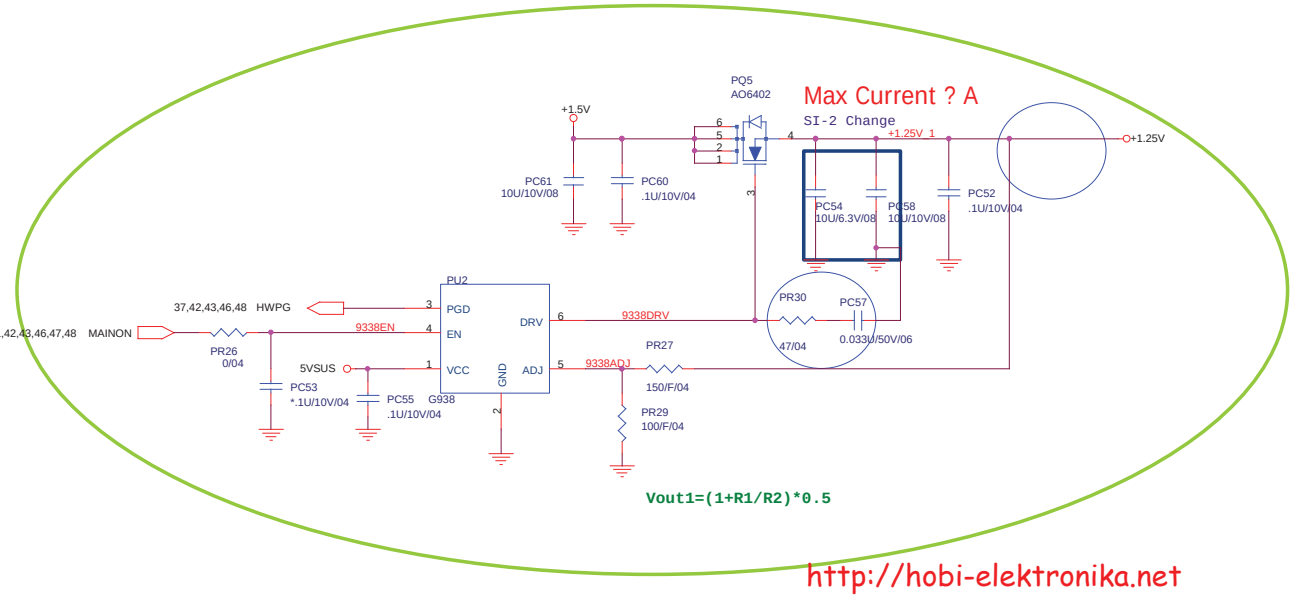
to exiternal
VGA core
power



V_PWRCNTL	NVDIA G3
HI	1.0V
LO	1.1V

VGA TYPE	VALUE	P/N
8M-GS	0_/F	CS00003J951
8P-SE	8.2K/F	CS28203F919

Vcs=I_L(A)*L_DCR(mOHM)=V_ILIM(mV)/10



Vout1=(1+R1/R2)*0.5

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NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

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Custom	VGACORE (MAX1993)	1A
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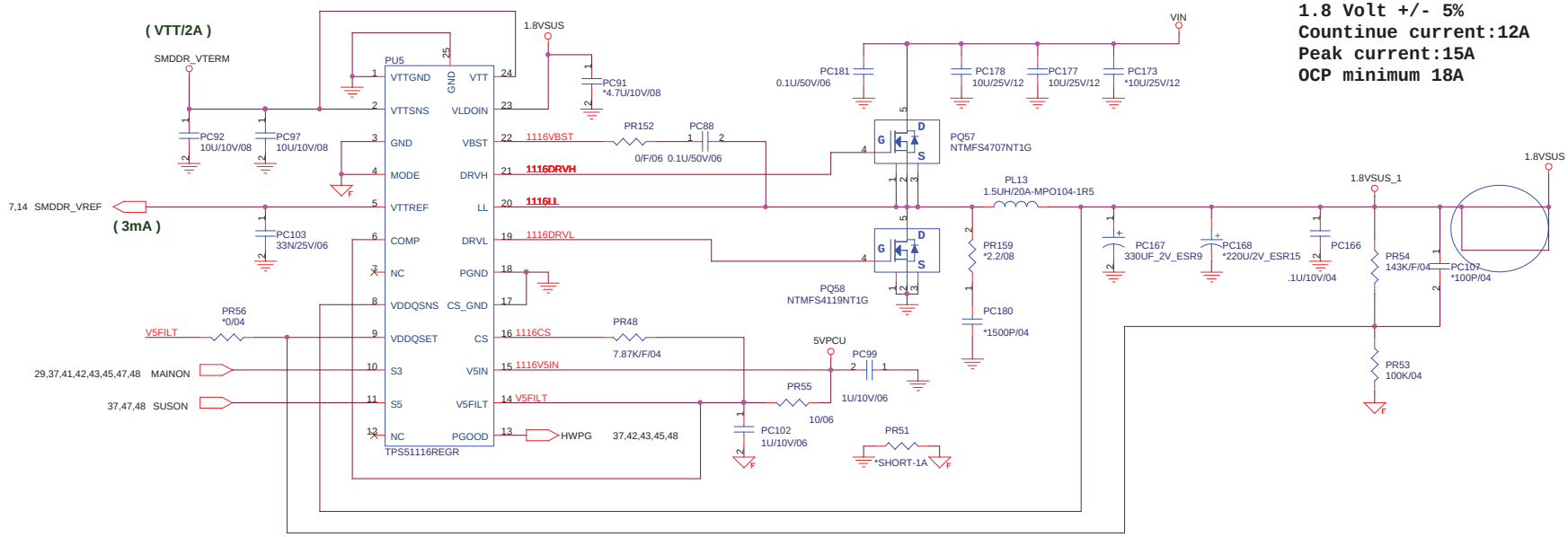
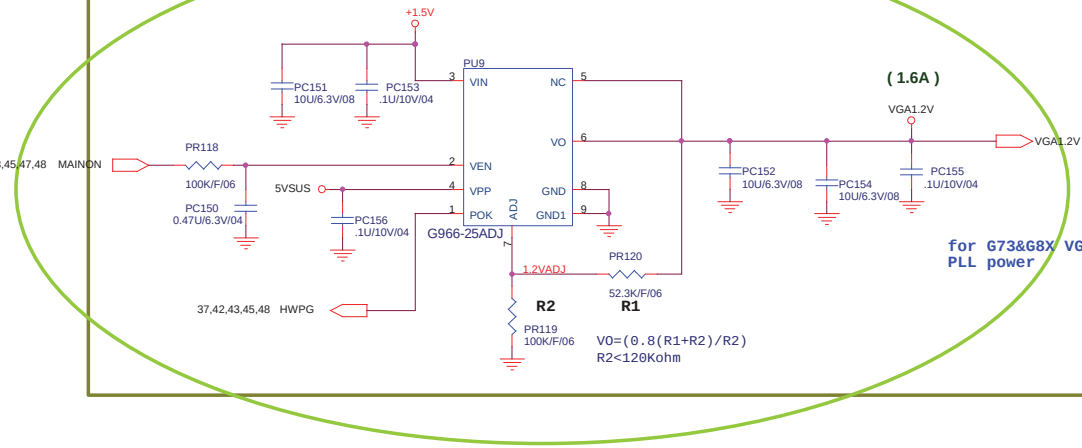
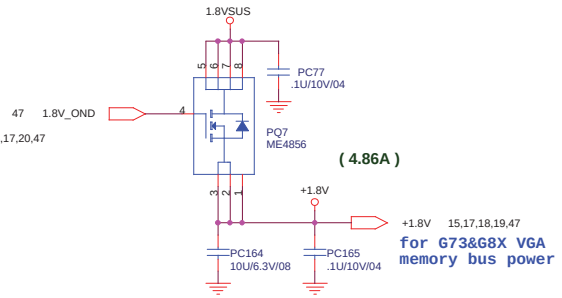


1.8 Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A

For Discrete Only





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NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII 1.8VSUS/SMDDR_VTERM	1A

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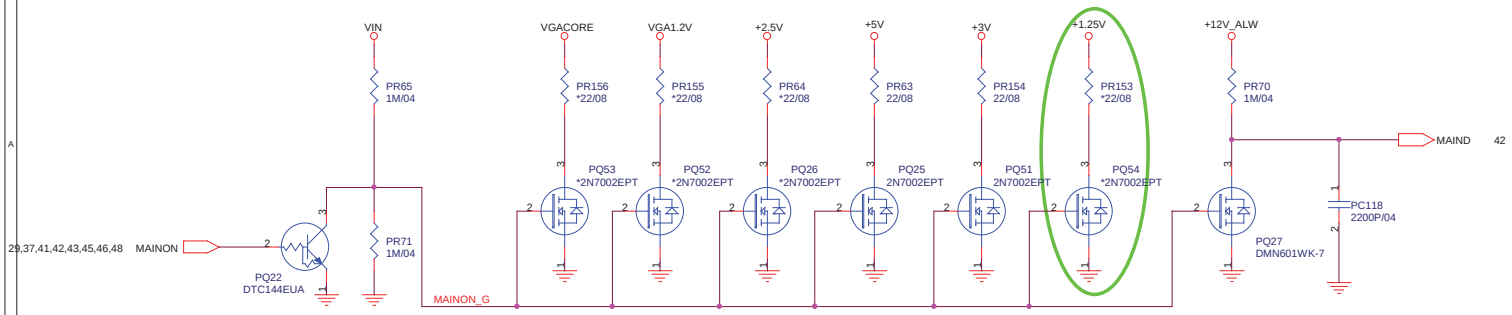

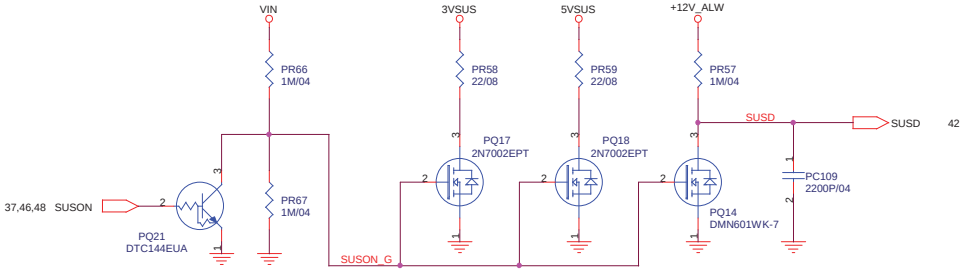

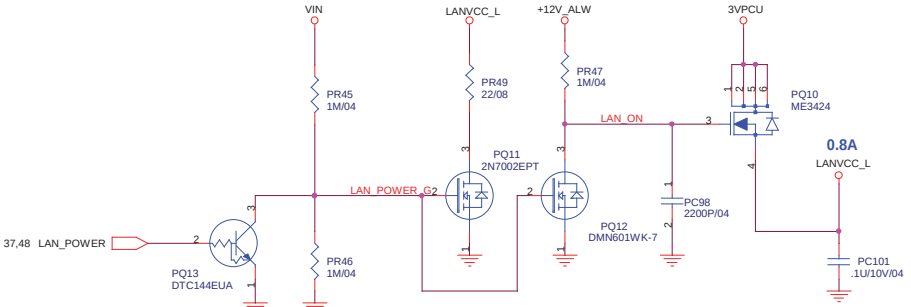

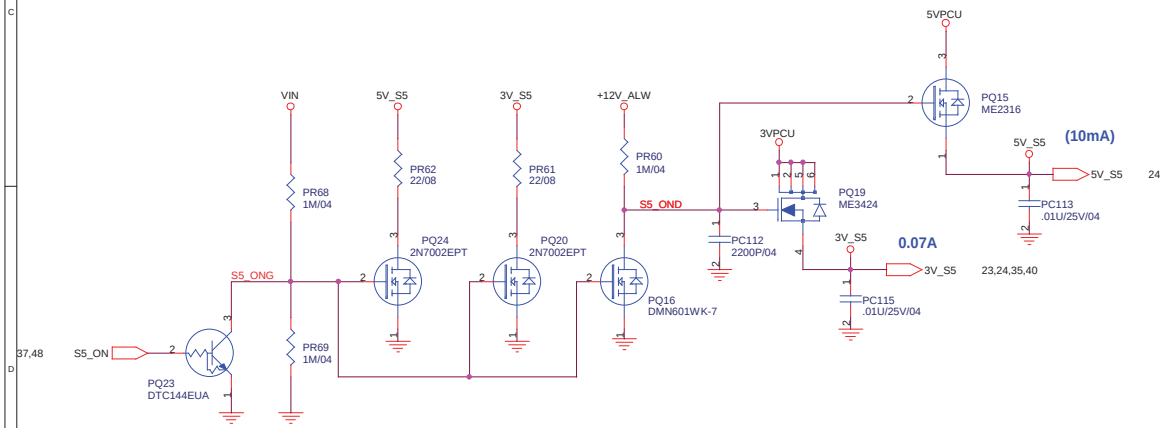

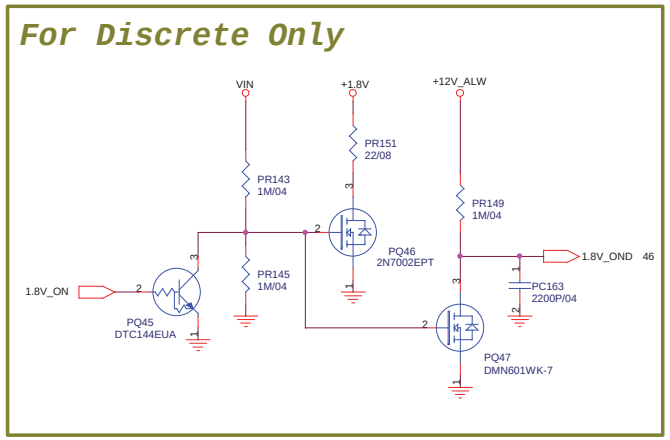

NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
Size: Custom	Document Number: DISCHARGE	Rev: 1A
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