


# LCFC Confidential

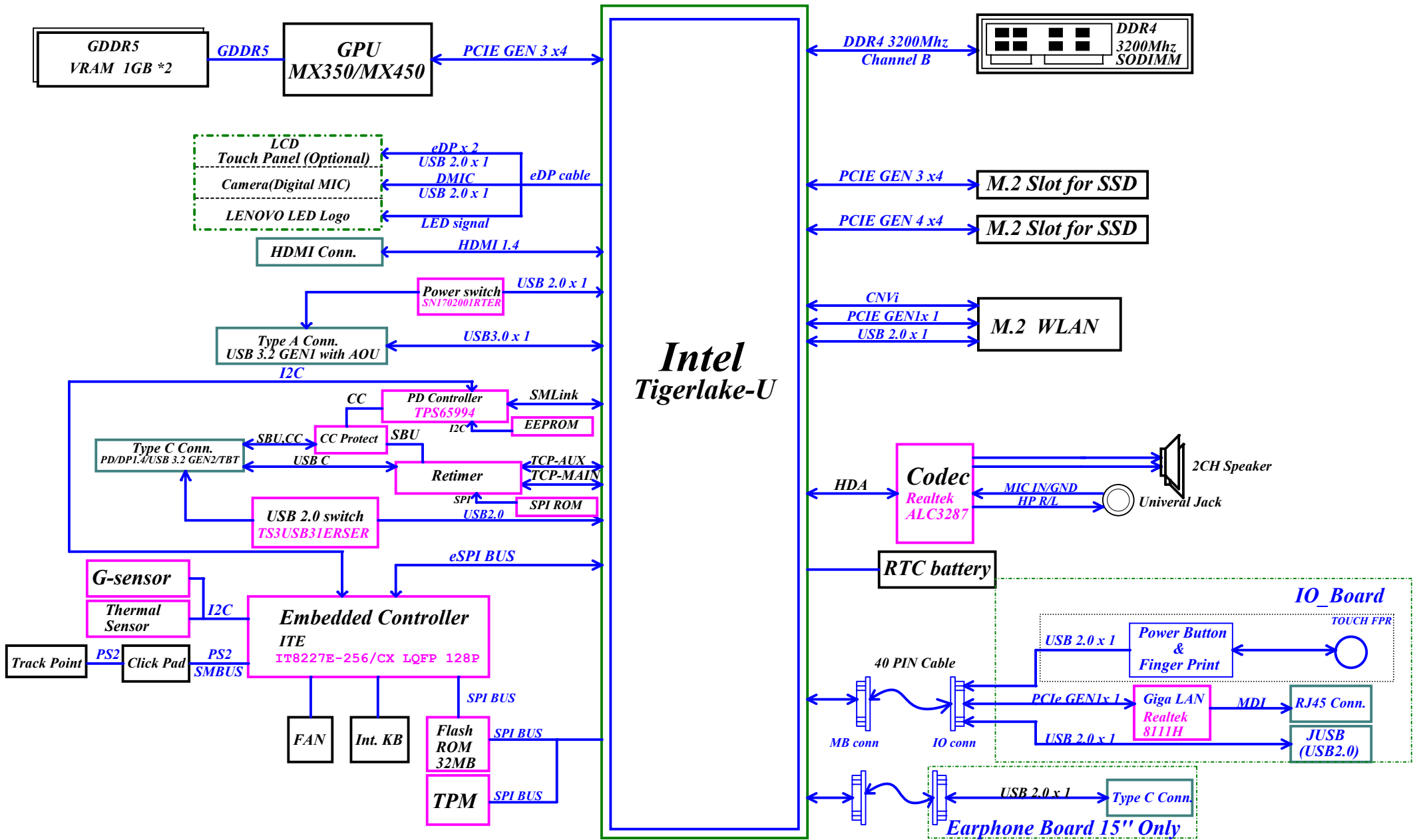
Customer Product name  
E14 Gen2 Intel/E15 Gen2 Intel

Project Code:  
GE4B0/GE5B0

Board Number:  
NM-D011

Customer Project name:  
Mercury/Mars

Security Classification	LC Future Center Secret Data		Title				
Issued Date	2019/12/24	Deciphered Date	2019/12/24	COVER PAGE			
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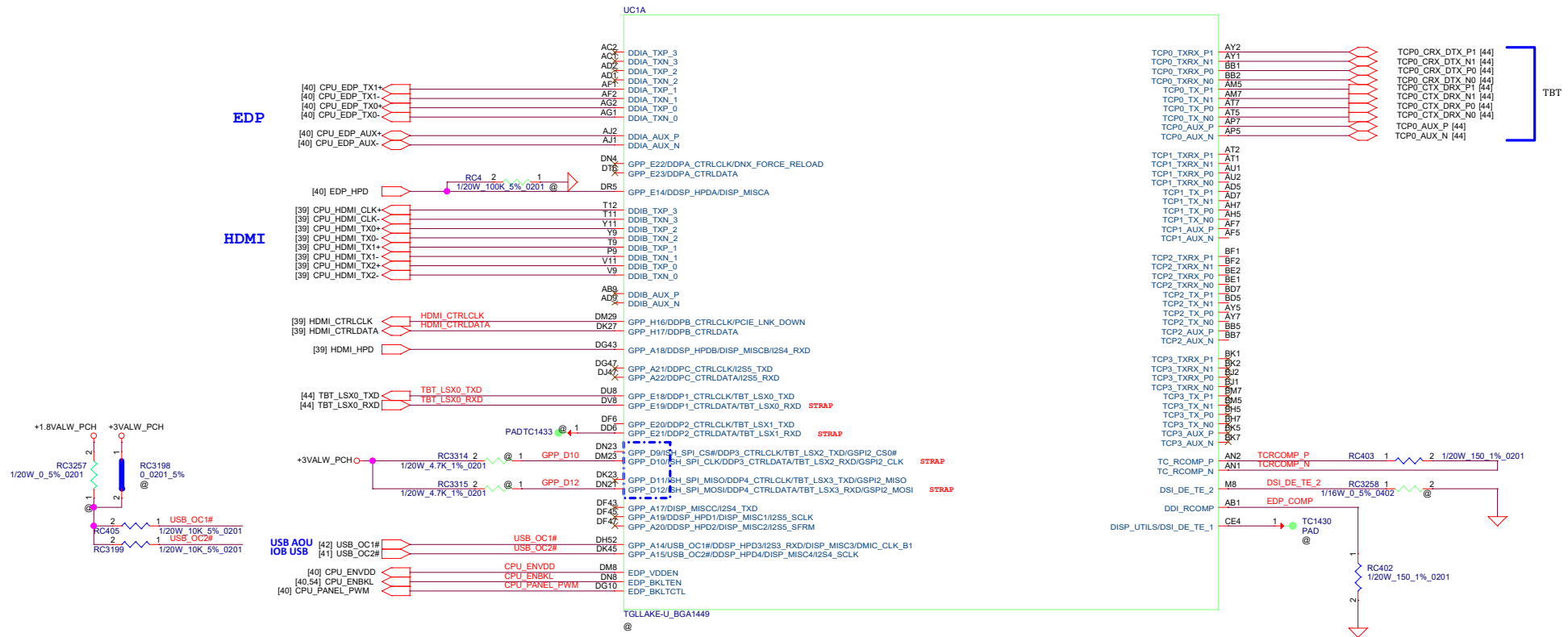


This strap has a 20 kohm  $\pm$  30% internal pull-down.  
0 = DDP1 I2C / TBT\_L SX0 pins at 1.8V  
1 = DDP1 I2C / TBT\_L SX0 pins at 3.3V  
Notes: 1. An external pull-up resistor is required if the pin is used as HDMI Display I2C, instead of TBT\_L SX.  
2. The internal pull-down is disabled after RSMRST# de-asserts.  
3. This signal is in the primary well.

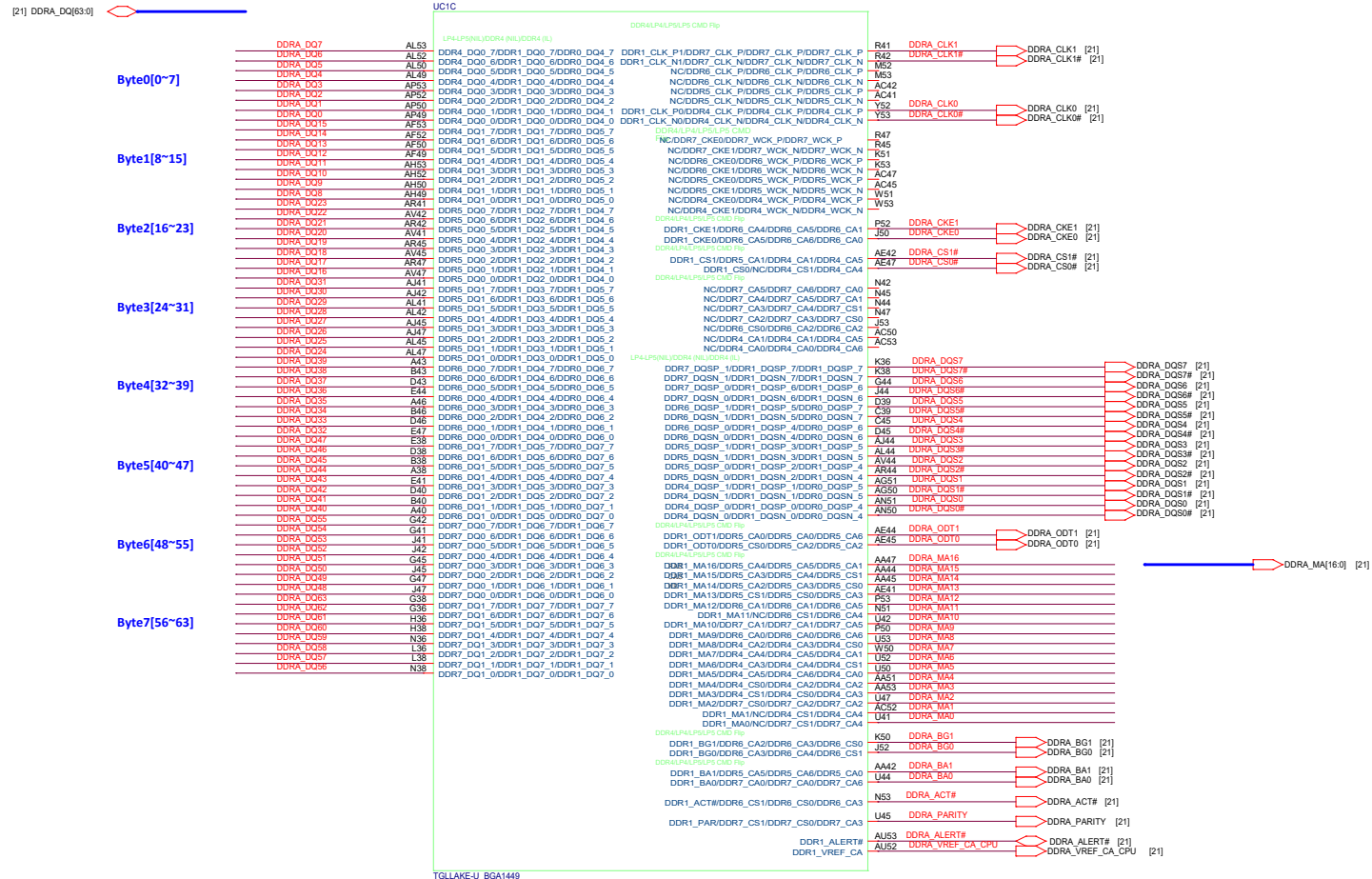
For Glitch Free  
Cap or pull-down resistor is required depending on panel power sequencing spec or power delivery


Option 1:Cap Implementation  
330 nF for 3.3v Ramp Rate from 5-50ms  
33 nF for 3.3v Ramp Rate Less than 5ms

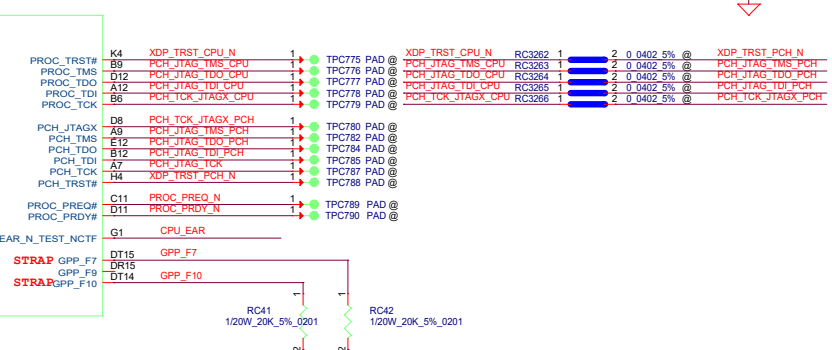
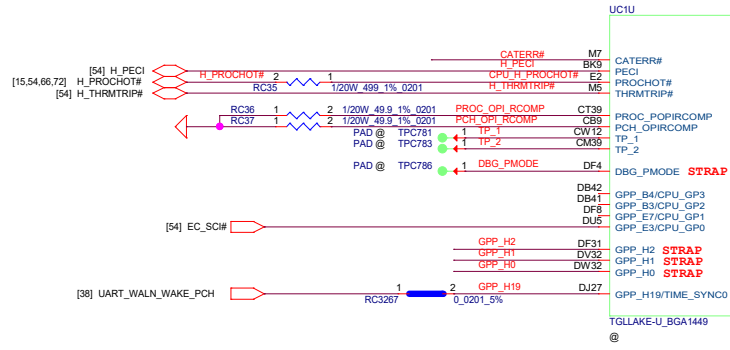
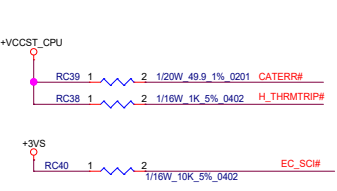
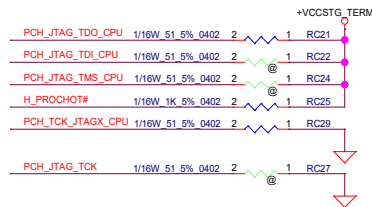
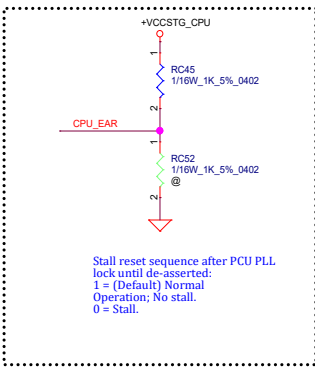
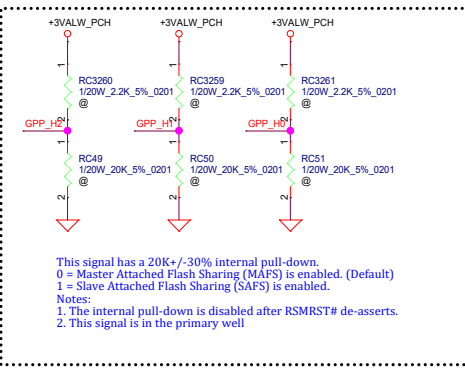
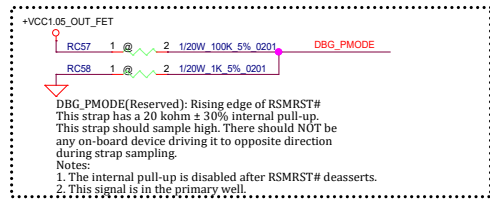
Option 2:Pull-down Resistor Implementation  
100K for 3.3V Signaling Mode  
75K for 1.8V Signaling Mode








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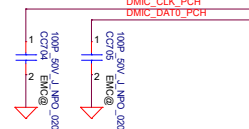





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- Notes:
- 1. The internal pull-down is disabled after PCH\_PWROK is high.
- 2. This signal is in the primary well.



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NVMe SSD

GPU

LAN

WLAN

USB Port3 (Left back AOU)

NVMe SSD

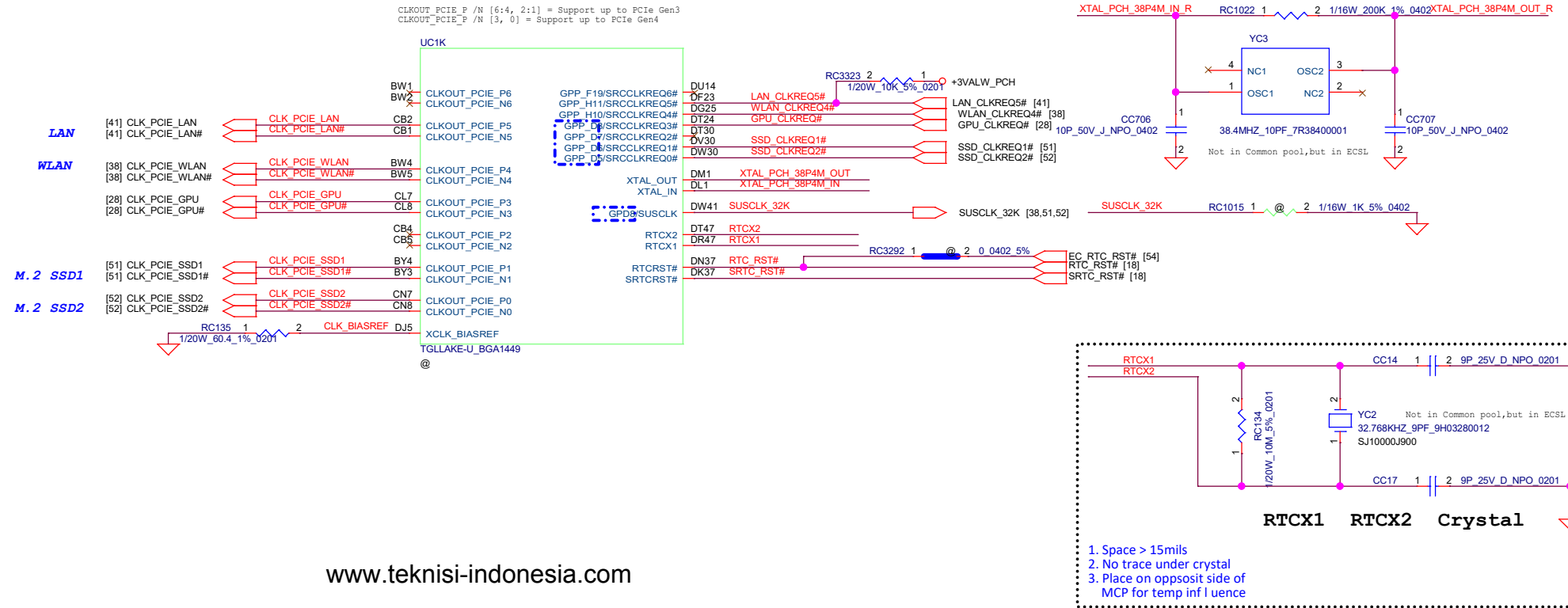
UC1H

TGLLAKE-U\_BGA1449


UC1H

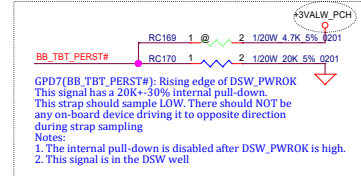
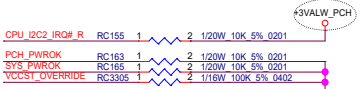
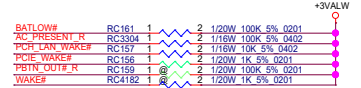
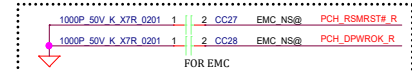
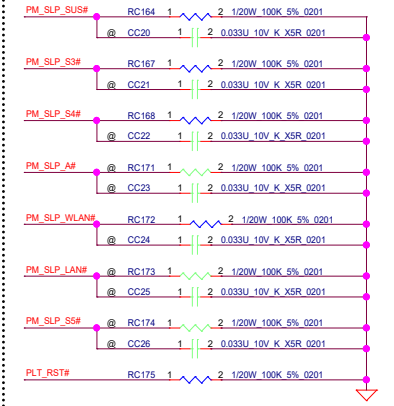
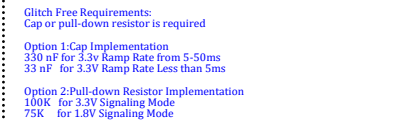
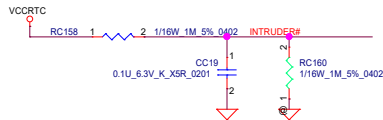
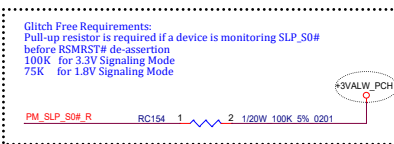
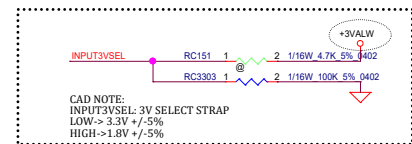
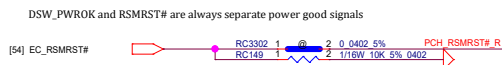
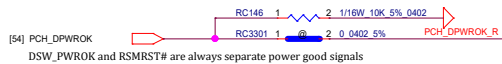
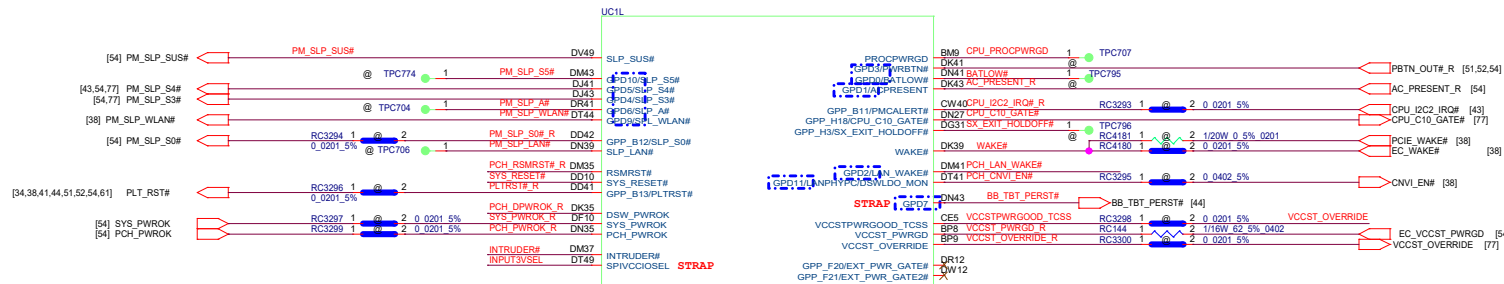
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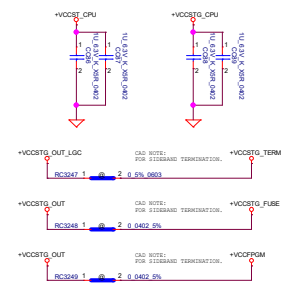
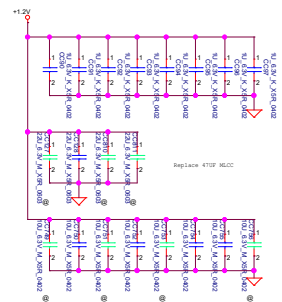
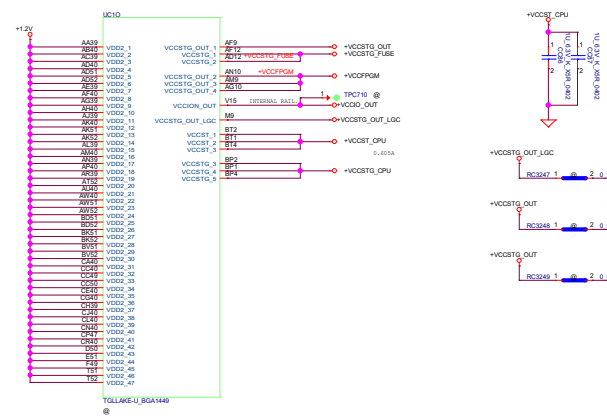
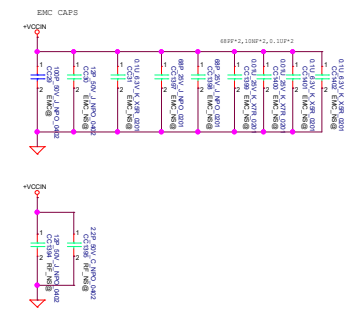
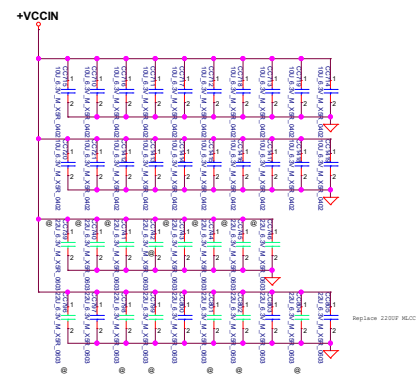
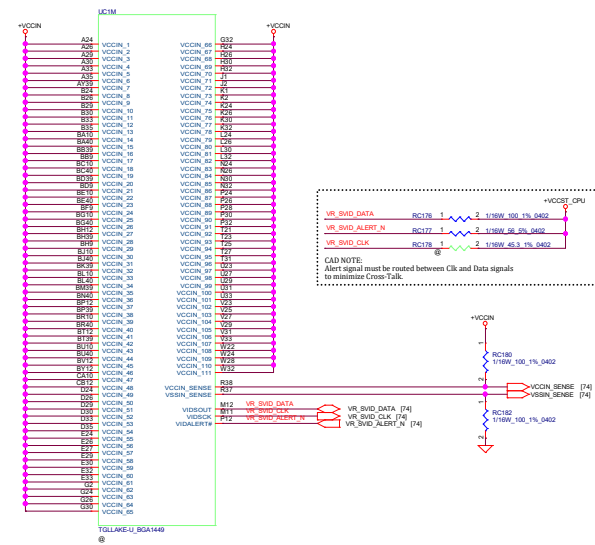


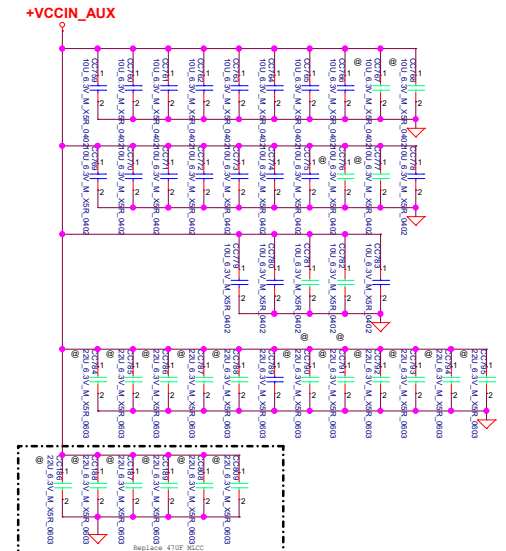
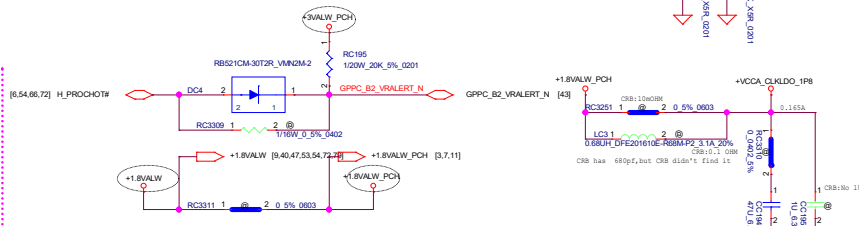
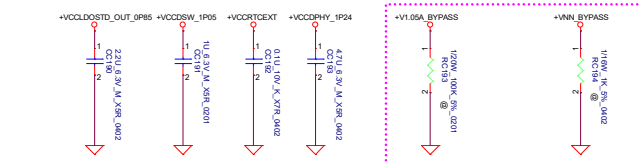


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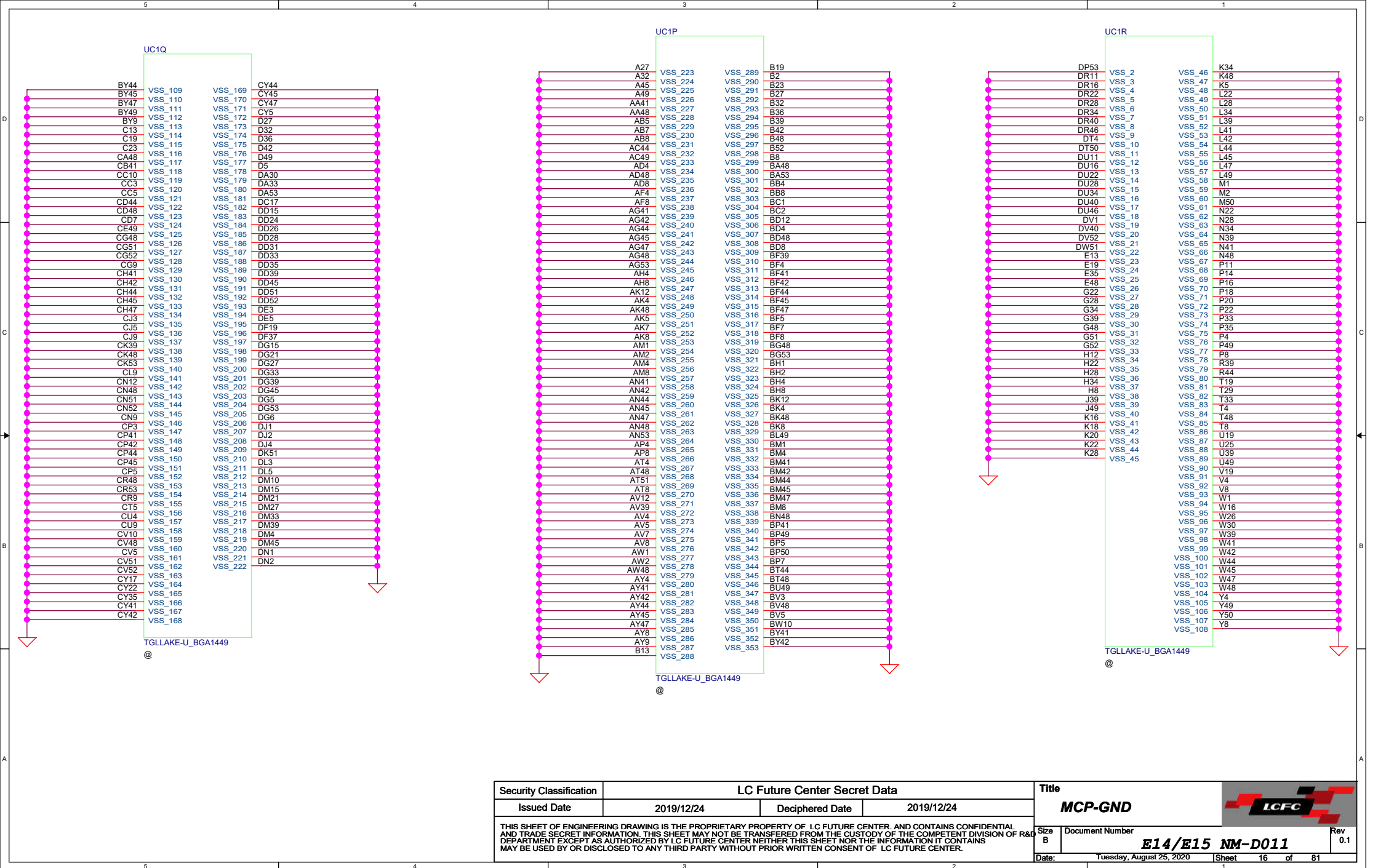




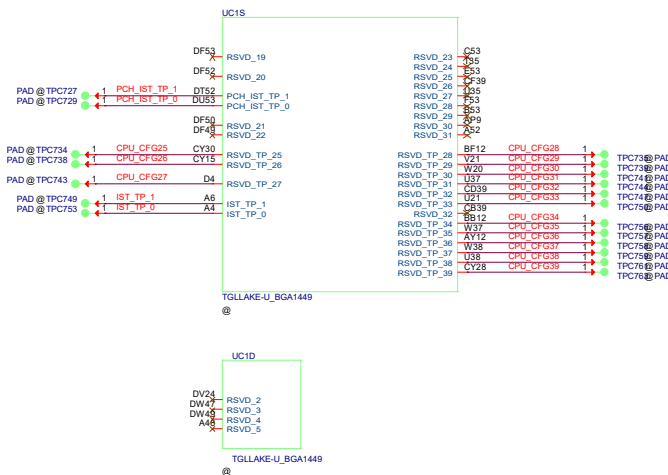
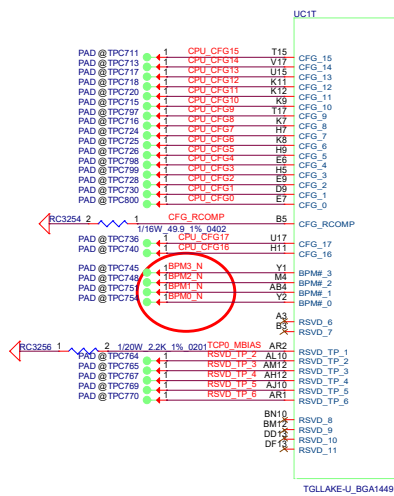


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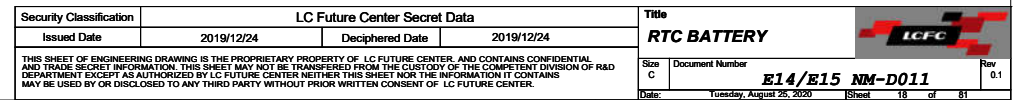


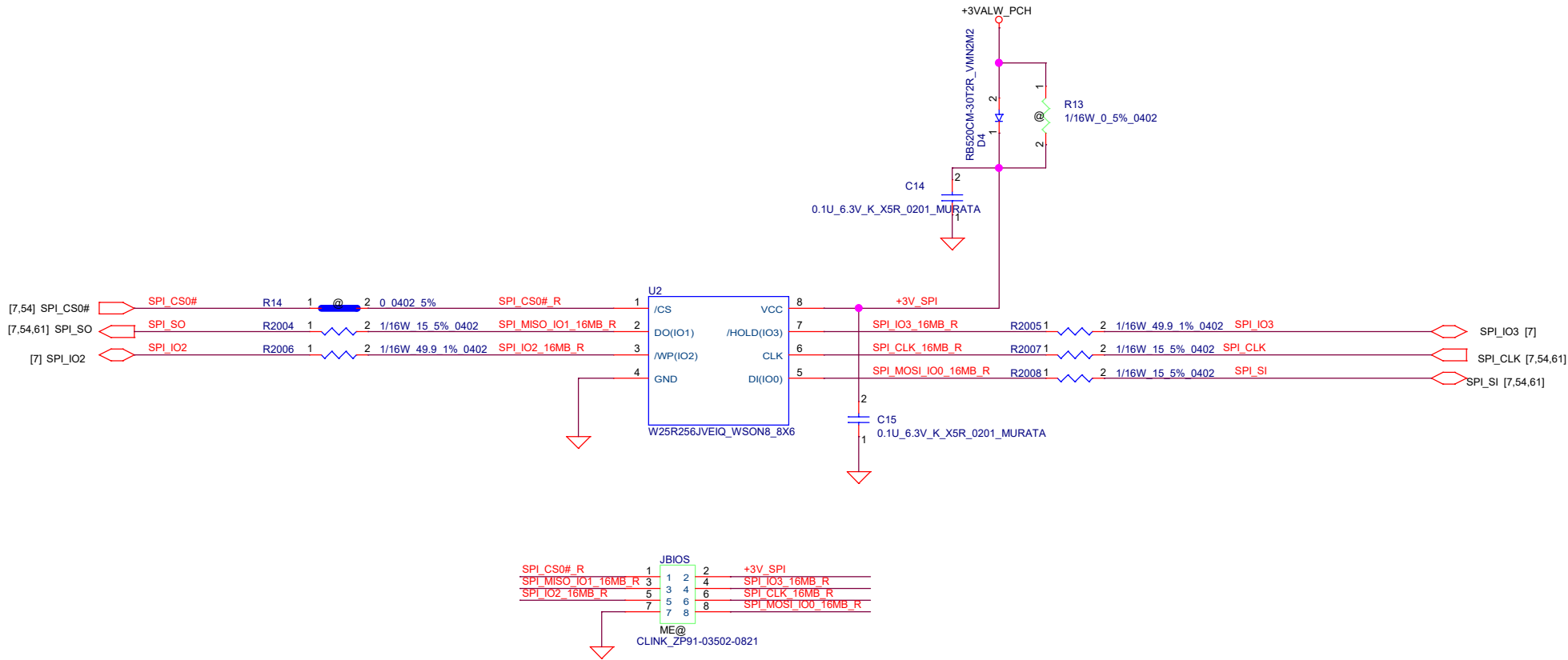





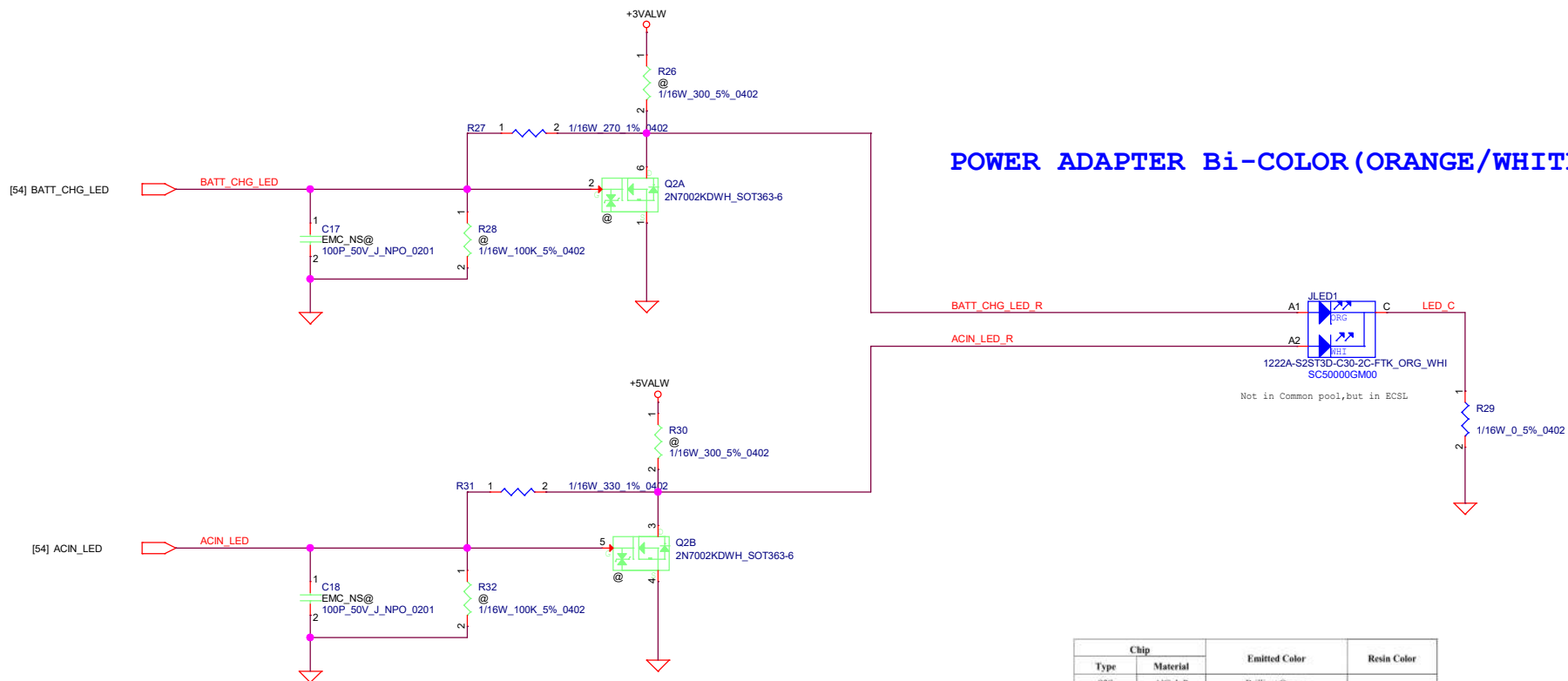
Pin Name	Description	Termination	Resistor
CFG[0]	RSVD	None	
CFG[1,2,3]	RSVD	FU to VCCIO	1K
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO/Pull down -Platform design dependent	1K
CFG[5,6]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO/Pull down -Platform design dependent	1K
CFG[8]	RSVD	None	
CFG[9,10,11]	RSVD	FU to VCCIO	1K
CFG[12,13]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: -1- (Default): Normal -0-Reversed	Pull-up to VCCIO/Pull down -Platform design dependent	1K
CFG[15,16,17]	RSVD	None	

**Earphone CONN.**




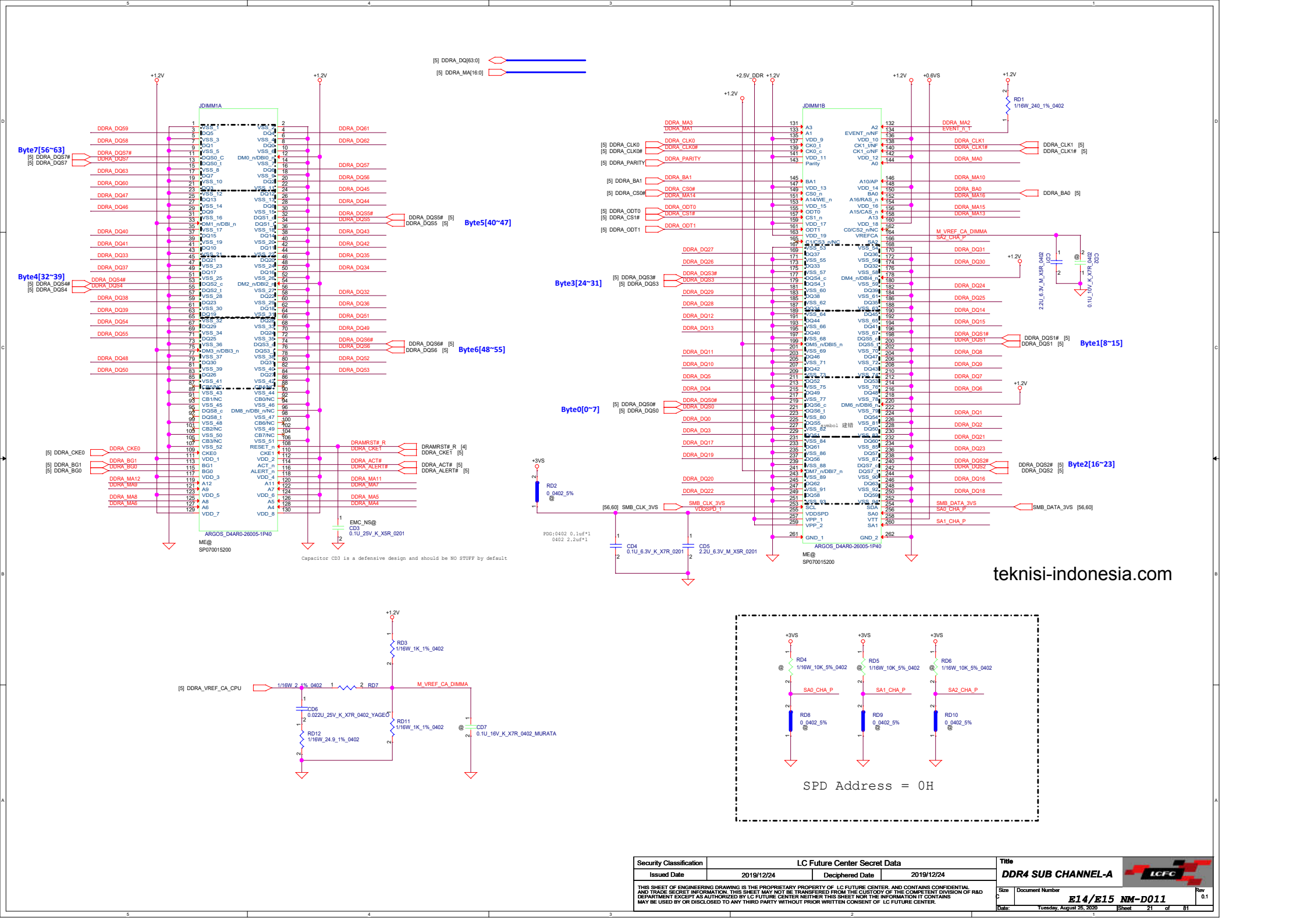


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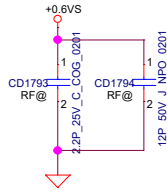
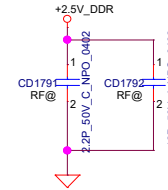
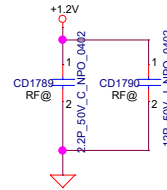
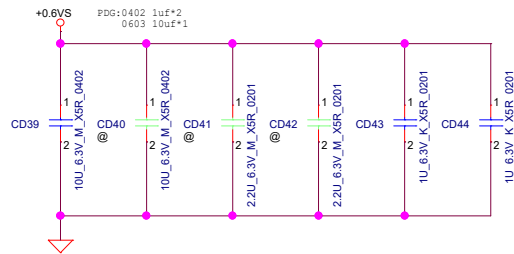
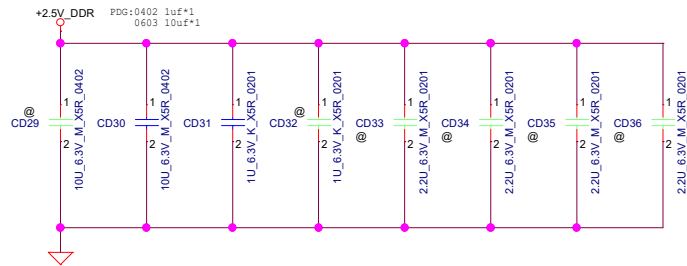
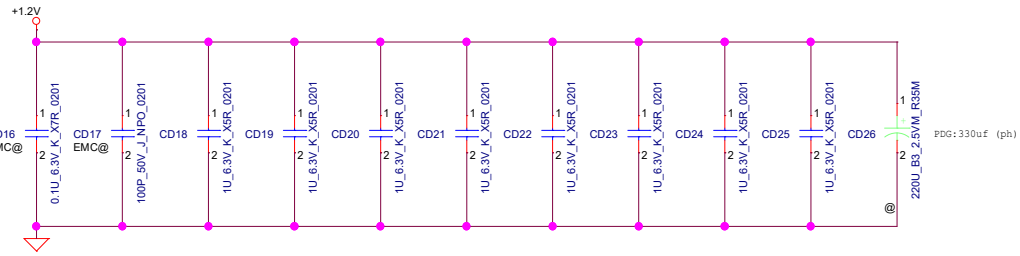
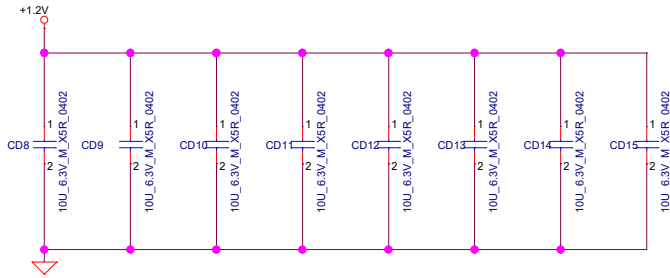


Chip		Emitted Color	Resin Color
Type	Material		
S2S	AlGaInP	Brilliant Orange	Yellow Diffused
T3	InGaN	Pure White	

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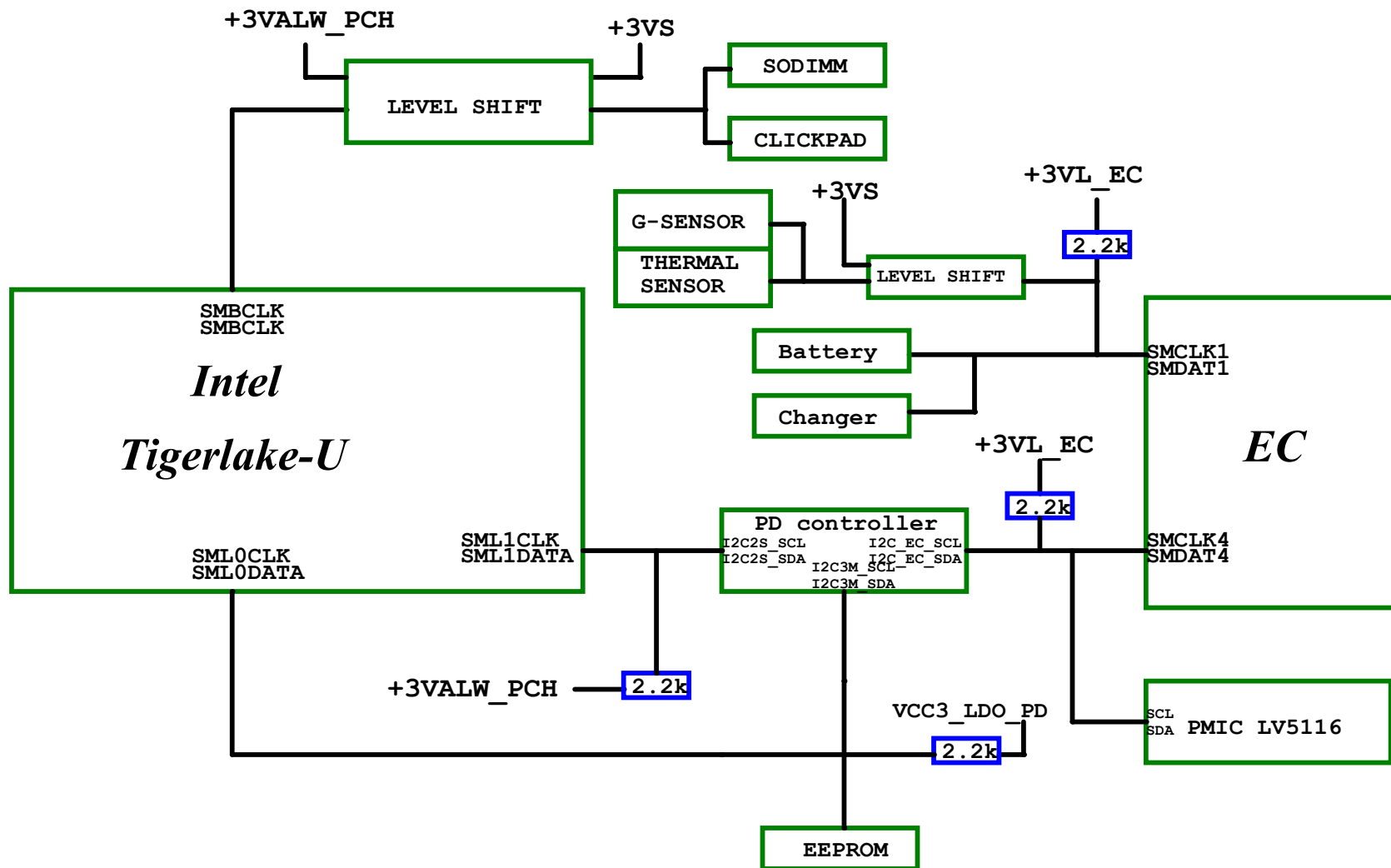


PDG: 0402 1uf\*8  
PDG: 0603 10uf\*8  
PDG: 7343 330uf\*1 (PH)



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				Page	1/1






BOM Structure Table

BOM Structure	NOTE
EAR@	BT EARPHONE FUNCTION
NEAR@	None EARPHONE SKU
FP@	Fingerprint Function
NFP@	None Fingerprint Function SKU
TPM@	Trusted Platform Module(TPM)
NTPM@	None Trusted Platform Module SKU
TPM@	Trusted Platform Module(TPM)
ME@	ME Connector
EMC@	For EMI function
EMC NS@	EMC Reserves
RF@	For RF function
RF NS@	RF Reserves
PCB@	PCB
USB_DEBUG@	USB DEBUG Function
SKU1~SKU19@	CPU
	X76
OPT17@	N17S-G5 Reserve
OPT18@	N18S-G5 Reserve
OPT@	GPU
OPT EMC@	GPU EMC
OPT EMCNS@	GPU EMC Reserve
OPT RF@	GPU RF
OPTNS@	GPU Reserve
UMA@	UMA
EMC_EAR@	Earphone EMC function

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[35,36] FBA\_D0[0..63]  
[35,36] FBA\_CMD[31..0]  
[35,36] FBA\_EDC[7..0]  
[35,36] FBA\_DB[7..0]

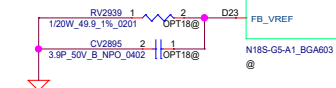
UV1B

FBA\_D0 E18  
FBA\_D1 F18  
FBA\_D2 E16  
FBA\_D3 F17  
FBA\_D4 D20  
FBA\_D5 D21  
FBA\_D6 F20  
FBA\_D7 E21  
FBA\_D8 E15  
FBA\_D9 D15  
FBA\_D10 F15  
FBA\_D11 F13  
FBA\_D12 C13  
FBA\_D13 B13  
FBA\_D14 E13  
FBA\_D15 D13  
FBA\_D16 B15  
FBA\_D17 C16  
FBA\_D18 A13  
FBA\_D19 A15  
FBA\_D20 A18  
FBA\_D21 A19  
FBA\_D22 C19  
FBA\_D23 B18  
FBA\_D24 B24  
FBA\_D25 A23  
FBA\_D26 A25  
FBA\_D27 A24  
FBA\_D28 A21  
FBA\_D29 B21  
FBA\_D30 C20  
FBA\_D31 C21  
FBA\_D32 R22  
FBA\_D33 R24  
FBA\_D34 T22  
FBA\_D35 R23  
FBA\_D36 R25  
FBA\_D37 N25  
FBA\_D38 N23  
FBA\_D39 N24  
FBA\_D40 V22  
FBA\_D41 V22  
FBA\_D42 T23  
FBA\_D43 U22  
FBA\_D44 Y24  
FBA\_D45 AA24  
FBA\_D46 Y22  
FBA\_D47 AA23  
FBA\_D48 AB27  
FBA\_D49 AB25  
FBA\_D50 AD26  
FBA\_D51 AC25  
FBA\_D52 AA27  
FBA\_D53 AA26  
FBA\_D54 W26  
FBA\_D55 Y25  
FBA\_D56 R26  
FBA\_D57 T25  
FBA\_D58 N27  
FBA\_D59 R27  
FBA\_D60 V26  
FBA\_D61 V27  
FBA\_D62 W27  
FBA\_D63 W25

FBA\_DB0 D19  
FBA\_DB1 D14  
FBA\_DB2 C17  
FBA\_DB3 C22  
FBA\_DB4 P24  
FBA\_DB5 W24  
FBA\_DB6 AA25  
FBA\_DB7 U25

FBA\_EDC0 E19  
FBA\_EDC1 C15  
FBA\_EDC2 B16  
FBA\_EDC3 B22  
FBA\_EDC4 R25  
FBA\_EDC5 W23  
FBA\_EDC6 AB26  
FBA\_EDC7 T26

F19 OPT\_GND\_0  
C14 OPT\_GND\_1  
A16 OPT\_GND\_2  
A27 OPT\_GND\_3  
P25 OPT\_GND\_4  
W22 OPT\_GND\_5  
AB27 OPT\_GND\_6  
T27 OPT\_GND\_7



1/16W 60.4 1% 0402

1/16W 60.4 1% 0402

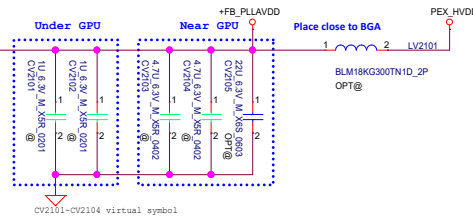
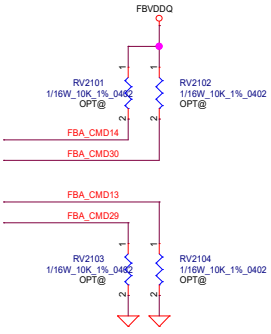
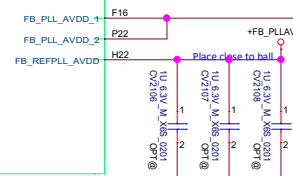
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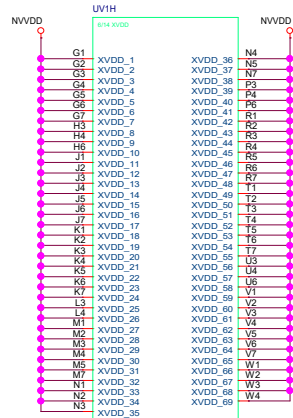
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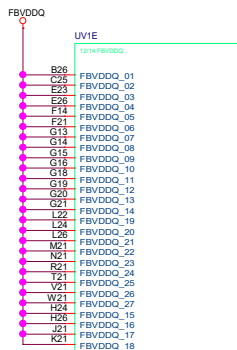
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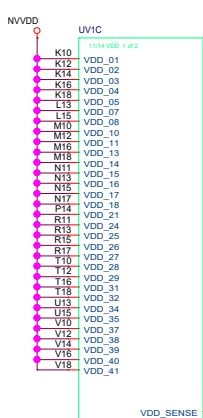




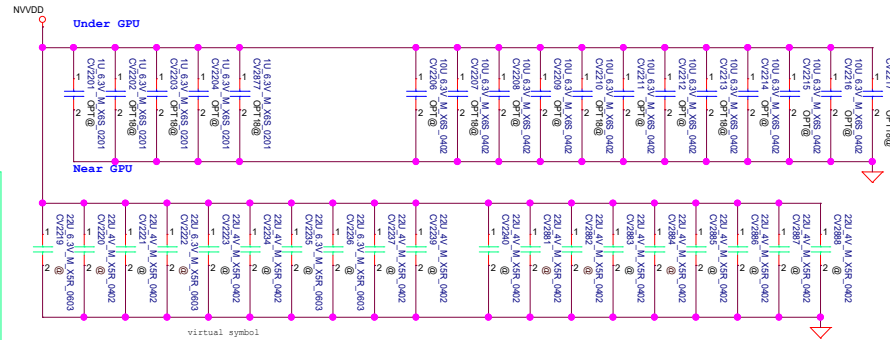
N18S-G5-A1\_BGA603



N18S-G5-A1\_BGA603

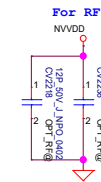


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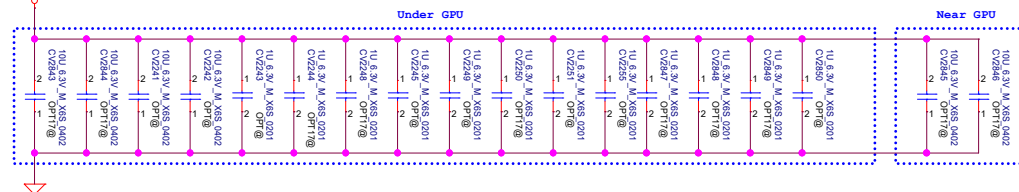


NVDD Decoupling

MLCC		N18/GB2E-64	location	
10uF	X6S	0603	12	Under
4.7uF	X6S	0603	0	
1.0uF	X6S	0201/0402	5	
0.47uF	X6S	0201/0402	0	
10uF	X6S	0603	0	Near
22uF	X6S	0805	10	
4.7uF	X6S	0603	0	
330uF	POS	7343	2	



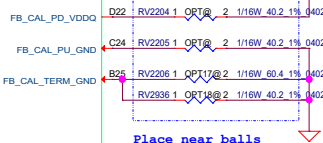
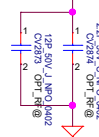
For RF



FBVDDQ Decoupling

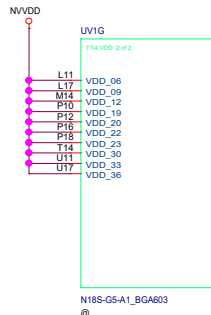
MLCC		N18/GB2E-64	location	
0.47uF	X6S	0201	24	Under
1.0uF	X6S	0201/0402	0	
10uF	X6S	0603	4	
10uF	X6S	0603	2	
22uF	X6S	0603	5	Near

For RF



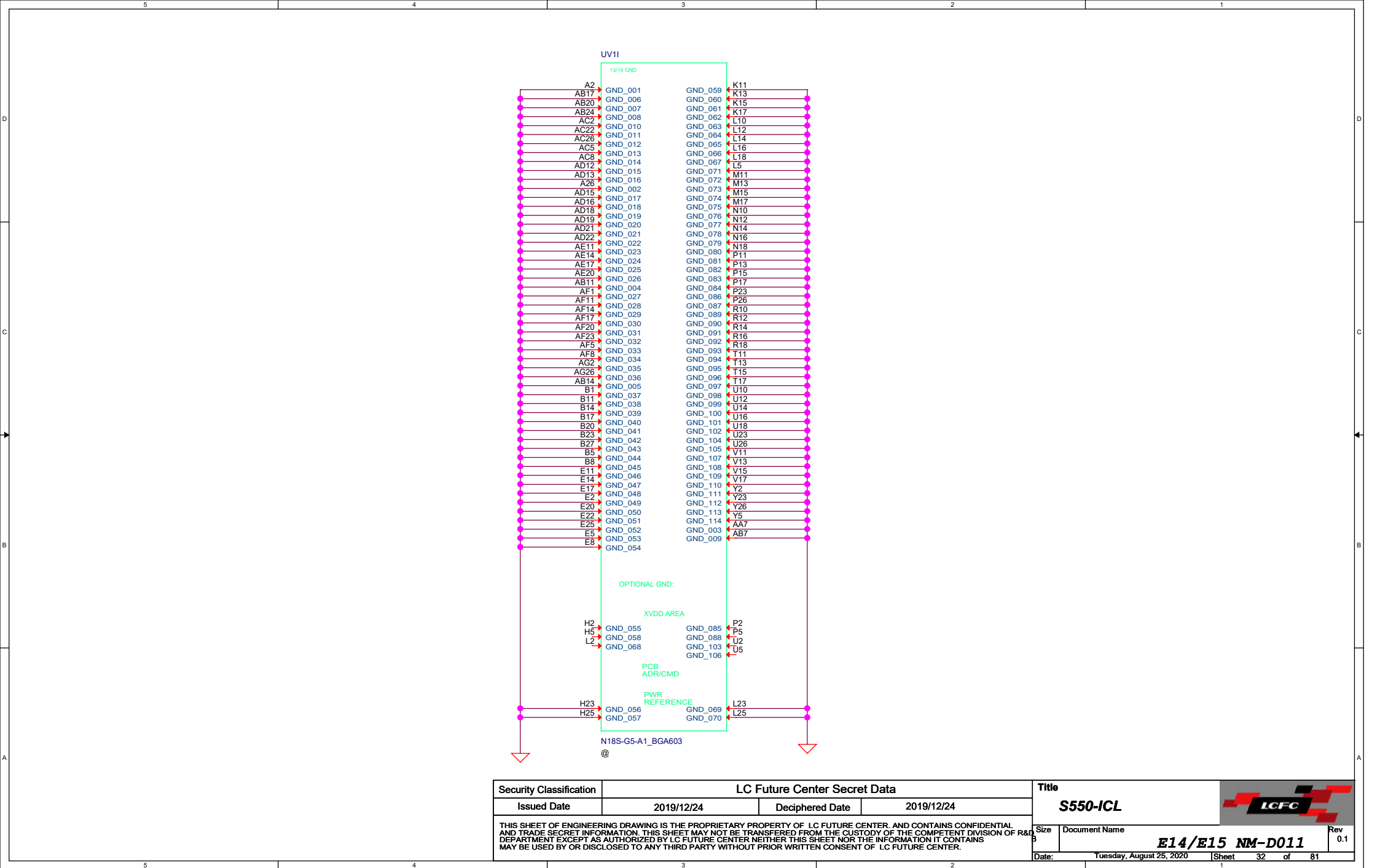
Place near balls

CALIBRATION PIN	GDDR5
FB_CAL x PD VDDQ	40.2Ohm
FB_CAL x PU GND	40.2Ohm
FB_CAL xTERM GND	60.4Ohm

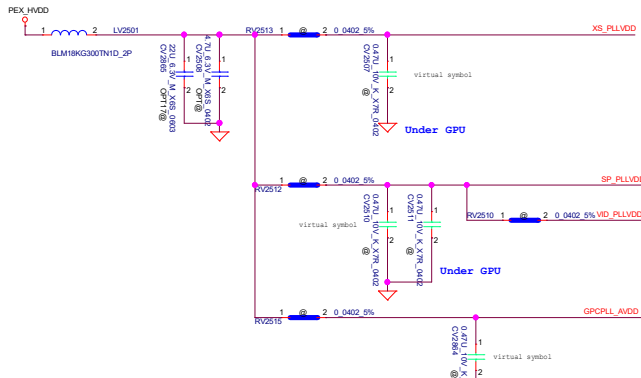
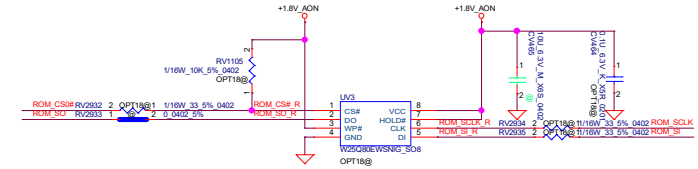


N18S-G5-A1\_BGA603





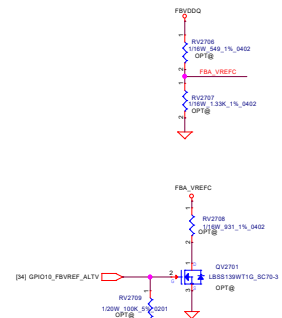
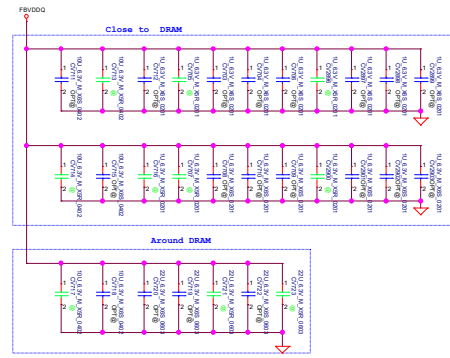
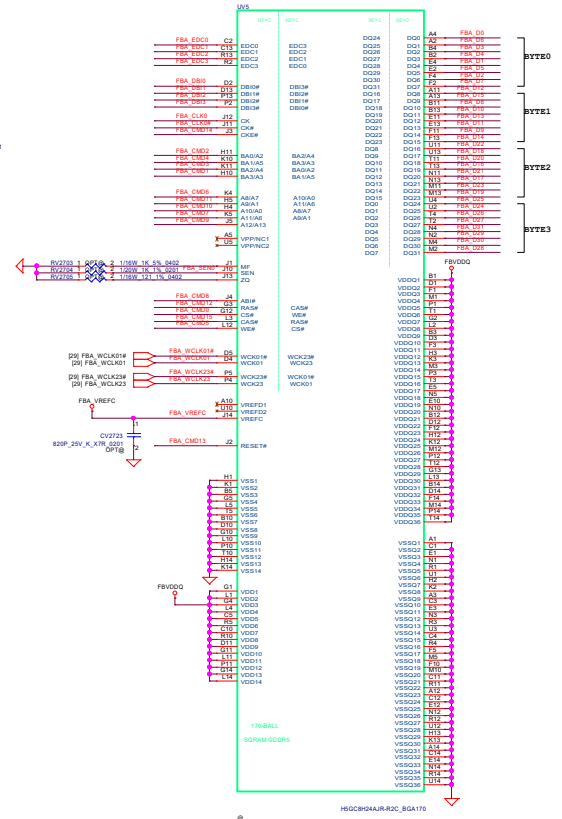
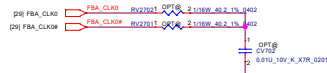




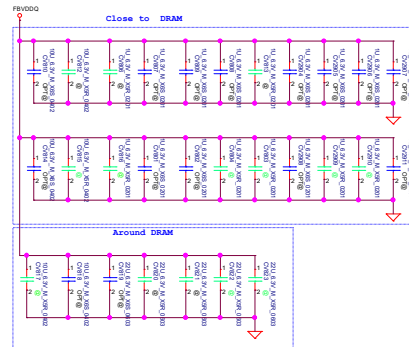
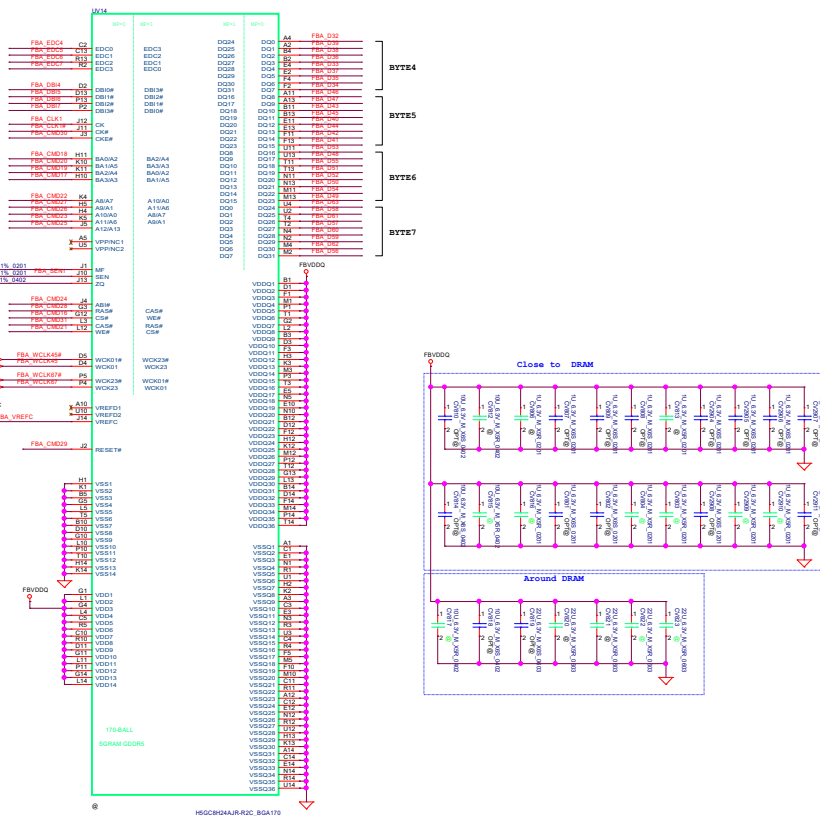
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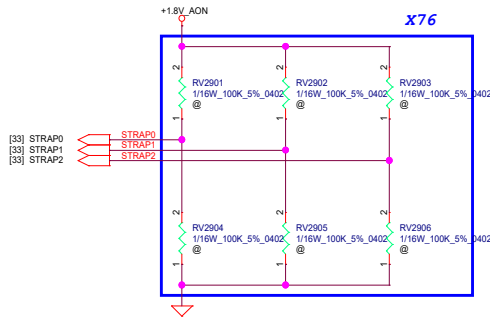


MF=0 No Mirror

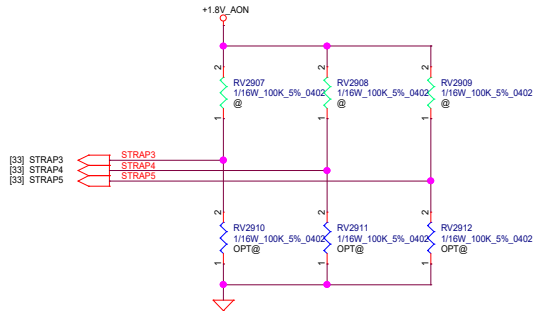


## MF=0 No Mirror





GPU	FB Memory (GDDR5)		STRAP	STRAP2	STRAP1	STRAP0
N18S	Micron 8Gb	MT51J256M32HF-80:B	0x1	L	L	H
	Hynix 8Gb	H5GC8H24AJR-R2C	0x2	L	H	L
	Samsung 8Gb	K4G80325FC-HC25	0x4	H	L	L
GPU	FB Memory (GDDR5)		STRAP	STRAP2	STRAP1	STRAP0
N17S	Micron 8Gb	MT51J256M32HF-80:B	0x9	L	M	L
	Hynix 8Gb	H5GC8H24AJR-R2C	0xA	L	M	H
	Samsung 8Gb	K4G80325FC-HC25	0xB	L	H	M



STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

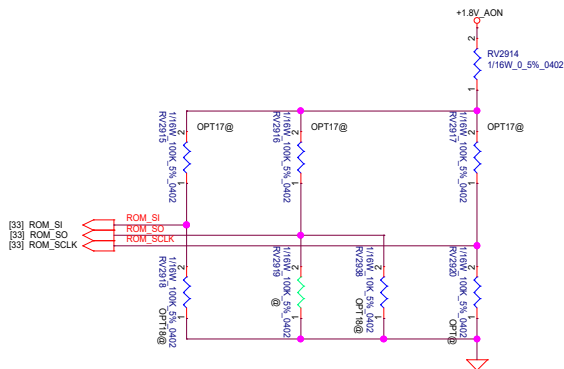
- 1: SMB\_ALT\_ADDR ENABLE  
0: SMB\_ALT\_ADDR DISABLE
- 1: DEVID\_SEL REBRAND  
0: DEVID\_SEL ORIGINAL
- 1: PCIE\_CFG LOW POWER  
0: PCIE\_CFG HIGH POWER
- 1: VGA\_DEVICE ENABLE  
0: VGA\_DEVICE DISABLE

DEVID_SEL	
0	(Default)
1	

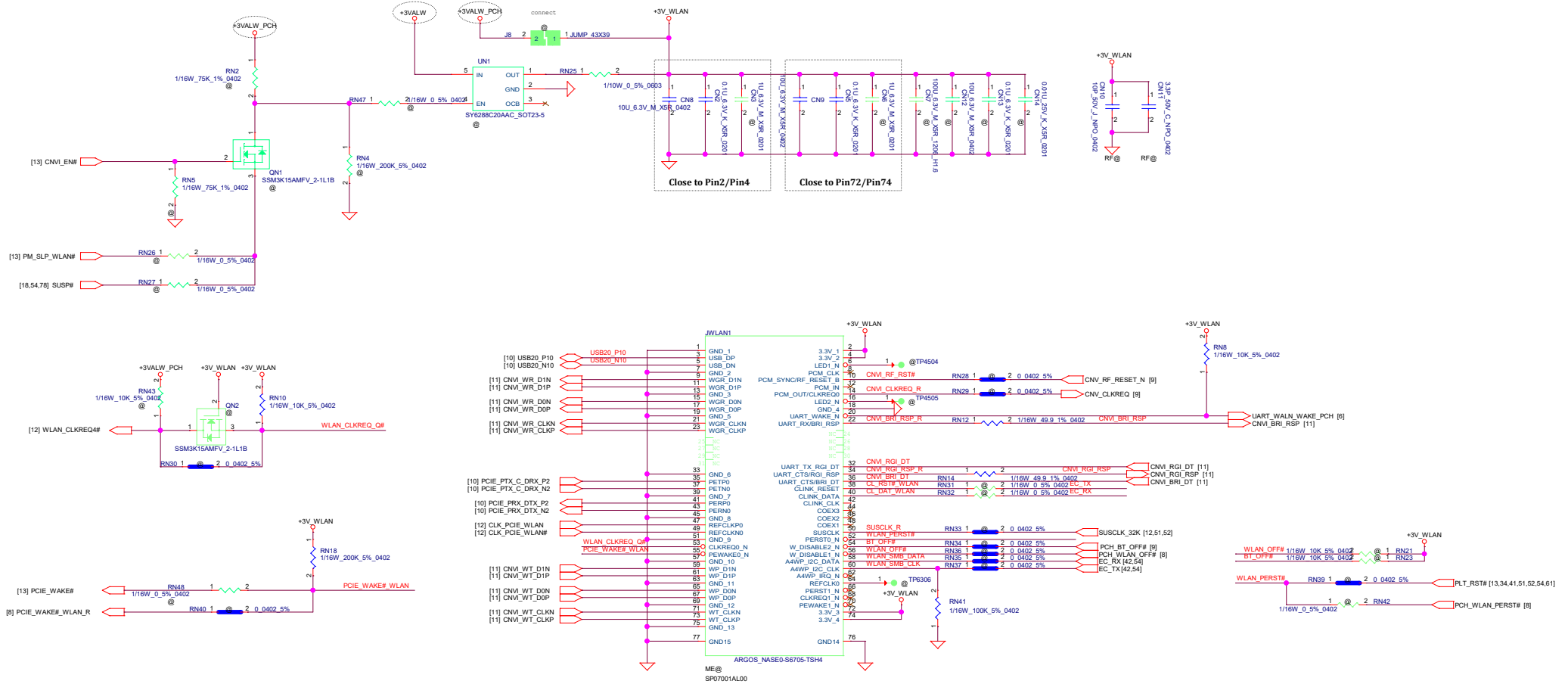
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)


PCIE_CFG	
0	(Default)
1	

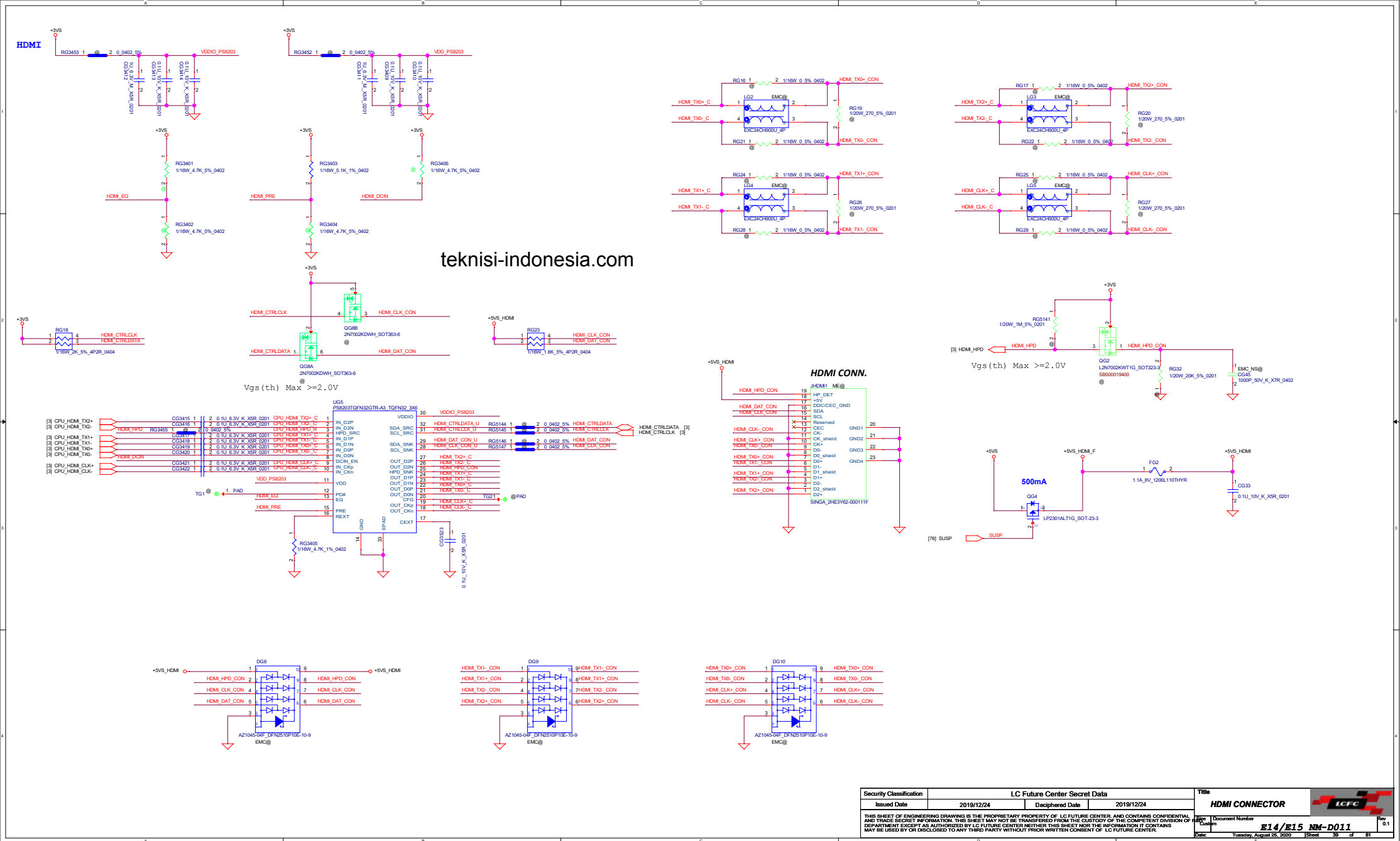
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)



# Mini-Express Card(WLAN/WiMAX)

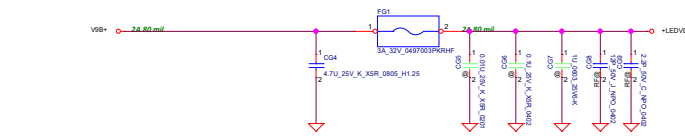


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			Revision	Document Number
			Date	Issued
			E14/E15 NM-D011	Rev 0.1
			Tuesday, August 28, 2020	Sheet 38 of 81



The diagram illustrates the LCDVDD circuit, which is a power distribution network for a display module. It features a central IC labeled 'U51' with pins 1 (IN), 2 (OUT), 3 (GND), 4 (EN), and 5 (CS). The circuit includes a 100nF capacitor (C23) connected to the IN pin (pin 1) and a 100k resistor (R02) connected to the EN pin (pin 4). The CS pin (pin 5) is connected to a 100k resistor (R03) and a 100nF capacitor (C22). The OUT pin (pin 2) is connected to a 100k resistor (R04) and a 100nF capacitor (C21). The GND pin (pin 3) is connected to a 100k resistor (R05) and a 100nF capacitor (C20). The circuit is powered by a 3.3V supply (V3.3) and a 1.8V supply (V1.8). The output of the circuit is labeled 'LCDVDD\_CON'. The circuit is designed with a width of 60 mil.

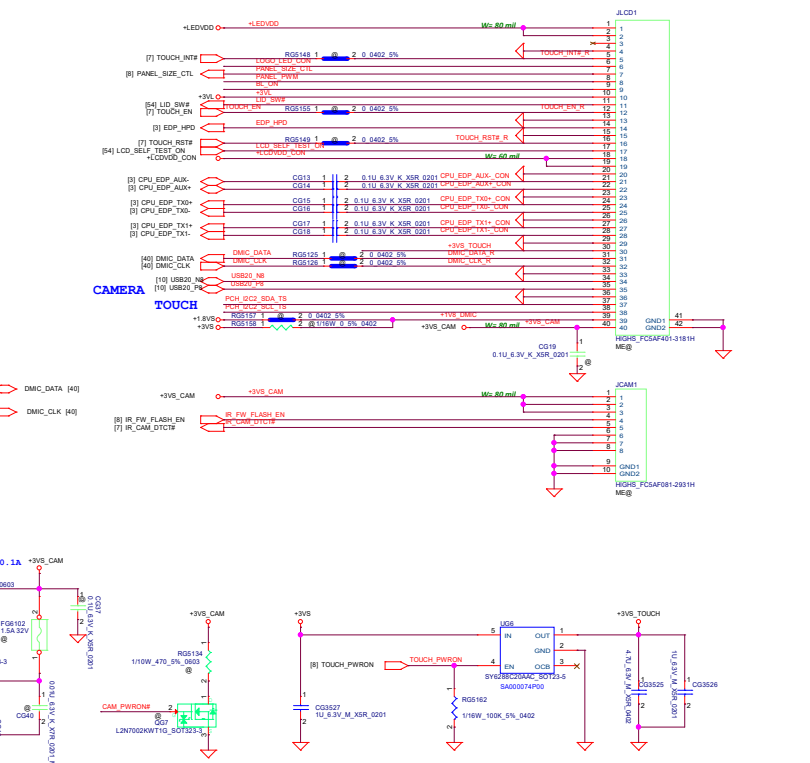
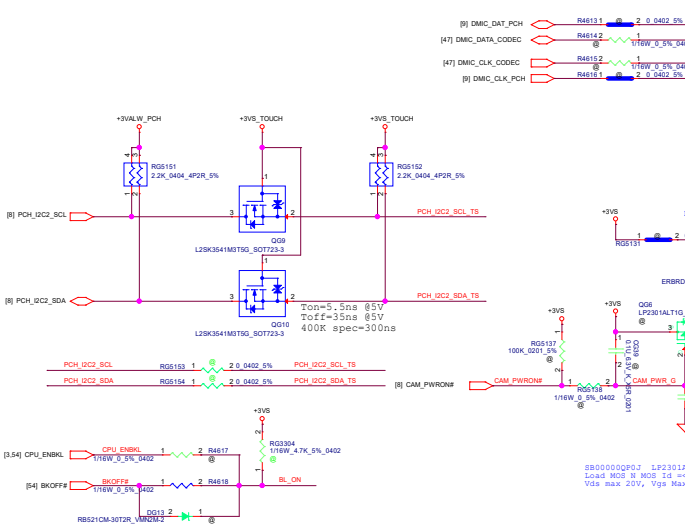
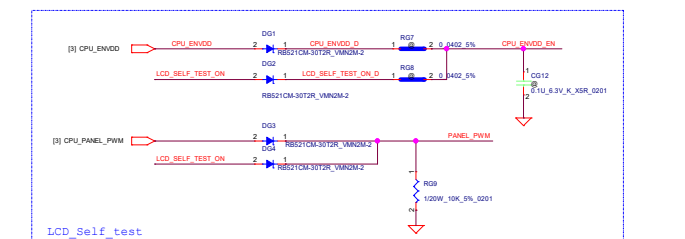
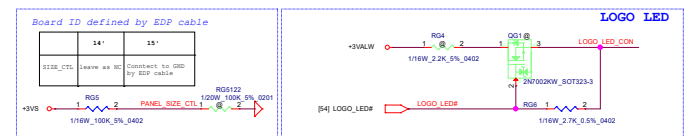
TABLE of POWER SWITCH (U1)		
Vendor	LCFC P/N	Description
SILERGY	SA000074P00	S IC SY628B2C0A2AC SOT23 5P POWER SWITCH
GMT	SA000075T00	S IC G5247T11U SOT-23 5P POWER SWITCH



The ESD request schematic shows the following components and connections:

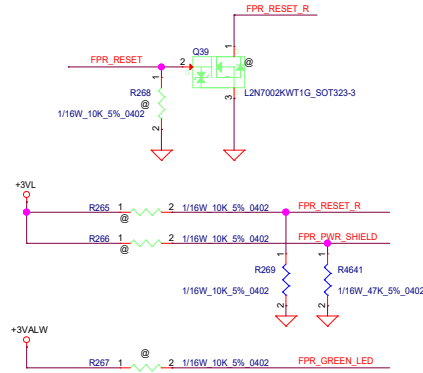
- LOGO\_LED\_CON**: Connected to D07 (ESD07\_1150F\_1000V) and ESD07\_1150F\_1000V.
- USB20\_N8**: Connected to D07 (ESD07\_1150F\_1000V) and ESD07\_1150F\_1000V.
- USB20\_P8**: Connected to D05 (ESD05\_1150F\_1000V) and ESD05\_1150F\_1000V.
- TOUCH\_RST#**: Connected to D09 (ESD09\_1150F\_1000V) and ESD09\_1150F\_1000V.
- TOUCH\_EN\_R**: Connected to D3324 (ESD3324\_10V\_K\_XSR\_0201) and ESD3324\_10V\_K\_XSR\_0201.
- TOUCH\_EN**: Connected to D3324 (ESD3324\_10V\_K\_XSR\_0201) and ESD3324\_10V\_K\_XSR\_0201.
- DMIC\_CLK\_R**: Connected to EMD1 (ESD01\_1150F\_1000V) and EMD1\_1150F\_1000V.
- DMIC\_DATA\_R**: Connected to EMD1 (ESD01\_1150F\_1000V) and EMD1\_1150F\_1000V.
- PCB\_Q2C\_SCL\_TS**: Connected to D011 (ESD011\_10V\_Q\_NPO\_0201) and ESD011\_10V\_Q\_NPO\_0201.
- PCB\_Q2C\_SDA\_TS**: Connected to D012 (ESD012\_10V\_Q\_NPO\_0201) and ESD012\_10V\_Q\_NPO\_0201.
- EMC\_N8#**: Connected to EMD35 (ESD035\_1150F\_1000V) and EMD35\_1150F\_1000V.
- EMC\_N8**: Connected to EMD35 (ESD035\_1150F\_1000V) and EMD35\_1150F\_1000V.
- ESD request**: A red arrow pointing to the schematic.

Board ID defined by EDP cable	LOGO LED	eDP/CAMERA/DMIC/LOGO-LED CONN.
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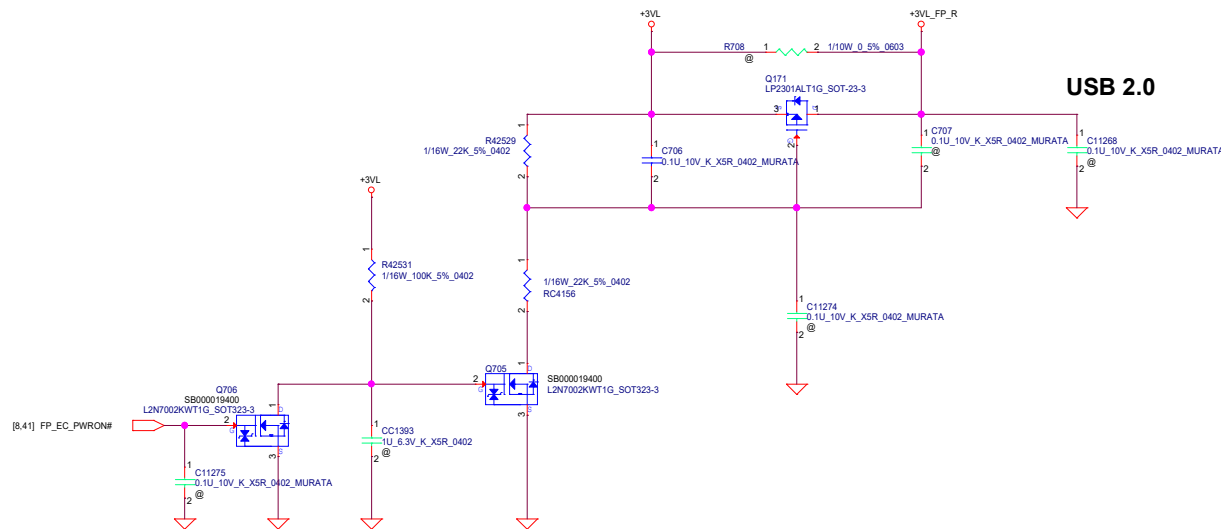
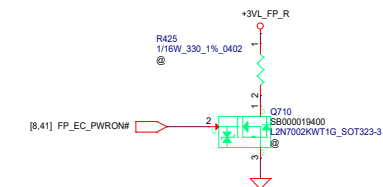
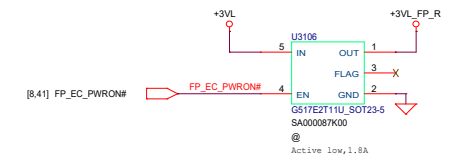
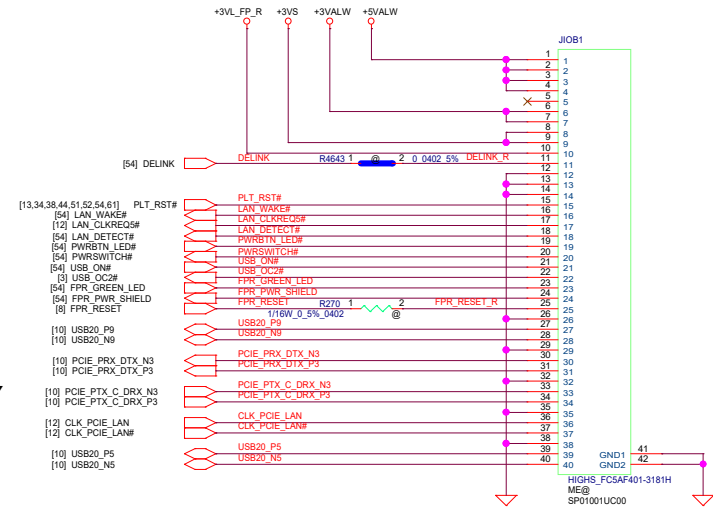



## IO\_40\_Pin conn



## Finger Printer

GBE LAN PHY

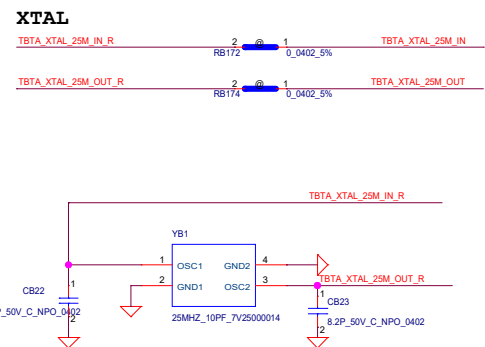
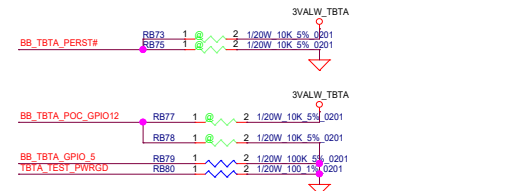
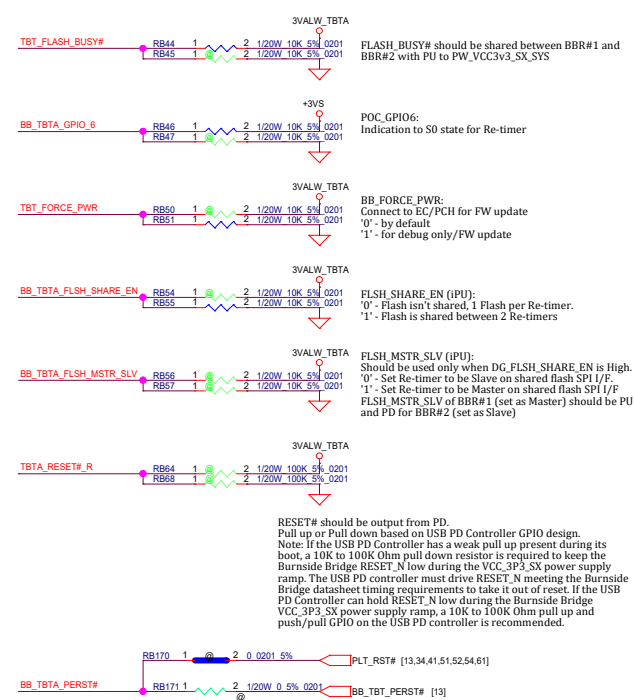
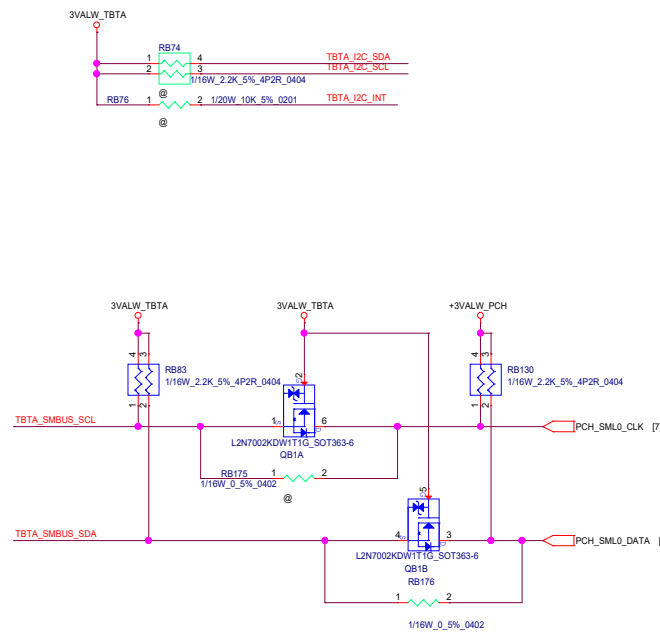
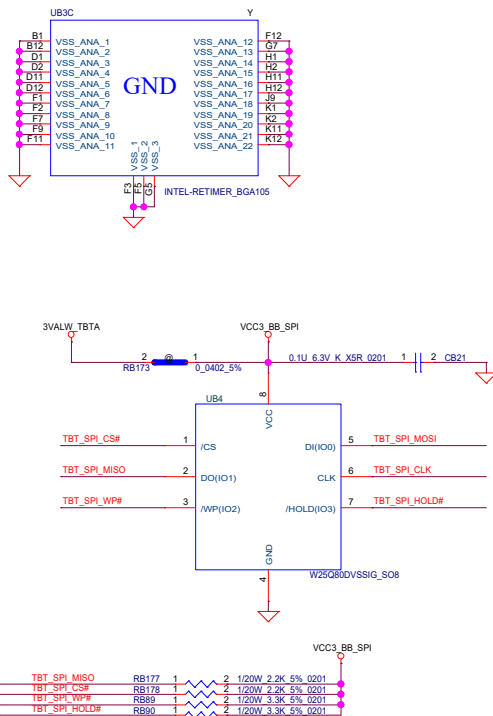
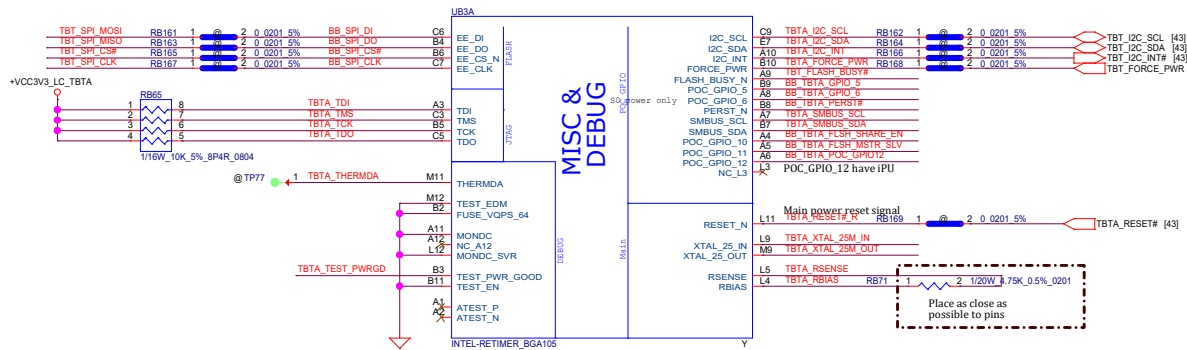
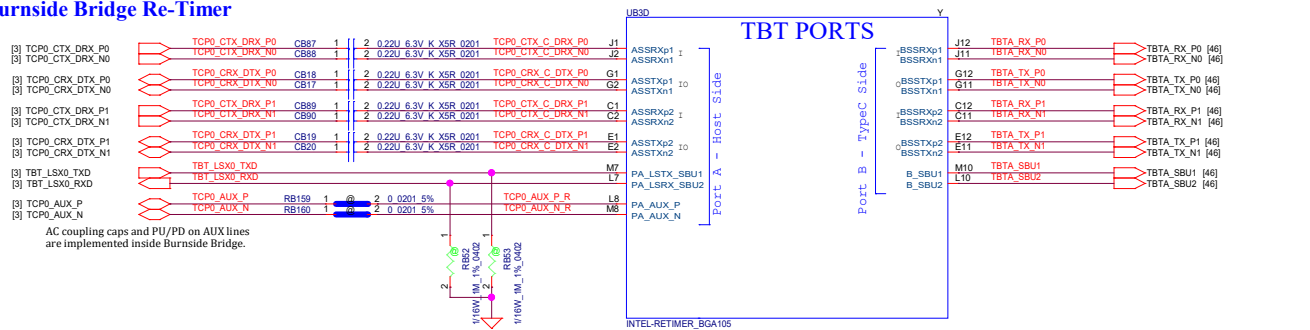



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Issued Date	2019/12/24	Deciphered Date	2019/12/24	IO BOARD CONN.		
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				<b>E14/E15 NM-D011</b>		Rev.
				Date: Tuesday, August 25, 2020		Sheet 41 of 81

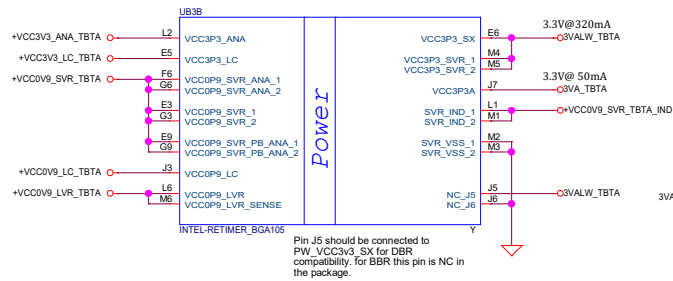
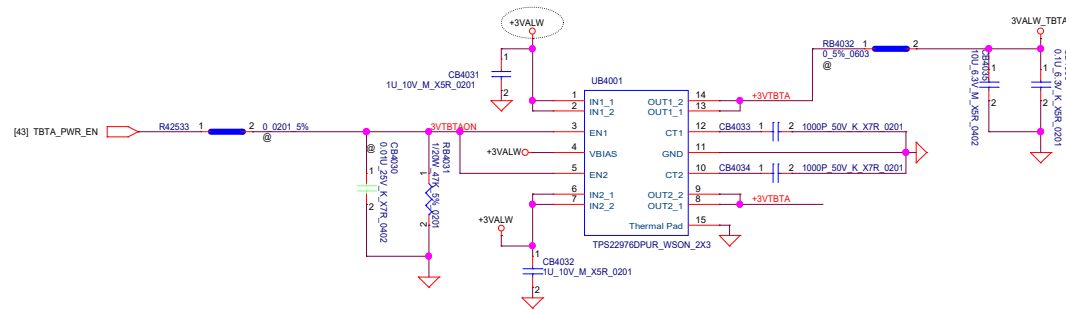
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USB TYPE-A CONNECTOR							
Size		Document Number		Revision		E14/E15 NM-D011	
Custodian		Date		Sheet		45 of 61	



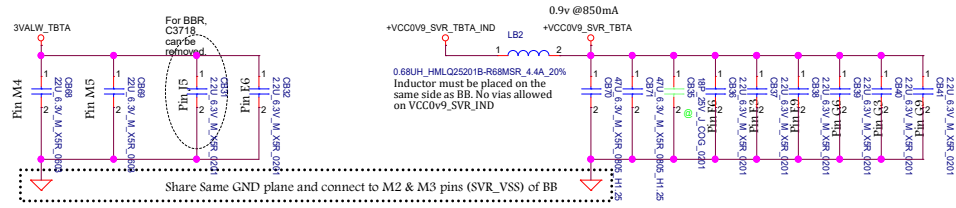
## Burnside Bridge Re-Timer



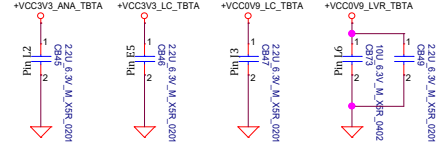
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Date		Tuesday, August 25, 2020		Sheet		44		of		81	

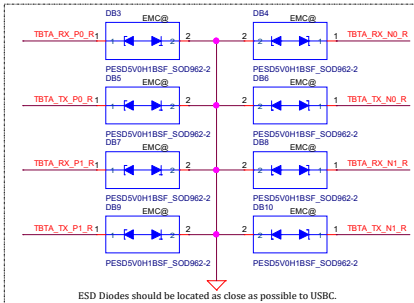
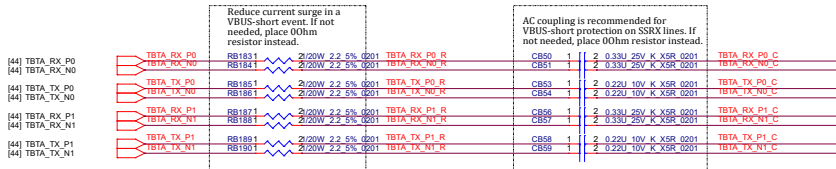


IN  
IN  
OUT

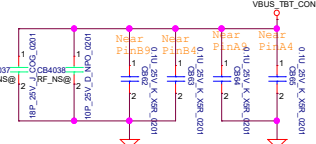
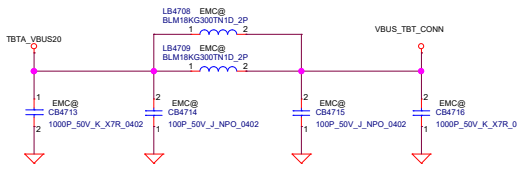
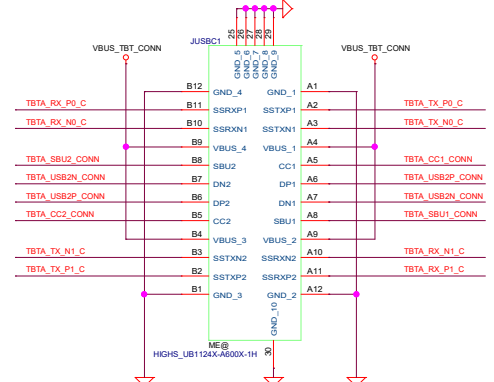
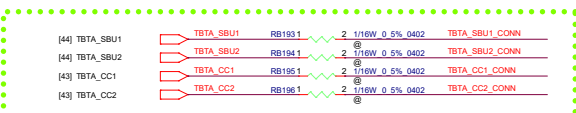
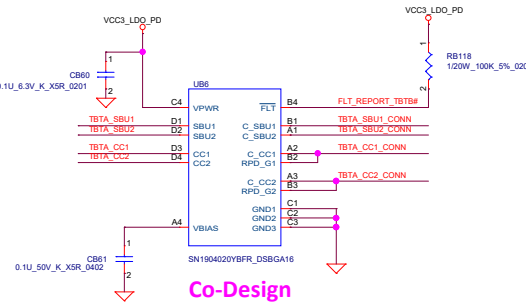
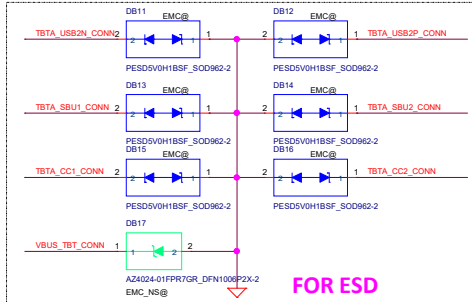
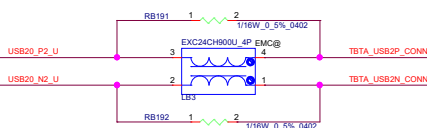
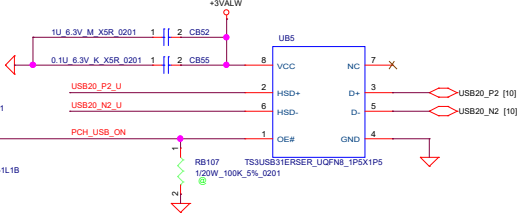
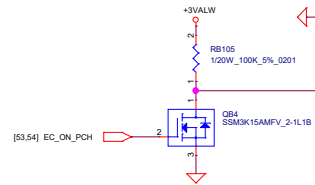
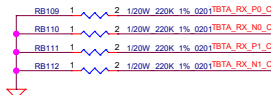


Place holder for RC filter to reduce ripple to VCC3v3A pin

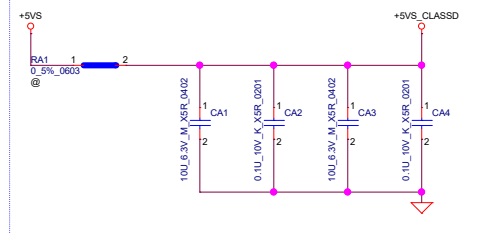




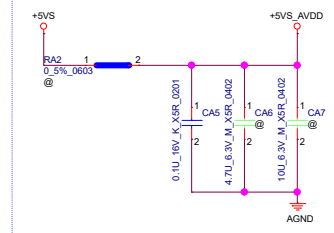
Bleeding SSTX/SSRX resistors must be placed near USB connector if 330nf cap is being used. Otherwise de-populate.



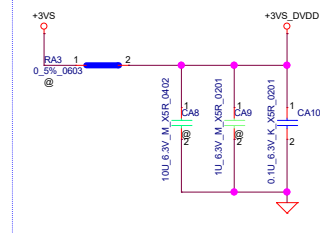
Close to Pin41,46



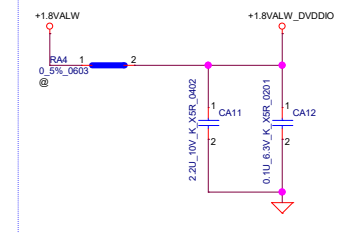
Close to Pin40



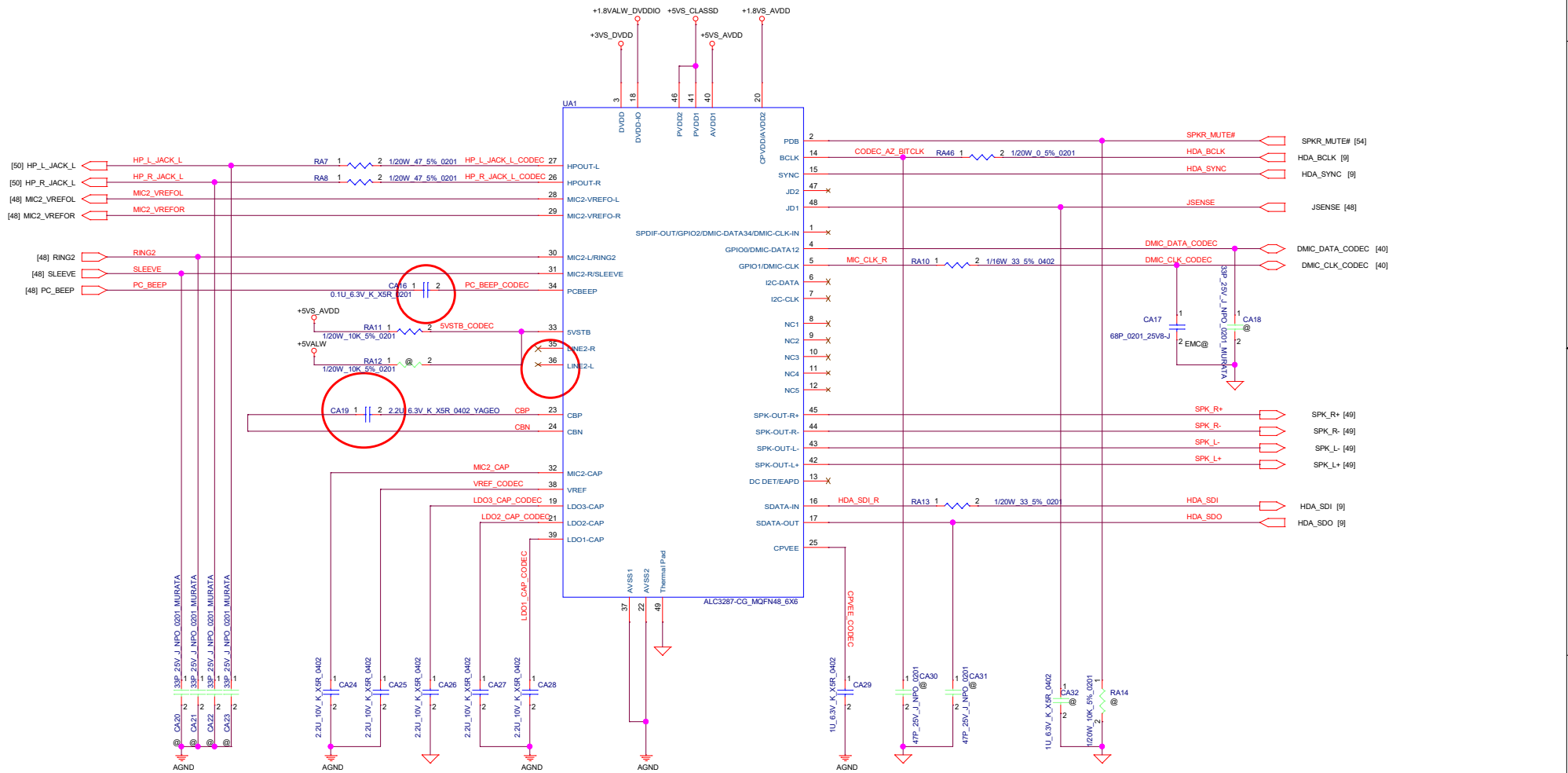
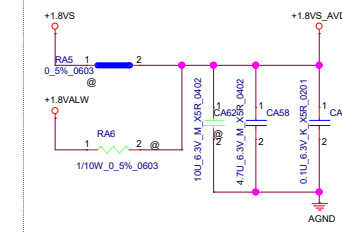
Please Close to Pin3



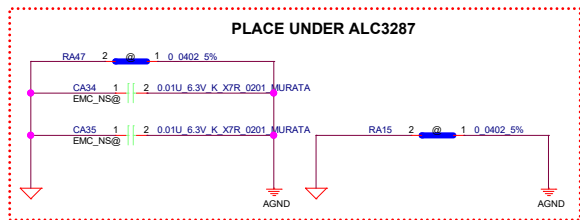
Close to Pin18

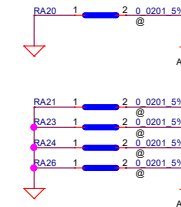
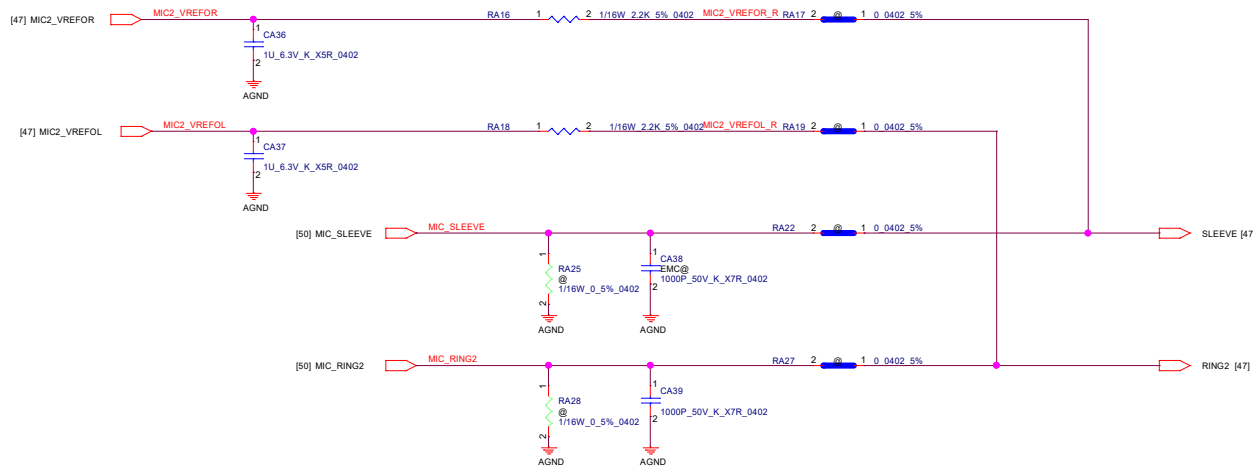


Close to Pin20



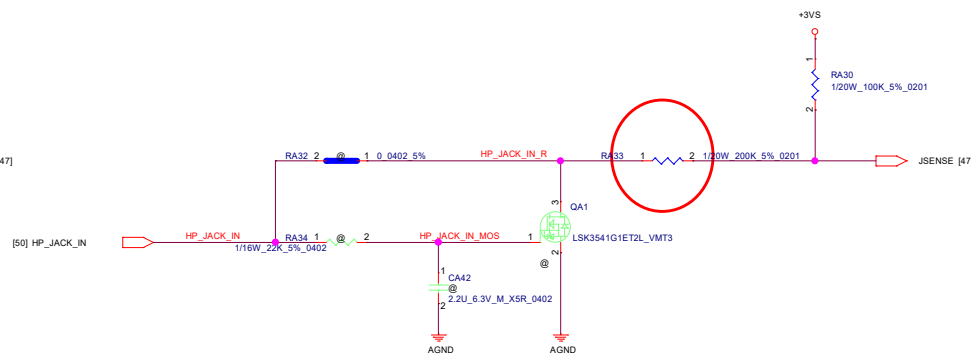
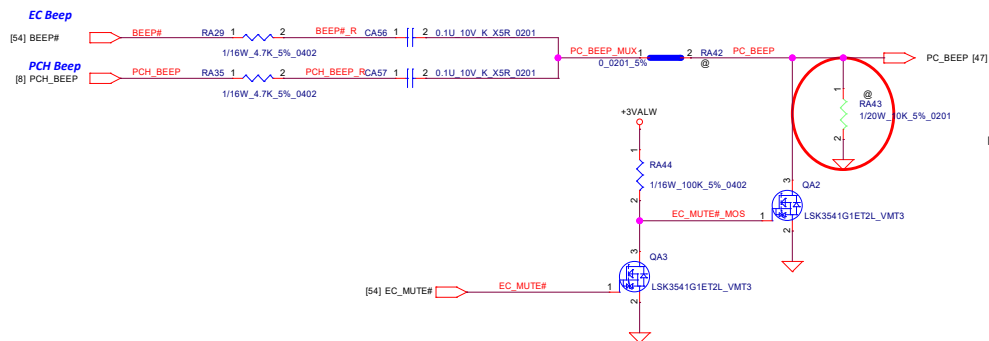
PLACE UNDER ALC3287






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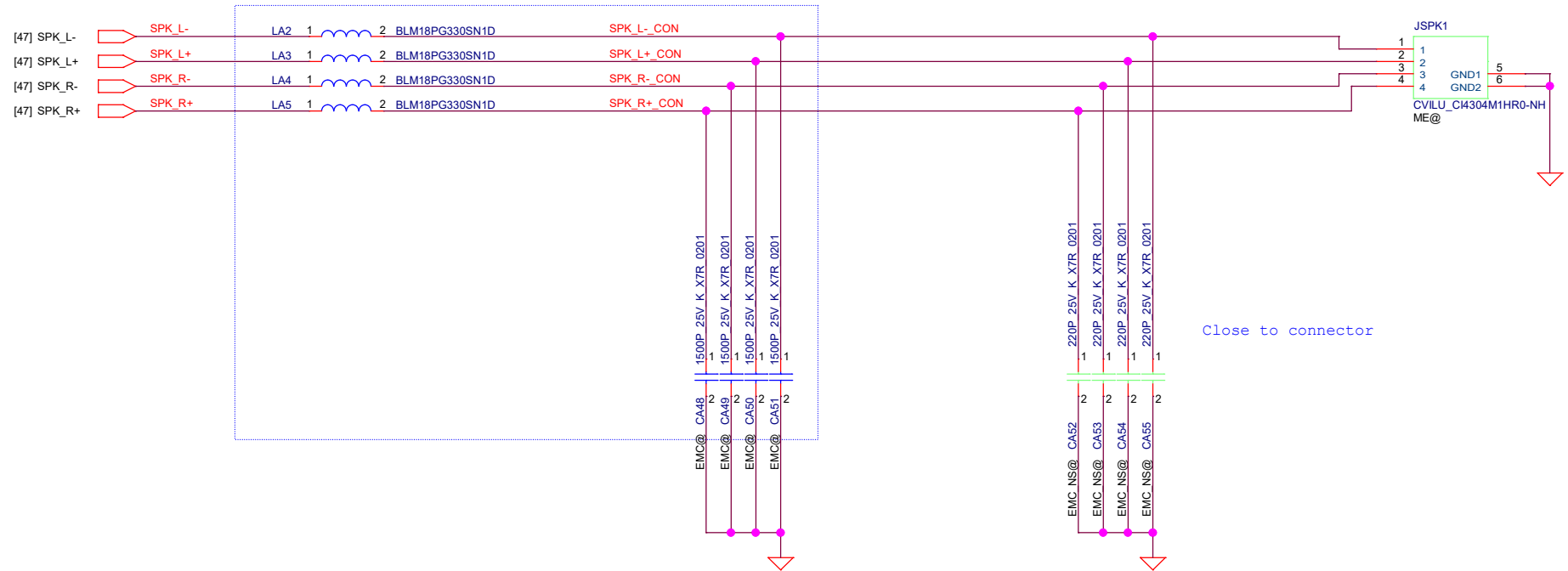
## PC Beep




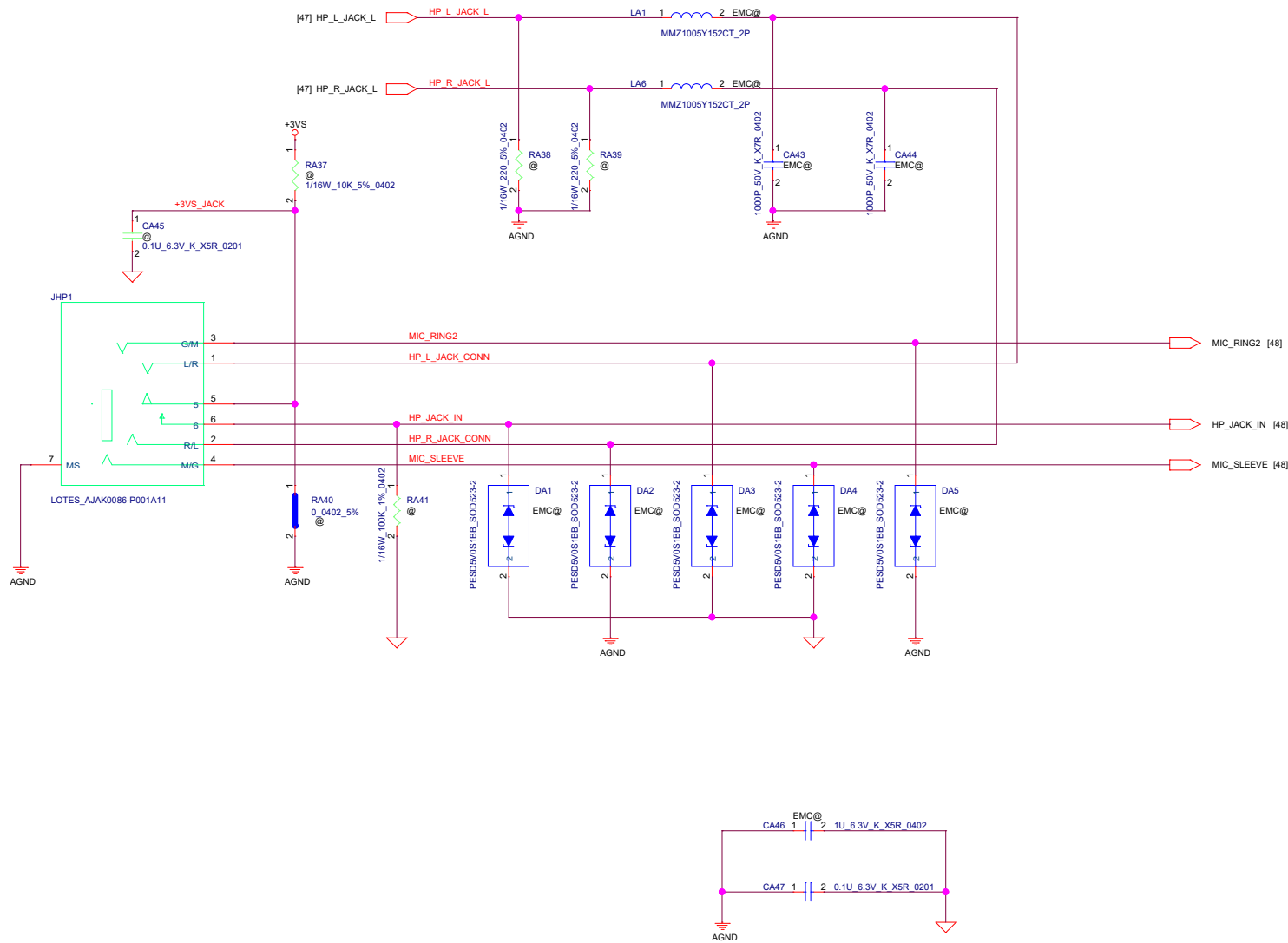
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Issued Date	2019/12/24	Deciphered Date	2019/12/24			
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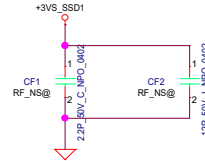
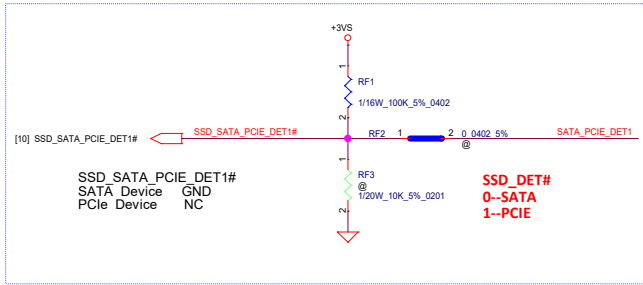
**SPK CONN.**



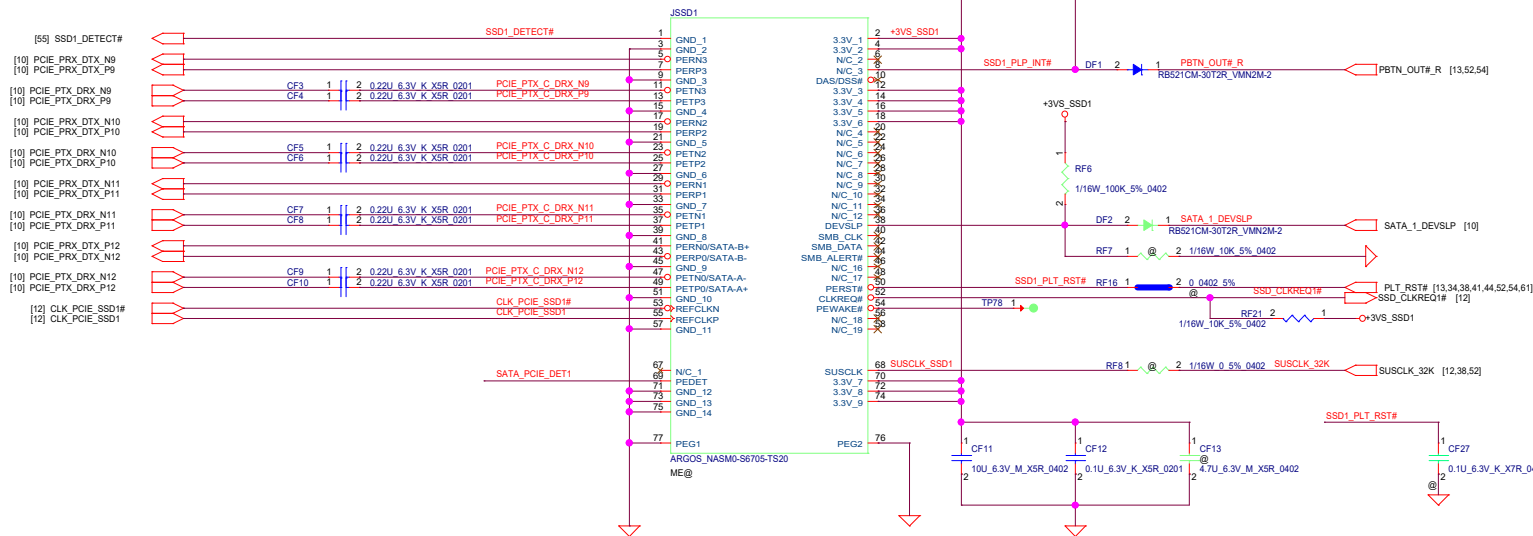
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Issued Date	2019/12/24	Deciphered Date	2019/12/24	AUDIO		
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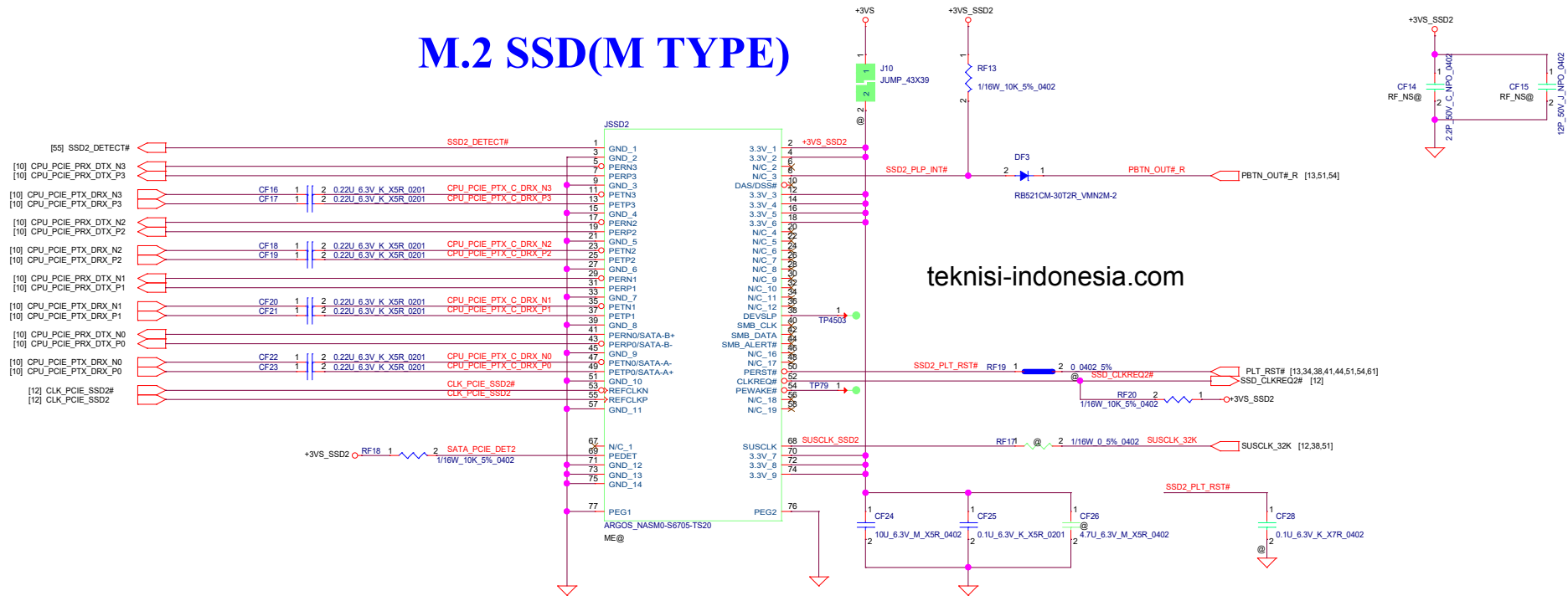
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Issued Date	2019/12/24	Deciphered Date	2019/12/24
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Size	Custom	Document Number	E14/E15 NM-D011
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## M.2 SSD(M TYPE)

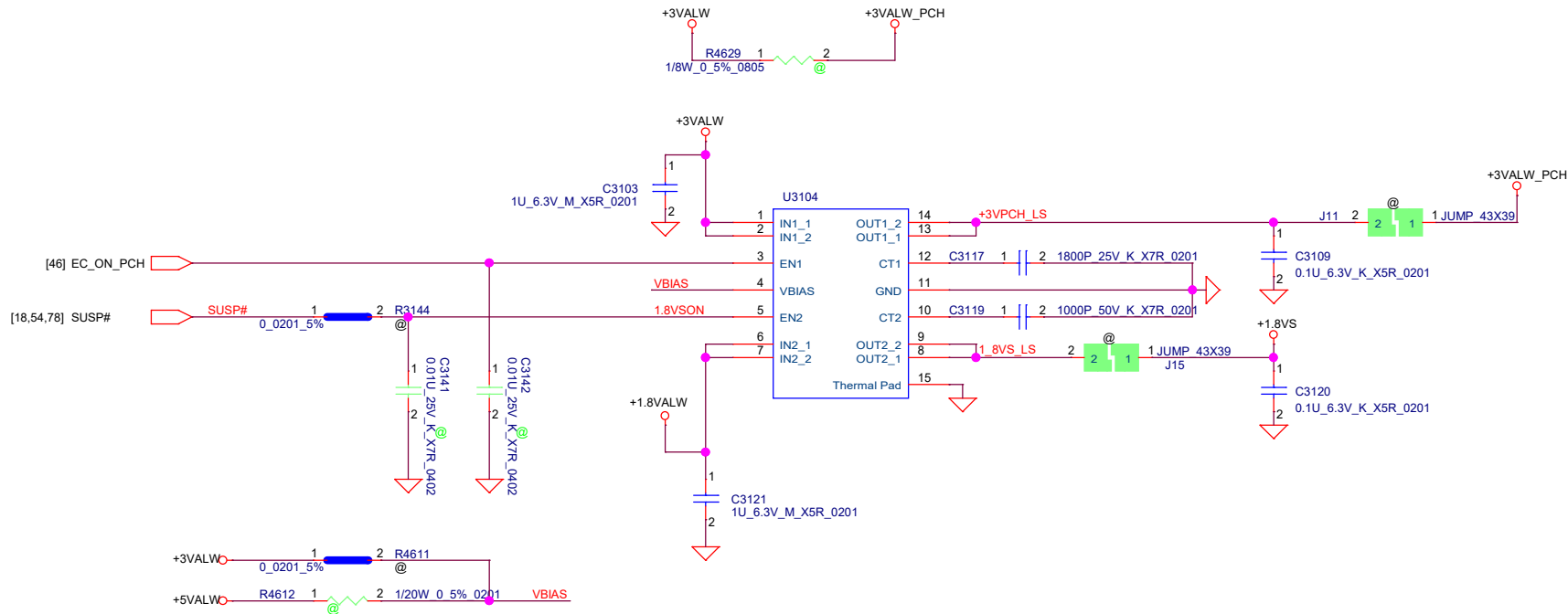


# M.2 SSD(M TYPE)



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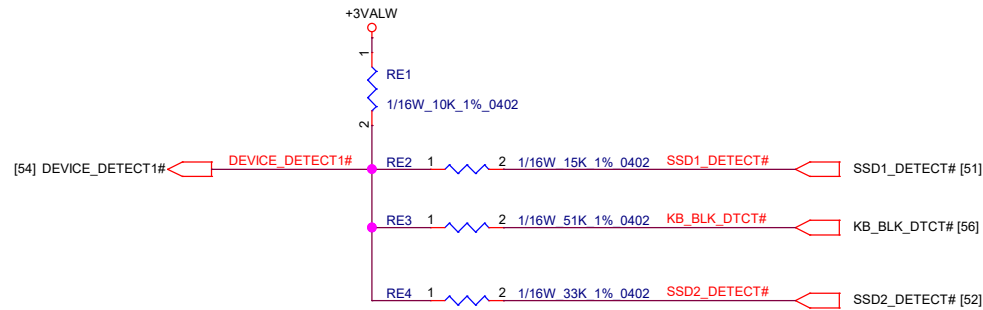
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Issued Date		2019/12/24		M.2 SOCKET PCIE GEN4 MODUL IFC	
Deciphered Date		2019/12/24		Size   Document Number	
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Size	Document Number		
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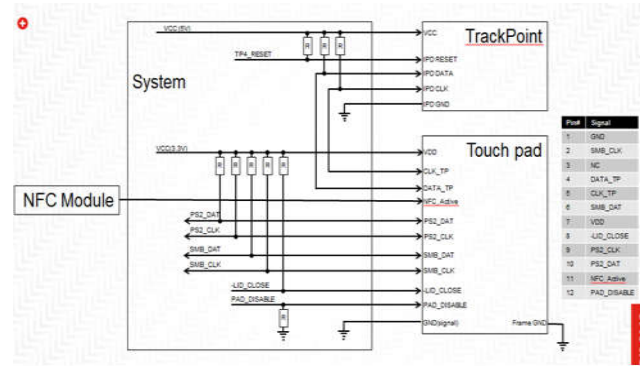
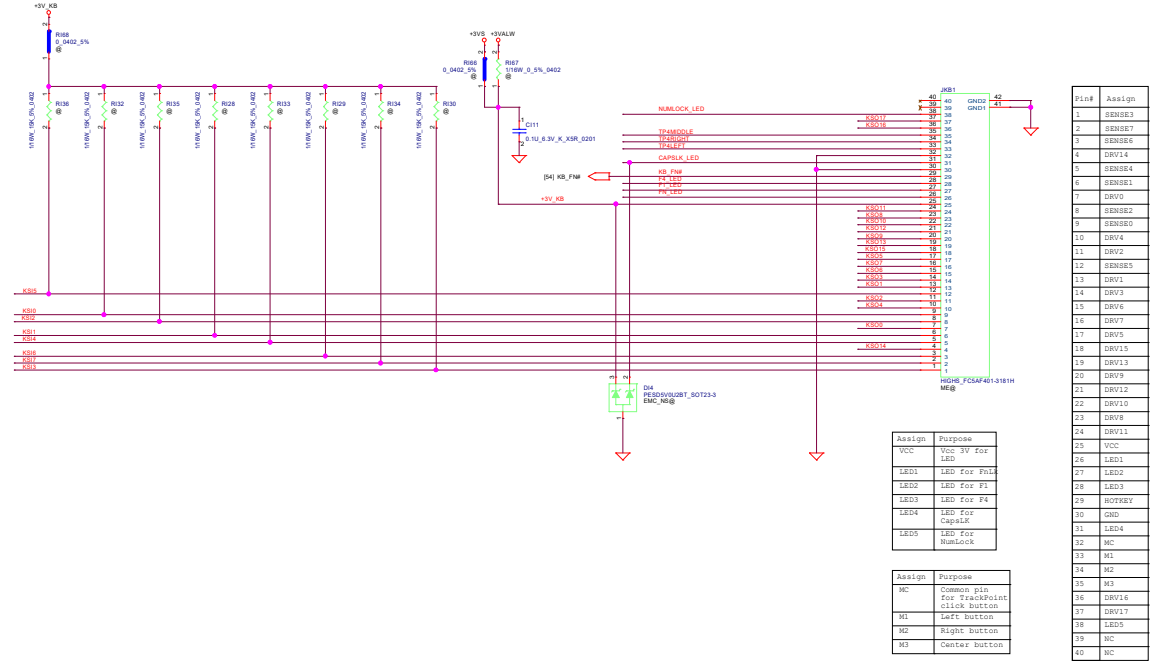
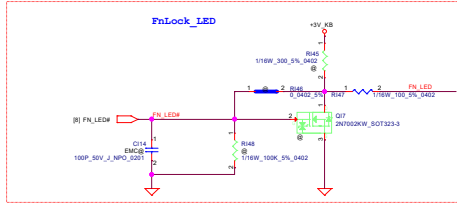
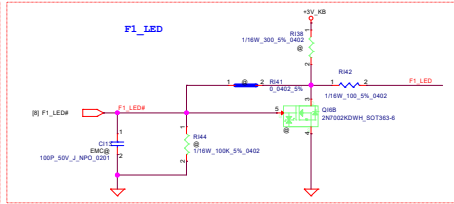
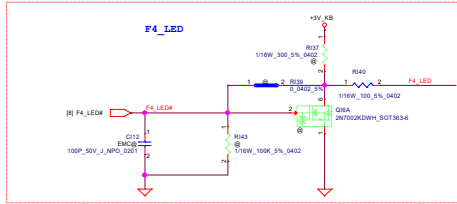
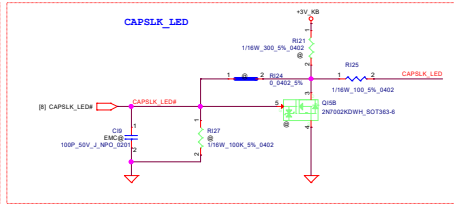
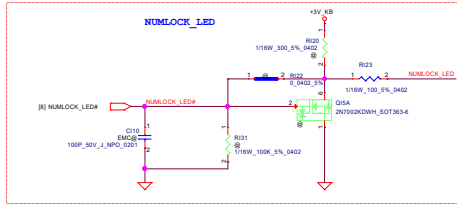




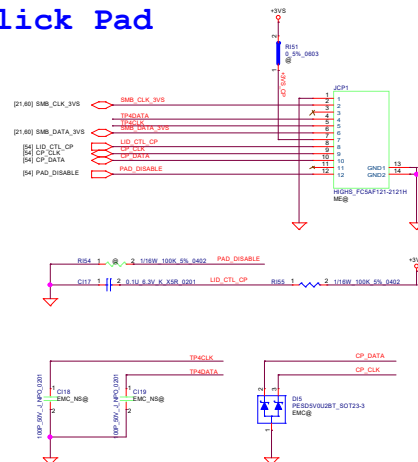
Vcc	3.3V					
RE1	10K +/- 5%					
DEVICE_DETECT1#	1.98V	1.675V	1.772V	2.759V	2.533V	3.3V
SSD1_DETECT#	V	V	V	X	X	X
KB_BLK_DTCT#	X	V	X	X	V	X
SSD2_DETECT#	X	X	V	V	X	X

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# Keyboard CONN

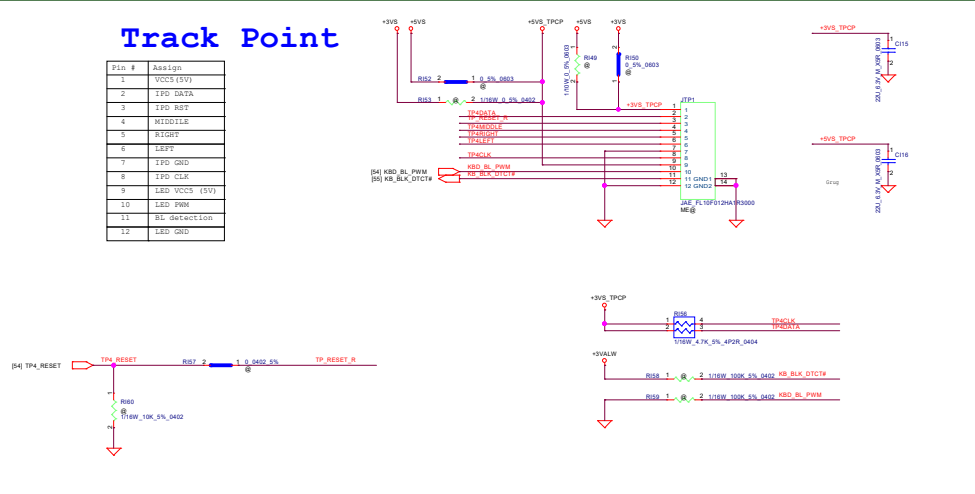


## Click Pad

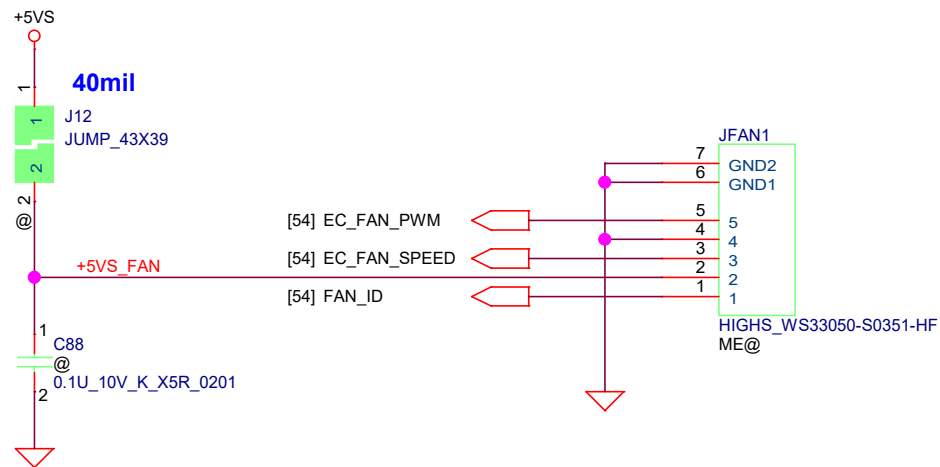


## Track Point


Pin #	Assign
1	VCC3 (3V)
2	TPD DATA
3	TPD RST
4	WIDTCLK
5	RIGDS
6	LEFT
7	TPD GND
8	TPD CLK
9	LED VCC3 (3V)
10	LED PM
11	LED SW
12	LED GND







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APS G-Sensor

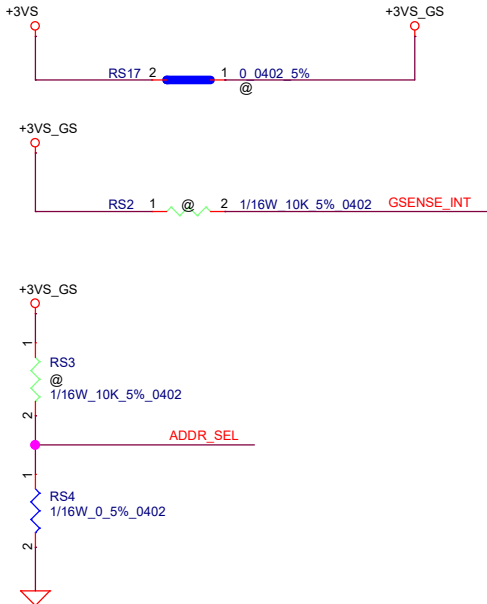
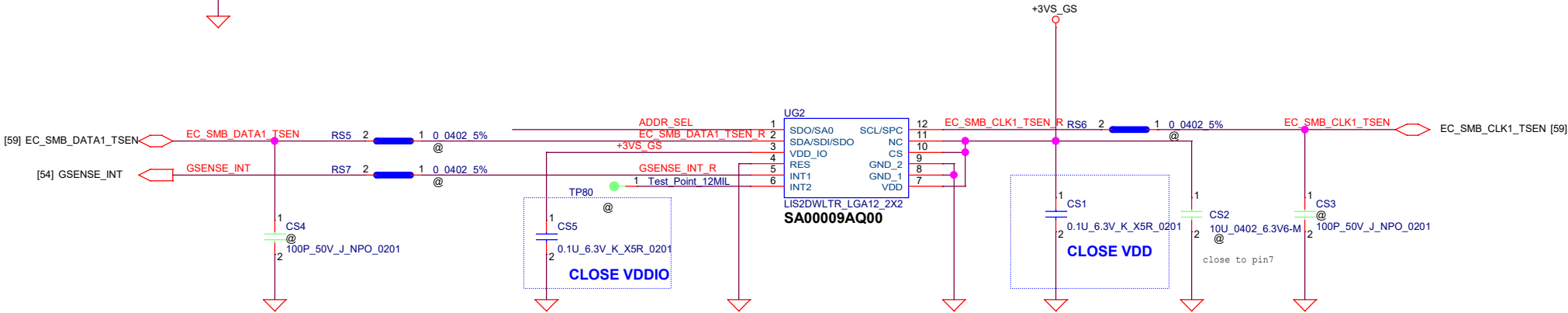


TABLE of G-Sensor (UG1)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00
BOSCH	BMA280	SA0000A1600

TABLE		
P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)
BMA280	H	0X18
	L	0X19



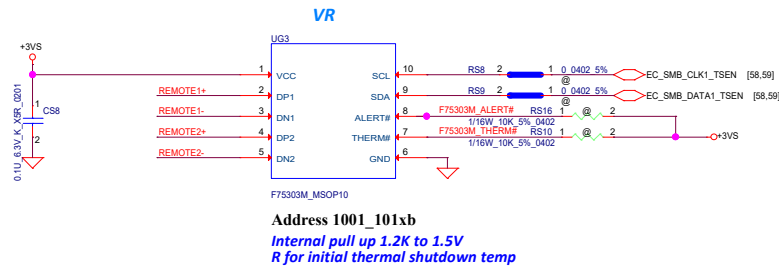
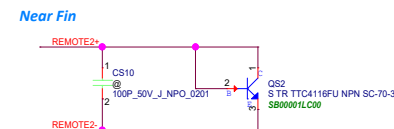
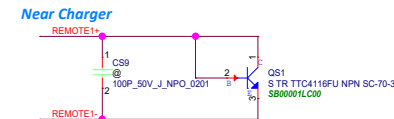
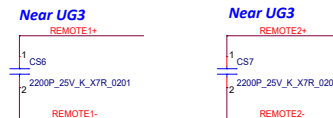
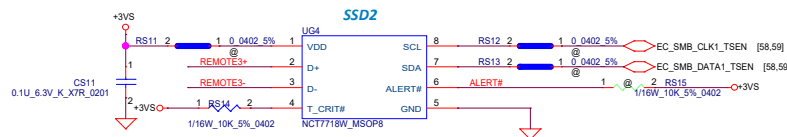


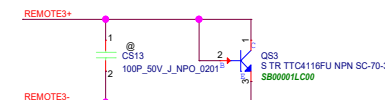
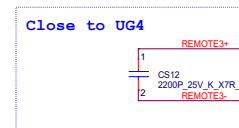
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Vendor	LCFC P/N	Description
FINTEK	SA000046C0J	S IC F75303M MSOP 10P SENSOR



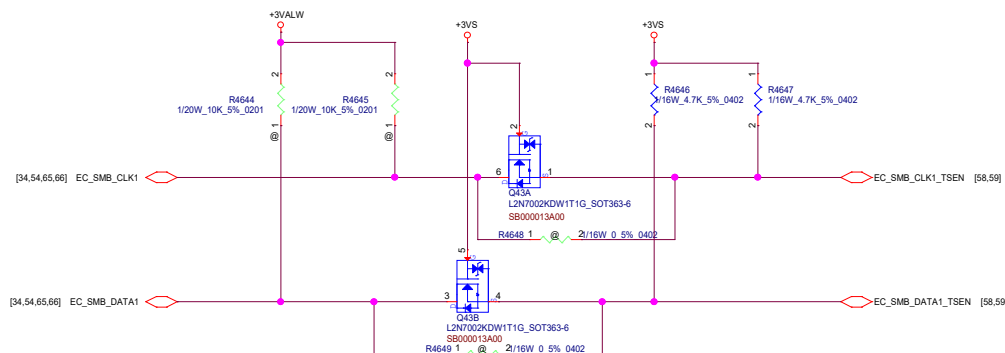
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Trace width/space:10/10 mil  
Trace length:<8"



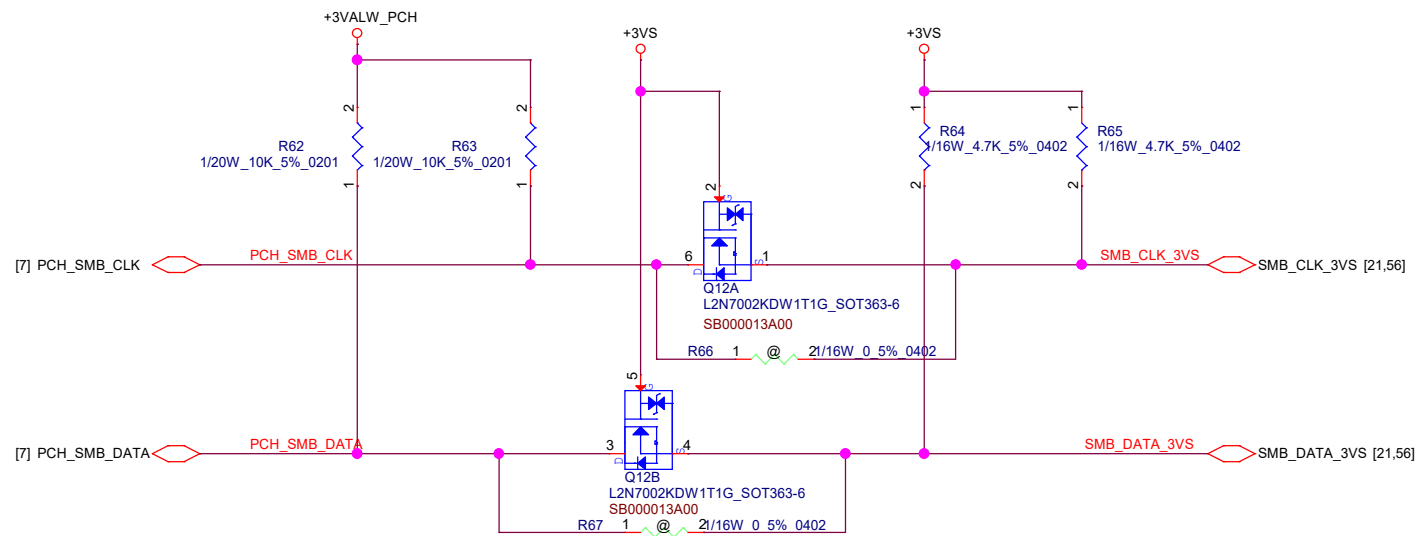
NCT7718W I2C  
C/ SMBus™ address is 1001100xb (x is R/W bit).




REMOTE+/-\_R, REMOTE1+/-, REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"



# DIMM1,CP



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TPM IC

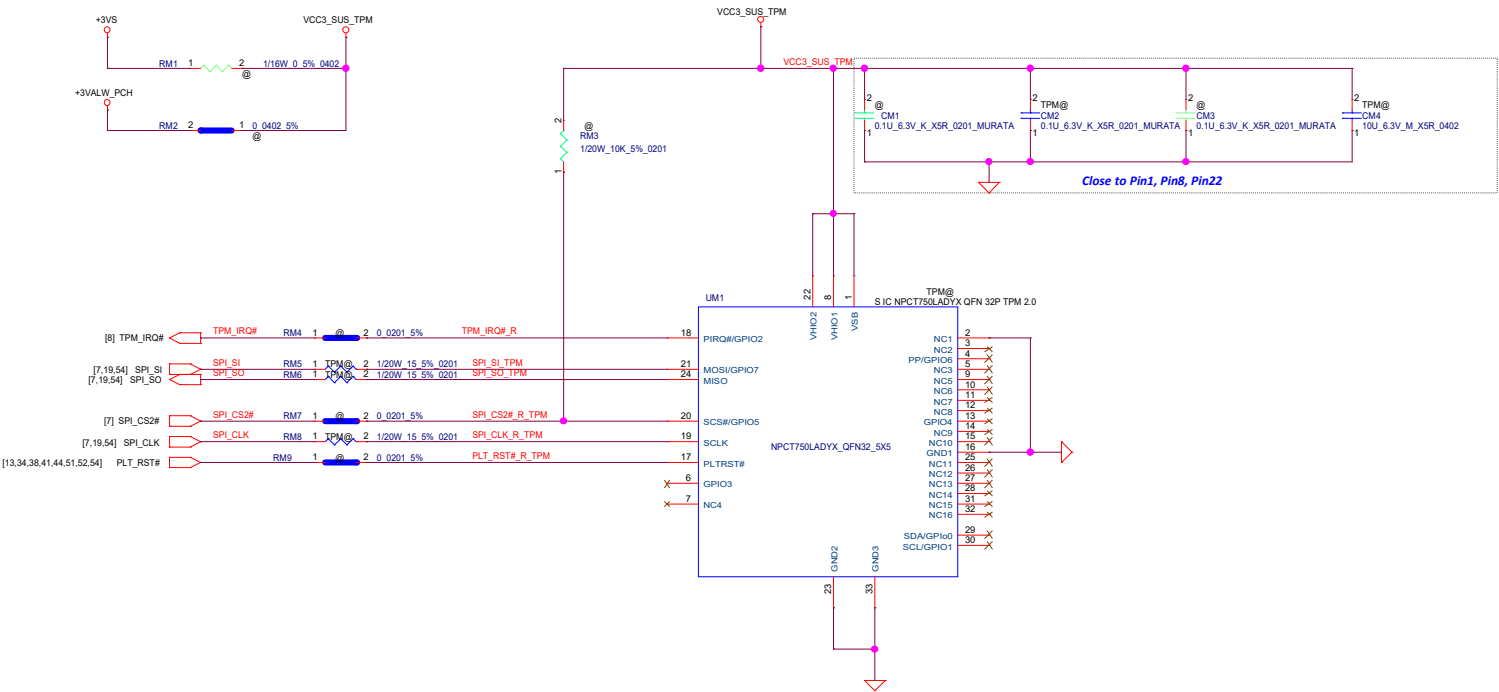
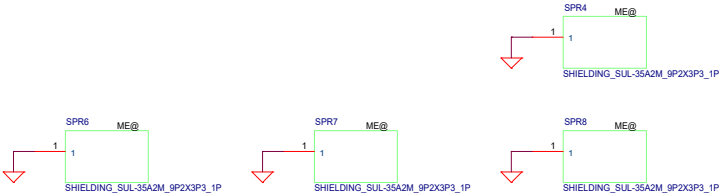
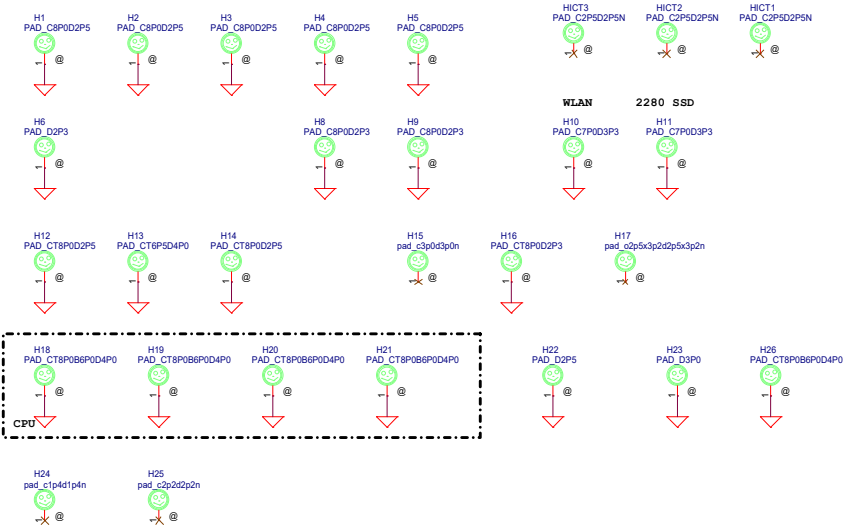


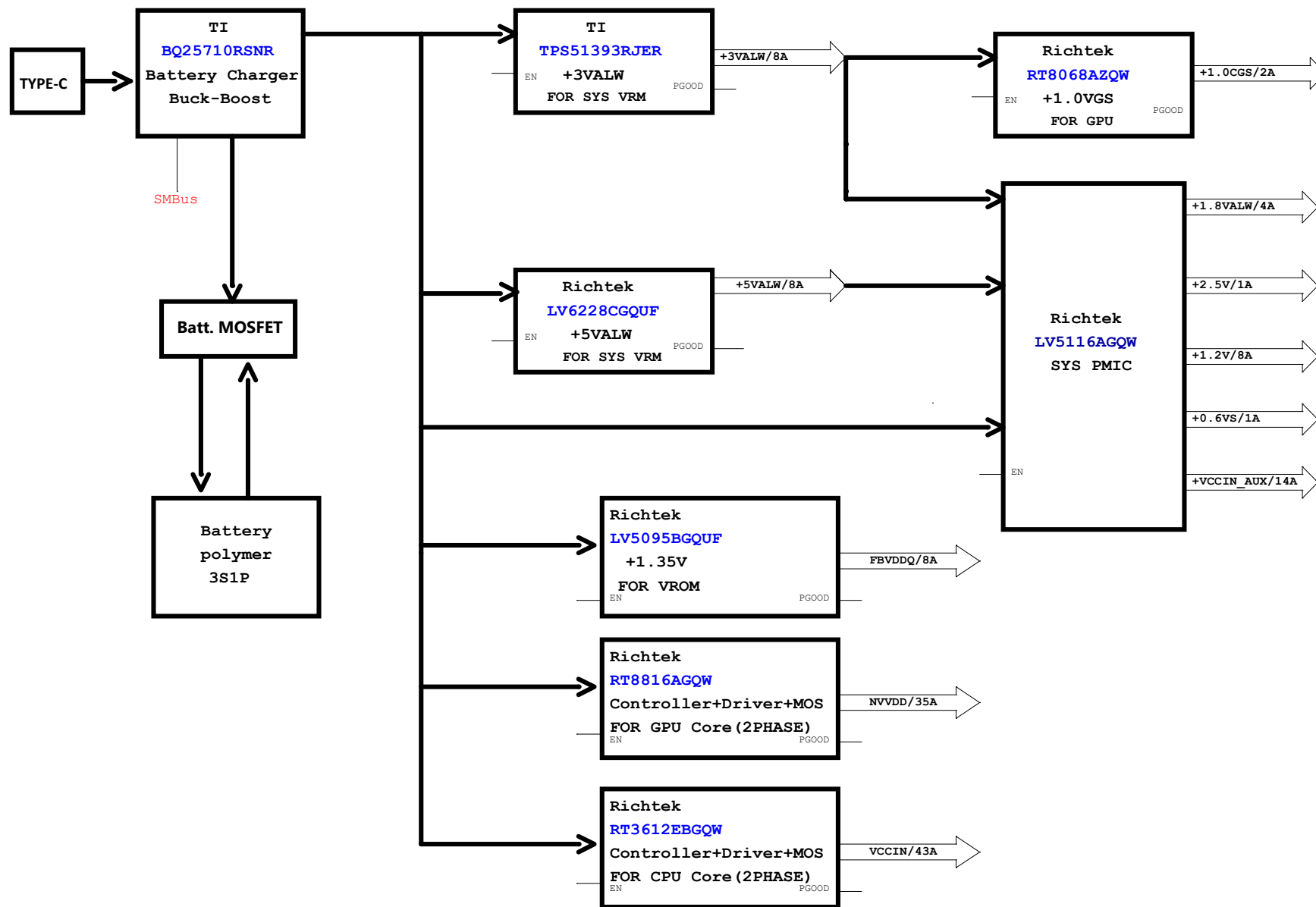
TABLE of TPM (UM1)		
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Nuvoton	NPCT750LADYX	SA00008KS30
ST Micro	ST33HTPH2X32AHD8	SA0000AB720

Screw Hole




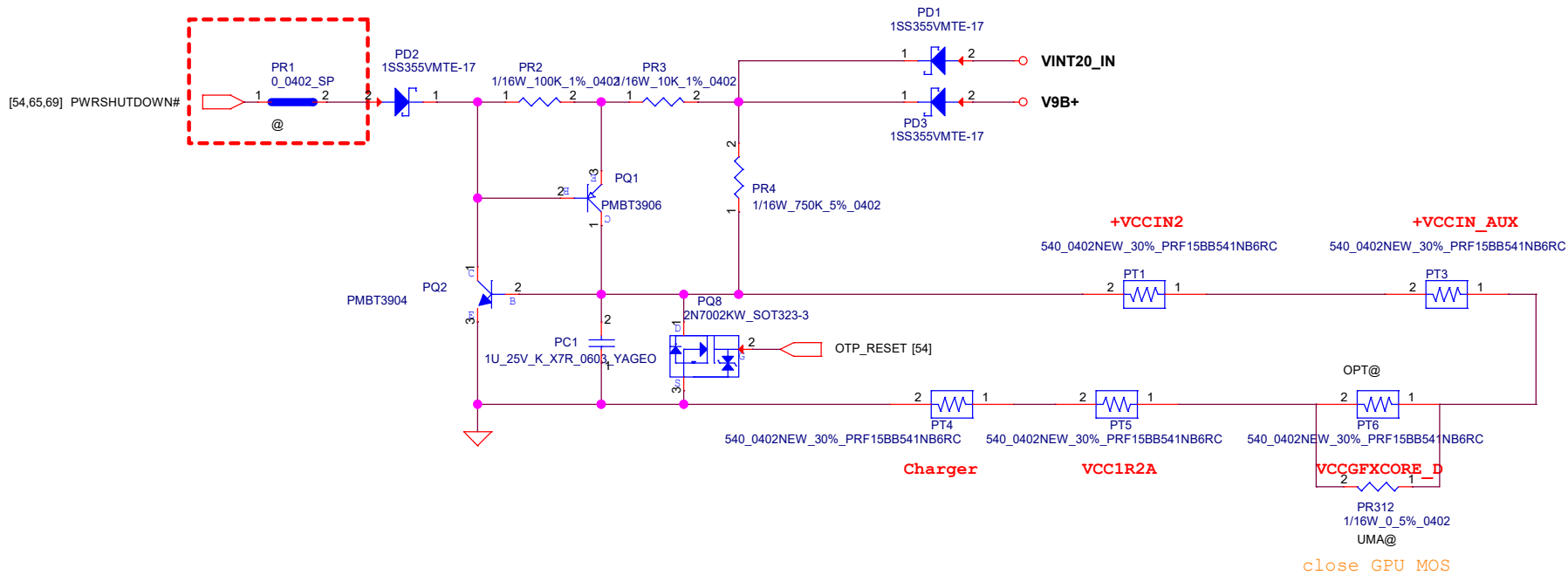
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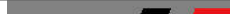




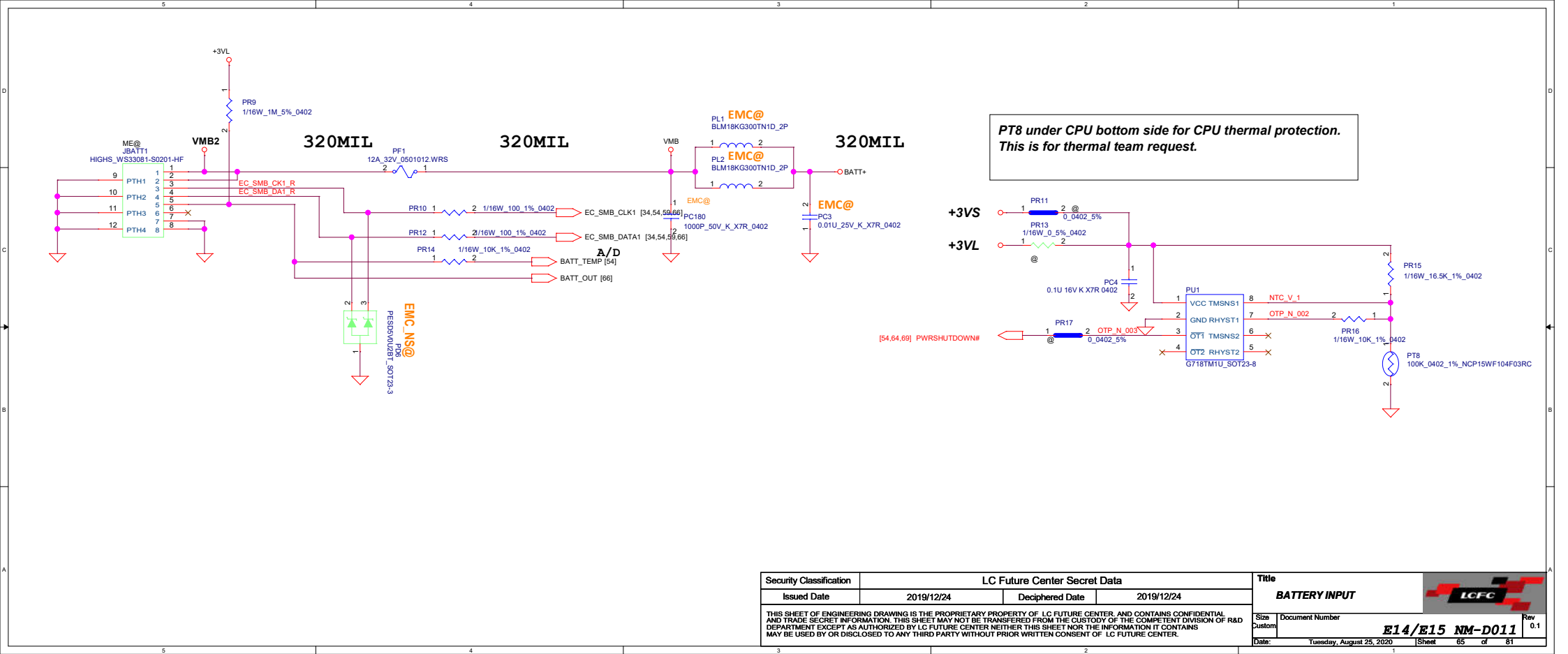
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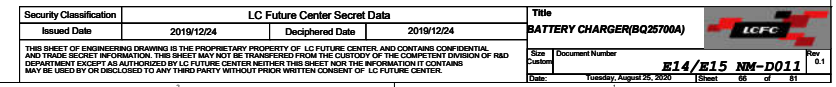
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				E14/E15 NM-D011		








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Issued Date					2019/12/24					Deciphered Date					2019/12/24					PWR_3VALW/5VALW									
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															E14/E15 NM-D011										0.1				
										Date:					Tuesday, August 25, 2020					Sheet					67 of 81				
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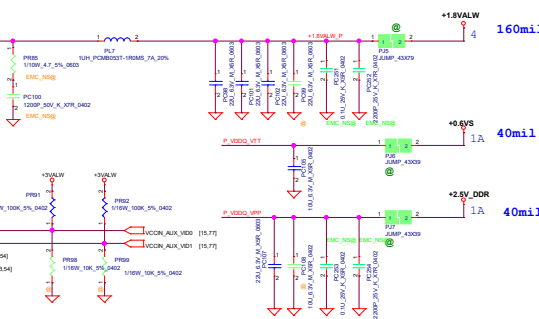
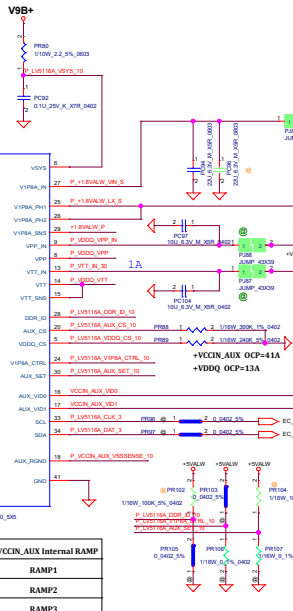
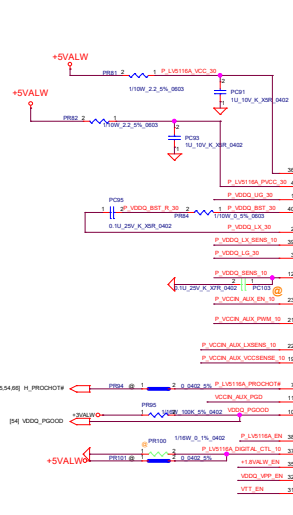
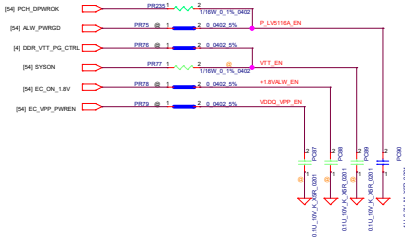
Security Classification	LC Future Center Secret Data			Title						
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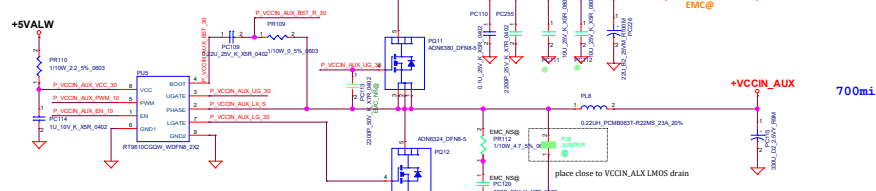
DIGITAL_CTRL	Control Mode
High	HW Control
Low	SW Control

AUX_SET	VCCIN_AUX Internal RAMP
High	RAMP1
Low	RAMP2
Floating	RAMP3

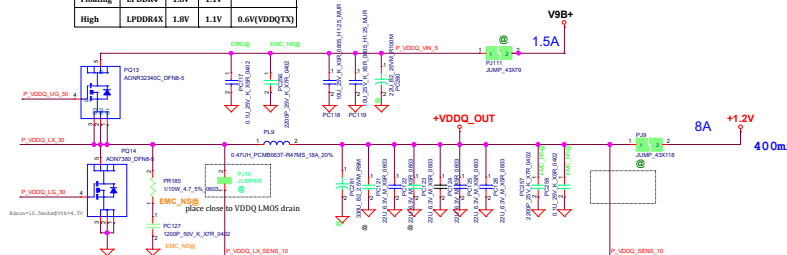
AUX_VID	AUX_VID0	Vout_AUX
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

DIGITAL_CTRL	VIPIA_CTRL	VIPIA Sequence
High	Low	VIPIA follow PMIC_EN
High	High	VIPIA follow SLP_SUS#
Low	Low	VIPIA follow PMIC_EN
Low	High	VIPIA follow I2C

DDR_ID	Type	VPP	VDDQ	VTT/VDDQTX
Low	DDR4	2.5V	1.2V	VDDQ/2(VTT)
Floating	LPDDR4	1.8V	1.1V	--
High	LPDDR4X	1.8V	1.1V	0.6V(VDDQTX)




Vboot=1.8V Loadline=6mG  
 ACDC Ripple=(-10%+5%)\*VOUT  
 TDC=14A Iccmax=32A  
 CURRENT LIMIT=45A  
 Max Overshoot=2.13V/500us  
 OVP=(1.2-1.3)\*Vref  
 OVP=(0.45-0.55)\*Vref  
 Psw=600ns

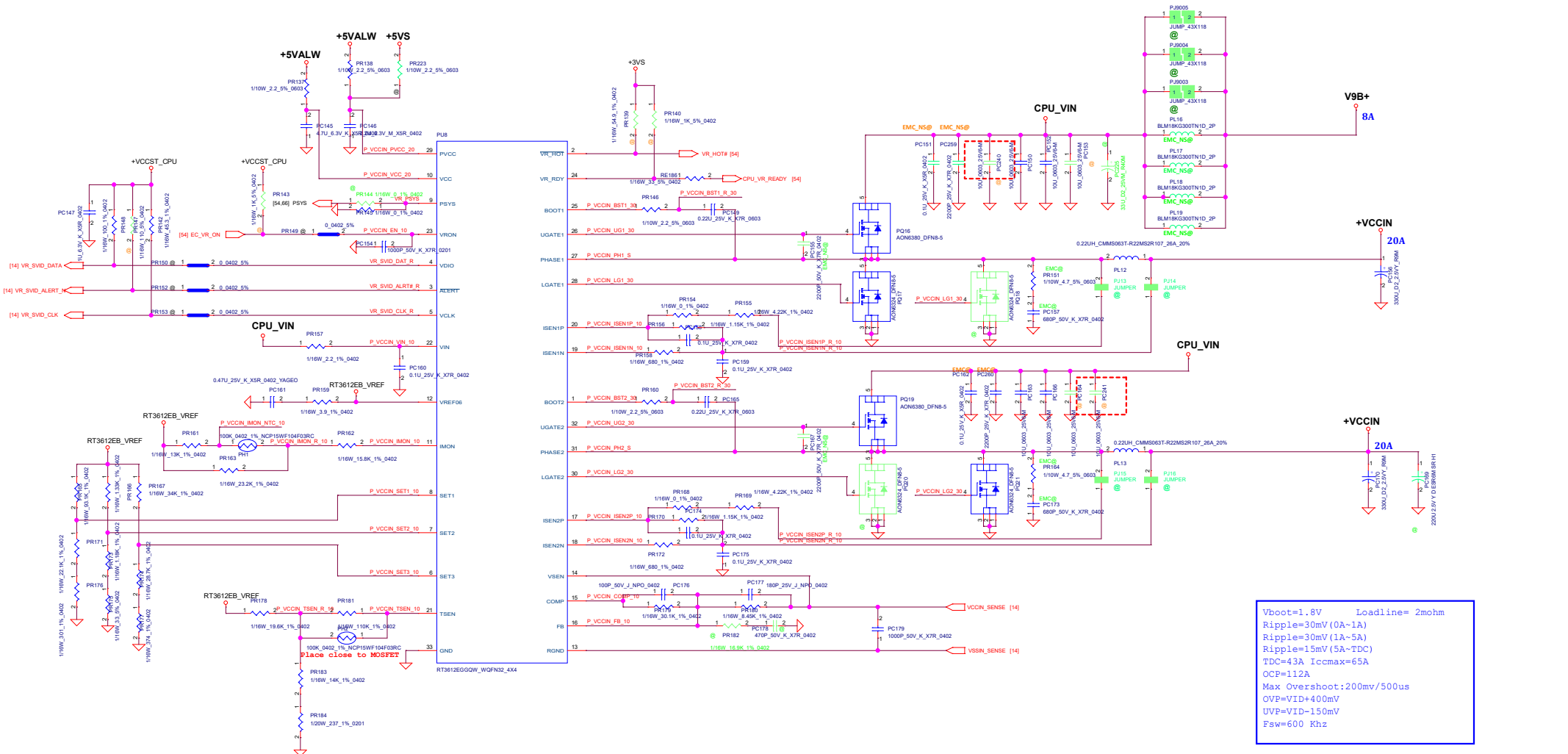



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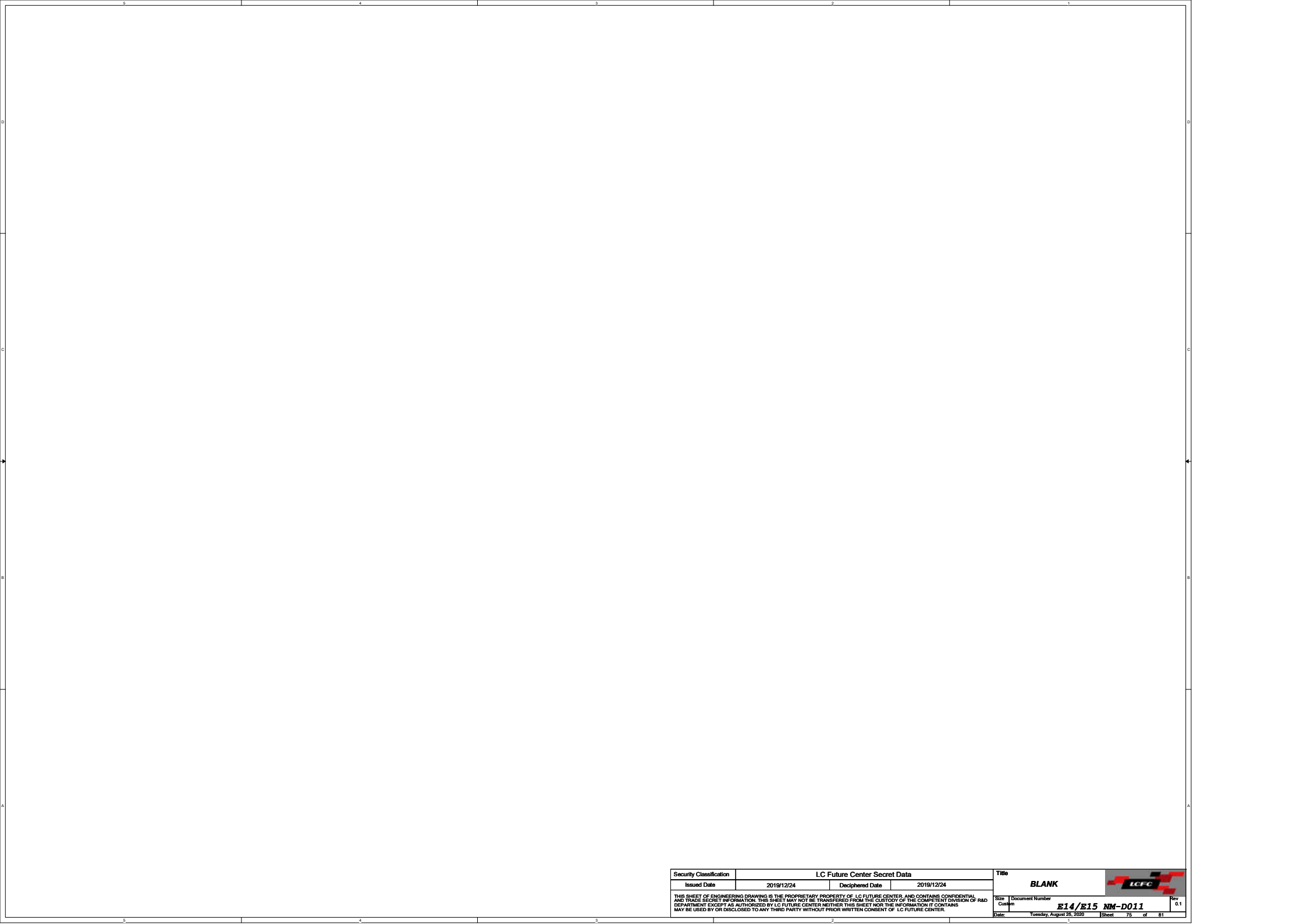



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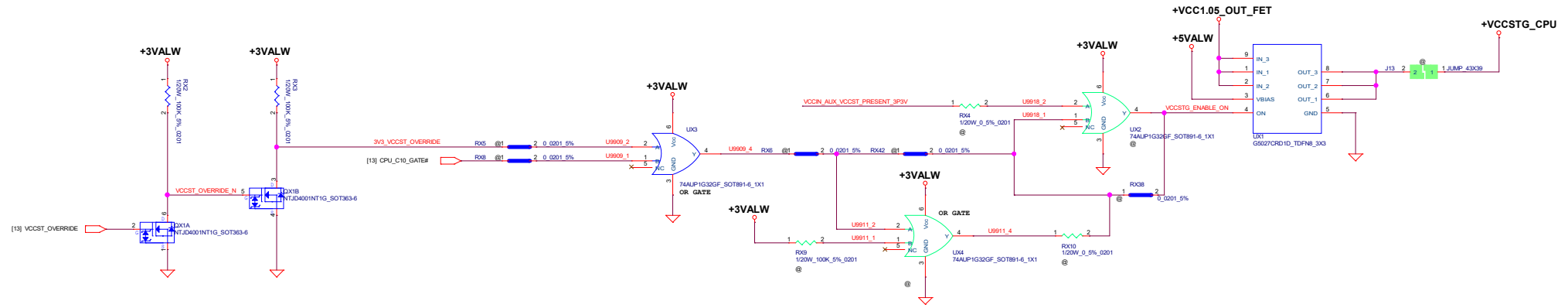
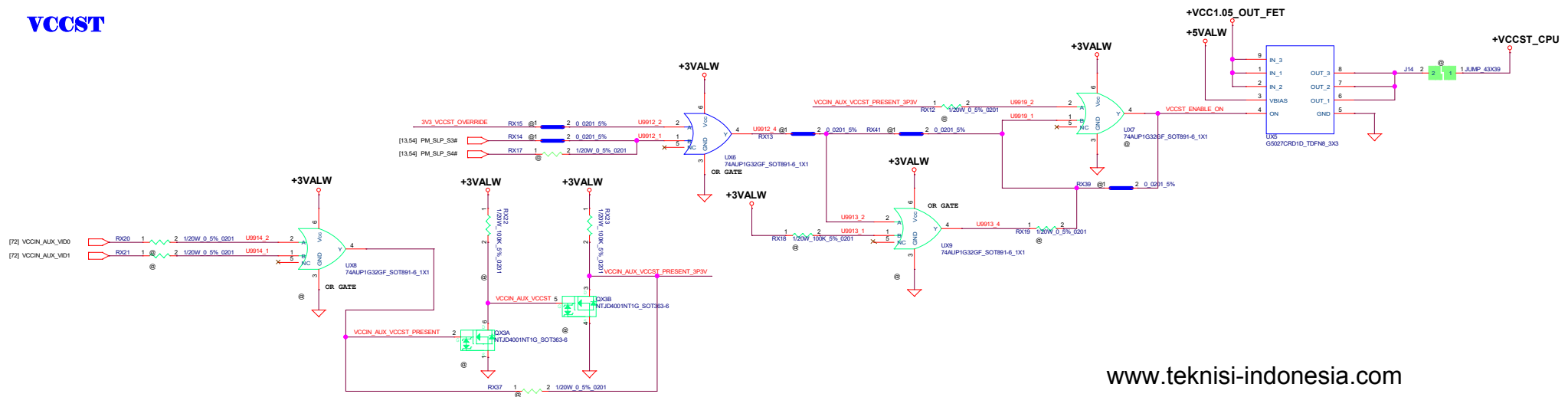
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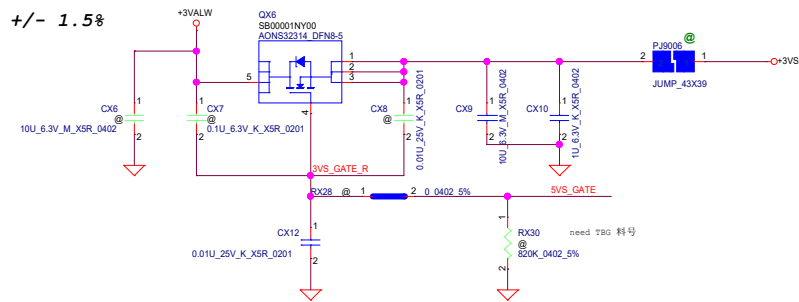
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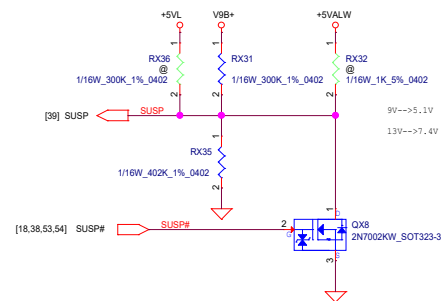
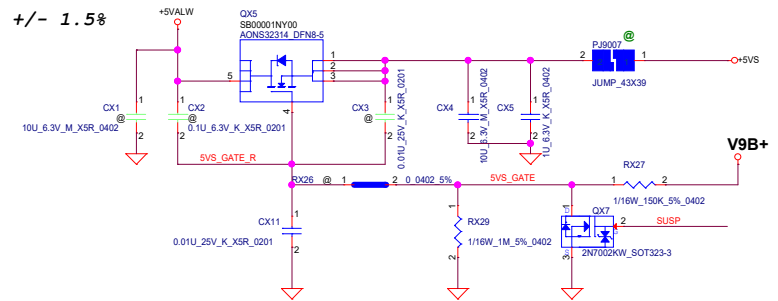
+/- 1.5%

Load MOS N MOS Id =< 40A Vgs(th) Max >= 2.6V  
Rds(on) >= 7.5mohm

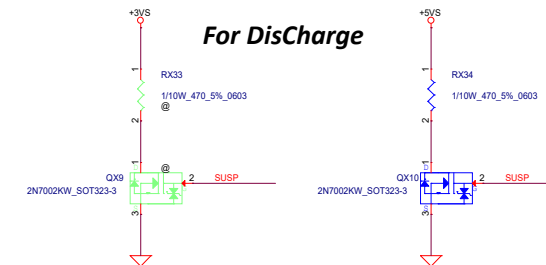



**+/- 1.5%**

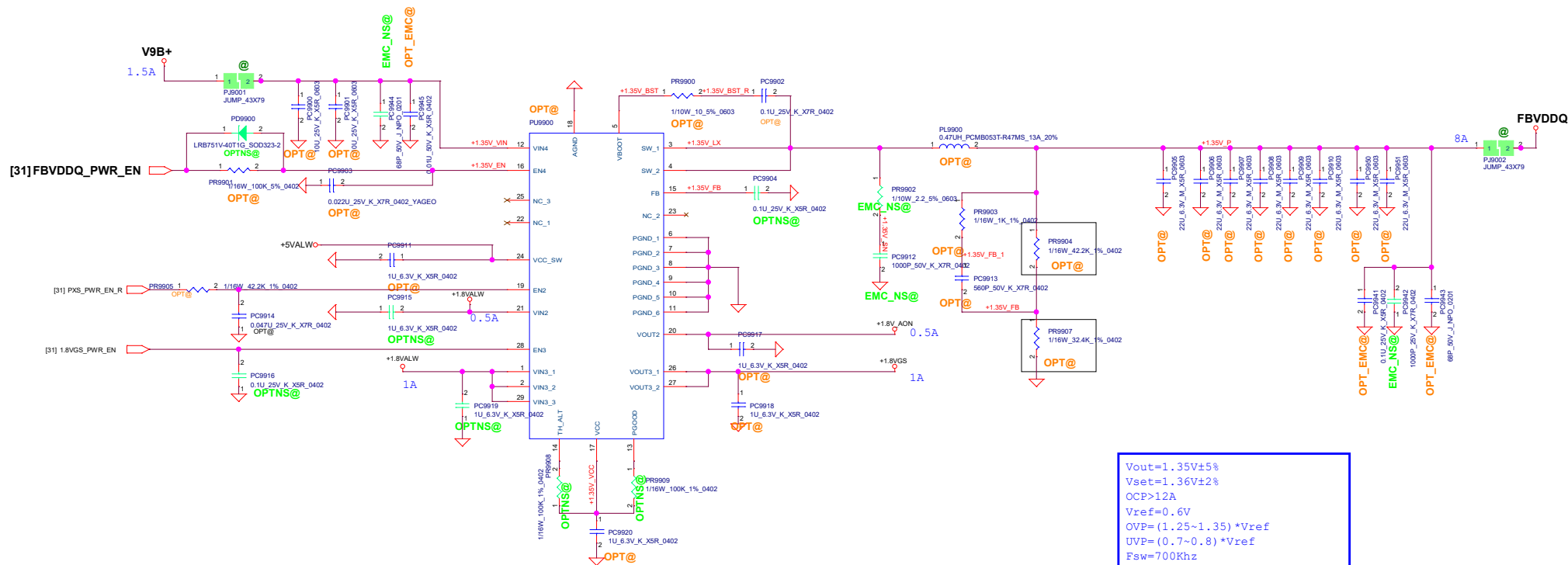
Load MOS N MOS Id =< 40A Vgs(th) Max >= 2.6V  
Rds(on) >= 7.5mohm



***For DisCharge***

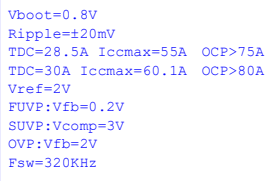


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Vout=1.35V±5%  
 Vset=1.36V±2%  
 OCP>12A  
 Vref=0.6V  
 OVP=(1.25~1.35)\*Vref  
 UVP=(0.7~0.8)\*Vref  
 Fsw=700KHz  
 LSW1 RDS=36~50mohm, Io=0.5A  
 LSW2 RDS=18~25mohm, Io=1A  
 LSW3 RDS=5~7mohm, Io=3.5A

RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM



UPI\_OPT@ : for UP1666  
RT\_OPT@ : for RT8816A

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