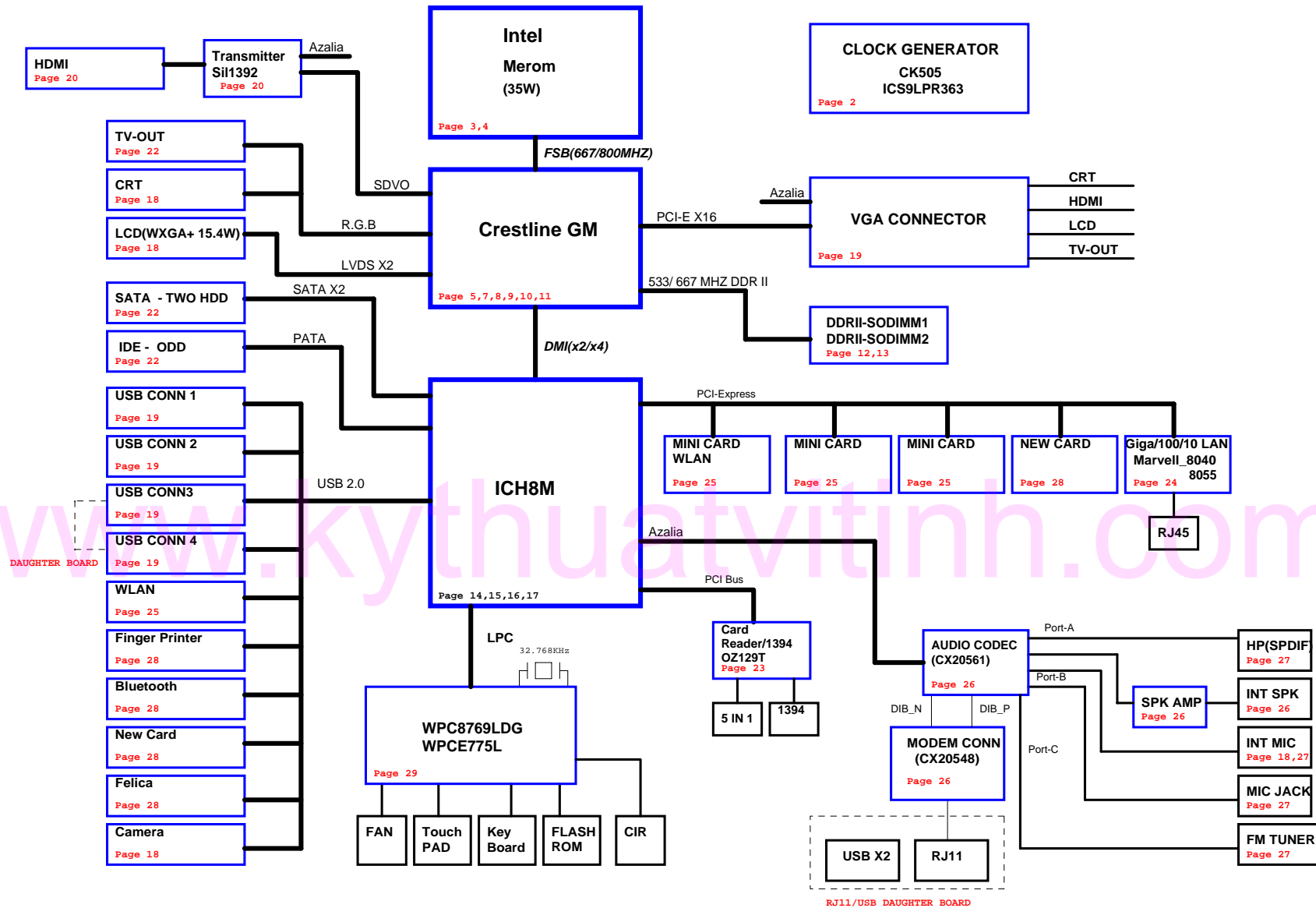


PCB STACK UP

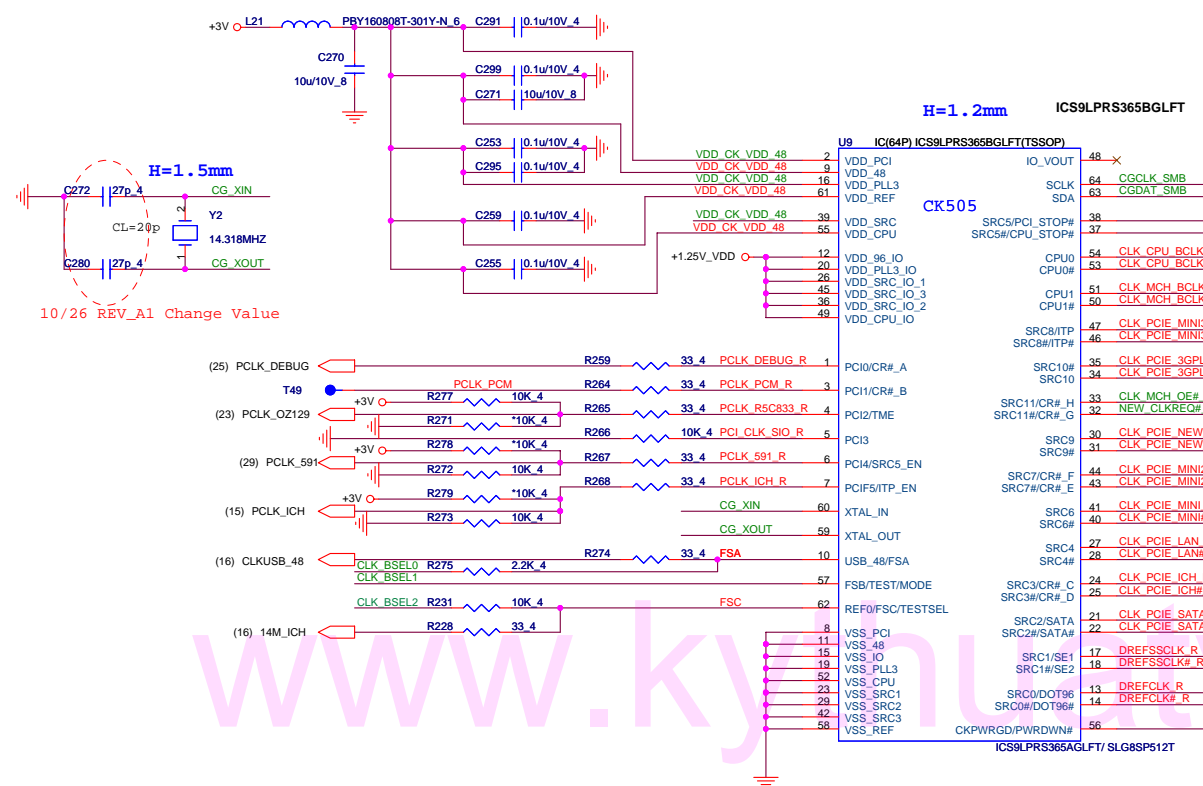
- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

- VCC_CORE
- +1.5V
- +1.05V
- +1.25V
- +1.8VSUS
- +3VPCU
- +3V_S5
- +3VSUS
- +3V
- +5VPCU
- +5V_S5
- +5V
- SMDDR_VTERM
- SMDDR_VREF

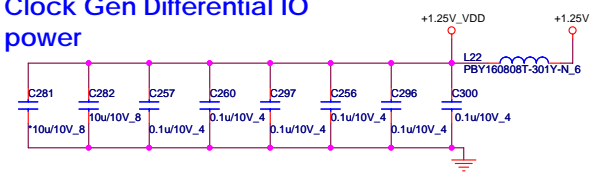
BL5S Block Diagram



Clock Generator

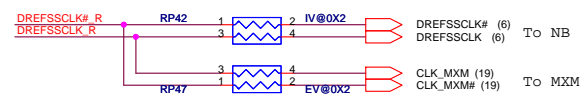
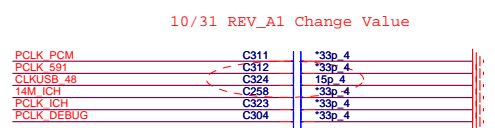


Clock Gen Differential IO power



www.kyoceraelectronics.com

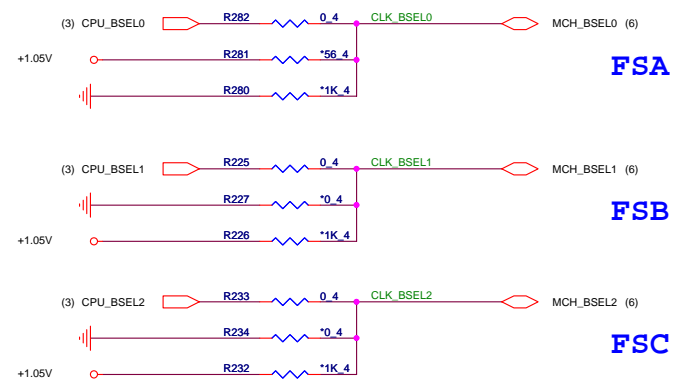
ICS9LPRS365 (ALPRS365K13)	RTM875T-606 (AL000875K06)	FULL HIGH	PULL DOWN
Pin 4 PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5 PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS SRC5 PCI_STOP/CPU_STOP (default)
Pin 6 PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS 27MHz IS SRC/DOT (default)
Pin 7 PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)



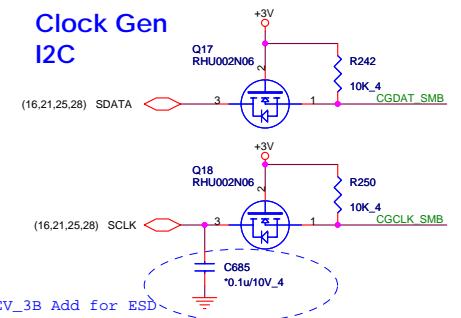
CPU Clock select

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

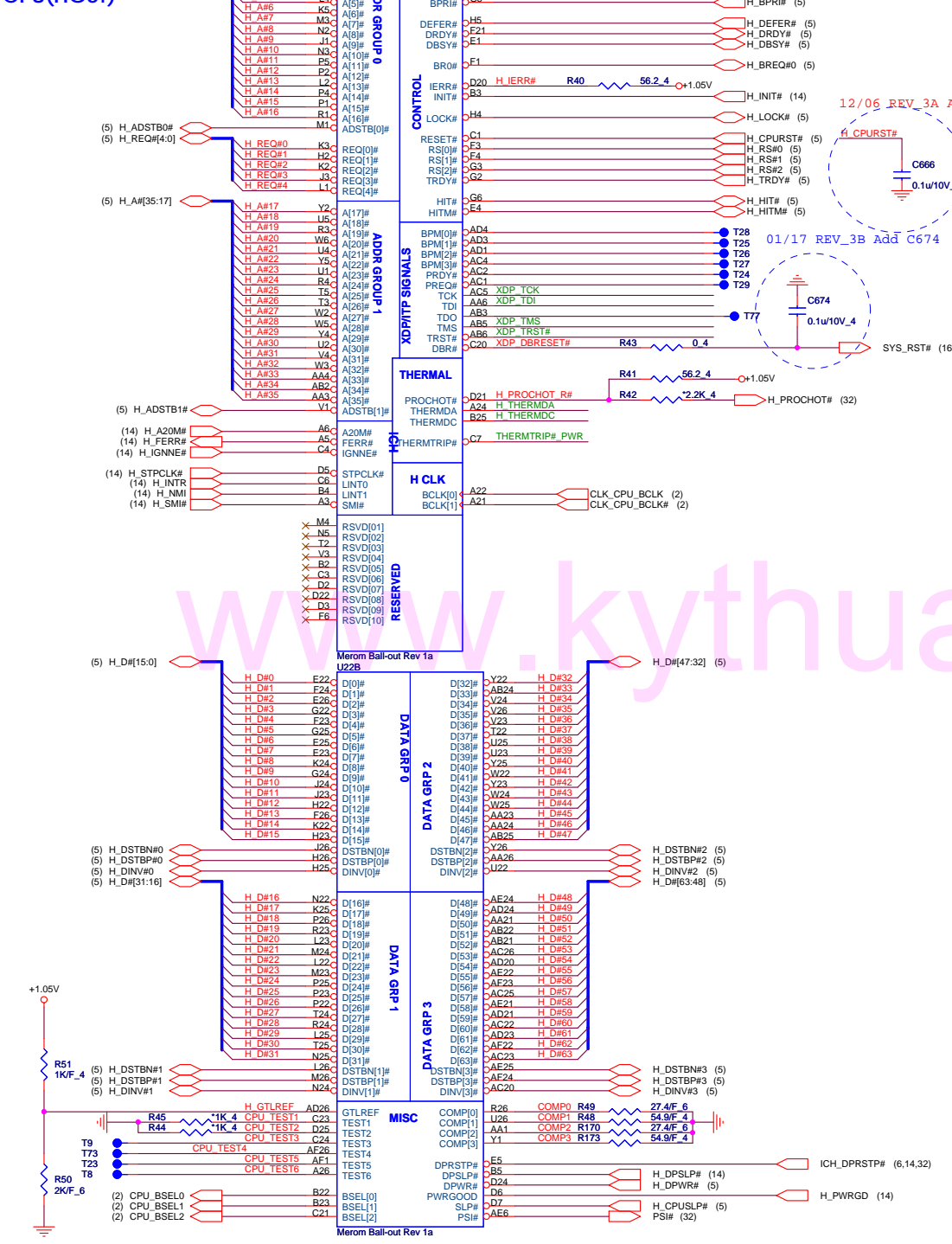


Clock Gen I2C

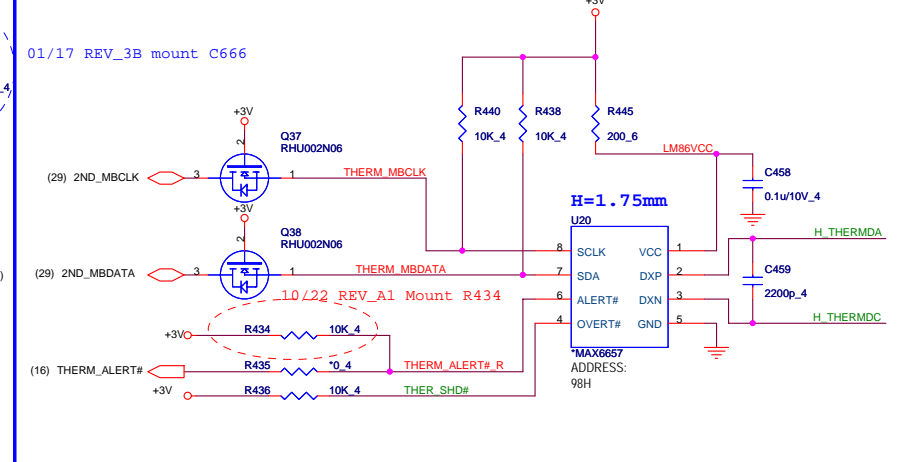


Quanta Computer Inc.
 PROJECT : BL5S Santa Rosa
 Size Document Number CLK_GEN./CK505 Rev 1A
 Date: Tuesday, January 22, 2008 Sheet 2 of 37

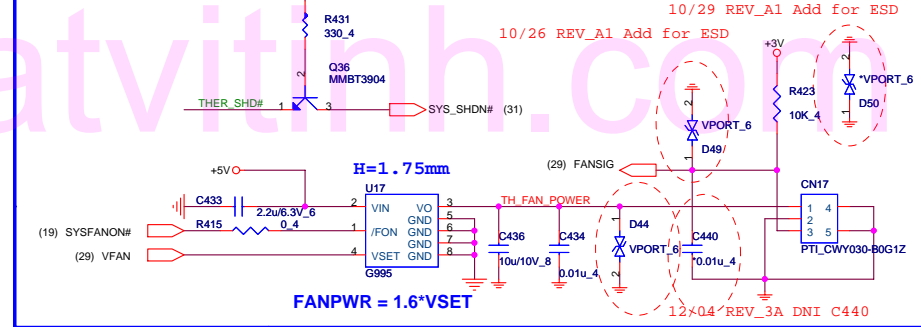
CPU(HOST)



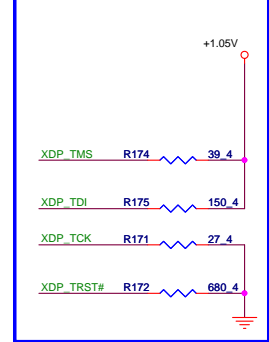
CPU Thermal monitor



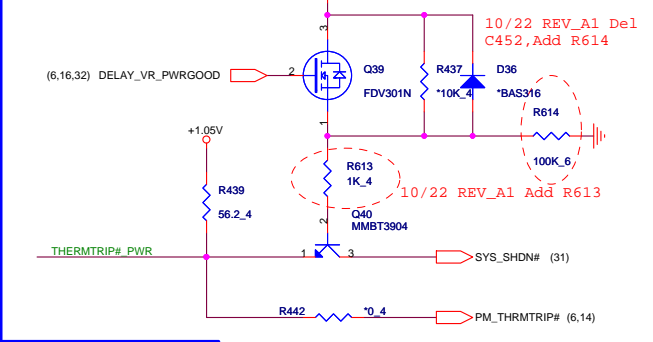
CPU FAN



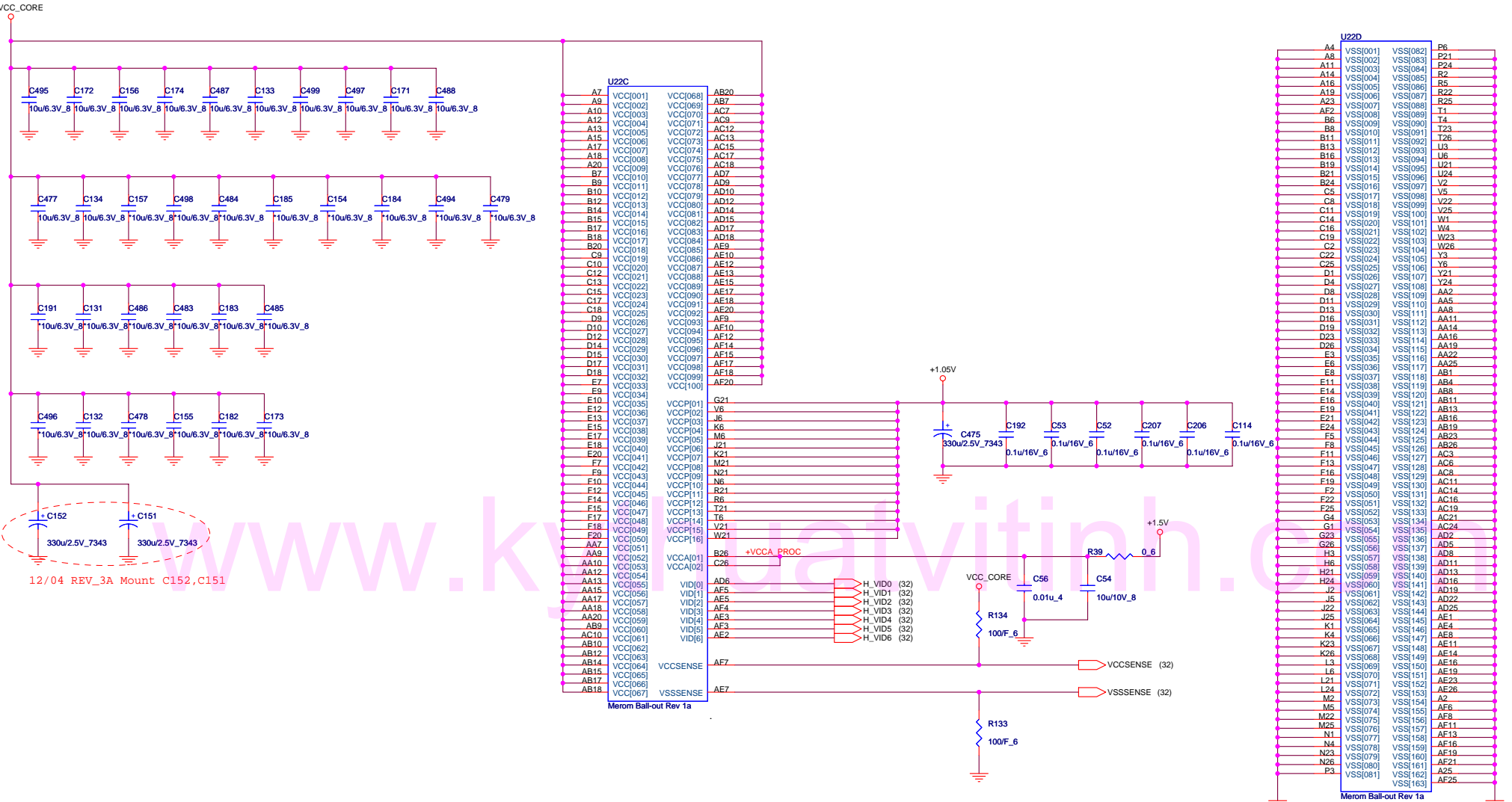
PU/PD (ITP700)



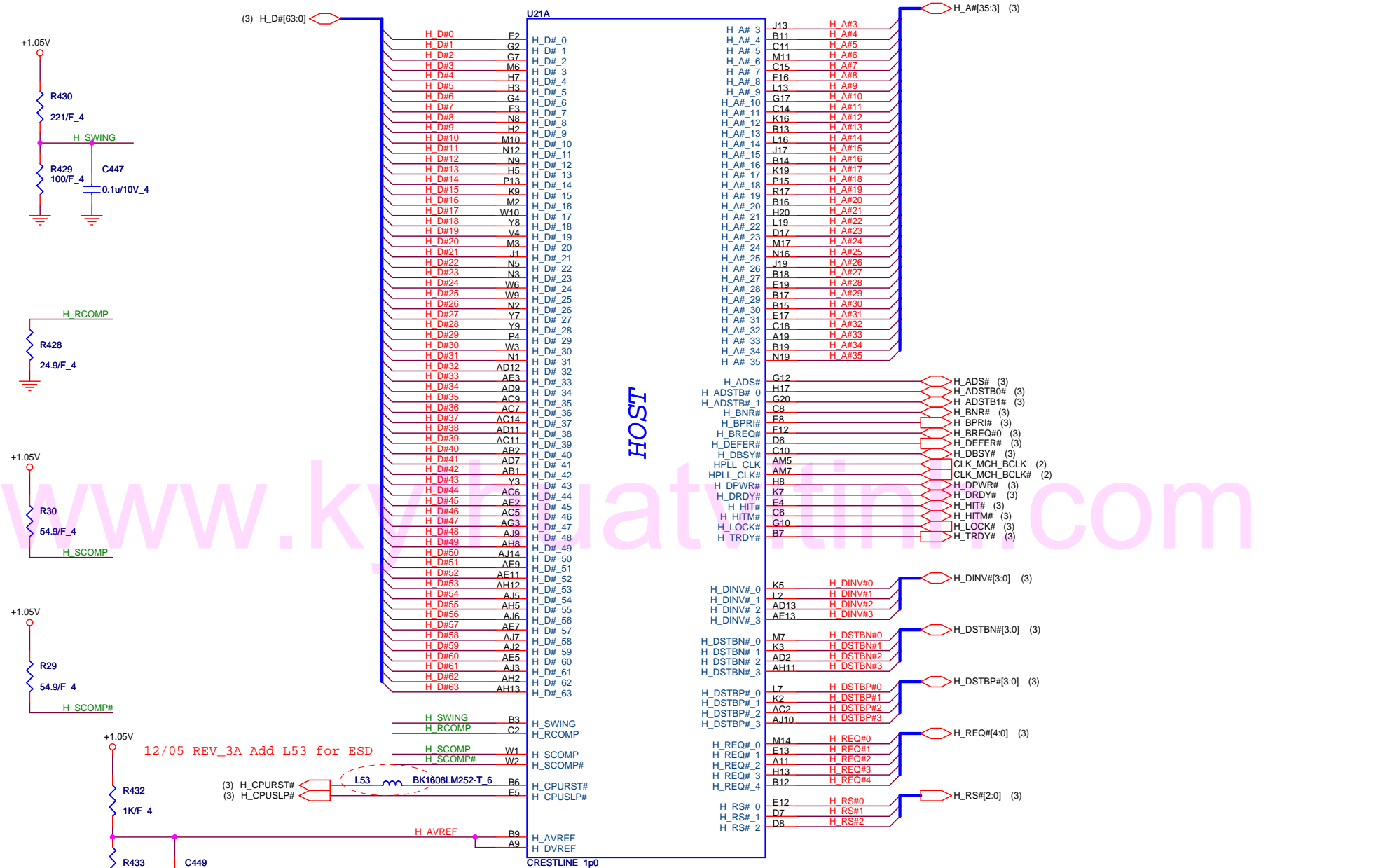
Thermal Trip



CPU(Power)



12/04 REV_3A Mount C152,C151



(3) H_D#[63:0]

H_A#[35:3] (3)

HOST

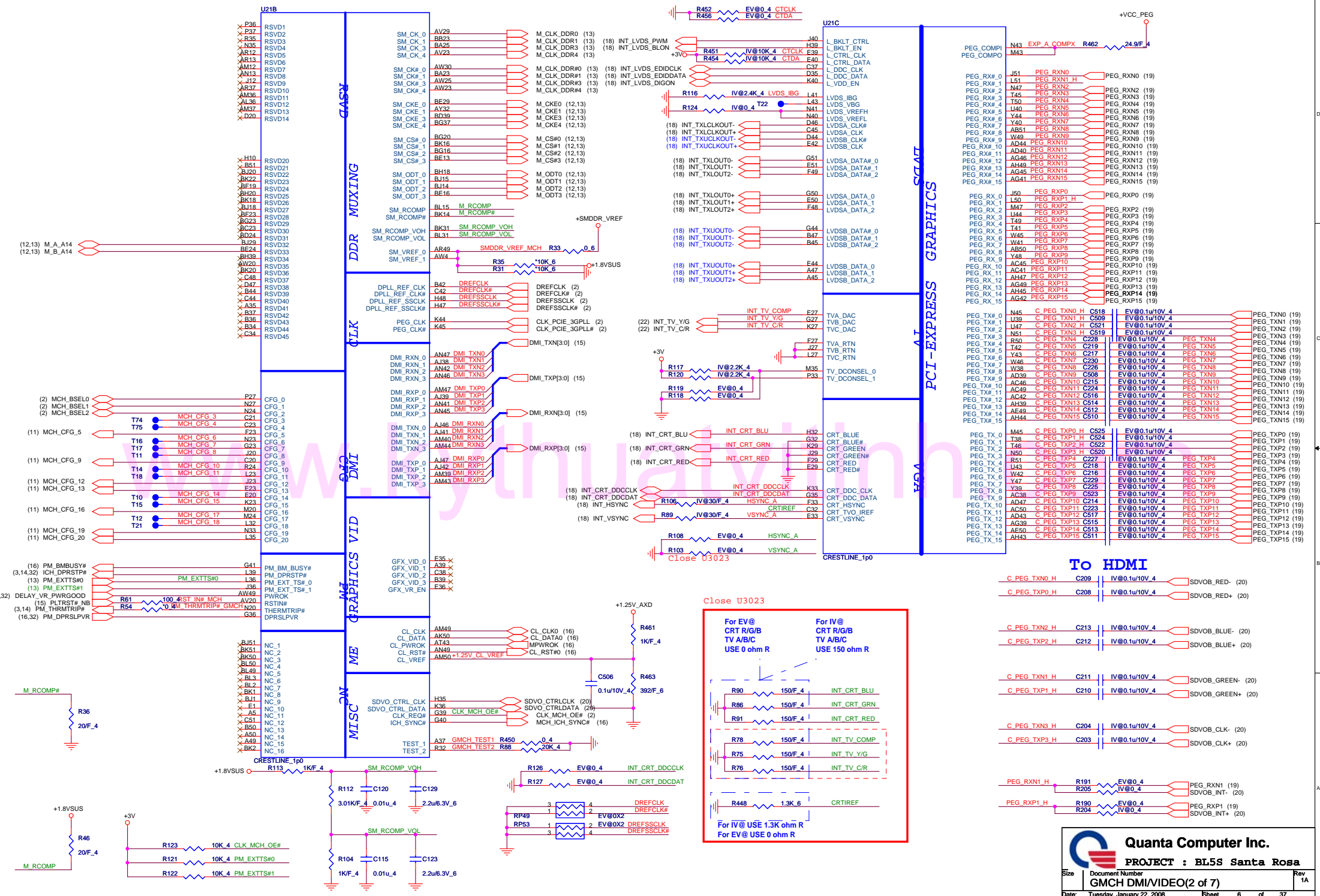
12/05 REV_3A Add L53 for ESD

(3) H_CPURST#
(3) H_CPUSLPH#

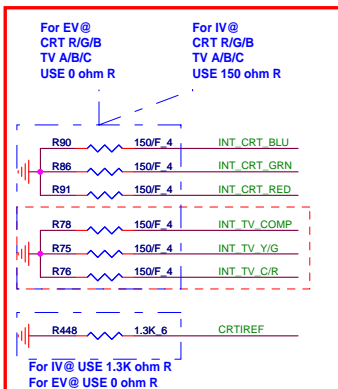
965GM : AJSLA5T0T20
 965PM : AJSLA5U0T25
 960GL : AJSLA5V0T09

Quanta Computer Inc.
 PROJECT : BL5s Santa Rosa

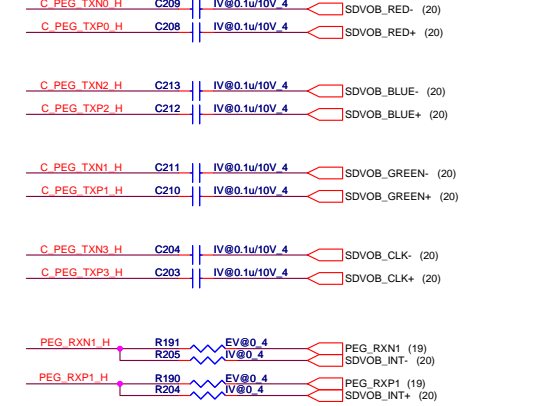
Size	Document Number	Rev
	GMCH HOST(1 of 7)	1A
Date:	Tuesday, January 22, 2008	Sheet 5 of 37



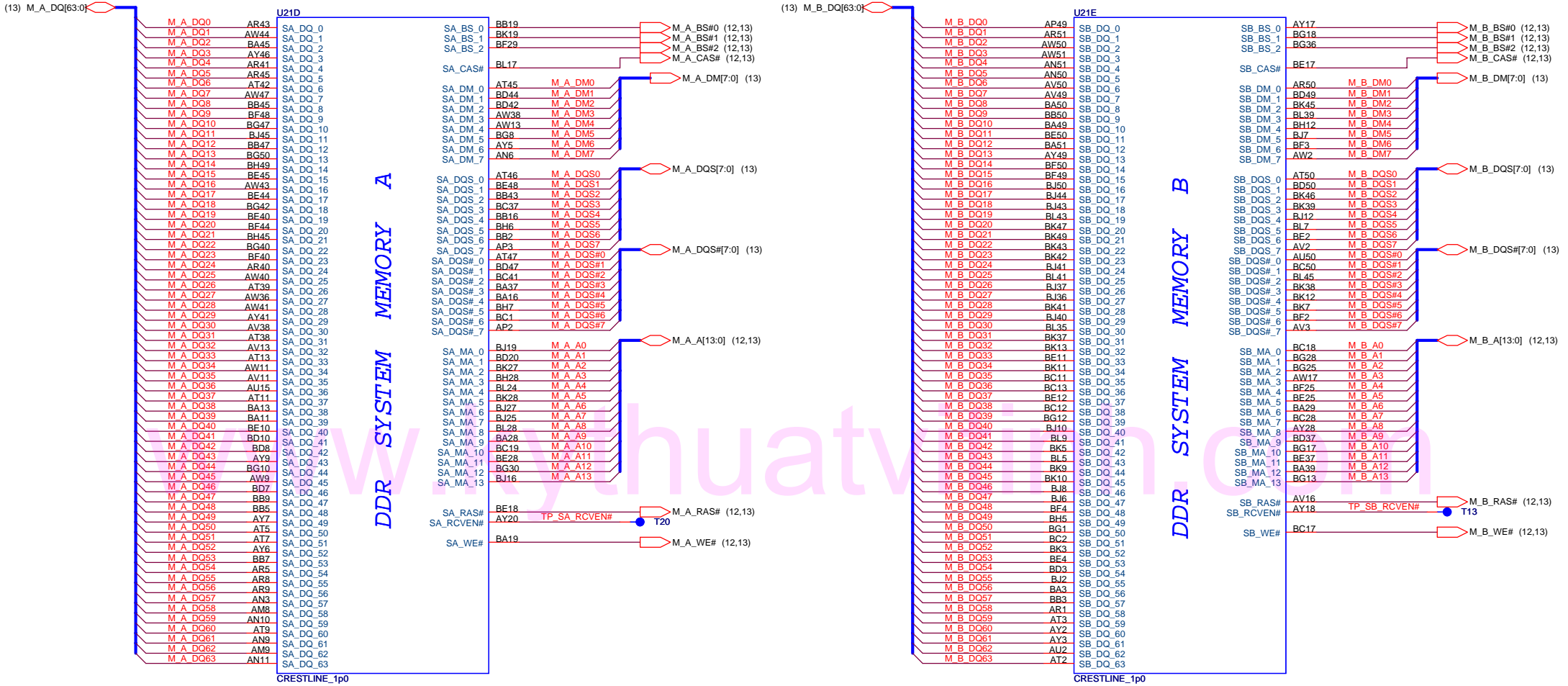
Close U3023



To HDMI



NB(Memory controller)

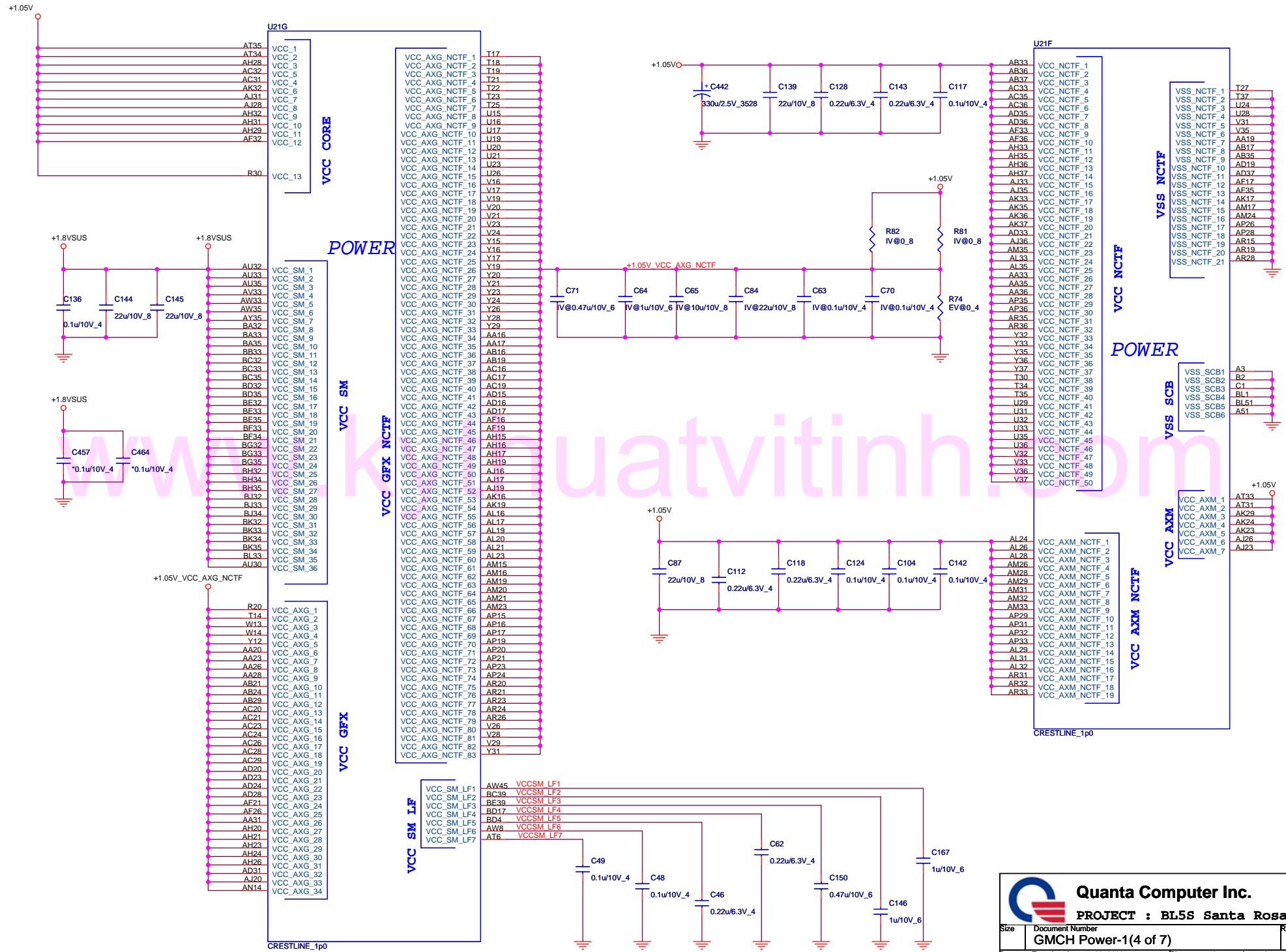


CRESTLINE_1p0

Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

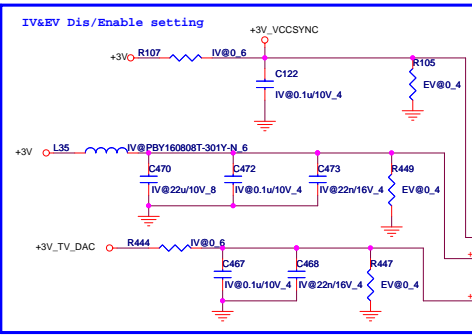
Size	Document Number	Rev
	MCH DDR(3 of 7)	1A
Date:	Tuesday, January 22, 2008	Sheet 7 of 37

NB(Power-1)



Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
 Size Document Number
GMCH Power-1(4 of 7)
 Date: Tuesday, January 22, 2008 Sheet 8 of 37 Rev 1A

NB(Power-2)



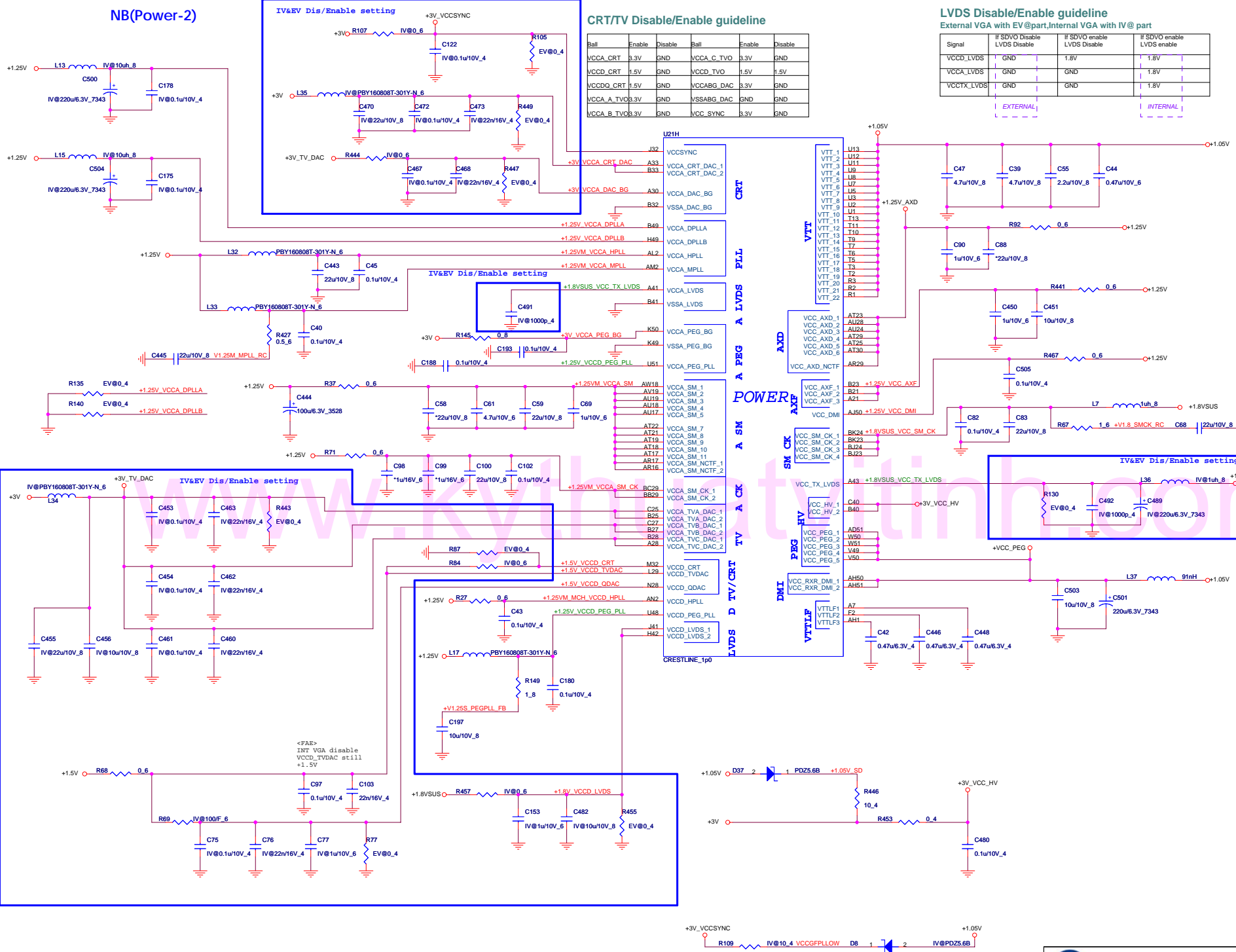
CRT/TV Disable/Enable guideline

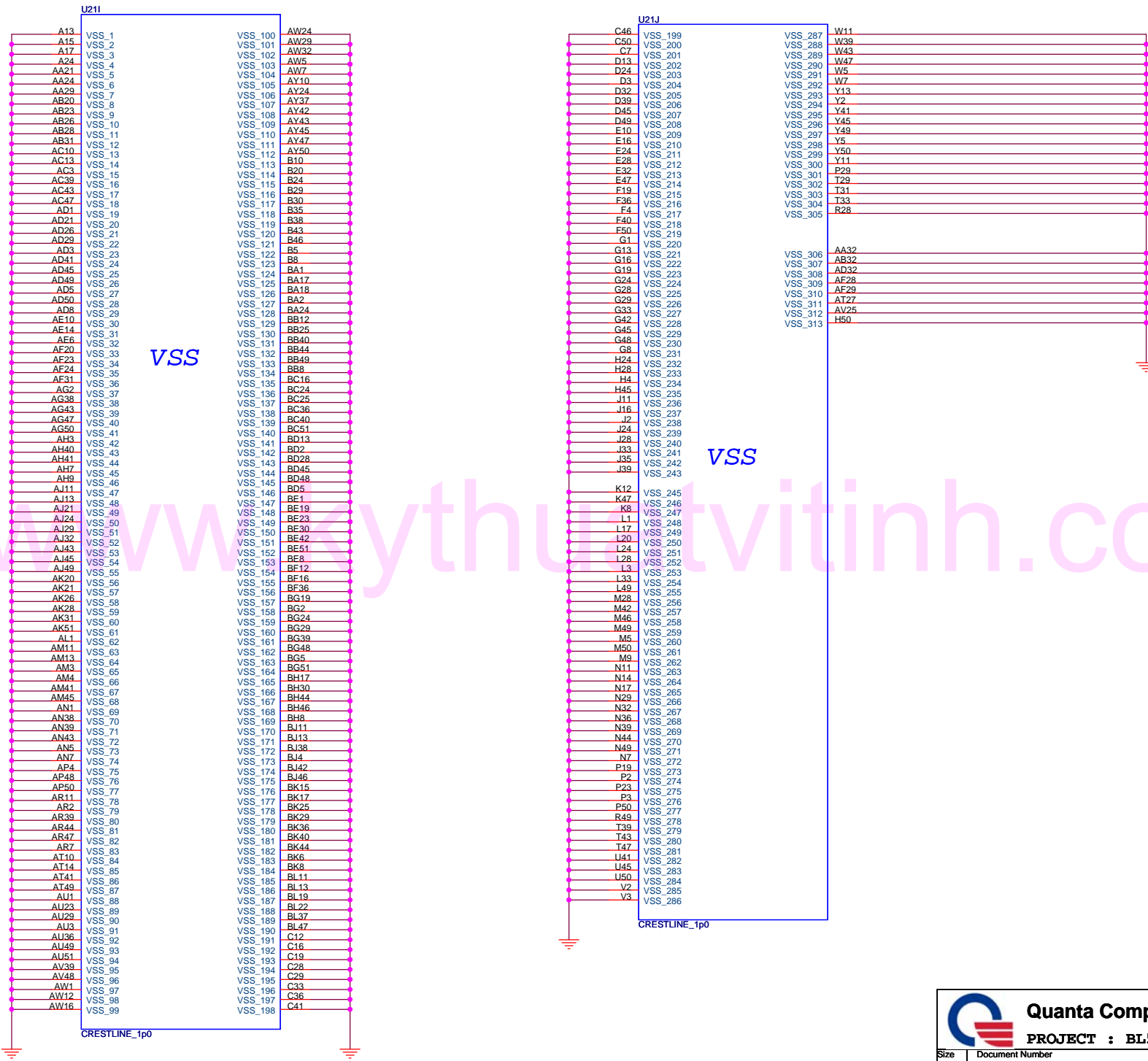
Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TV0	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TV0	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TV03.3V	GND	GND	VSSABG_DAC	GND	GND
VCCA_B_TV03.3V	GND	GND	VCC_VSYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCC1X_LVDS	GND	GND	1.8V





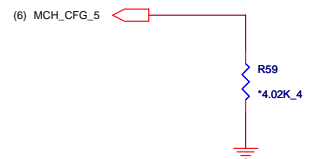
Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
 CFG[17:3] Have internal Pull-up
 CFG[18:19] Have internal Pull-down
 Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIx4(Default)
-----------	---------------------------------------



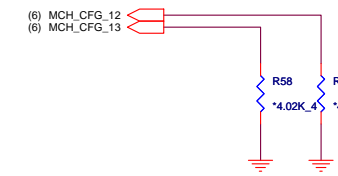
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--



XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--

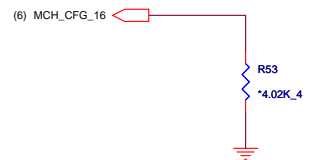


SDVO Present

Strap define at External DVI control page

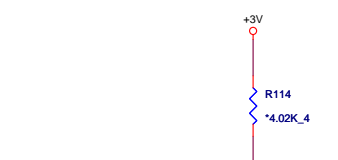
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	---



SDVO/PCIE Concurrent operation

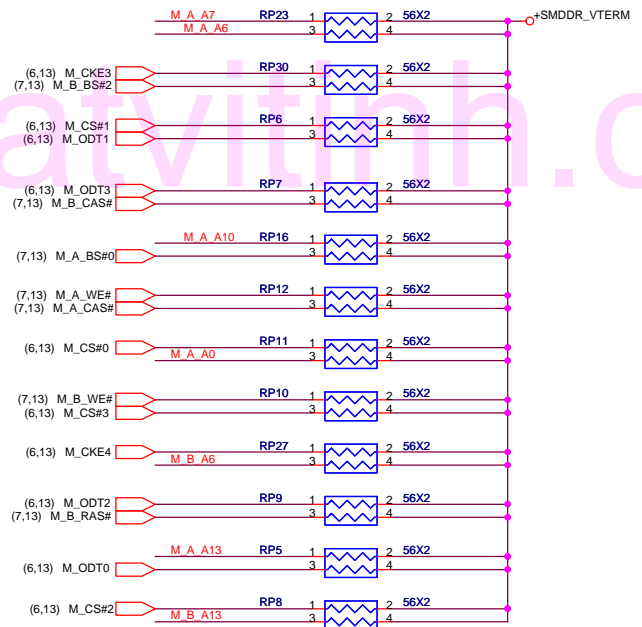
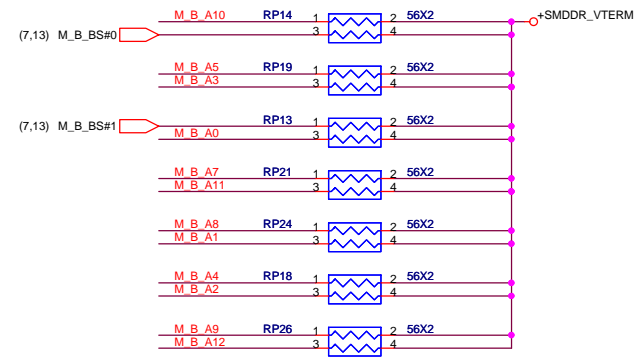
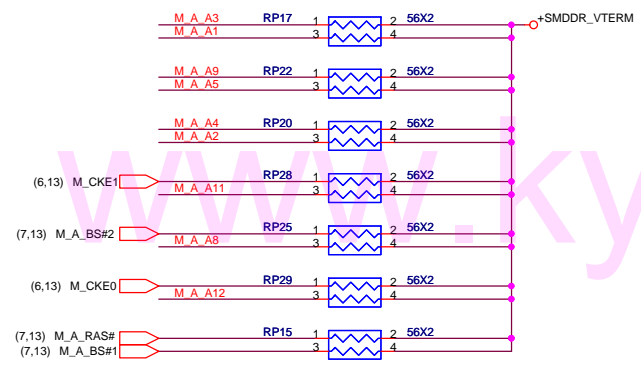
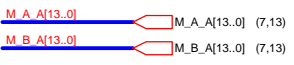
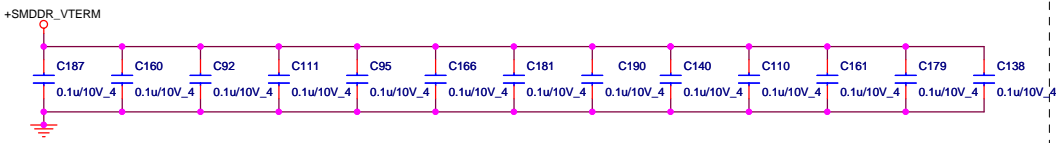
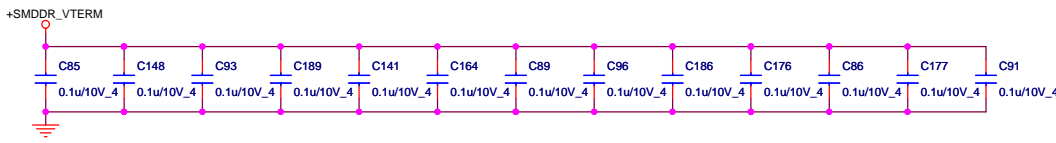
MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO and PCIE X1 are operating simultaneously via the PEG port
------------	---




Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
 Size | Document Number | Rev
GMCH Strap(7 of 7) | | 1A
 Date: Tuesday, January 22, 2008 | Sheet 11 of 37

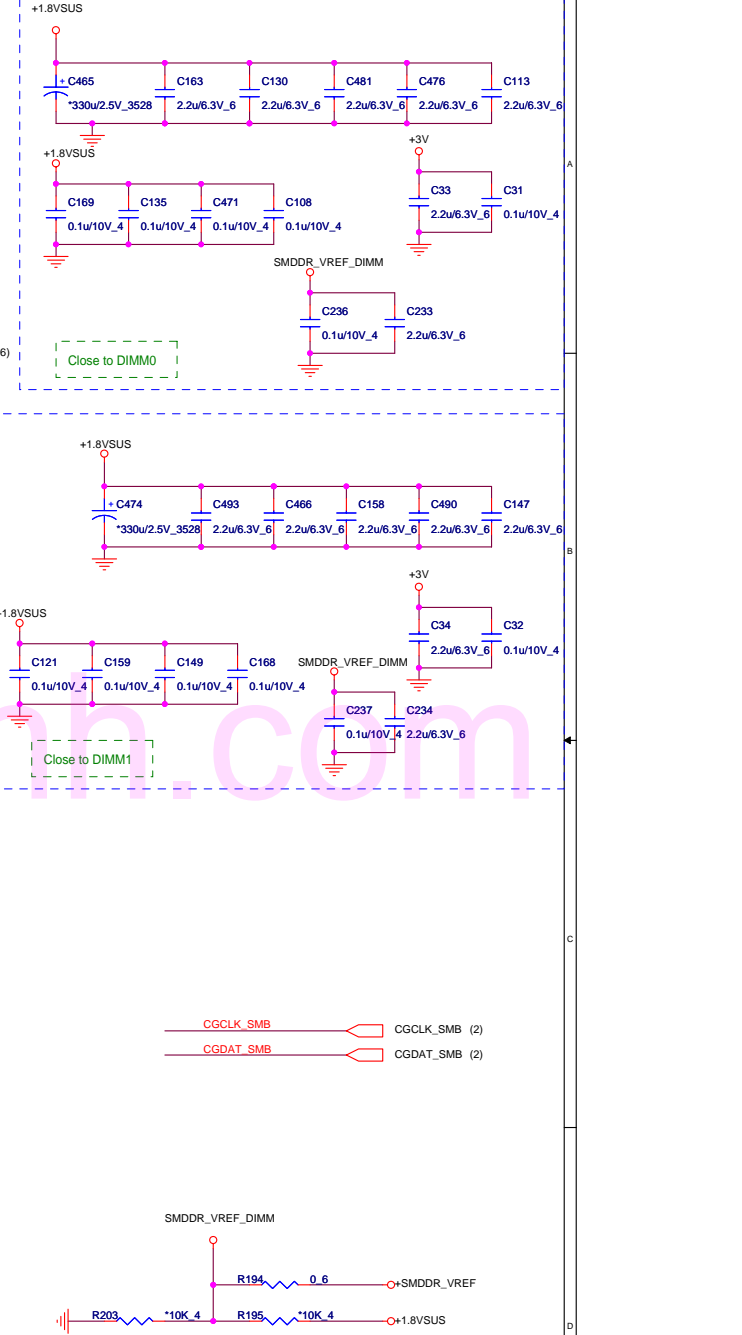
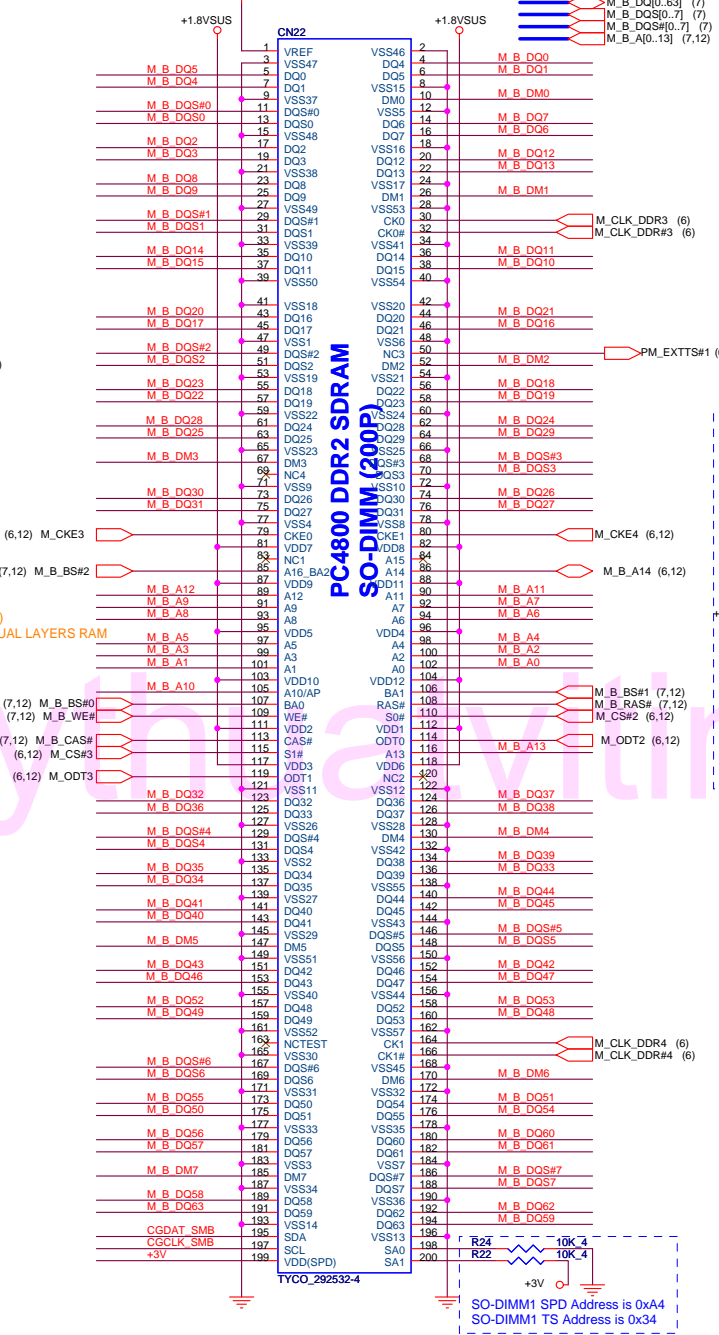
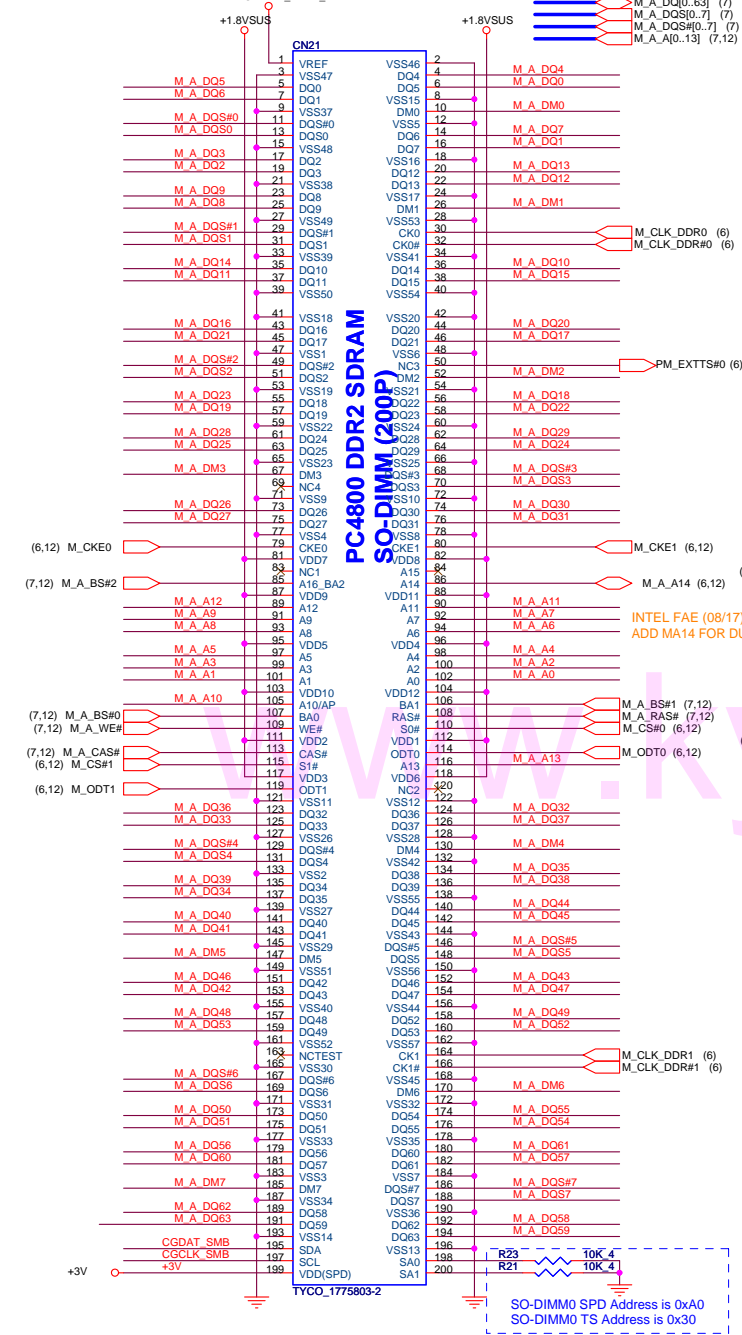
DDRII A CHANNEL

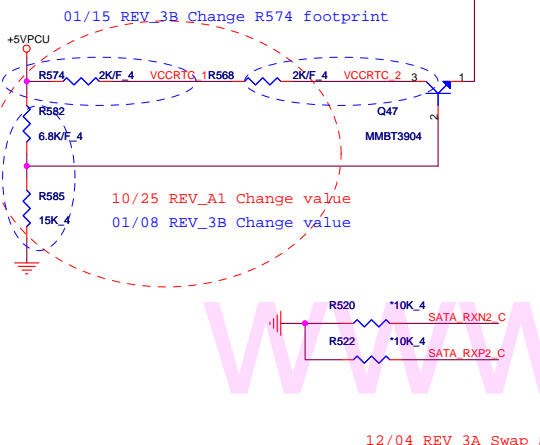
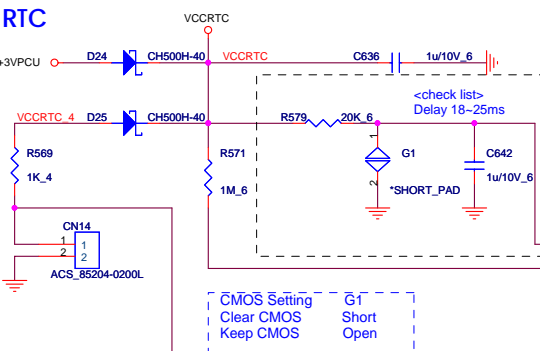
DDRII B CHANNEL




Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
 Size Document Number Rev
DDR RES. ARRAY
 Date: Tuesday, January 22, 2008 Sheet 12 of 37 Rev 1A

DDR2 Dual channel A/B CONN

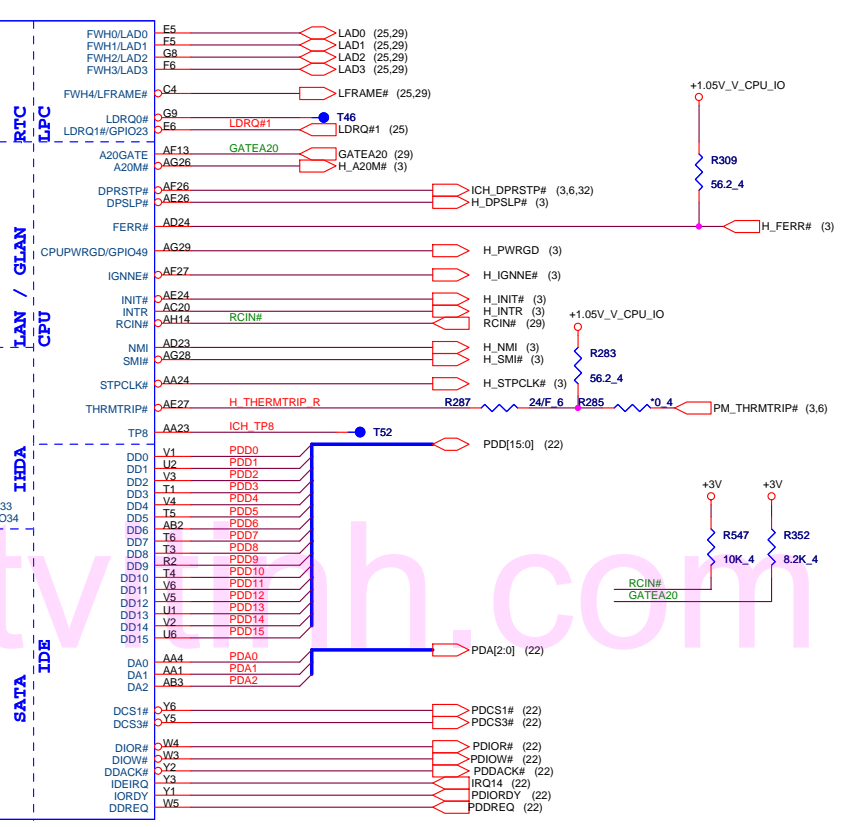
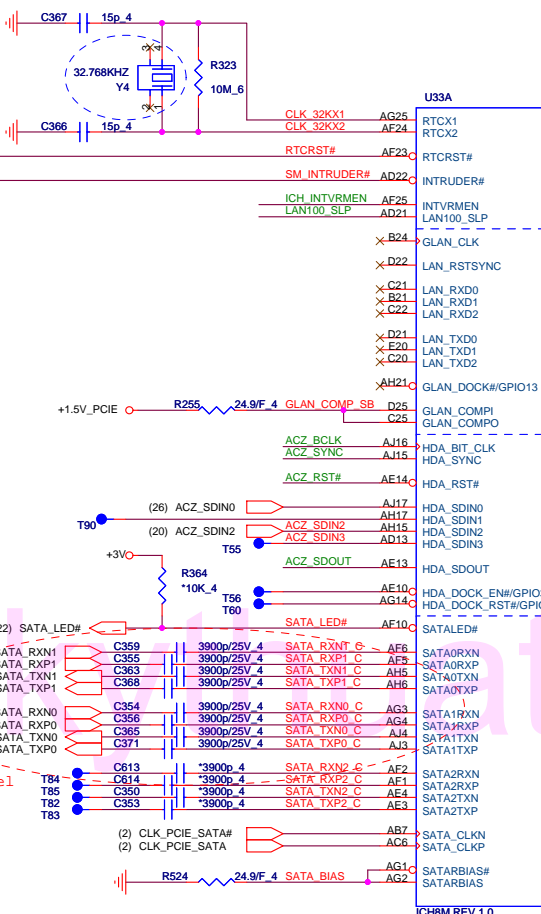




SATA Disable

- Connect to GND: SATA[2:0]RXp/n , SATARBIAS , SATARBIAS# , SATA_CLKP , SATACLKN
- NC: SATA[2:0]TXp/n , SATALED#
- VccSATAPLL should be connected directly to Vcc1_5, Filter cap are not required
- BIOS disable

01/21 REV_3B Change footprint



SB Strap

ICH8-M Internal VR Enable strap

(Internal VR for Vccsus1_05, VccSus1_5 and VccCL1_5)

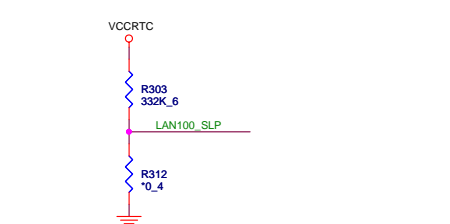
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---



ICH8-M LAN100_SLP Strap

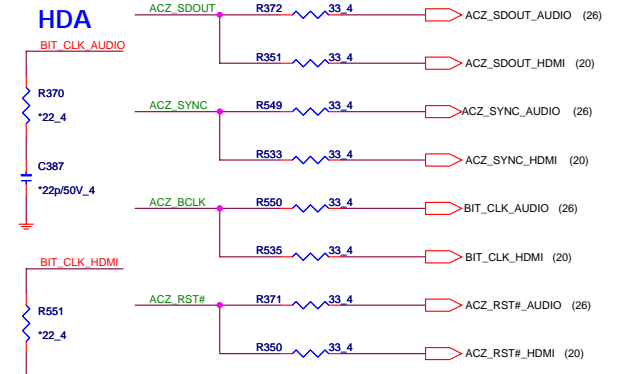
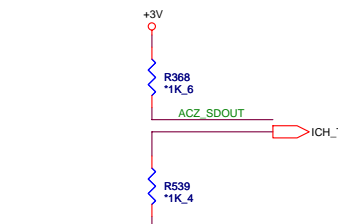
(Internal VR for VccLAN1_05 and VccCL1_05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---



XOR Chain Entrance Strap

ICH_RSVD0	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

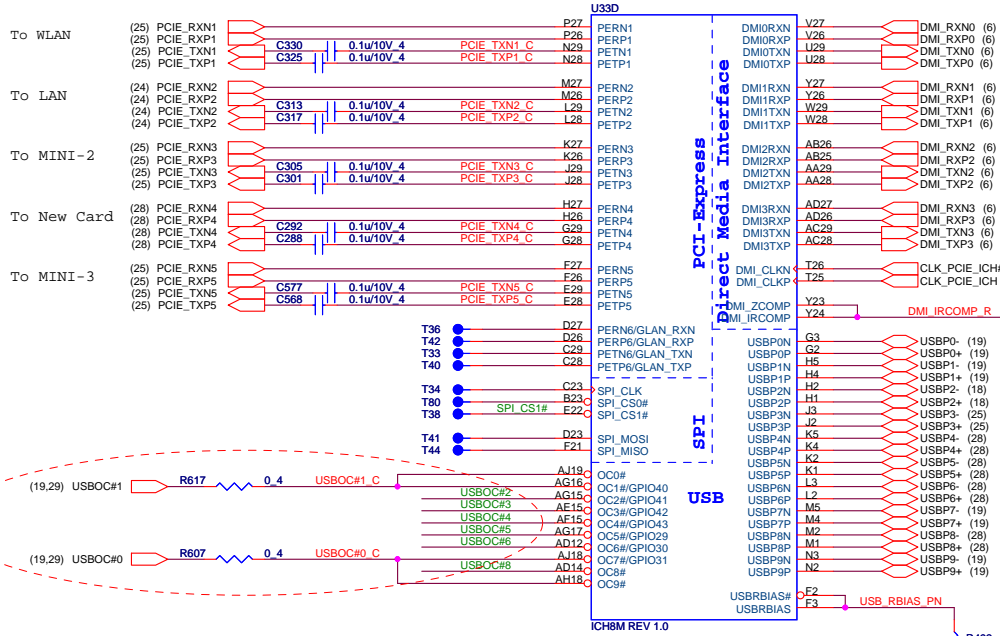


Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size Document Number
ICH8M HOST(1 of 4)

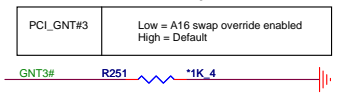
Date: Tuesday, January 22, 2008 Sheet 14 of 37

SB-PCIE/USB/DMI



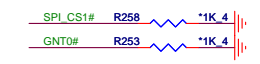
- To USB BOARD
- To USB BOARD
- To Camera
- To WLAN
- To Finger Printer
- To Bluetooth
- To New Card
- To eSATA
- To Felica
- To M/B USB

A16 SWAP Override strap

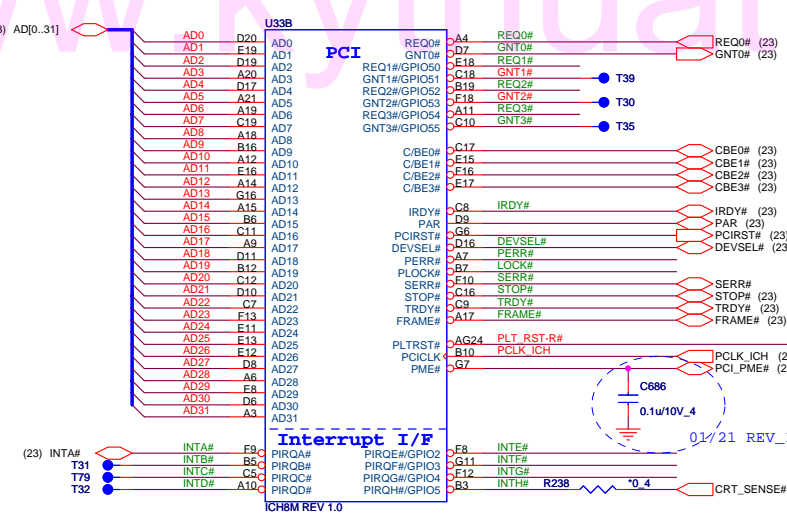


ICH8 Boot BIOS select

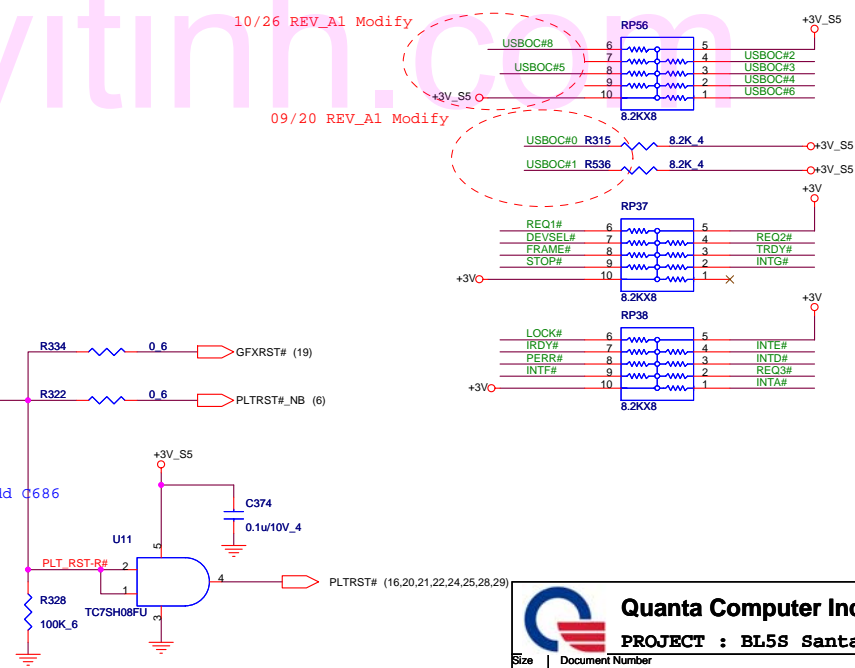
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC




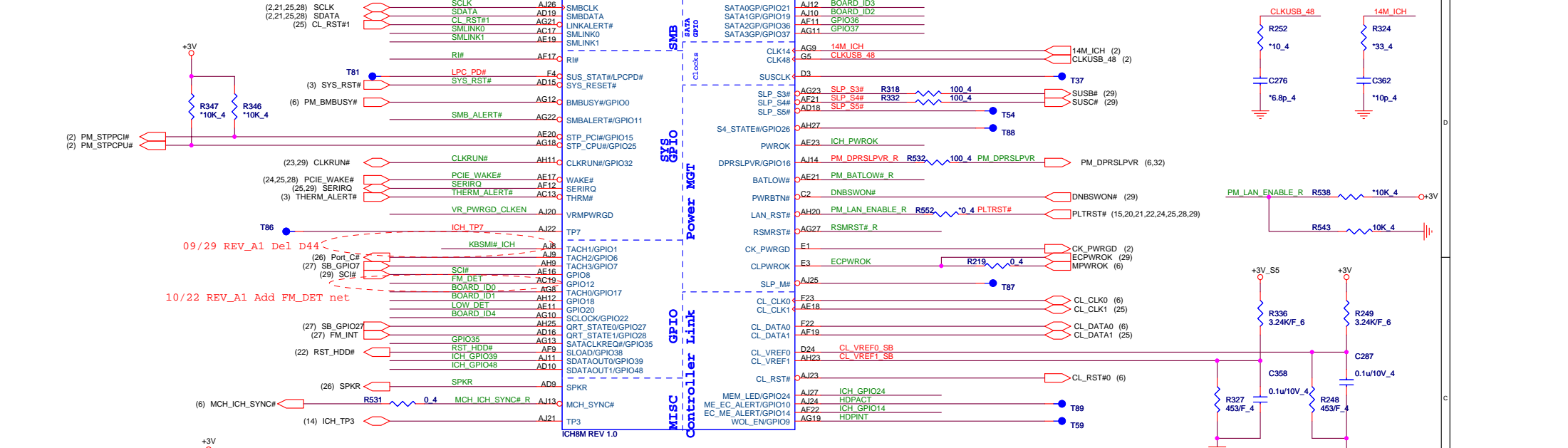
SB-PCI



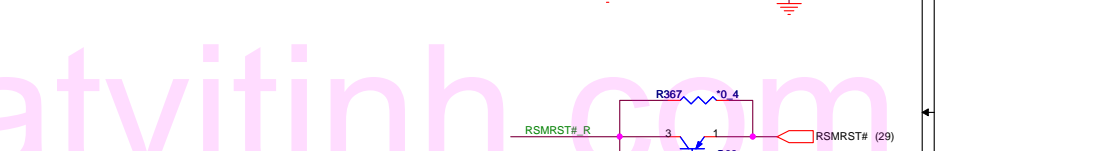
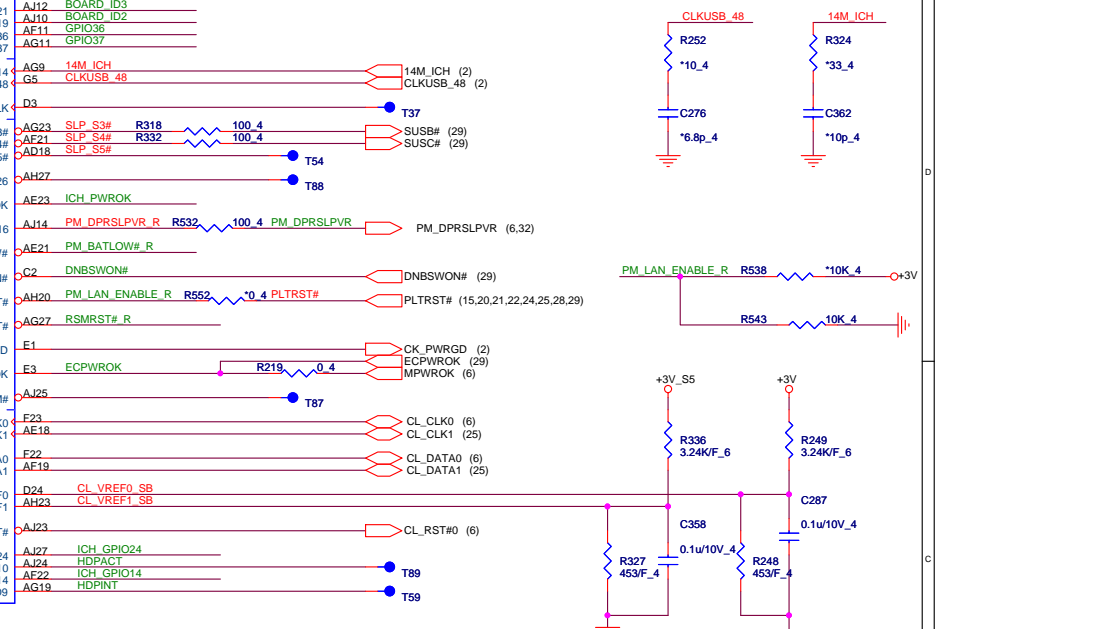
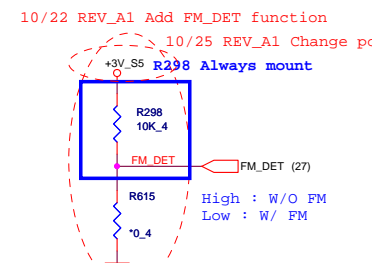
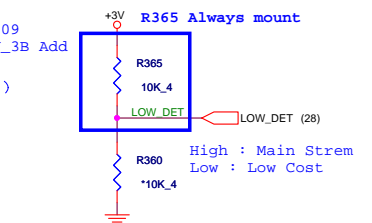
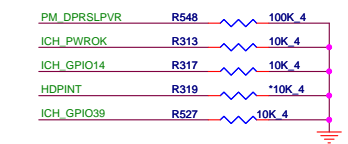
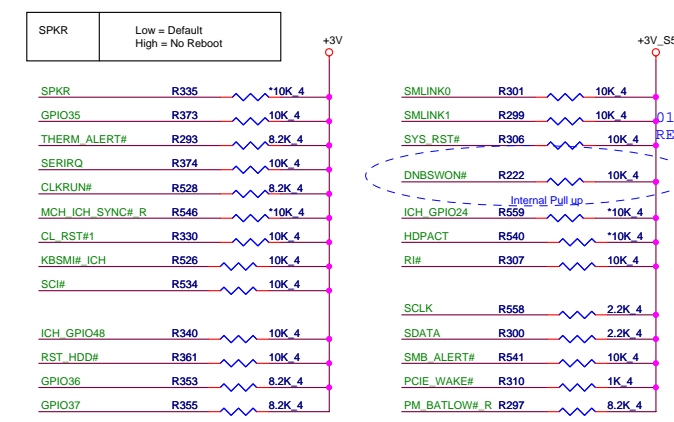
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#	OZ129



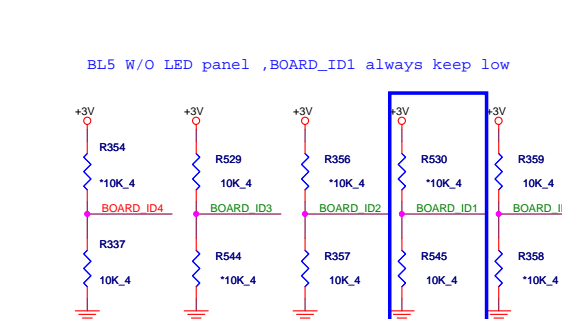

Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
 Document Number: **ICH8M PCIE(2 of 4)/ BIOS**
 Date: Tuesday, January 22, 2008 Sheet 15 of 37



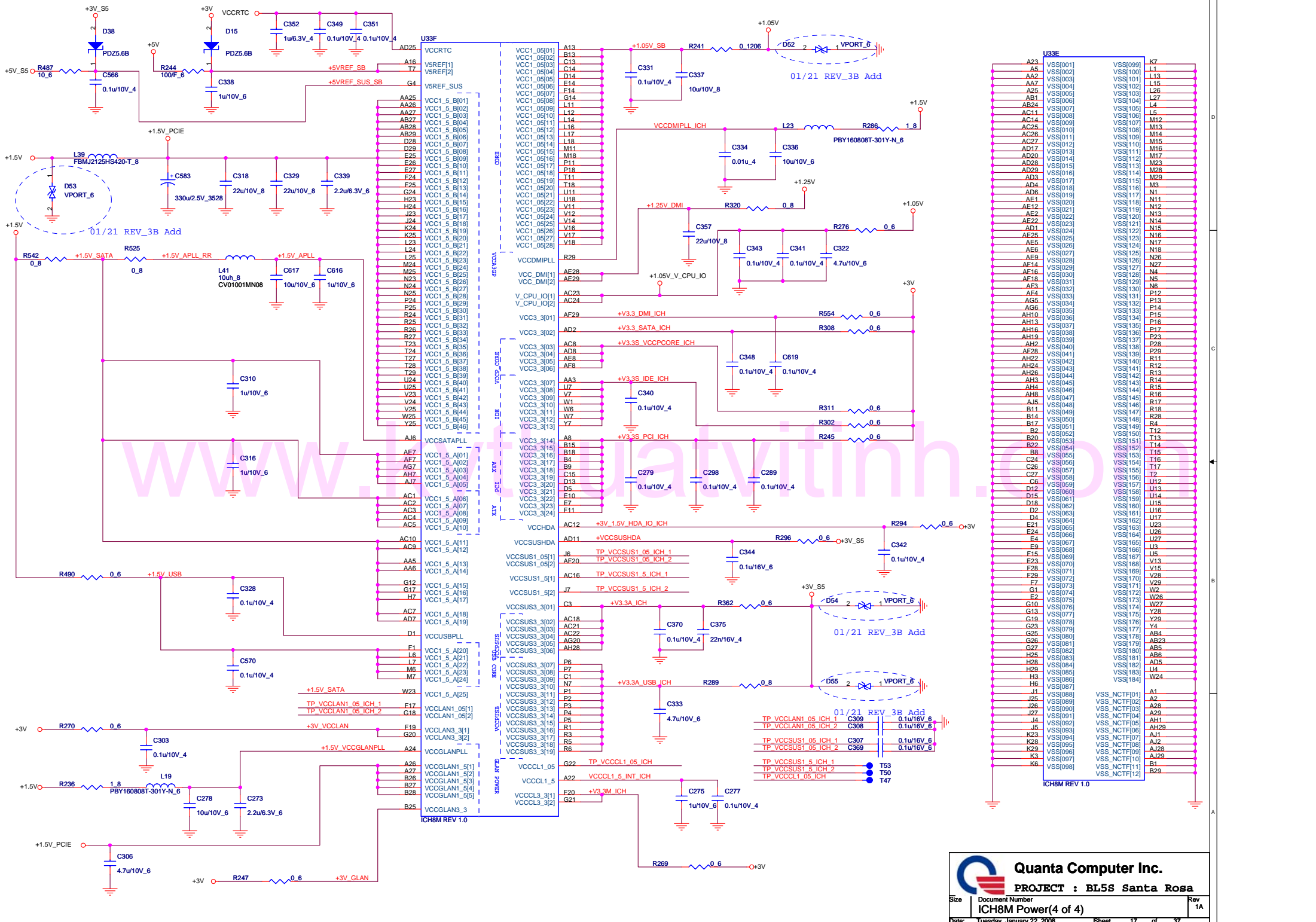
No Reboot strap



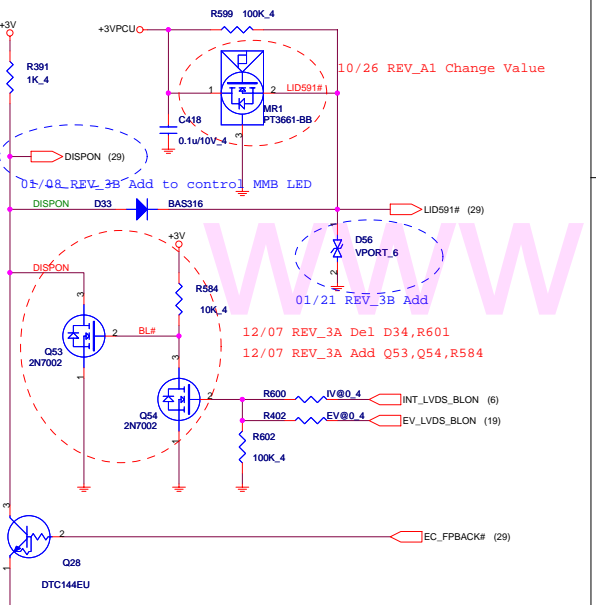
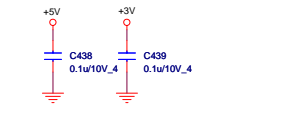
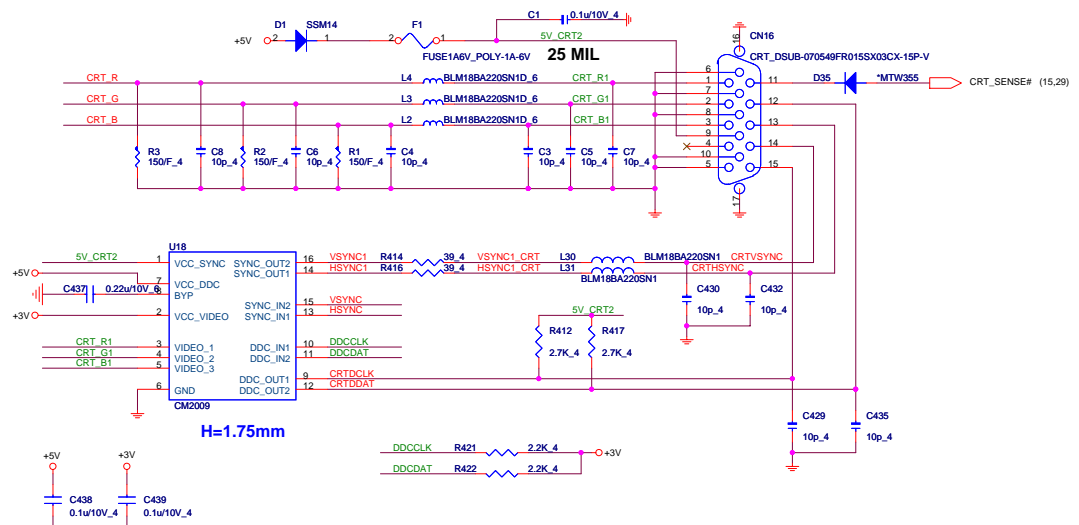
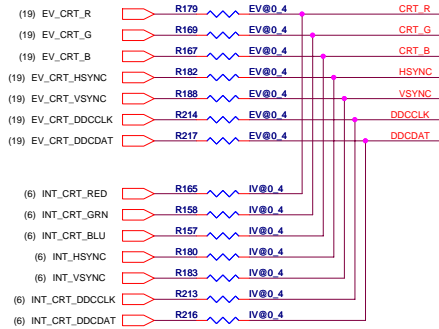
BL5 W/O LED panel ,BOARD_ID1 always keep low



Board ID	ID5	ID4	ID3	ID2	ID1	ID0
NEW CARD						H
CARD BUS						L
LED Panel					H	L
CCFL Panel					L	L
W/ G-SENSOR				H	L	
W/O G-SENSOR				L	L	
W/ S-VIDEO				H	L	
W/O S-VIDEO				L	L	
W/ HDMI			H	L		
W/O HDMI			L	L		
W/ FM	L					
W/O FM	H					

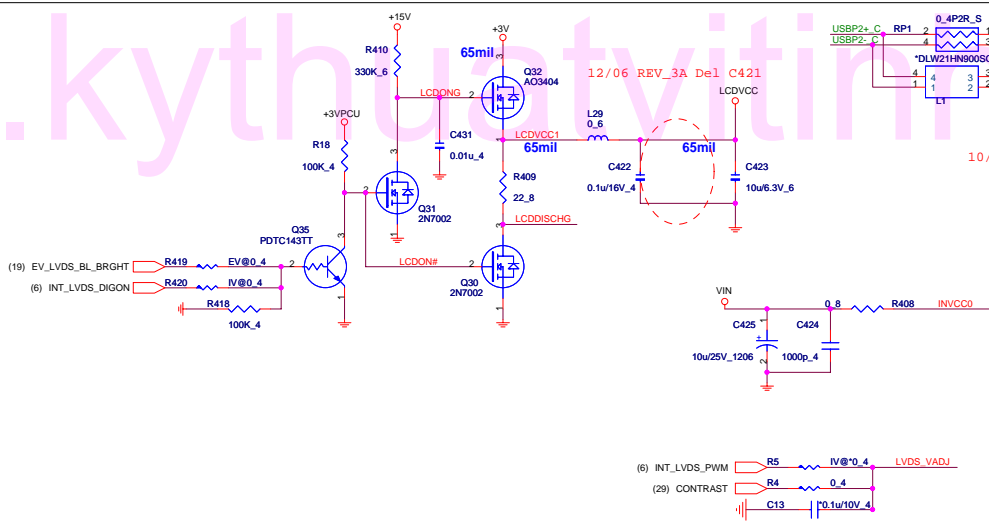
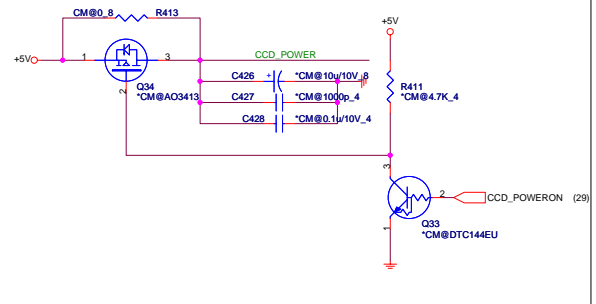


CRT PORT

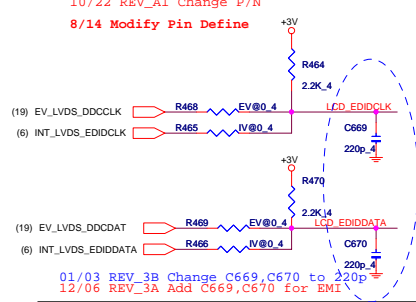
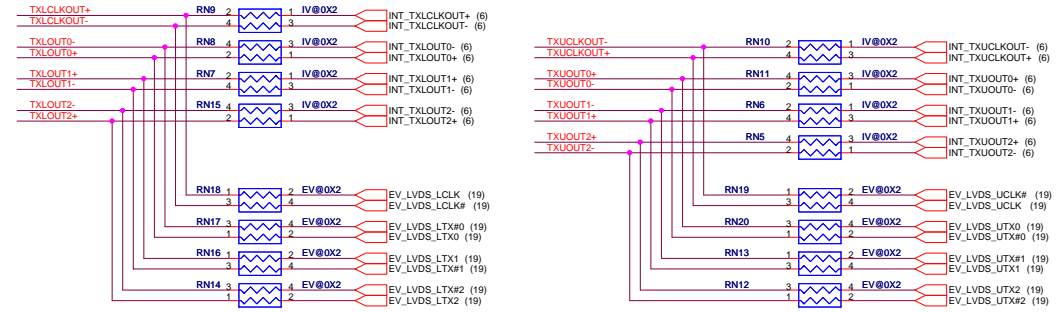
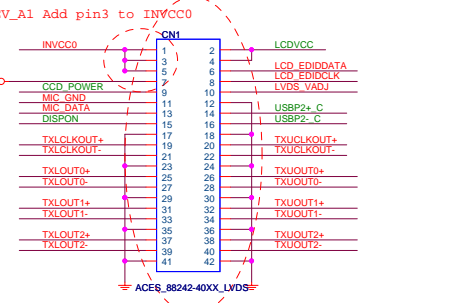


HALL SENSOR

CAMERA MODULE

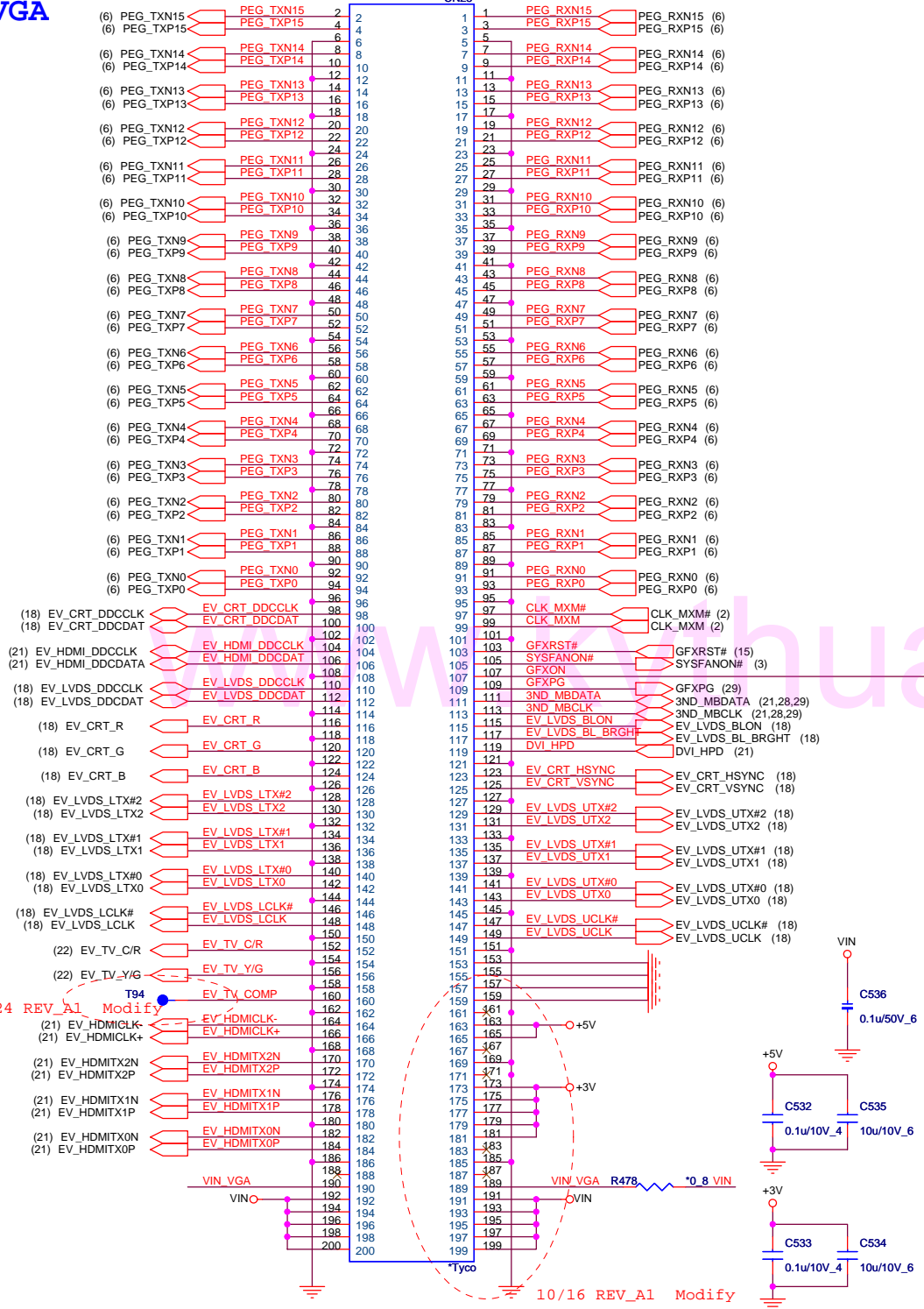


LCD PANEL MODULE

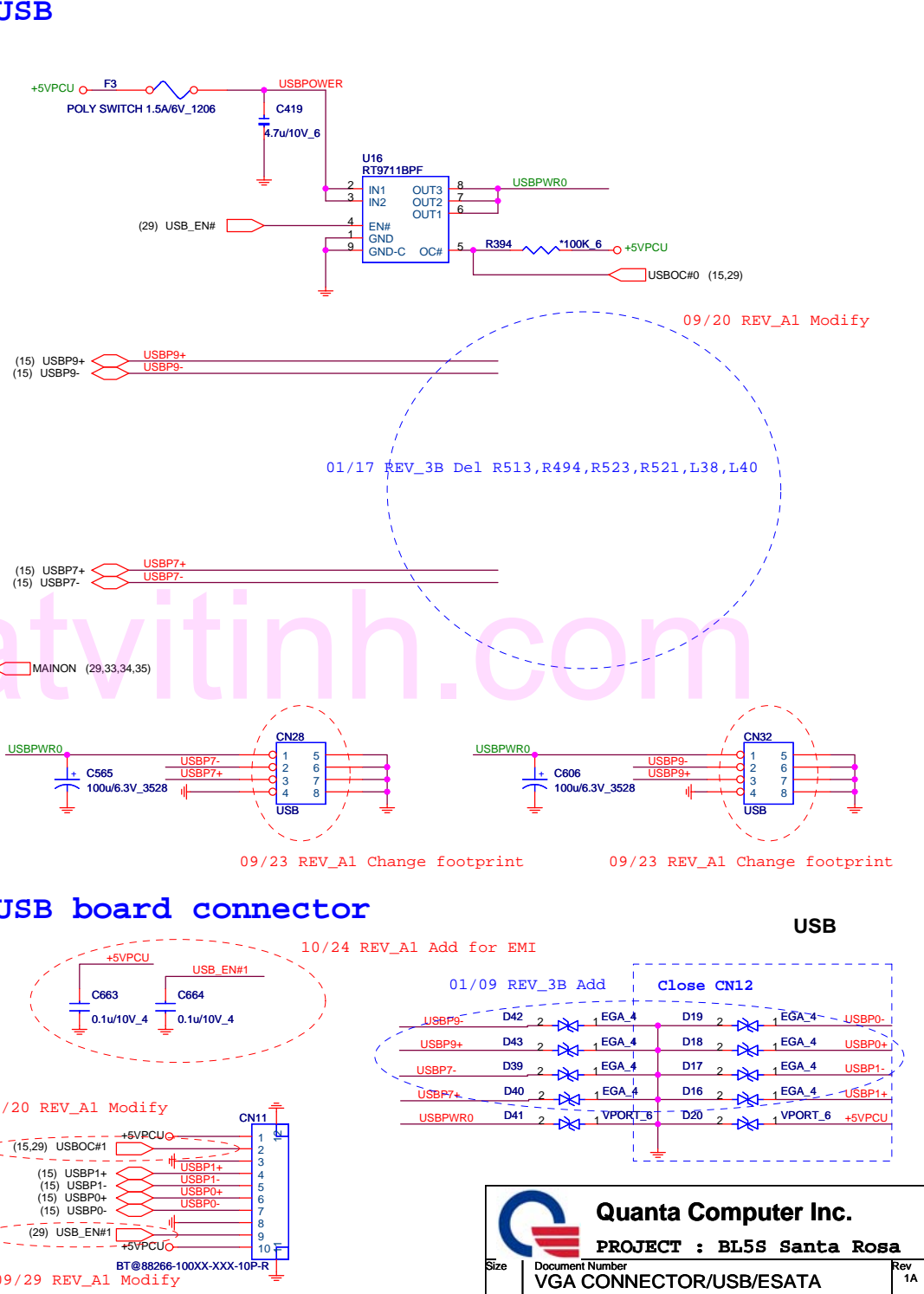


Quanta Computer Inc.
PROJECT : BL58 Santa Rosa
 Document Number: LCD/CRT/LID/CAMERA
 Date: Tuesday, January 22, 2008
 Sheet: 18 of 37

VGA



USB



Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

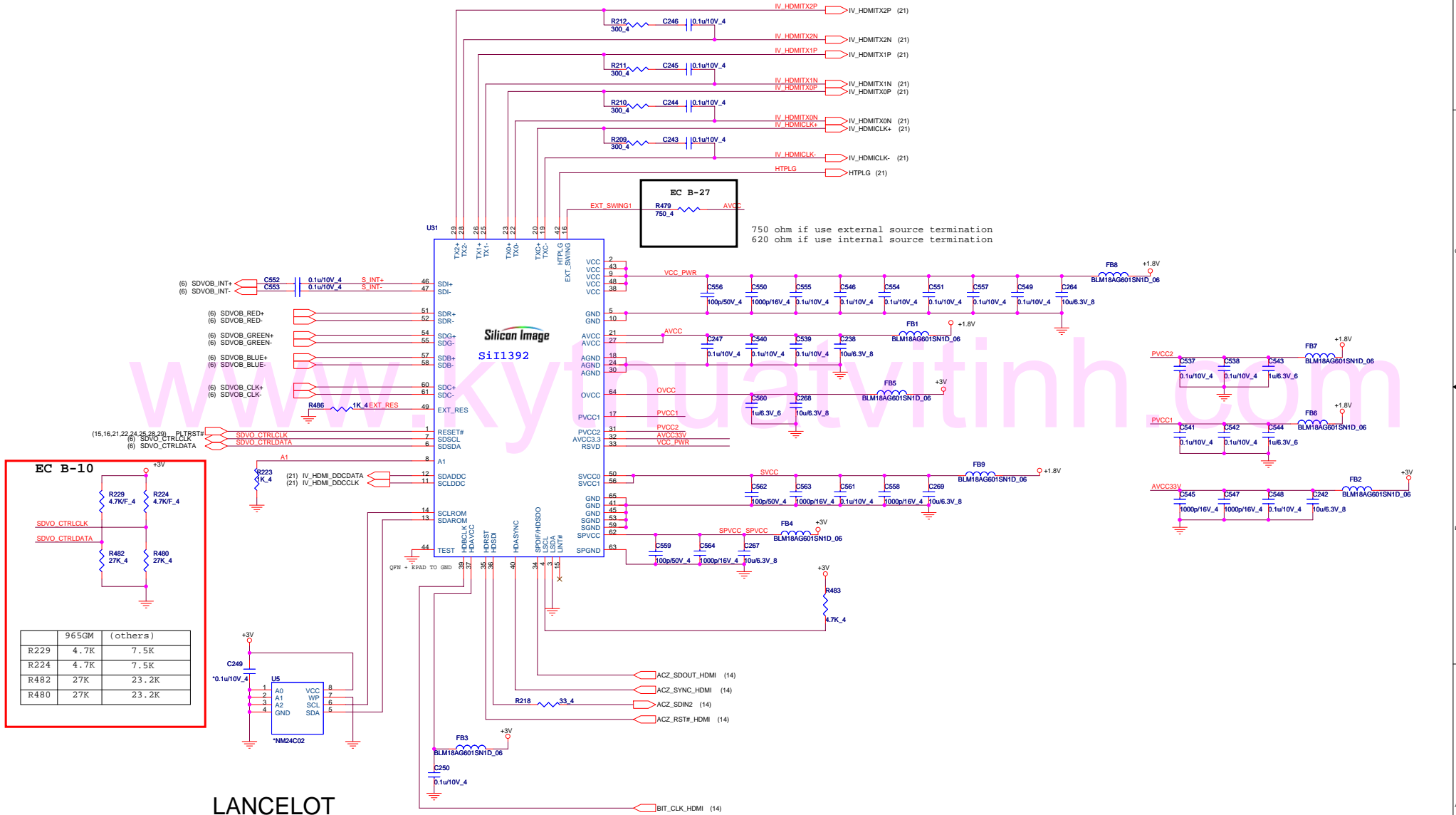
Size: Document Number: **VGA CONNECTOR/USB/ESATA** Rev: 1A

Date: Tuesday, January 22, 2008 Sheet: 19 of 37

SiI1392 HDMI TX

LAYOUT RULES:

Route traces with 100 Ohm Differential Impedance
 Avoid placing GND Copper or traces adjacent to TMD5 Trace
 Put these 4 resistors and 4 capacitors as close as possible to the TMD5 output pins of the SiI1392

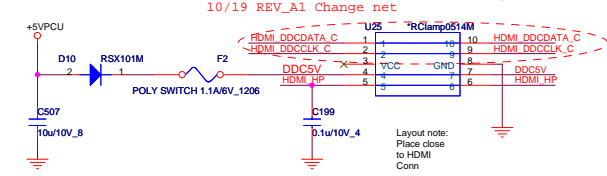
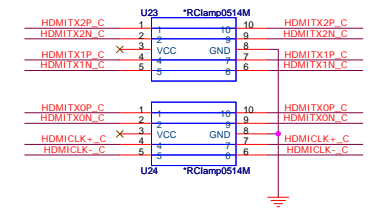
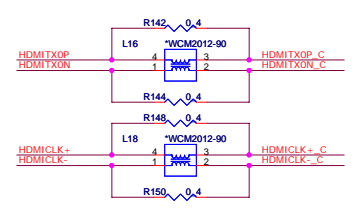
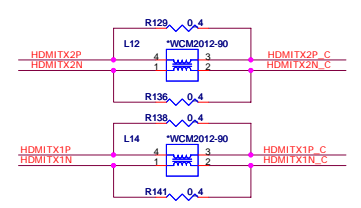
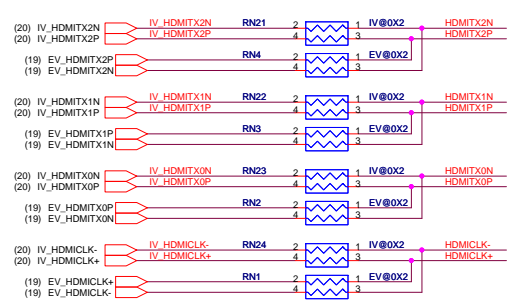


EC B-10

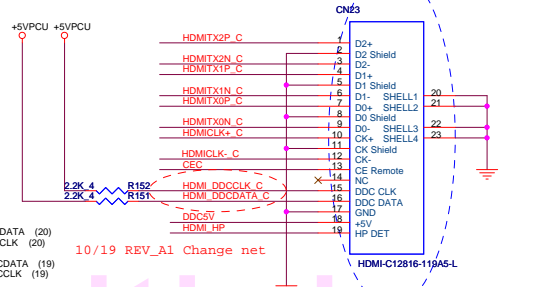
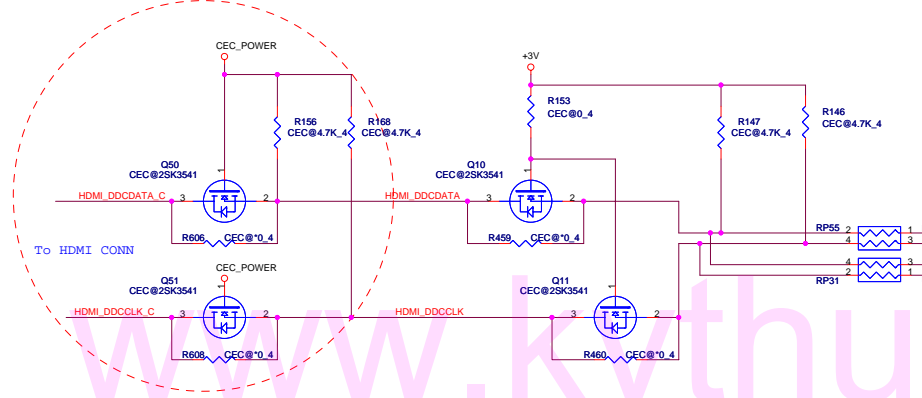
SDVO_CTRLCLK
 SDVO_CTRLDATA

	965GM	(others)
R229	4.7K	7.5K
R224	4.7K	7.5K
R482	27K	23.2K
R480	27K	23.2K

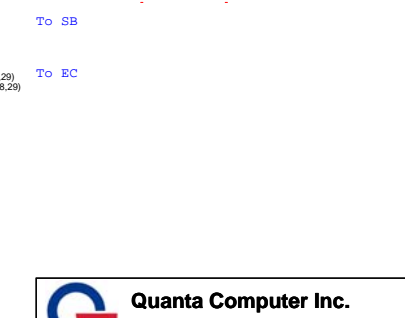
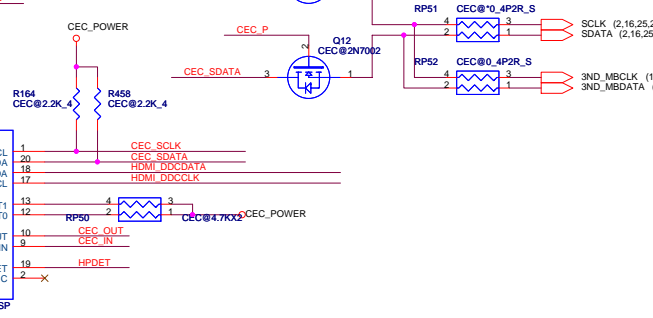
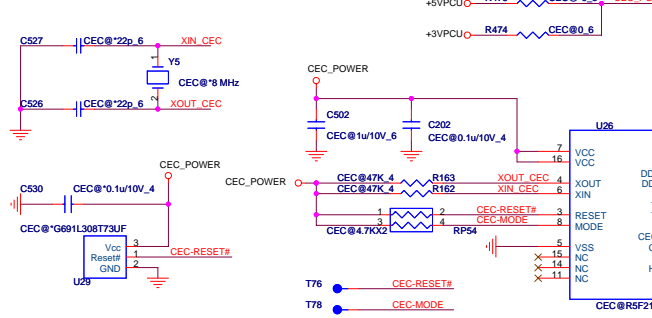
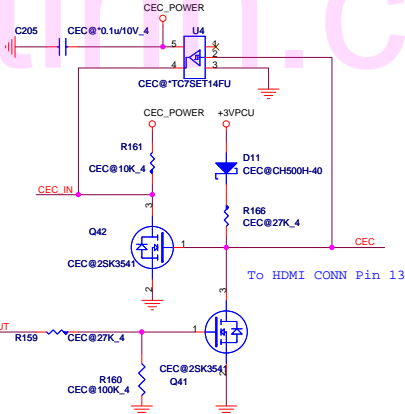
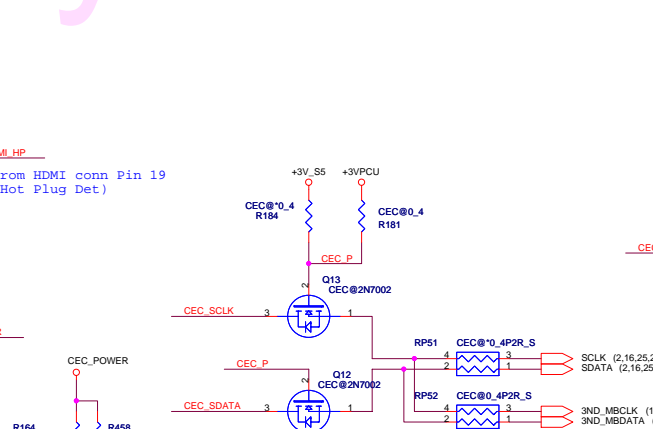
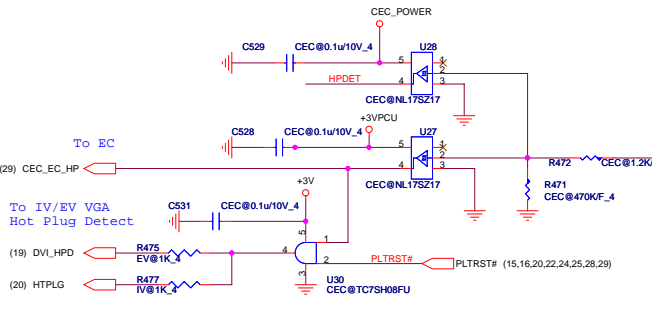
LANCELOT

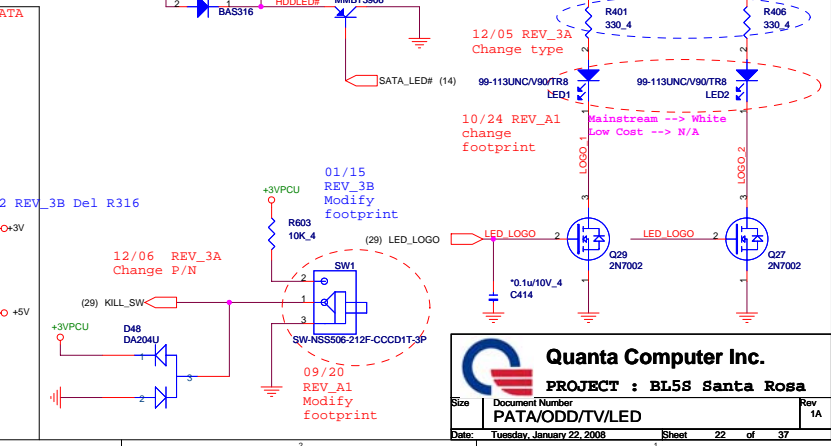
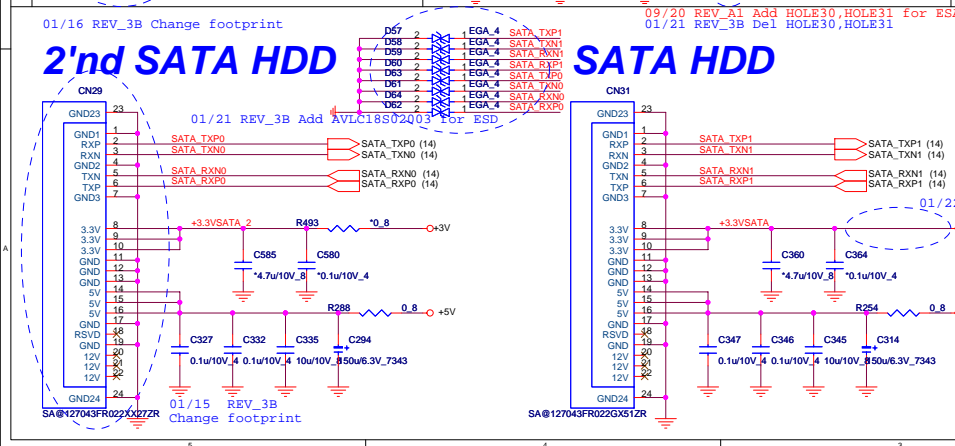
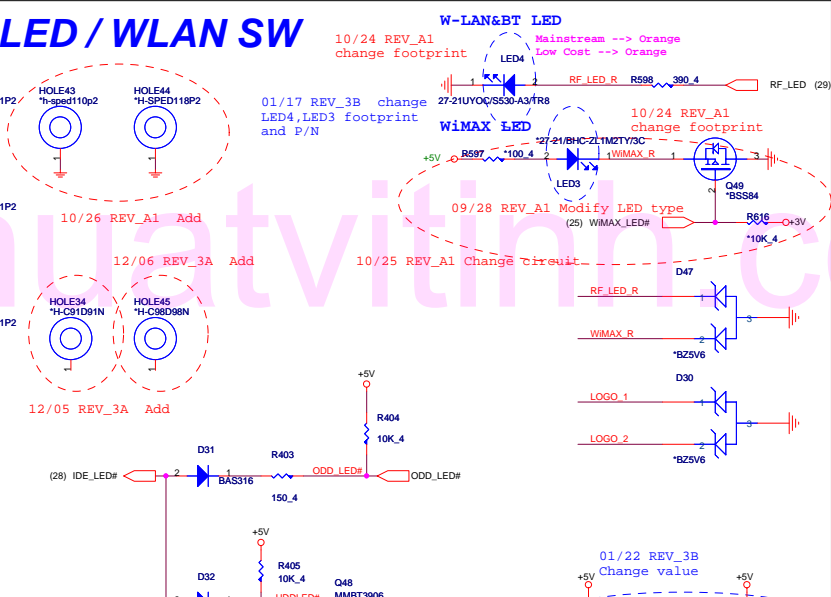
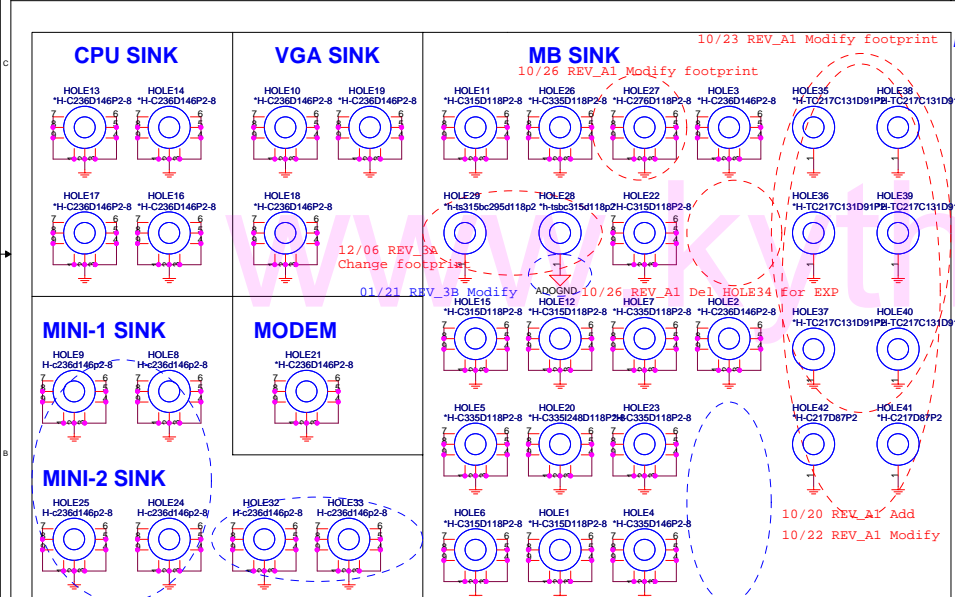
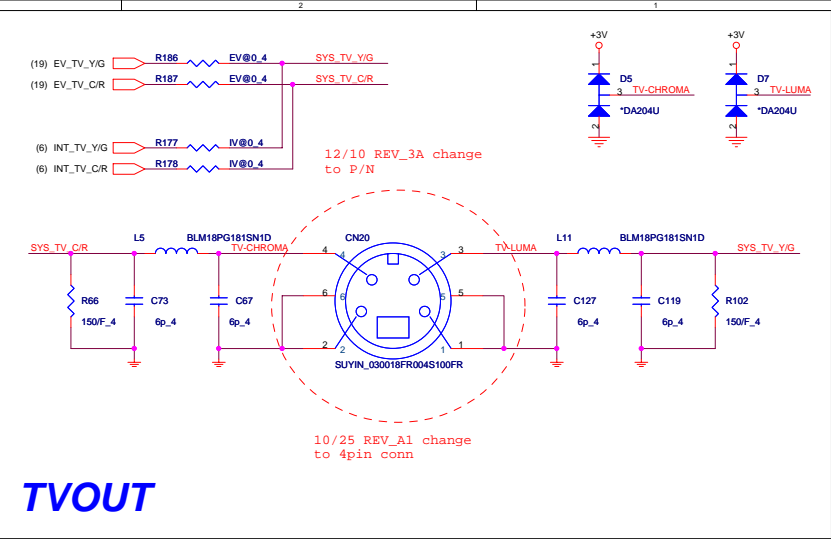
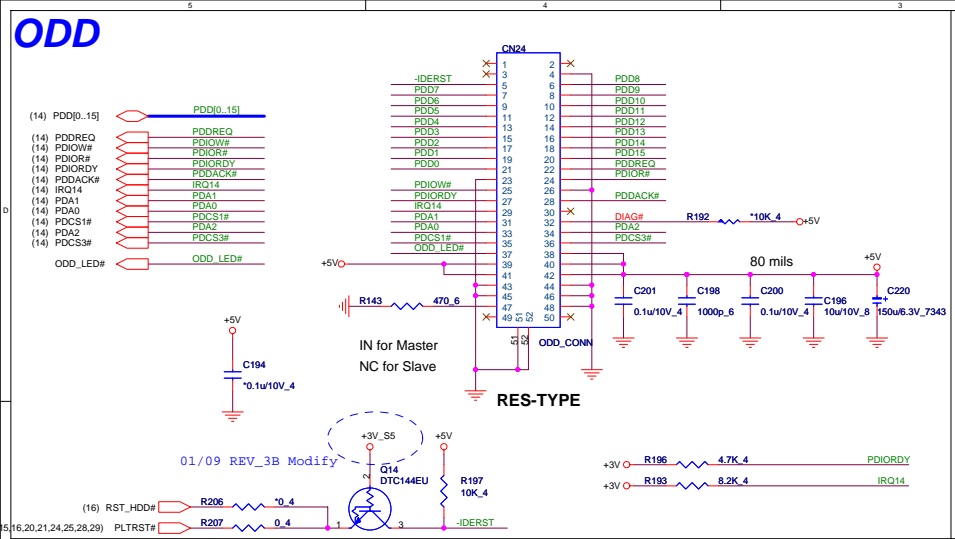


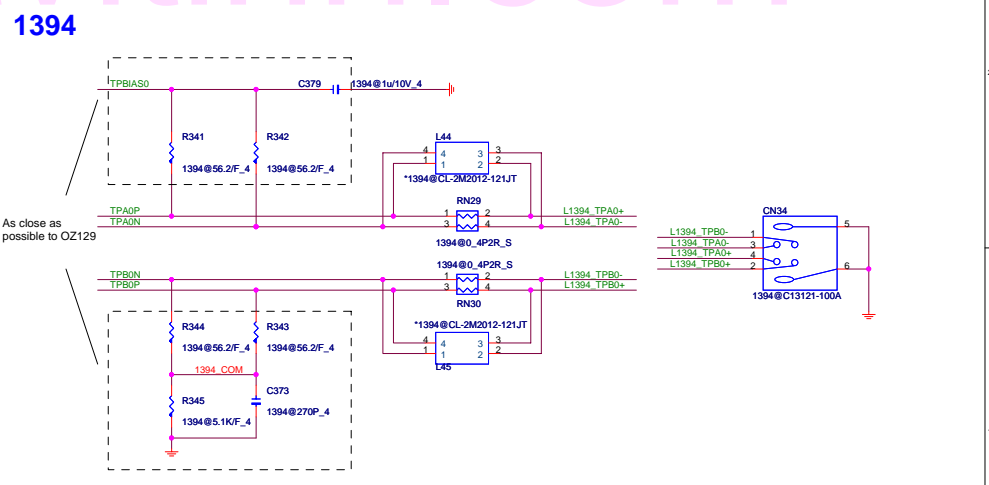
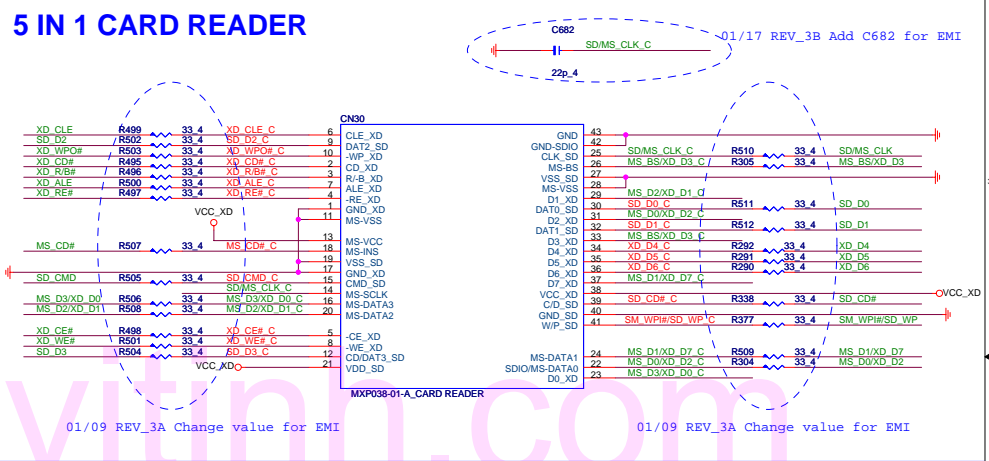
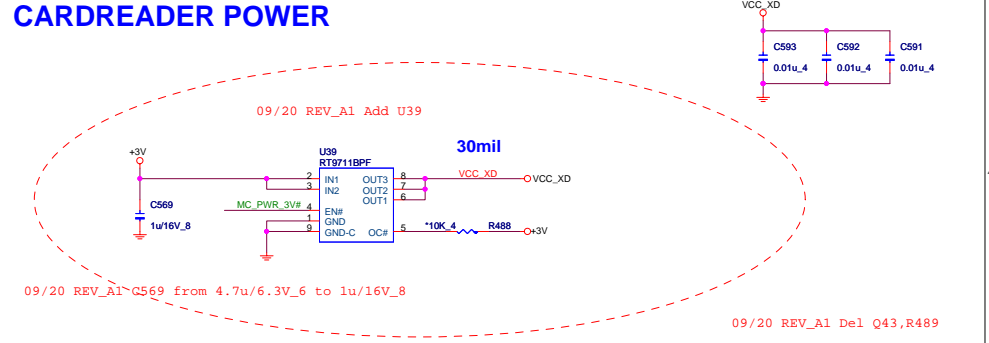
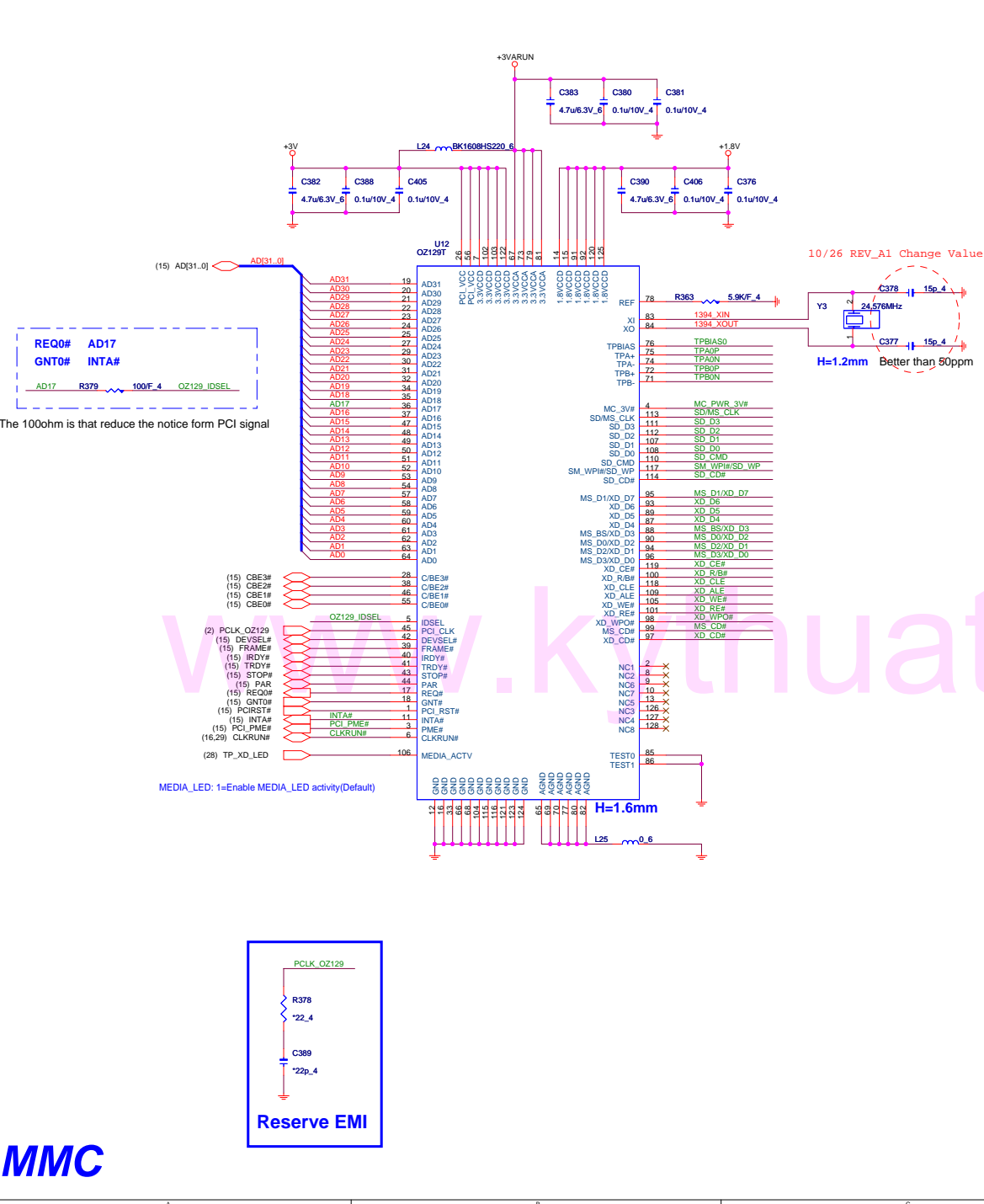
10/19 REV_A1 Add Q50,Q51,R156,R168,R606,R608



01/09 REV_3A Change footprint
10/19 REV_A1 Change footprint
12/07 REV_3A Change footprint



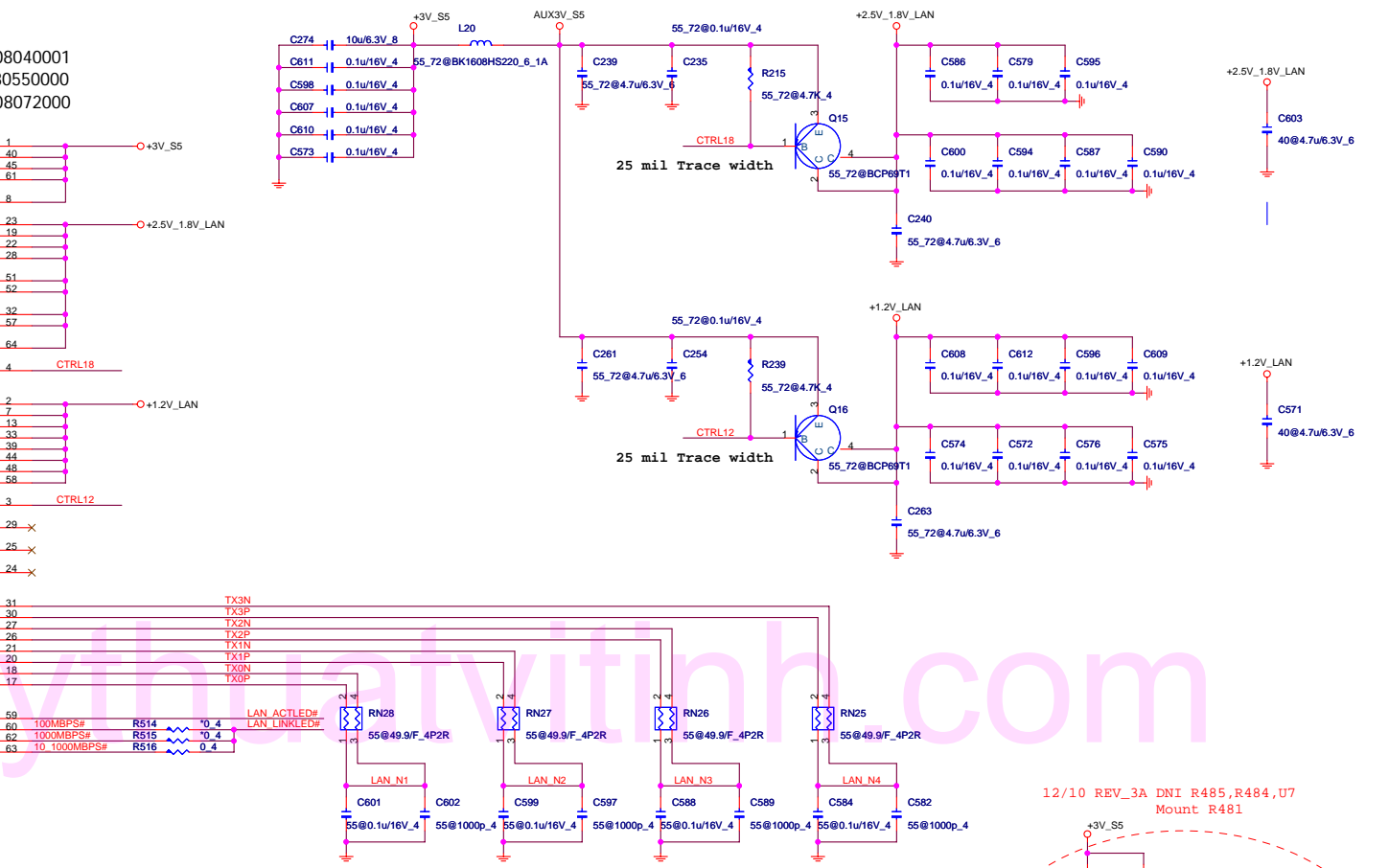
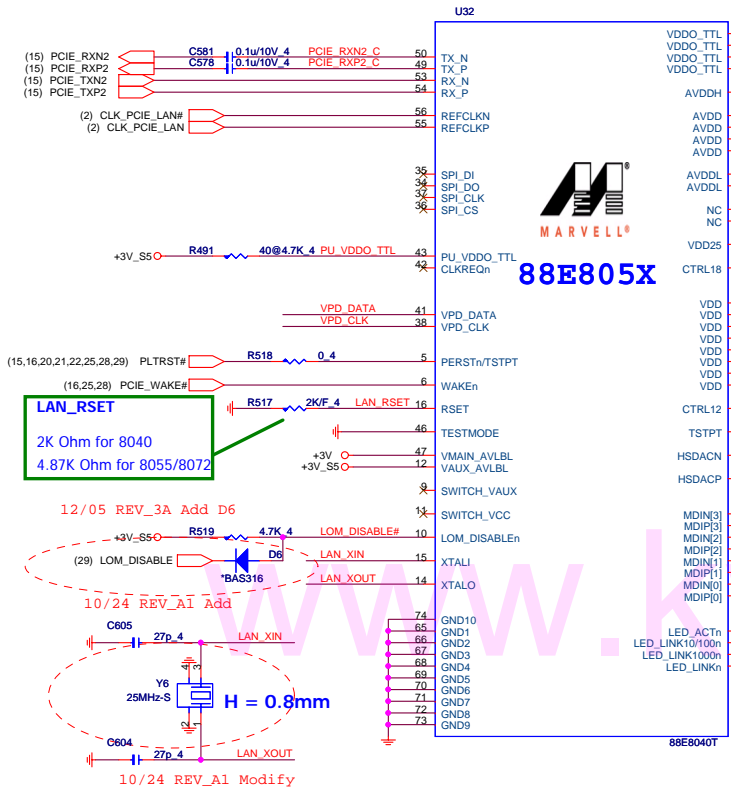




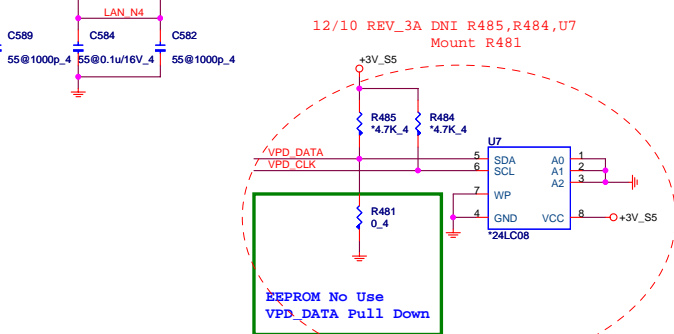
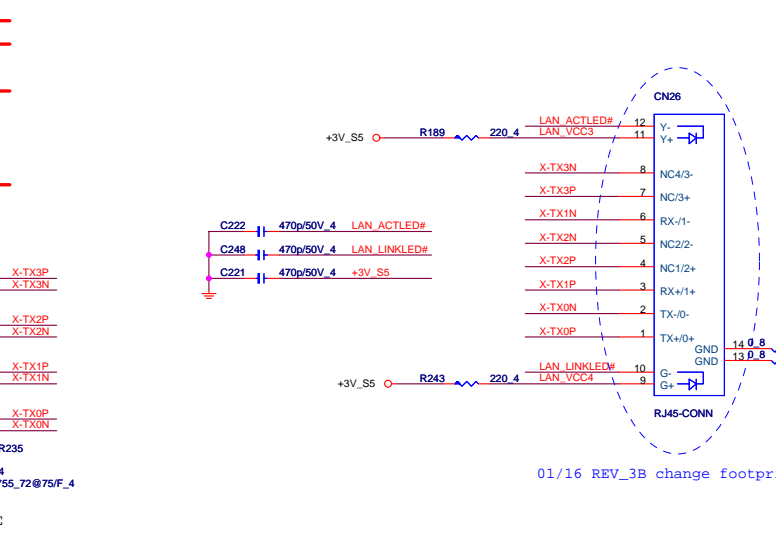
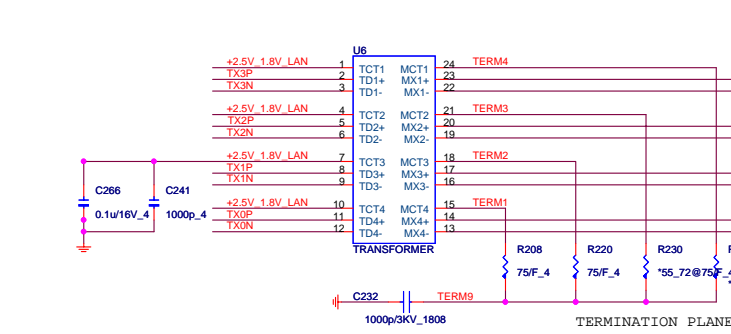
MMC

LAN_MARVELL_88E8040/88E8055/88E8072

10/100 : 88E8040 P/N : AL008040001
 GIGA : 88E8055 P/N : AJ080550000
 GIGA : 88E8072 P/N : AL008072000

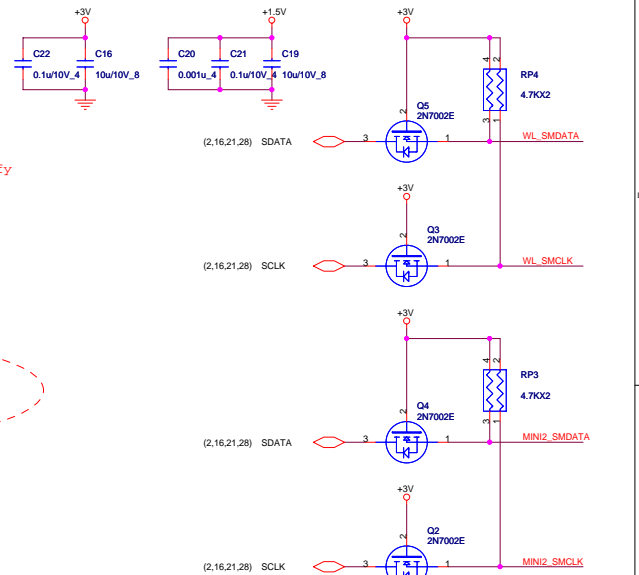
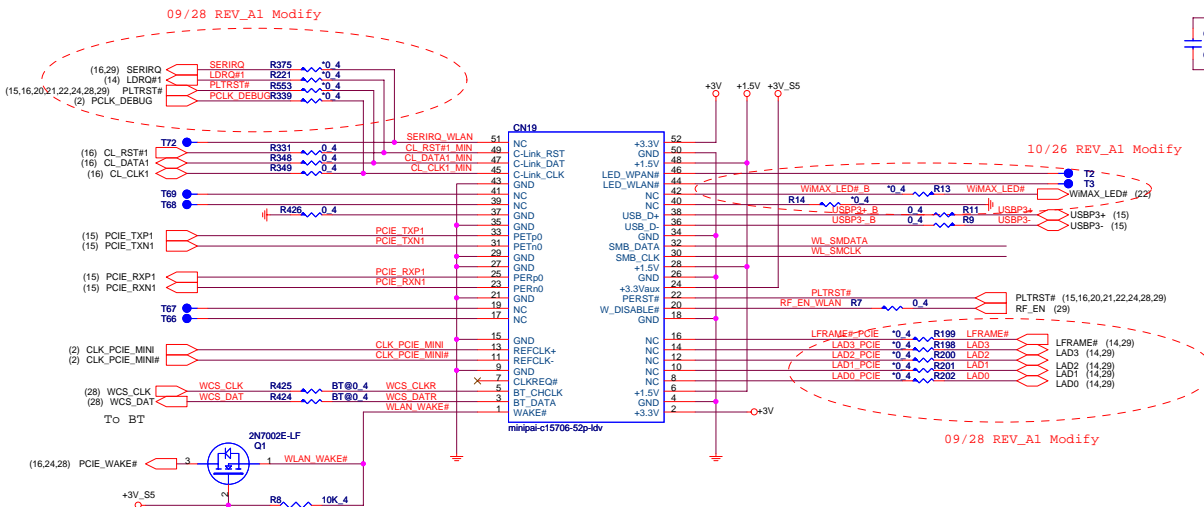


- ~~DELTA 10/100 : LFE8696-R P/N : DB0M8LAN00 H = 4mm~~
- ~~GIGA : LFE9249-R P/N : DB0ZR1LAN11~~
- ~~HWS 10/100 : HPL-4001B P/N : DB0SA1LAN01 H = 4mm~~
- ~~GIGA : HPL-68 P/N : DB0ZB1LAN12~~
- ~~BOTHHAND 10/100 : TST1284 LF P/N : DB0KN7LAN24 H = 4mm~~
- ~~GIGA : GST5009-LF P/N : DBKN1NLAN03~~

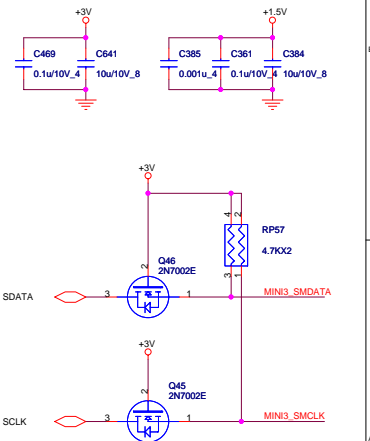
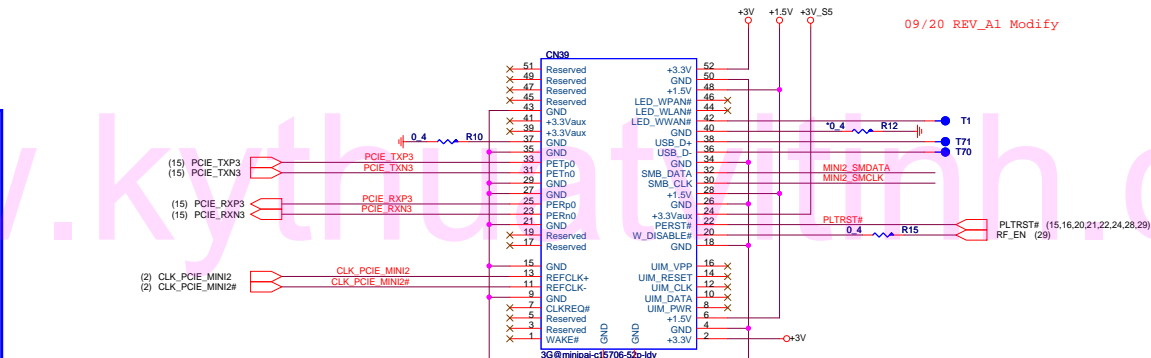
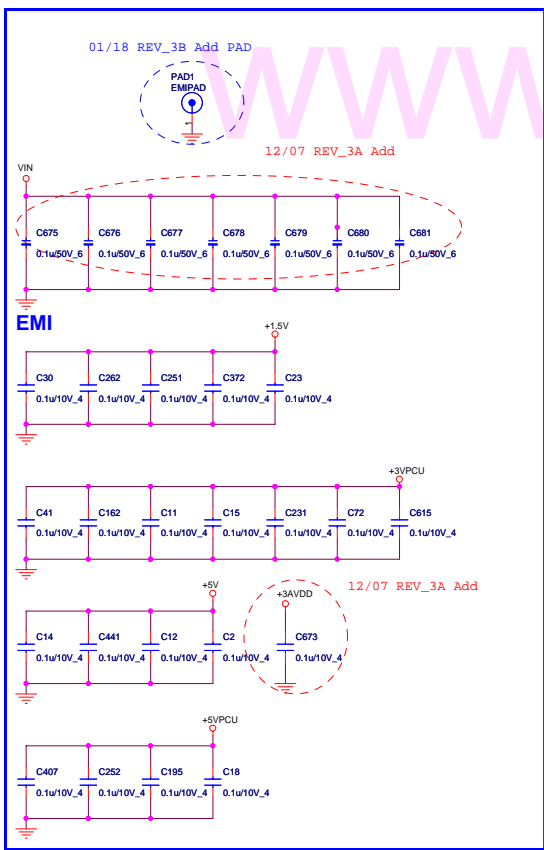


Mini PCI-E Card WLAN

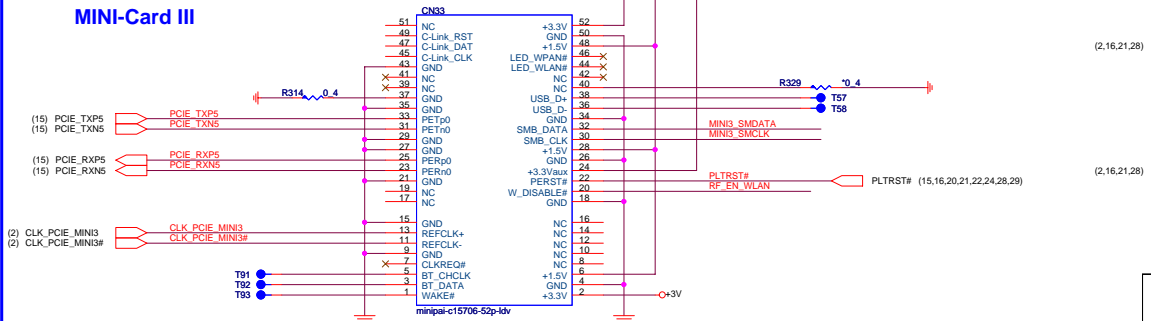
MINI-Card I



MINI-Card II

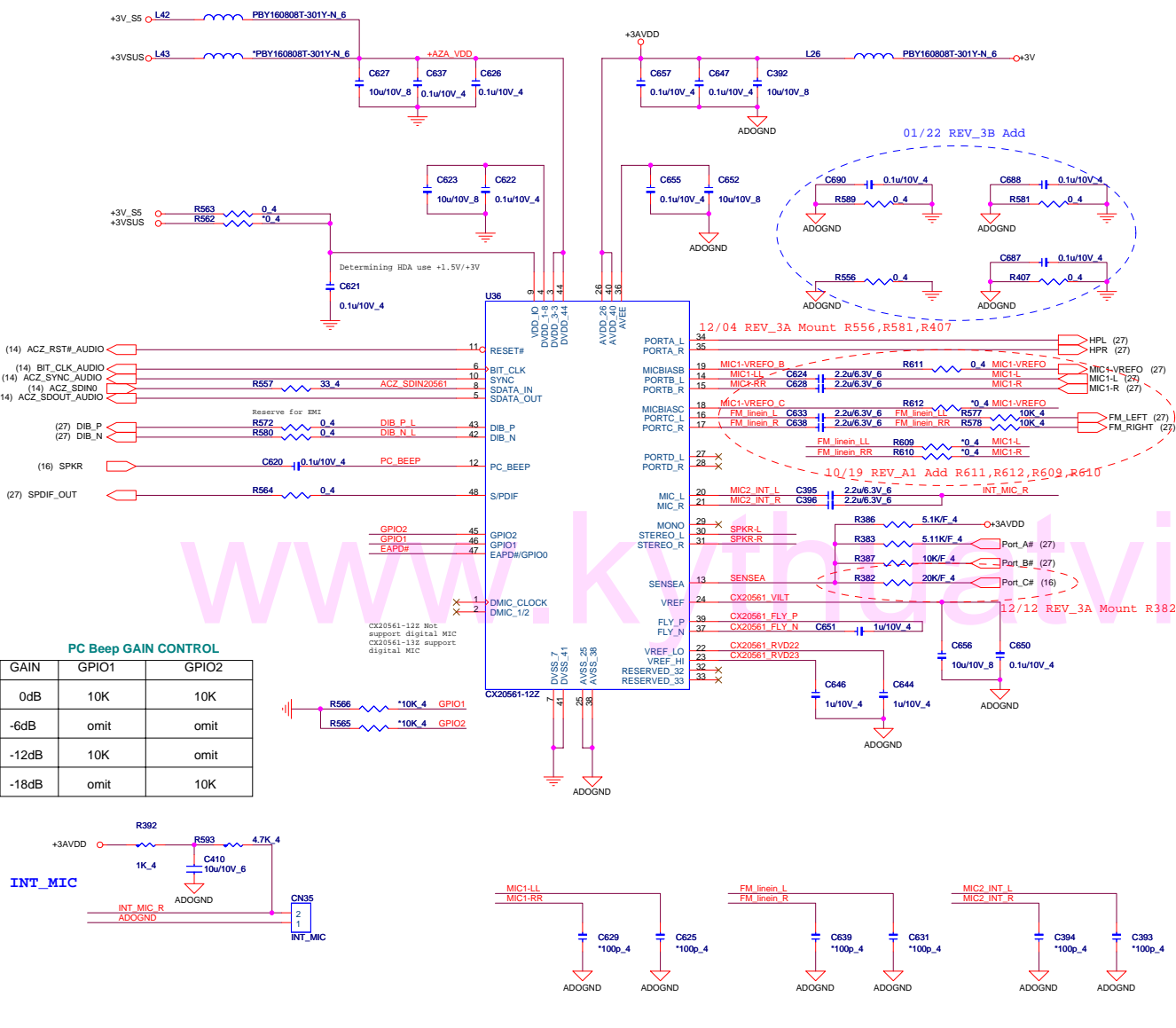


MINI-Card III



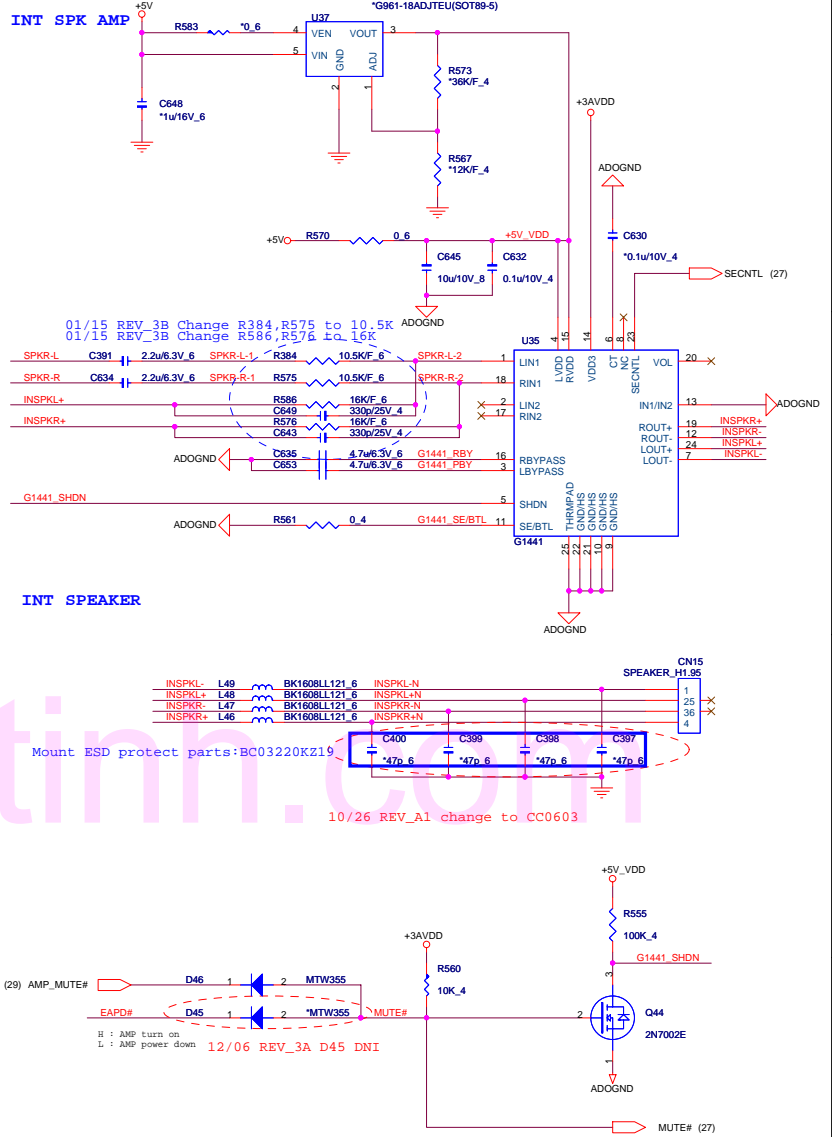
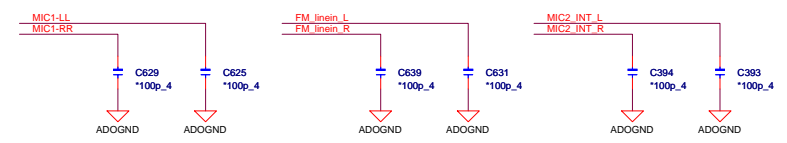
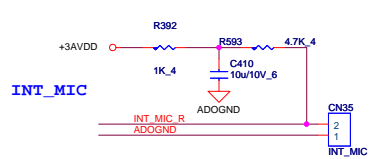
H= 8mm

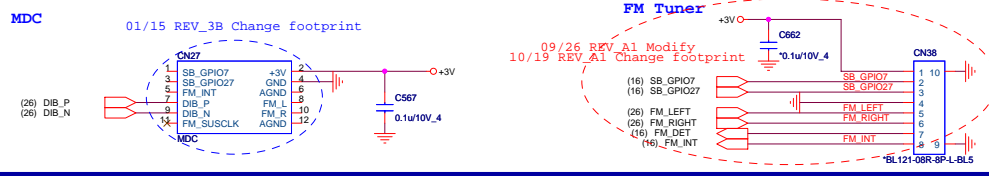
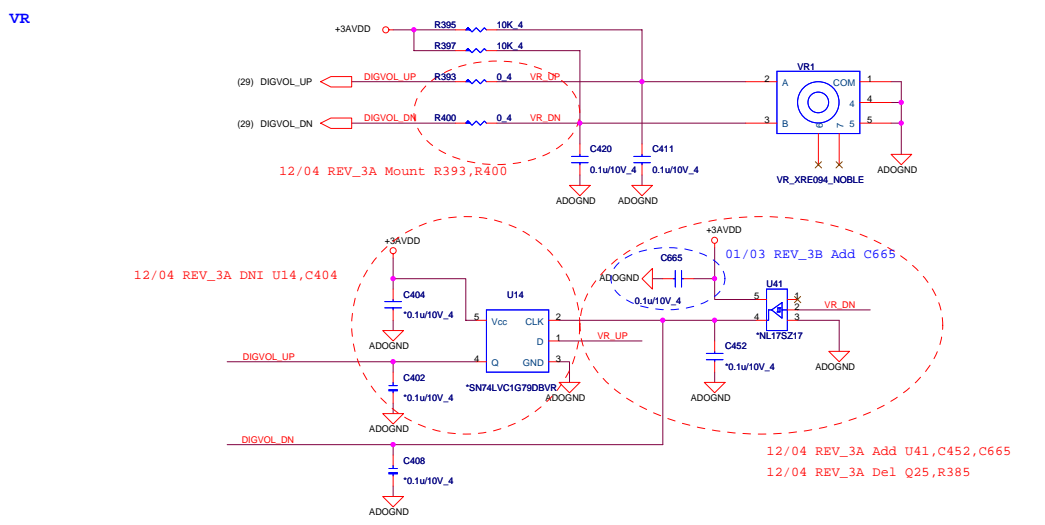
Codec (CX20561)



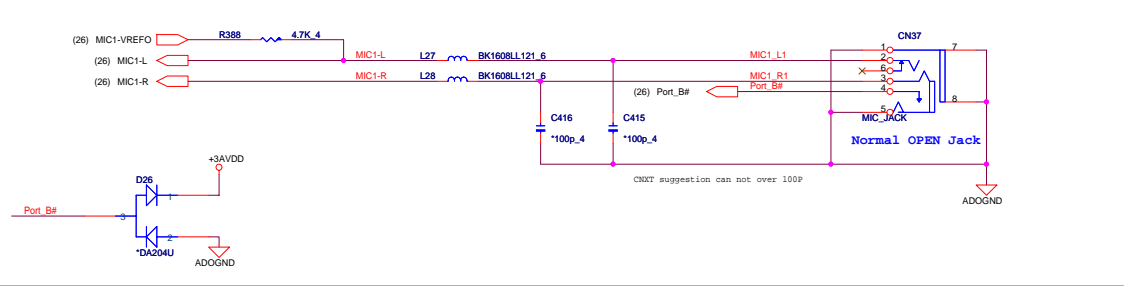
PC BEEP GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

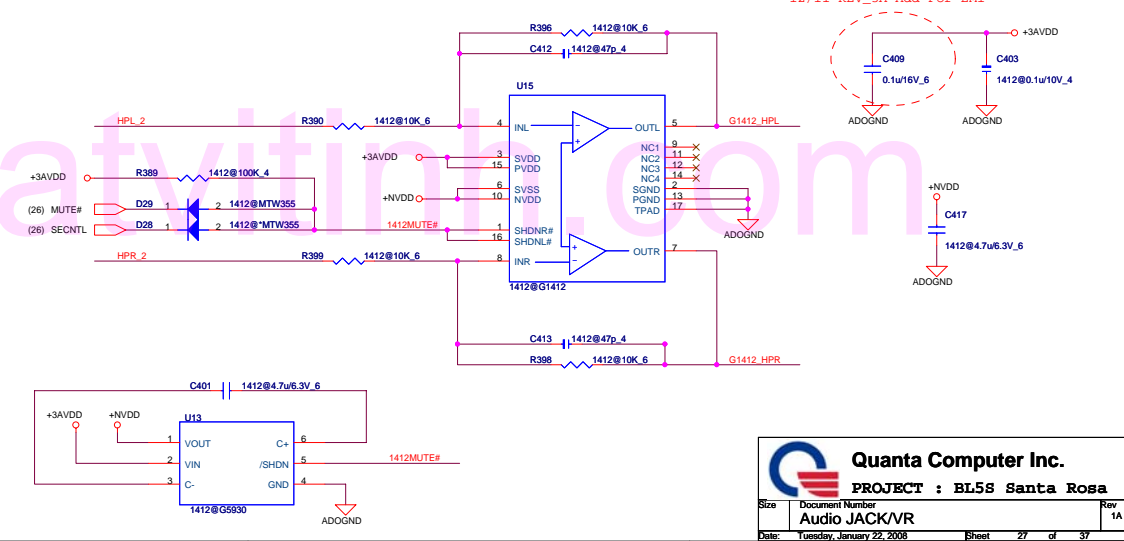




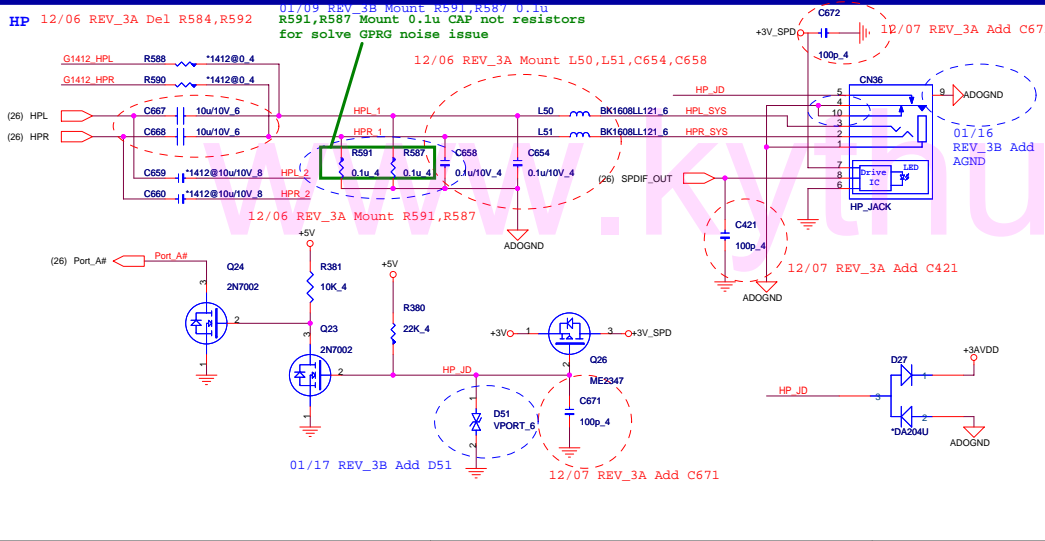
SYSTEM MIC



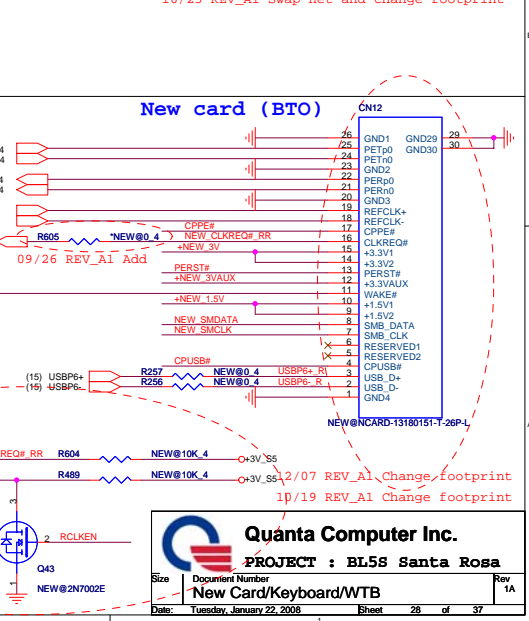
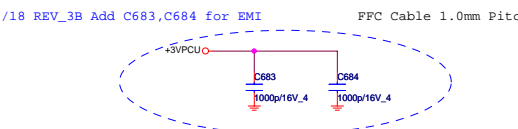
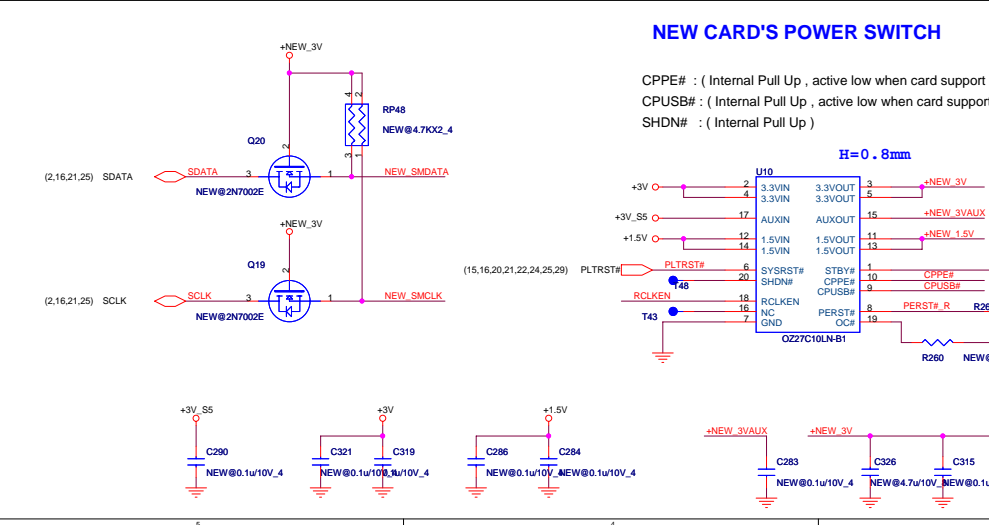
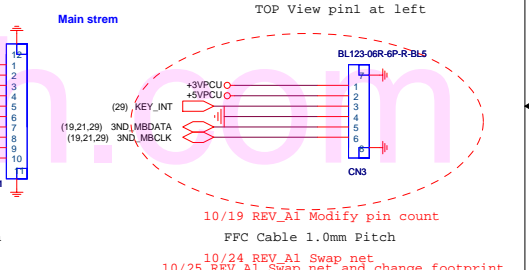
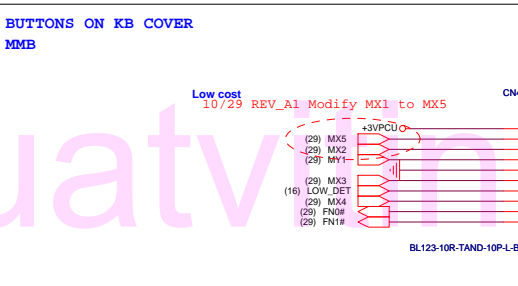
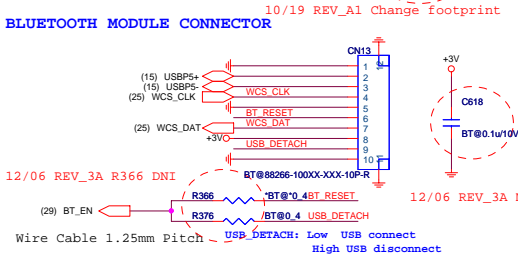
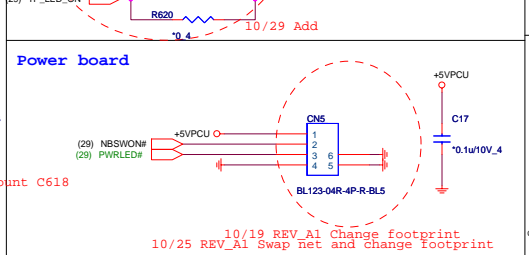
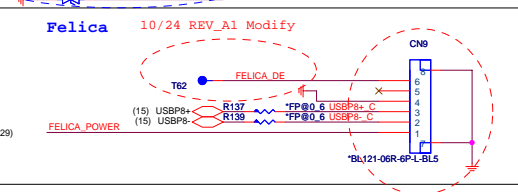
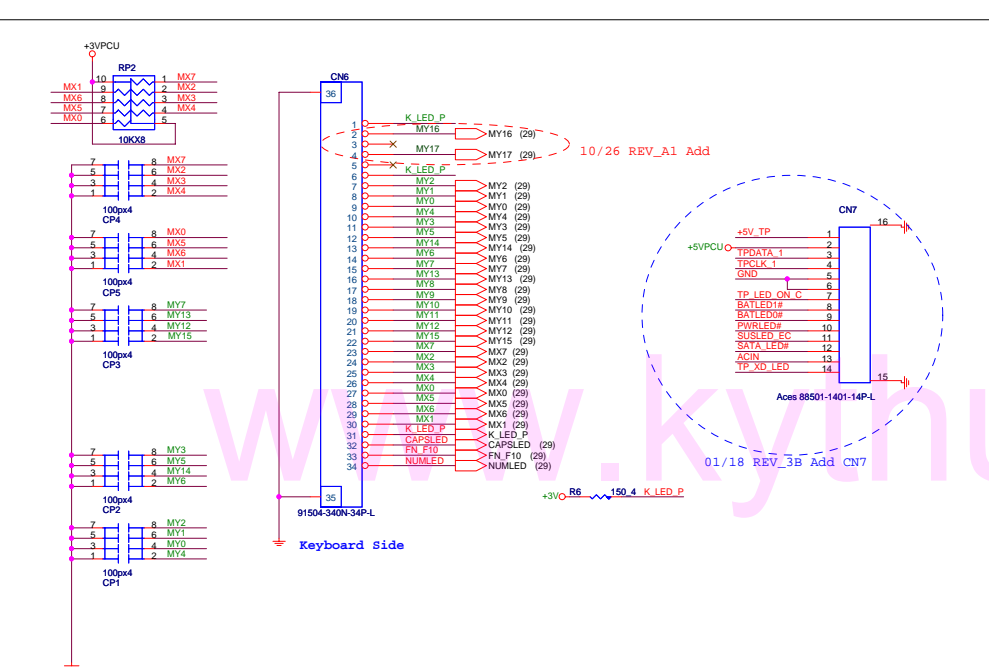
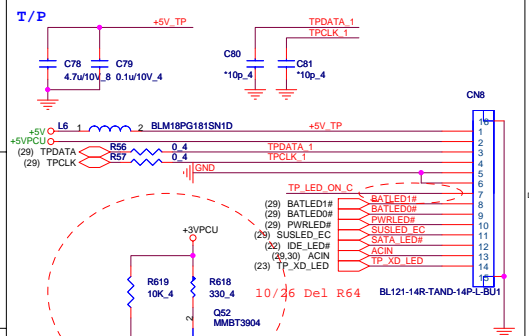
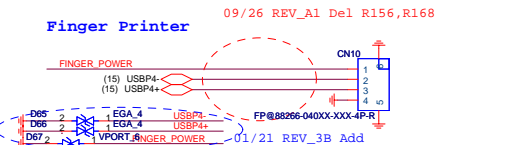
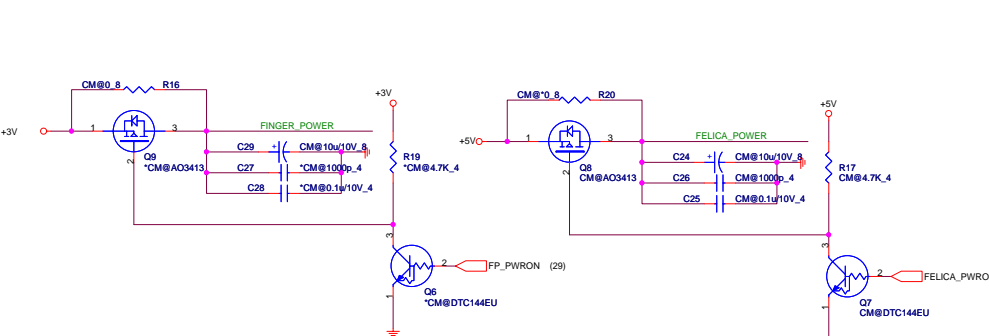
HP Amplifier



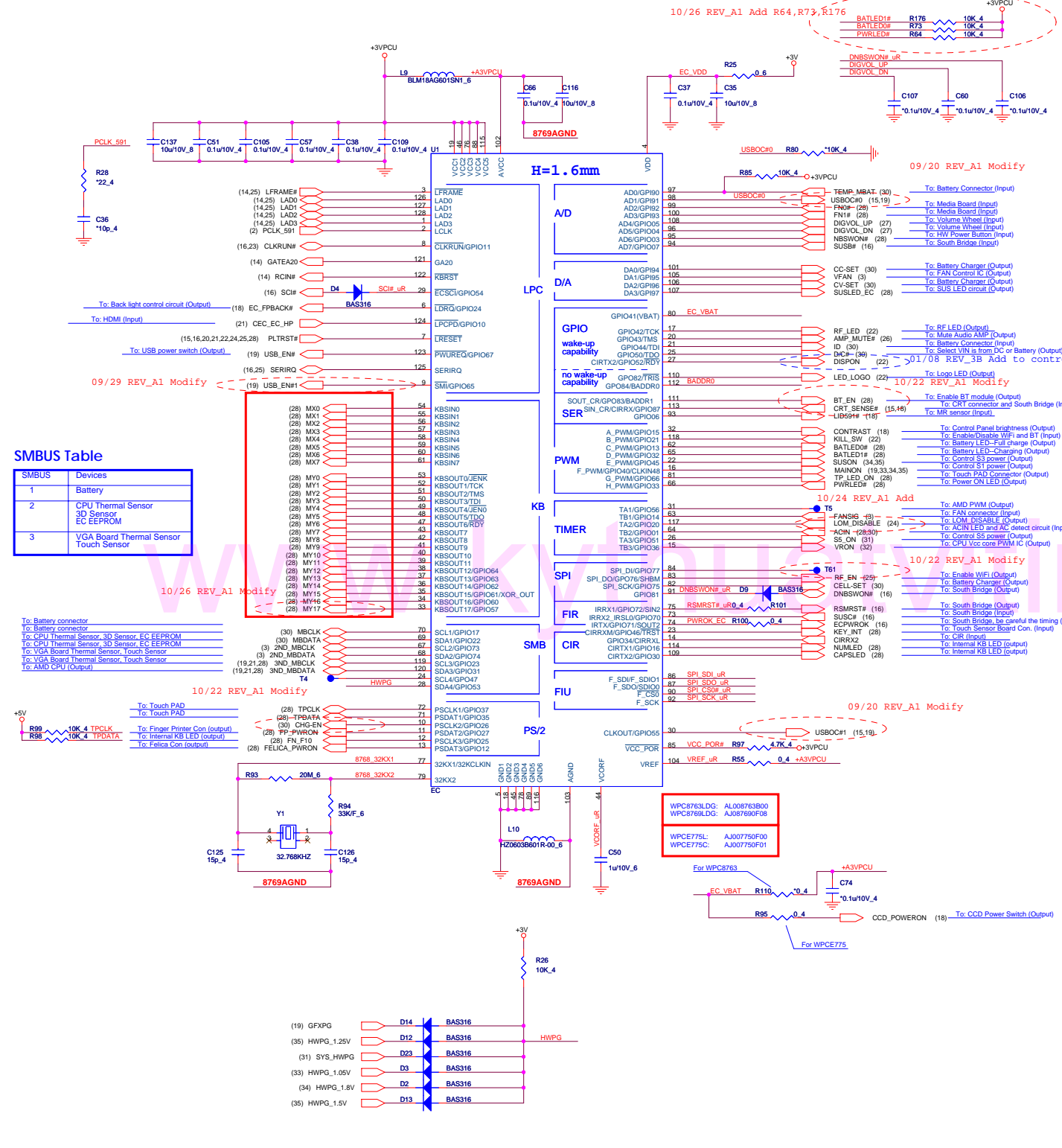
HP 12/06 REV_3A Del R584,R592



Quanta Computer Inc.
PROJECT : BL55 Santa Rosa
 Size Document Number Rev
 Audio JACK/VR 1A
 Date: Tuesday, January 22, 2008 Sheet 27 of 37



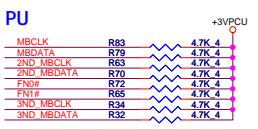
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
 Document Number
 New Card/Keyboard/WTB
 Date: Tuesday, January 22, 2008 Sheet 28 of 37



SMBUS Table

SMBUS	Devices
1	Battery
2	CPU Thermal Sensor 3D Sensor EC EEPROM
3	VGA Board Thermal Sensor Touch Sensor

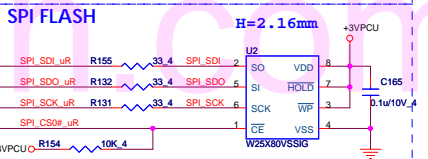
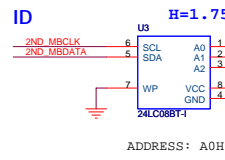
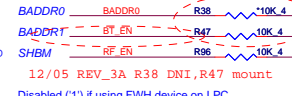
- To: Battery connector
- To: Battery connector
- To: CPU Thermal Sensor, 3D Sensor, EC EEPROM
- To: CPU Thermal Sensor, 3D Sensor, EC EEPROM
- To: VGA Board Thermal Sensor, Touch Sensor
- To: VGA Board Thermal Sensor, Touch Sensor
- To: AMD CPU (Output)



I/O Base Address

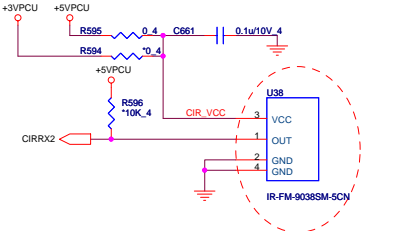
BADDR1-0	Index	Data
0 0		XOR TREE TEST MODE
0 1		CORE DEFINED
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

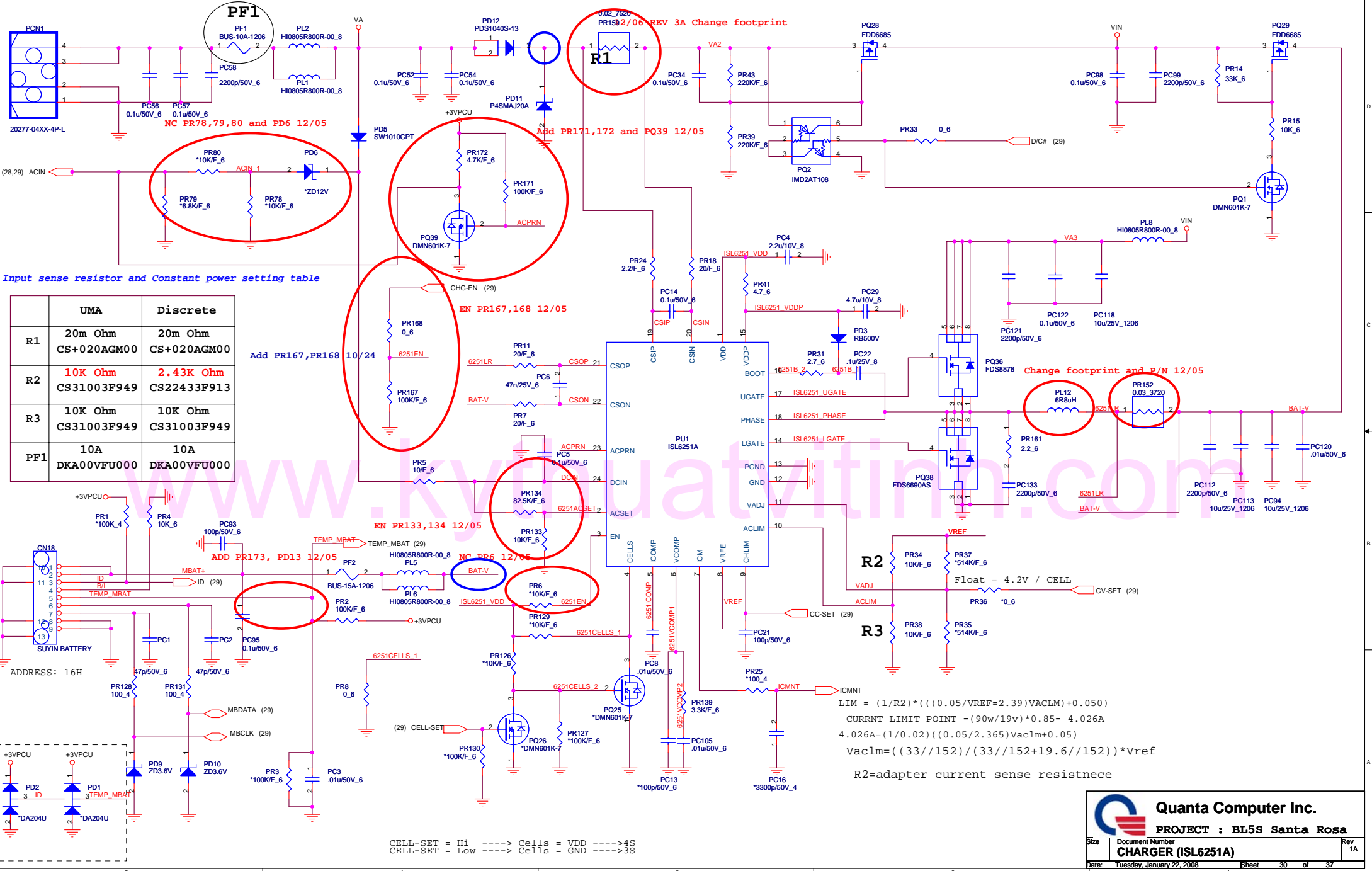


INTERNAL KEYBOARD SET

CIR (Copy from PB2A) Only for 8769/775C



10/19 REV_A1 Change footprint
10/21 REV_A1 Change pin define
12/07 REV_3A Change P/N



Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size: Document Number: **CHARGER (ISL6251A)** Rev: 1A
 Date: Tuesday, January 22, 2008 Sheet: 30 of 37

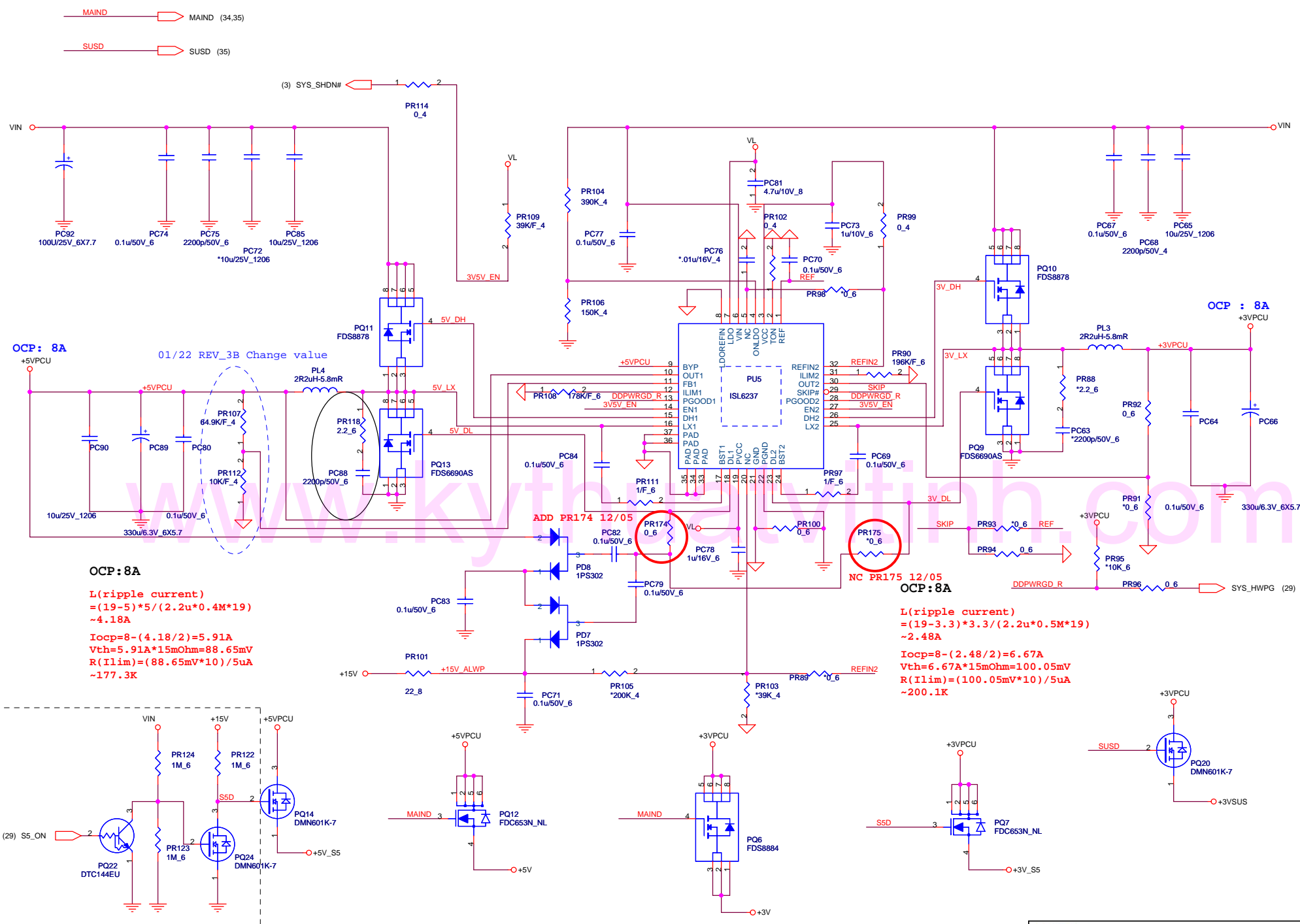
$$LIM = (1/R2) * (((0.05/VREF=2.39) * VACLm) + 0.050)$$

$$CURRNT LIMIT POINT = (90w/19v) * 0.85 = 4.026A$$

$$4.026A = (1/0.02) * (((0.05/2.365) * VACLm) + 0.05)$$

$$VACLm = ((33//152) / ((33//152) + 19.6//152)) * Vref$$

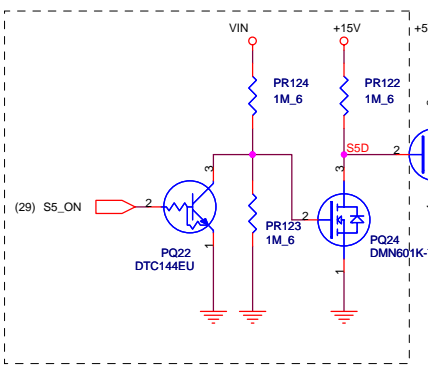
R2=adapter current sense resistnece

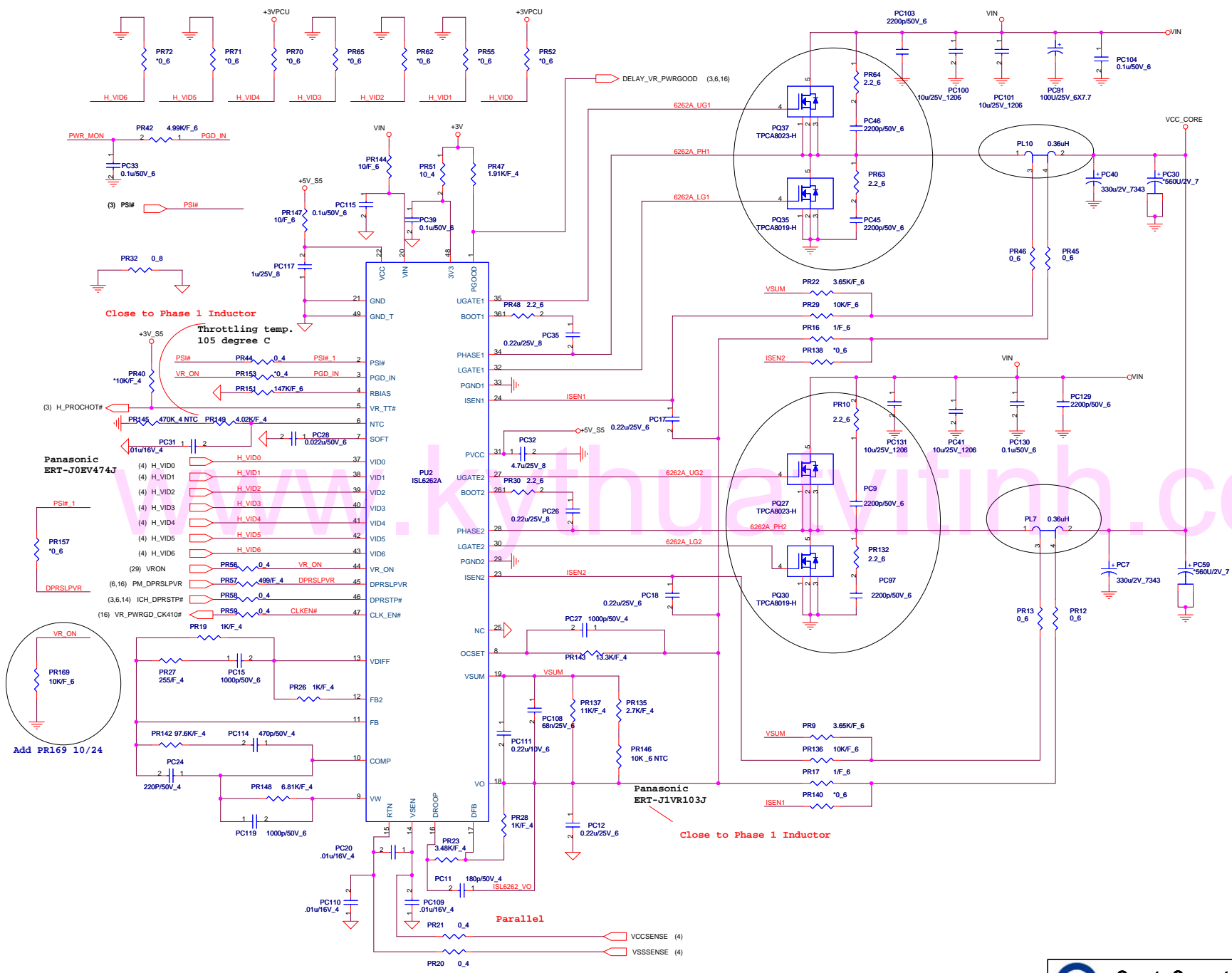


OCP: 8A
01/22 REV_3B Change value

OCP: 8A
 $L(\text{ripple current}) = (19-5) * 5 / (2.2 * 0.4 * 19) \sim 4.18A$
 $I_{ocp} = 8 - (4.18 / 2) = 5.91A$
 $V_{th} = 5.91A * 15m\Omega = 88.65mV$
 $R(I_{lim}) = (88.65mV * 10) / 5\mu A \sim 177.3K$

OCP: 8A
 $L(\text{ripple current}) = (19-3.3) * 3.3 / (2.2 * 0.5 * 19) \sim 2.48A$
 $I_{ocp} = 8 - (2.48 / 2) = 6.67A$
 $V_{th} = 6.67A * 15m\Omega = 100.05mV$
 $R(I_{lim}) = (100.05mV * 10) / 5\mu A \sim 200.1K$





Close to Phase 1 Inductor

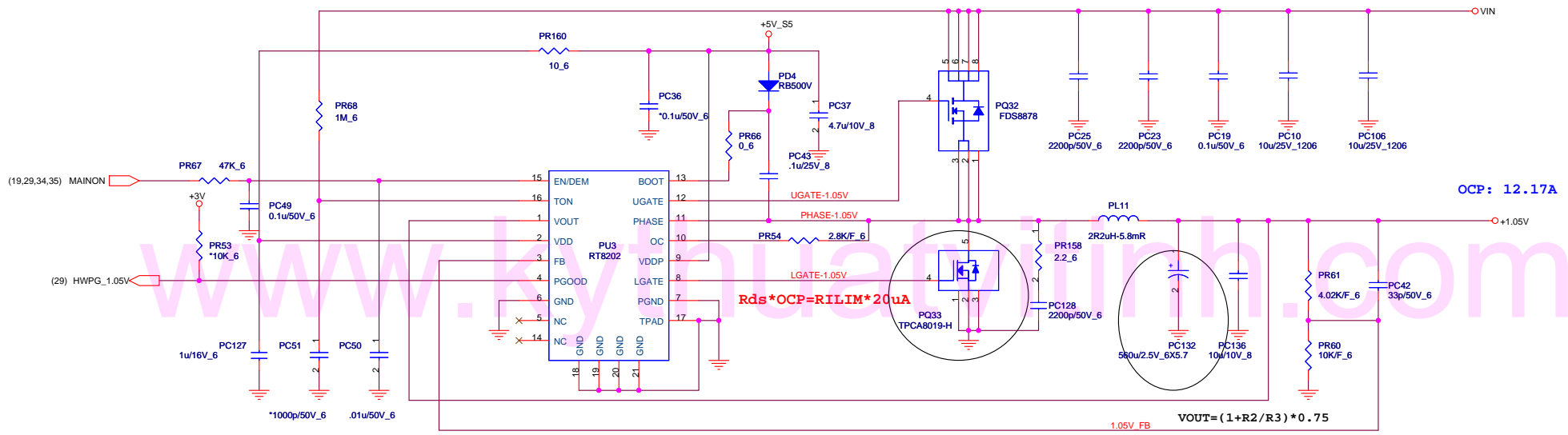
Throttling temp. 105 degree C

Close to Phase 1 Inductor

Add PR169 10/24

Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	CPU CORE(ISL6262A)	1A
Date:	Tuesday, January 22, 2008	Sheet 32 of 37



OCP: 12.17A

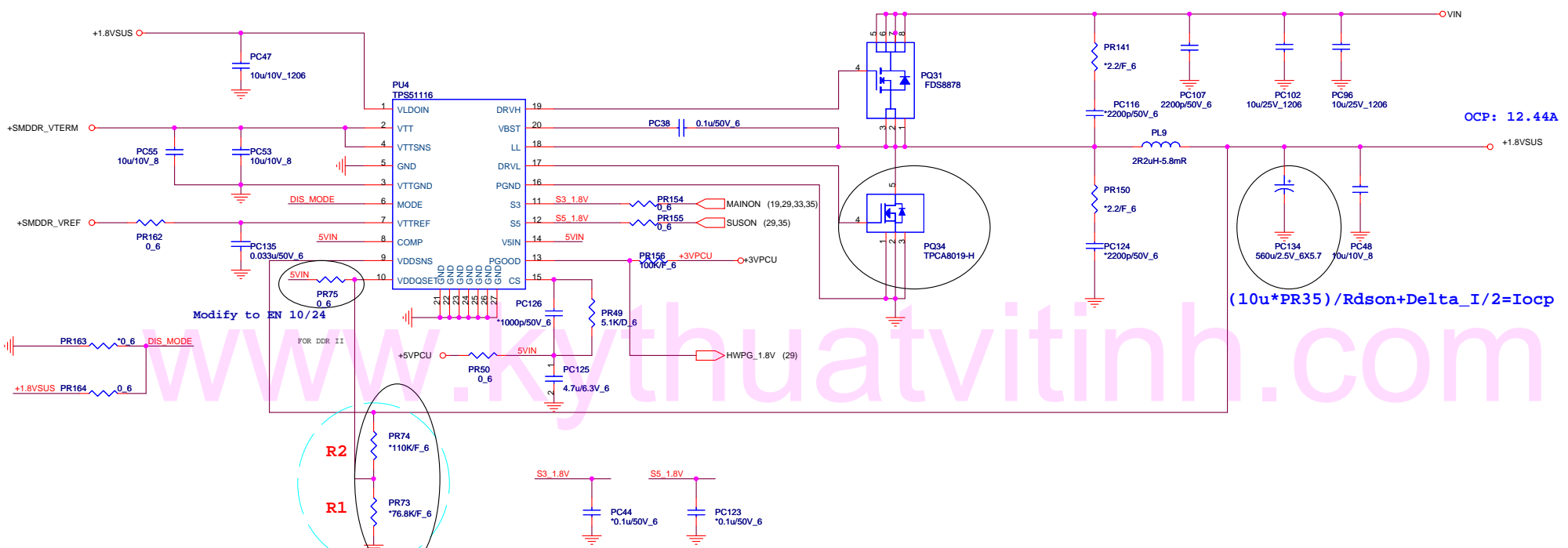
$$R_{ds} * OCP = R_{ILIM} * 20 \mu A$$

$$V_{OUT} = (1 + R_2 / R_3) * 0.75$$

$$T_{ON} = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} * T_{ON})$$

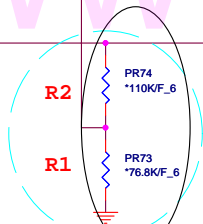
- AOL1412 R_{ds}=4.6mOhm
- 12.17A OCP --- OC=2.8K
- SI7636 R_{ds}=4.8mOhm
- 11.67A OCP --- OC=2.8K



OCP: 12.44A

$$(10\mu * PR35) / R_{dson} + \Delta I / 2 = I_{ocp}$$

Modify to EN 10/24

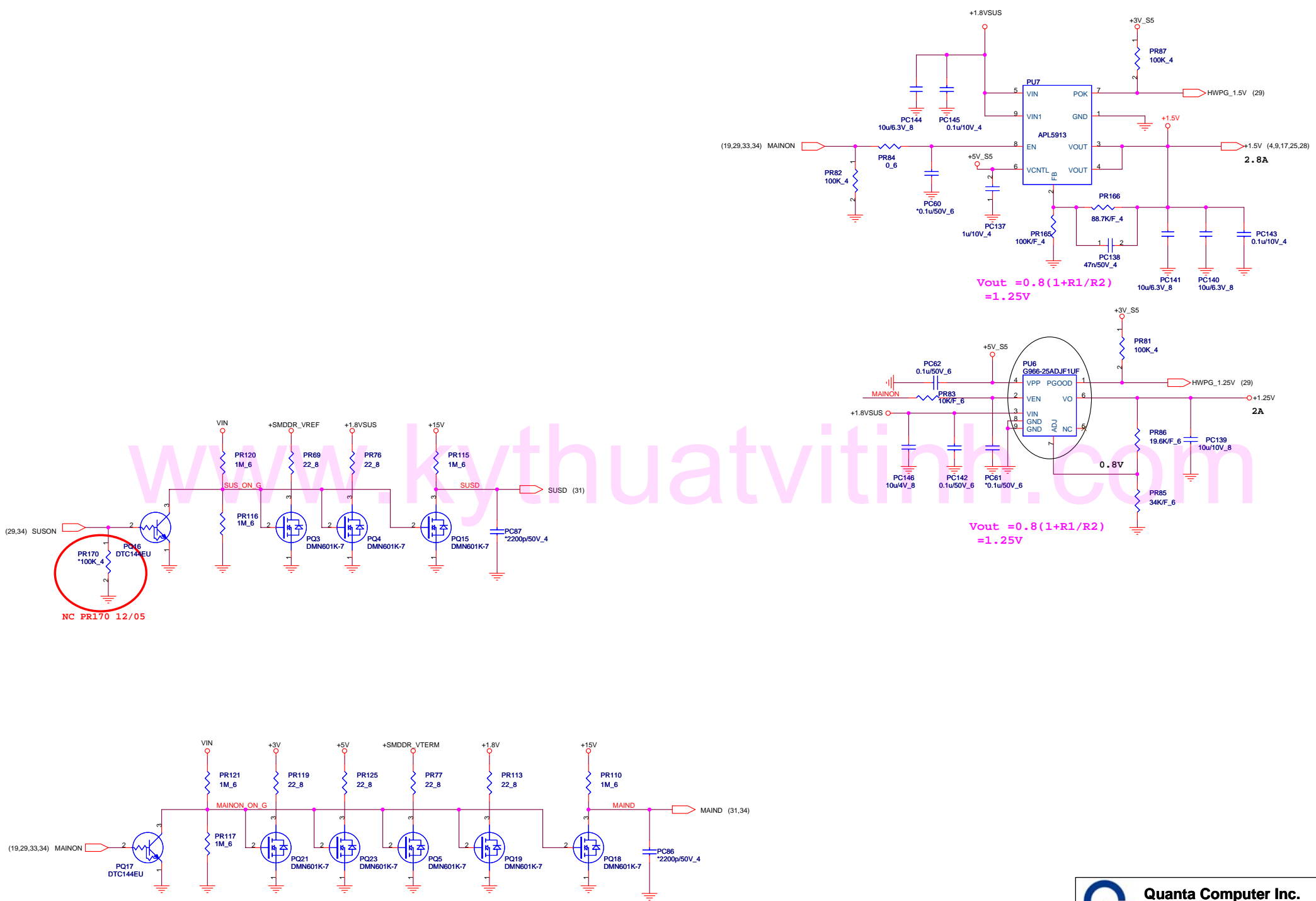


$$R1 = (100 * V_{out} - R2) * K$$

Modify to NC 10/24

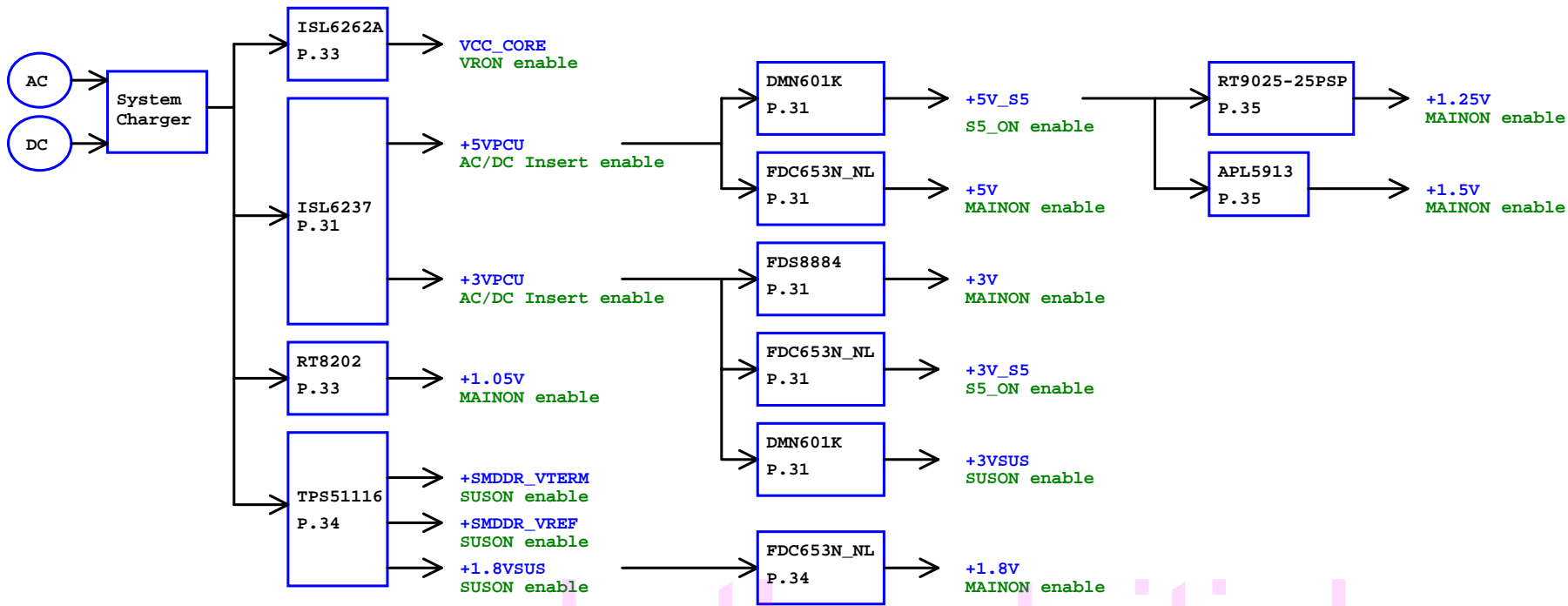
if tune Vout PR38 un-mount, PR156 PR165 mount





Model	REV	DATE	CHANGE LIST	NOTE
BL5S	00	20070824	FIRST RELEASED : 20070824	
	1A	20070914	FIRST RELEASED : E200709-2519	

www.kythuatvitinh.com



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M