NWQAA

Marseille 10G

LA-6062P REV 2.0 Schematic

Intel Processor(CFD/ARD) / PCH(HM57/HM55/PM55)

2010-03-24 Rev 2.0

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: ***Cover Page***

Size	Document Number	Rev
B	NWQAA LA-6062P M/B	2.0

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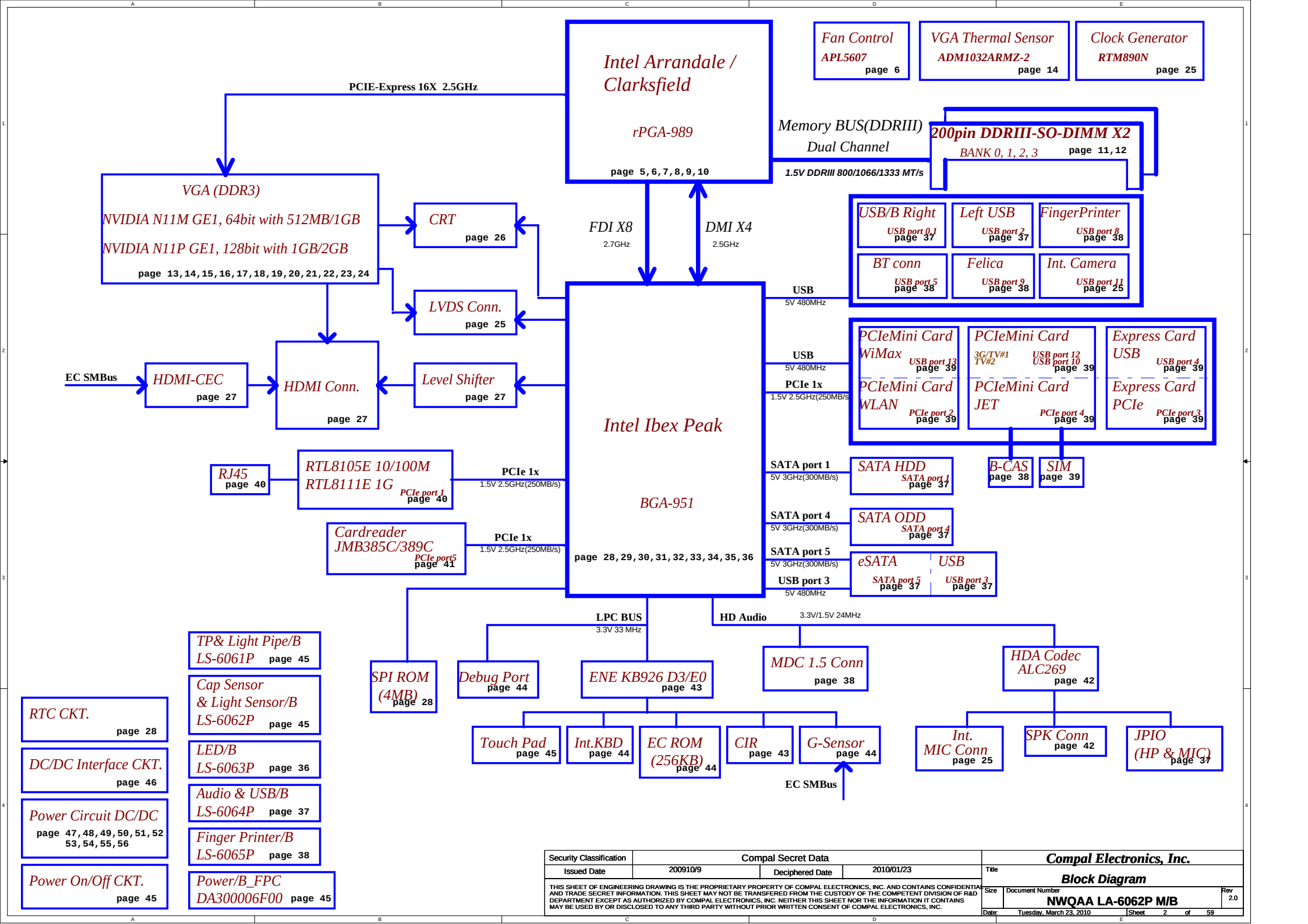

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Compal Electronics, Inc.			
Title: Block Diagram			
Size	Document Number: NWQAA LA-6062P M/B		Rev: 2.0
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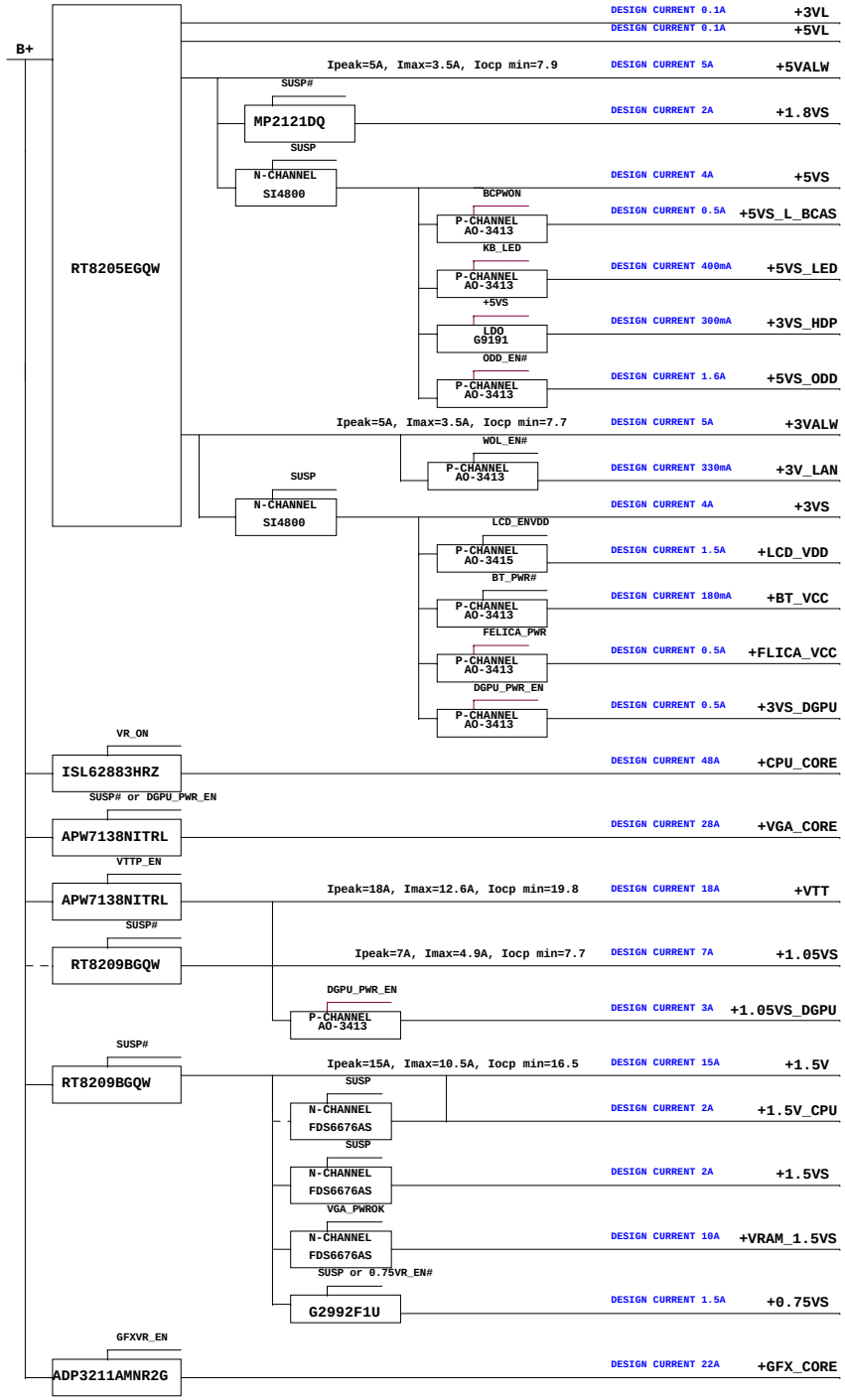

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Title: Power Tree

Size | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b

Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

Platform	SKU	CPU	PCH	VGA
Calpella	UMA(OPT@)	Arrandale	HM55@/HM57@	N/A
	Discrete (DIS@)	Clarksfield/ Arrandale	HM55@/HM57@/PM55@	N11P@/N11M@
	Optimus (OPT@)	Arrandale	HM55@/HM57@	N11P@/N11M@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/ Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS			Camera & Mic
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel			Camera & Mic
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving		GPU					New Card
description	S3 Power Saving		N11P & N11E			N11M		New Card
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-OP1	New Card
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE@	N11MOP@	NEW@

Function	Card reader	
description	JMB385C/389C	
explain	JMB385C	JMB389C
BTO	JMB385@	JMB389@

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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Size: Custom	Document Number: NWQAA LA-6062P M/B		Rev: 2.0
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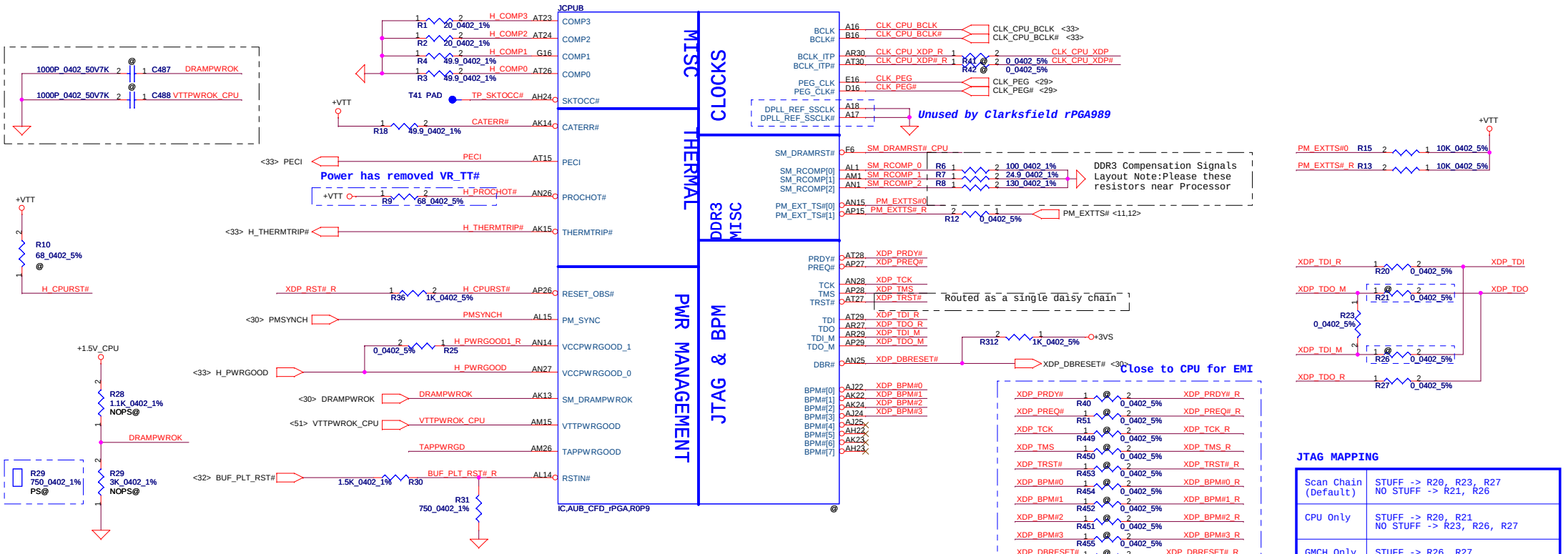
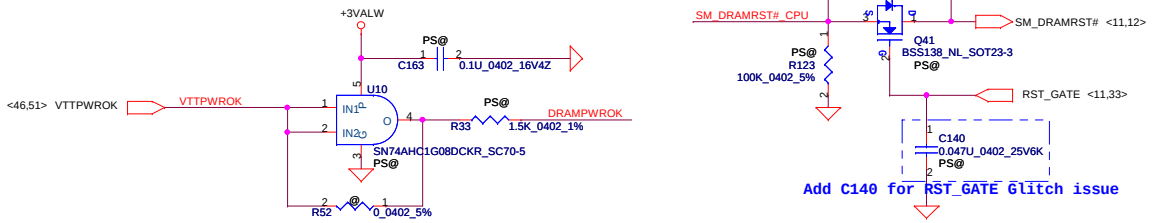


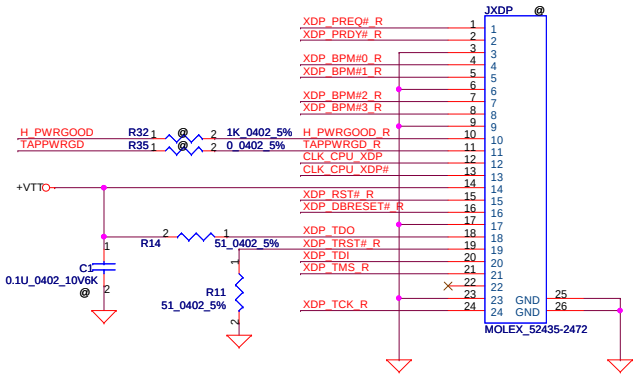
JTAG MAPPING

Scan Chain (Default)	STUFF -> R20, R23, R27 NO STUFF -> R21, R26
CPU Only	STUFF -> R20, R21 NO STUFF -> R23, R26, R27
GMCH Only	STUFF -> R26, R27 NO STUFF -> R20, R21, R23

For S3 CPU Power Saving



XDP Connector



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Title: *CPU_CLK/MISC/JTAG/XDP*

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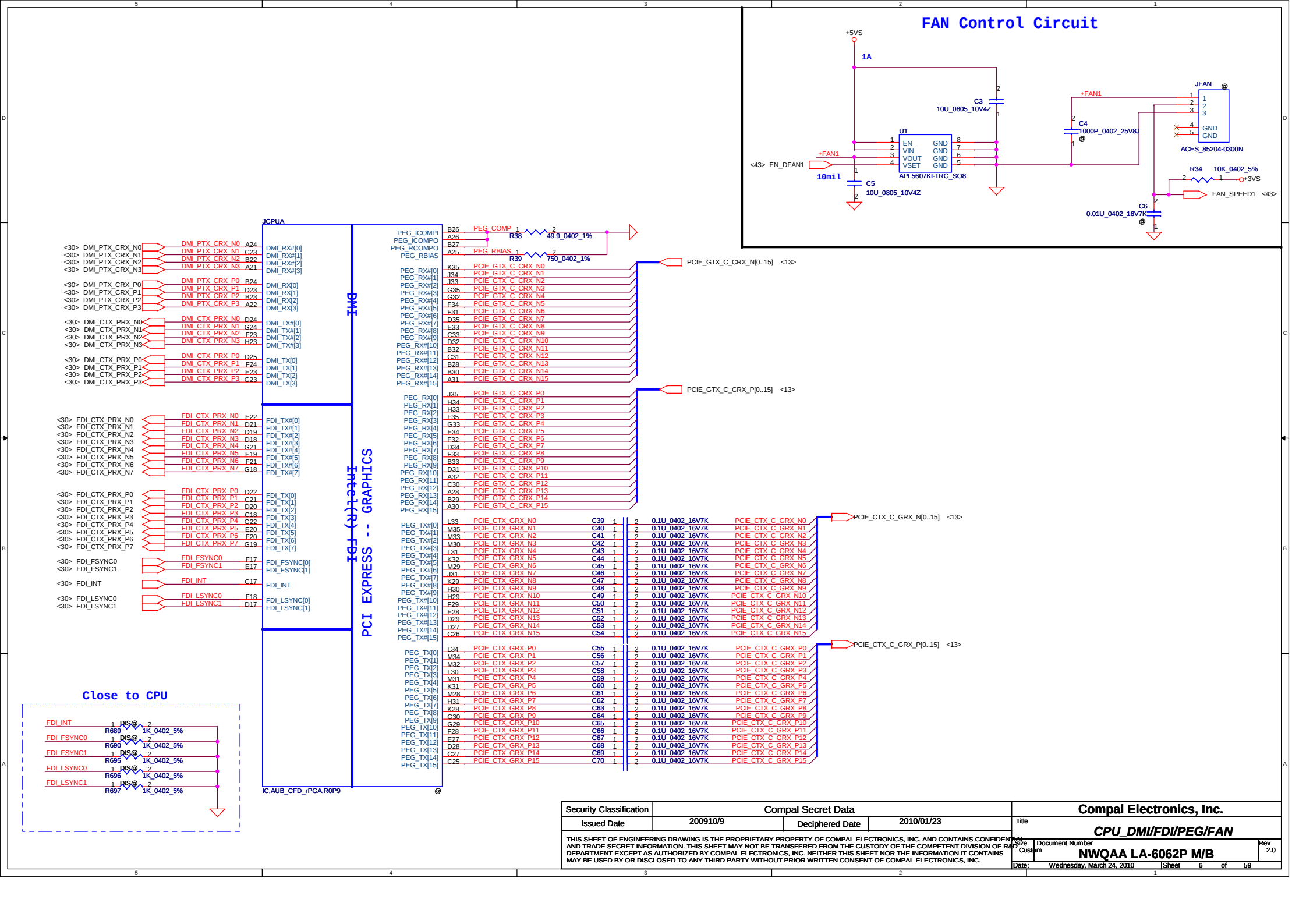

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Compal Electronics, Inc.			
Title: CPU_DMI/FDI/PEG/FAN			
Size: Custom	Document Number: NWQAA LA-6062P M/B		Rev: 2.0
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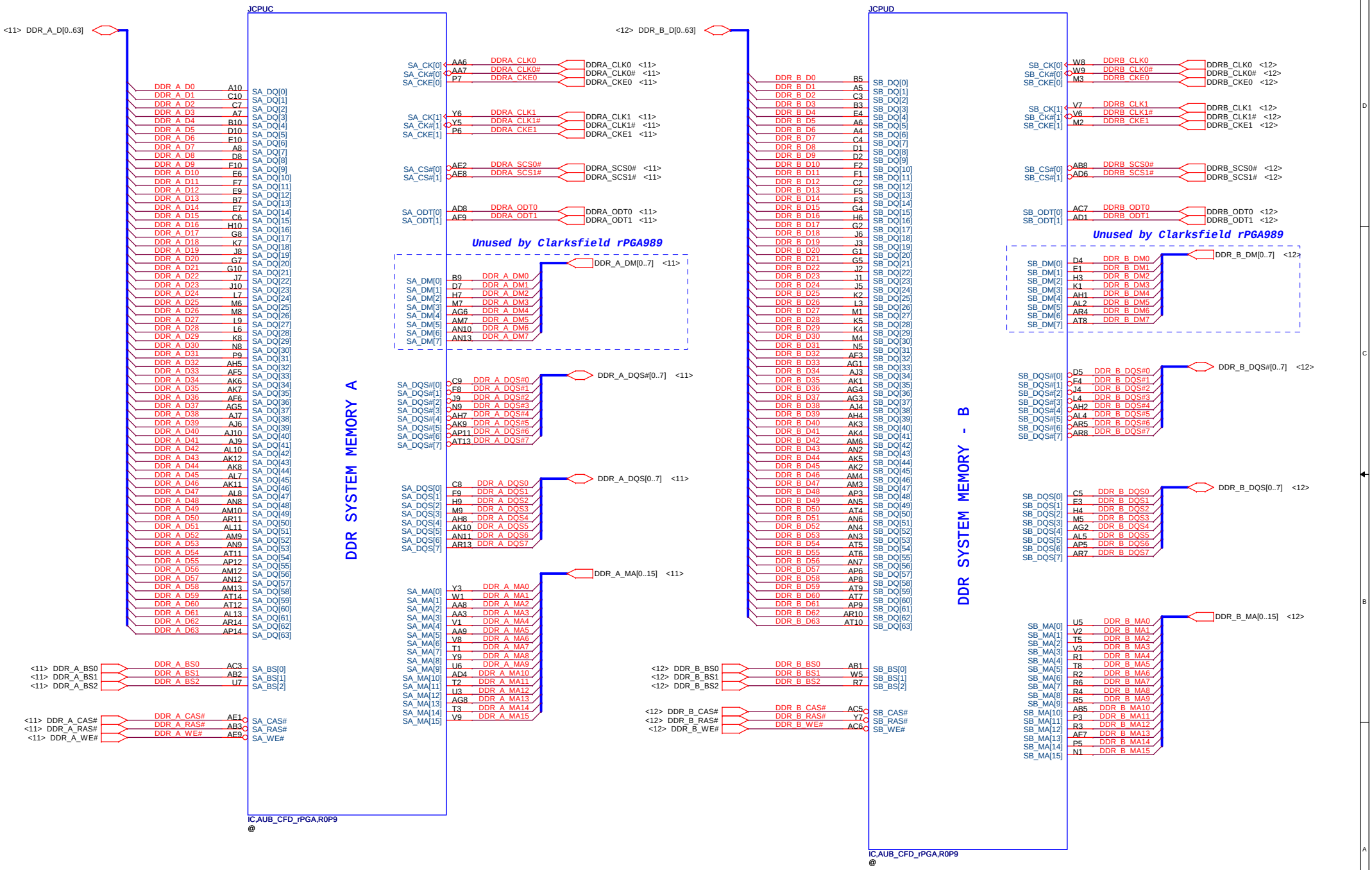

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Title: ***CPU_DDR3***

Size	Document Number	Rev
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Material Note (+VTT):
390uF/ 10mohm, number are 3,
power x1, HW x2

(Place these capacitors under CPU socket Edge, top layer)

Clarksfield: 65A
Auburndale:48A

Clarksfield: 21A
Auburndale:18A

JCPUF

+CPU_CORE

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
V35 VCC61
V34 VCC62
V33 VCC63
V32 VCC64
V31 VCC65
V30 VCC66
V29 VCC67
V28 VCC68
V27 VCC69
V26 VCC70
U35 VCC71
U34 VCC72
U33 VCC73
U32 VCC74
U31 VCC75
U30 VCC76
U29 VCC77
U28 VCC78
U27 VCC79
U26 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

IC,AUB_CFD_rPGA,R0P9
@

CPU CORE SUPPLY

1.1V RAIL POWER

VTT0_1 AH14
VTT0_2 AH12
VTT0_3 AH11
VTT0_4 AH10
VTT0_5 J14
VTT0_6 J13
VTT0_7 H14
VTT0_8 H12
VTT0_9 G14
VTT0_10 G13
VTT0_11 G12
VTT0_12 G11
VTT0_13 F14
VTT0_14 F13
VTT0_15 F12
VTT0_16 F11
VTT0_17 E14
VTT0_18 E12
VTT0_19 D14
VTT0_20 D13
VTT0_21 D12
VTT0_22 D11
VTT0_23 C14
VTT0_24 C13
VTT0_25 C12
VTT0_26 C11
VTT0_27 B14
VTT0_28 B12
VTT0_29 A14
VTT0_30 A13
VTT0_31 A12
VTT0_32 A11

VTT0_33 AE10
VTT0_34 AE10
VTT0_35 AC10
VTT0_36 AB10
VTT0_37 Y10
VTT0_38 W10
VTT0_39 U10
VTT0_40 T10
VTT0_41 J12
VTT0_42 J11
VTT0_43 J16
VTT0_44 J15

+VTT

Change C144 to 4.5mm height at DVT

C144 330U_2.5V_M_R17
C267 390U_2.5V_M_R10
C87 22U_0805_6.3V6M
C91 22U_0805_6.3V6M

C81 10U_0805_10V4K
C83 10U_0805_10V4K
C85 10U_0805_10V4K
C89 10U_0805_10V4K
C88 10U_0805_10V4K
C90 10U_0805_10V4K
C92 10U_0805_10V4K
C94 10U_0805_10V4K
@

5/25: Add for power team request.

+CPU_CORE

C158 C150 C128 C127 C120 C118 C119 C117 C129
22U_0805_6.3V6M

POWER

CPU VIDS

PSI# AN33 H_PSI# → H_PSI# <54>

VID[0] AK35 CPU_VID0 → CPU_VID0 <54>
VID[1] AK33 CPU_VID1 → CPU_VID1 <54>
VID[2] AK34 CPU_VID2 → CPU_VID2 <54>
VID[3] AL35 CPU_VID3 → CPU_VID3 <54>
VID[4] AL33 CPU_VID4 → CPU_VID4 <54>
VID[5] AM33 CPU_VID5 → CPU_VID5 <54>
VID[6] AM35 CPU_VID6 → CPU_VID6 <54>

PROC_DPRSLPVR AM34 H_DPRSLPVR_R R62 0_0402_5% → H_DPRSLPVR <54>

VTT_SELECT G15 H_VTTSELECT → H_VTTSELECT <51>

CRB default setting:
VID[6:0]=[0100111]

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

H_VTTSELECT = low, 1.1V
H_VTTSELECT = high, 1.05V

SENSE LINES

ISENSE AN35 IMVP_IMON → IMVP_IMON <54>

VCC_SENSE AJ34 VCCSENSE_R R65 0_0402_5%
VSS_SENSE AJ35 VSSSENSE_R R66 0_0402_5%

R64 100_0402_1% → +CPU_CORE
VCCSENSE → VCCSENSE <54>
VSSSENSE → VSSSENSE <54>
R67 100_0402_1%

VTT_SENSE B15 VTT_SENSE → VTT_SENSE <51>
VSS_SENSE_VTT A15 VSS_SENSE_VTT → VSS_SENSE_VTT <51>

Close to CPU

(Place these capacitors between inductor and socket on Bottom)

+CPU_CORE

C71 C72 C73 C74 C75 C76 C77 C78 C79
10U_0805_10V4K

(Place these capacitors under CPU socket, top layer)

+CPU_CORE

C98 C99 C100 C101 C102 C103 C104
10U_0805_10V4K

(Place these capacitors on CPU cavity, Bottom Layer)

+CPU_CORE

C105 C106 C107 C108 C109 C110
C111 C112 C113 C114 C115 C116
22U_0805_6.3V6M

TOP side (under inductor)

+CPU_CORE

C121 C122 C123 C124 C125 @
330U_D2_2.5VM_R9M

Check list:

+CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF

+VTT: 4x 330uF, 7x 22uF, 8x 10uF

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Title: CPU_POWER-1

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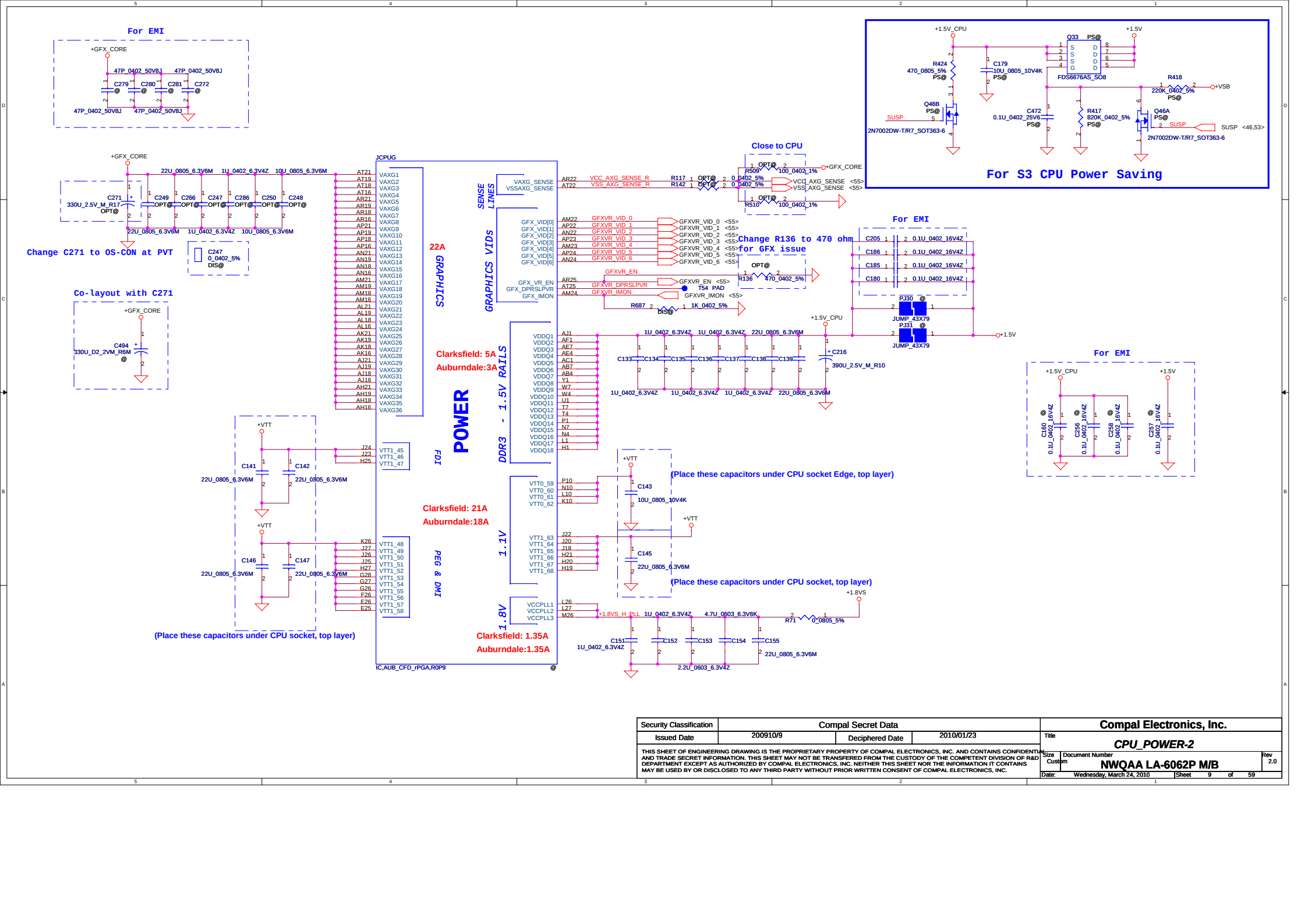
For EMI
+GFX_CORE
47P_0402_50V8J
C279 C280 C281 C272
For S3 CPU Power Saving
+1.5V_CPU
+1.5V
Q33 PS@
FDS6676AS_SO8
R424 470_0805_5% PS@
C179 10U_0805_10V4K PS@
R418 220K_0402_5% PS@
+VSB
Q46B PS@
Q46A PS@
2N7002DW-T/R7_SOT363-6
C472 0.1U_0402_25V6 PS@
R417 820K_0402_5% PS@
SUSP
SUSP <46,53>
Close to CPU
R509 100_0402_1%
R510 100_0402_1%
VCC_AXG_SENSE_R
VSS_AXG_SENSE_R
R117 R142 OPT@ 0_0402_5%
VCC_AXG_SENSE <55>
VSS_AXG_SENSE <55>
Change C271 to OS-CON at PVT
C271 330U_2.5V_M_R17 OPT@
C247 0_0402_5% DIS@
Co-layout with C271
C494 330U_D2_2VM_R6M @
Change R136 to 470 ohm for GFX issue
R136 470_0402_5%
GFXVR_EN
GFXVR_IMON
R687 1K_0402_5% DIS@
PJ30 PJ31 JUMP_43X79
C205 C186 C185 C180 0.1U_0402_16V4Z
C133 C134 C135 C136 C137 C138 C139 C216
390U_2.5V_M_R10
1U_0402_6.3V4Z
22U_0805_6.3V6M
C141 C142 C146 C147
C143 10U_0805_10V4K
C145 22U_0805_6.3V6M
C151 C152 C153 C154 C155
4.7U_0603_6.3V6K
2.2U_0603_6.3V4Z
R71 0_0805_5%
+1.8VS
+1.8VS_H_PLL
C160 C256 C258 C257 0.1U_0402_16V4Z
JCPUG
IC,AUB_CFD_rPGA,R0P9
SENSE LINES
VAXG_SENSE
VSSAXG_SENSE
GRAPHICS VIDs
GFX_VID[0]
GFX_VID[1]
GFX_VID[2]
GFX_VID[3]
GFX_VID[4]
GFX_VID[5]
GFX_VID[6]
GFX_VR_EN
GFX_DPRSLPVR
GFX_IMON
GRAPHICS
22A
POWER
DDR3 - 1.5V RAILS
Clarksfield: 5A
Auburndale:3A
FDI
Clarksfield: 21A
Auburndale:18A
1.1V
PEG & DMI
1.8V
Clarksfield: 1.35A
Auburndale:1.35A
(Place these capacitors under CPU socket Edge, top layer)
(Place these capacitors under CPU socket, top layer)
(Place these capacitors under CPU socket, top layer)
For EMI
For EMI
Security Classification
Compal Secret Data
Issued Date
200910/9
Deciphered Date
2010/01/23
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Size Custom
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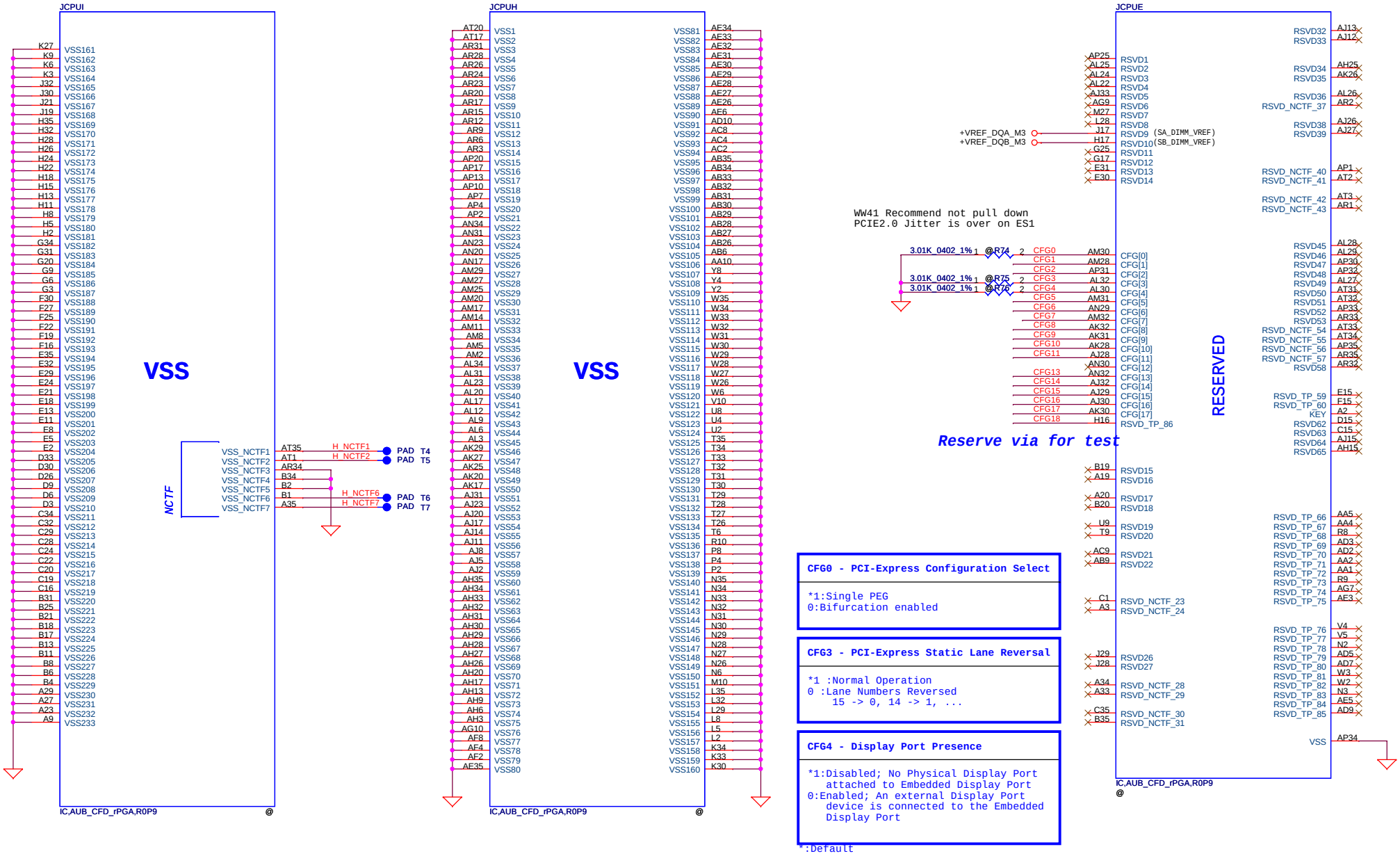

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Compal Electronics, Inc.	
Title	CPU_GND/RESERVED
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DDR3 SO-DIMM A
Reverse Type

JDDRL

FOX_AS0A626-U2SN-7F_204P
@

Close to JDDRL.1

For S3 CPU Power Saving

close to JDDRL.126

M1@: Arrandale

M3@: Clarksfield
For Clarksfield S3 CPU Power Saving

Change C218 to OSCON at DVT

Layout Note:
Place near JDDRL

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

Layout Note:
Place near JDDRL1.203 and 204

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

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Title: ***DDRIII-SODIMM0***

Size	Document Number	Rev
Custom	NWQAA LA-6062P M/B	2.0

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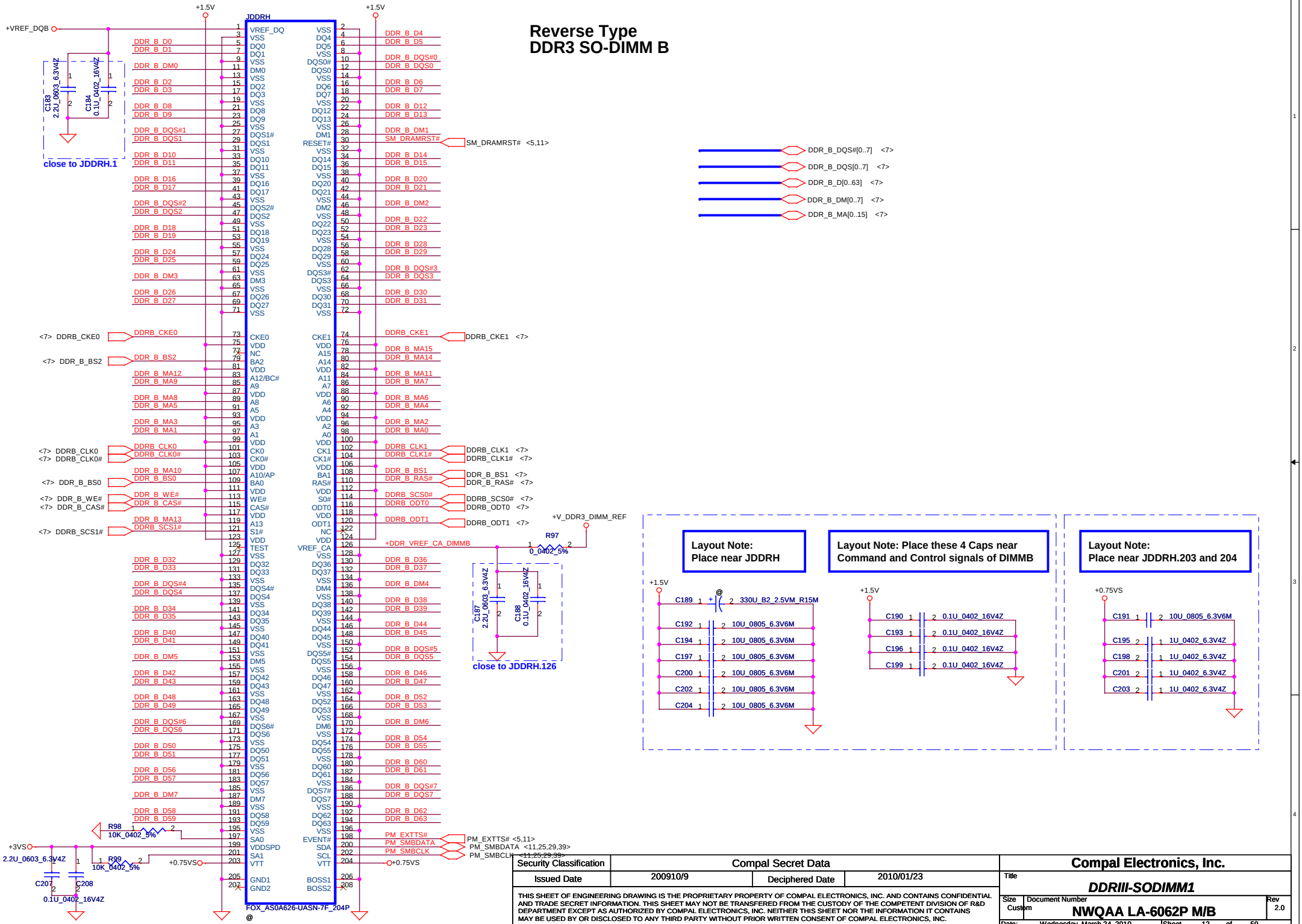
Reverse Type
DDR3 SO-DIMM B



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Title: ***DDRIII-SODIMM1***

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Custom	NWQAA LA-6062P M/B	2.0

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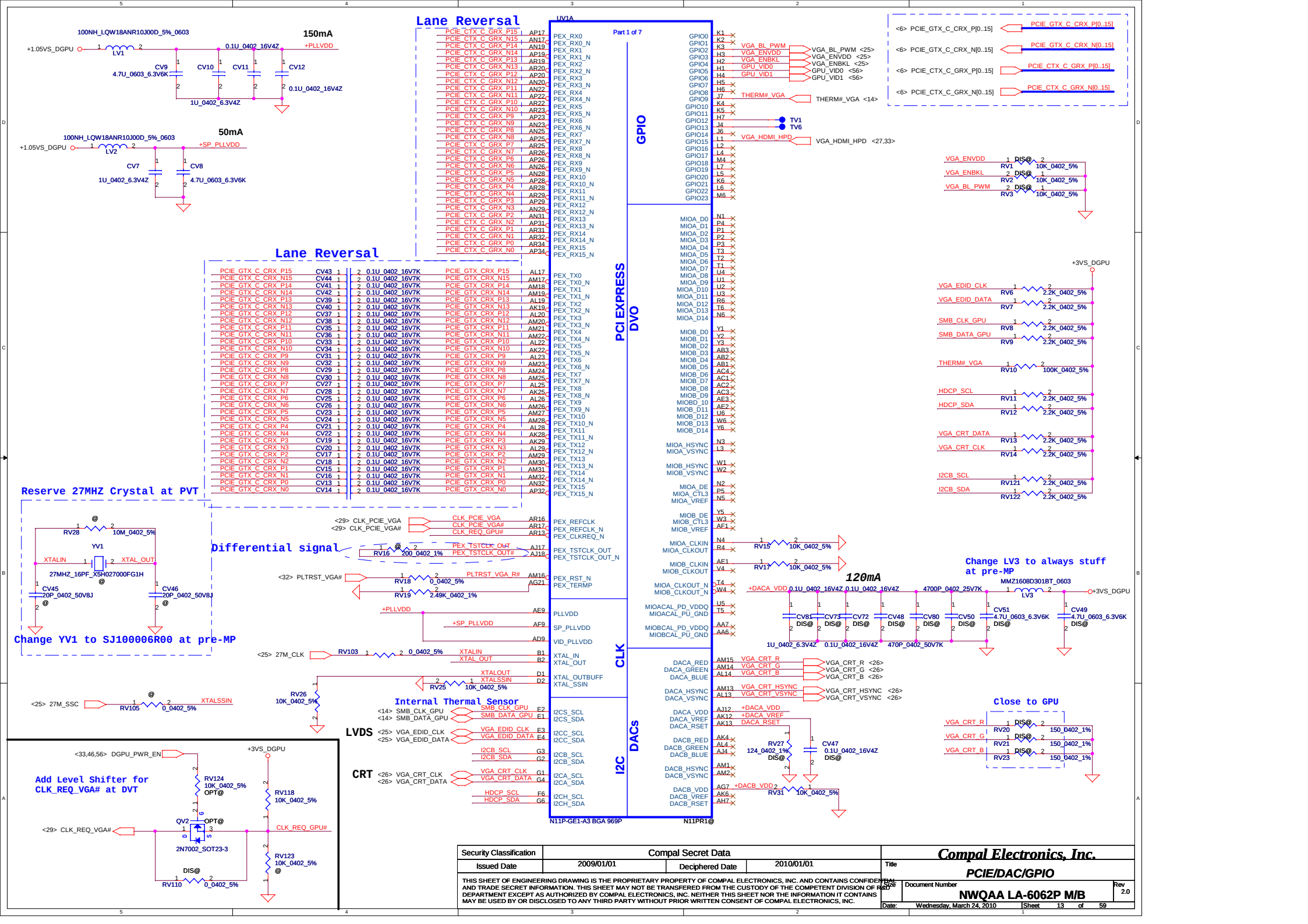

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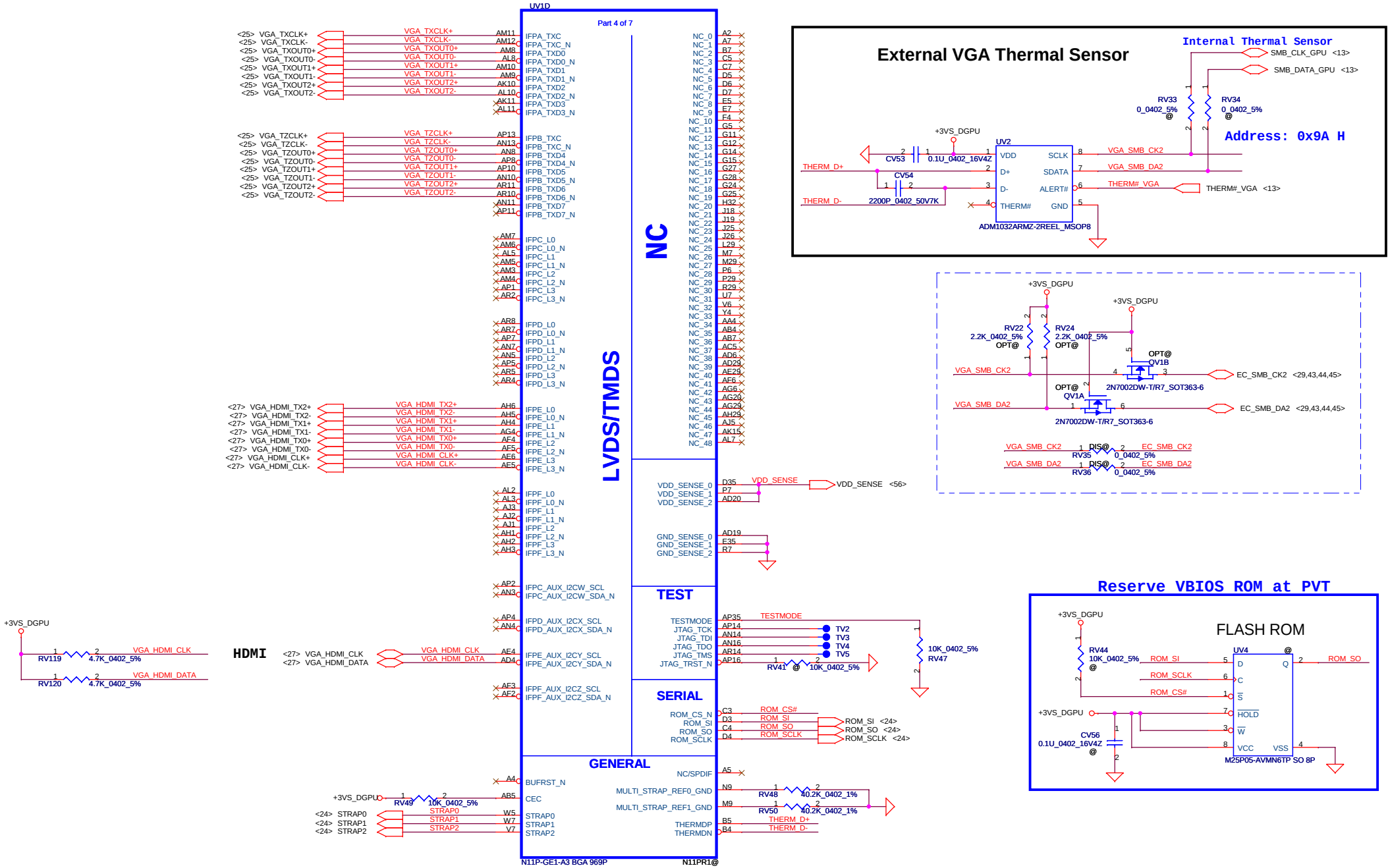

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: LVDS/HDMI/DP/THM

Size | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

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N11E-GE1-LP Performance Mode

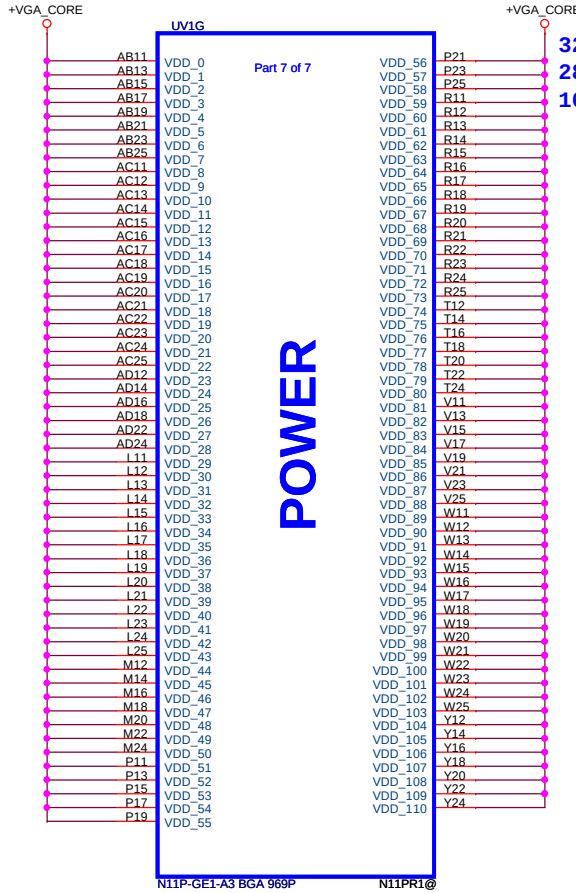
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	450	790	0.90 V
P8	405	324	0.85 V
P12	135	135	0.80 V

N11P-GE1 Performance Mode

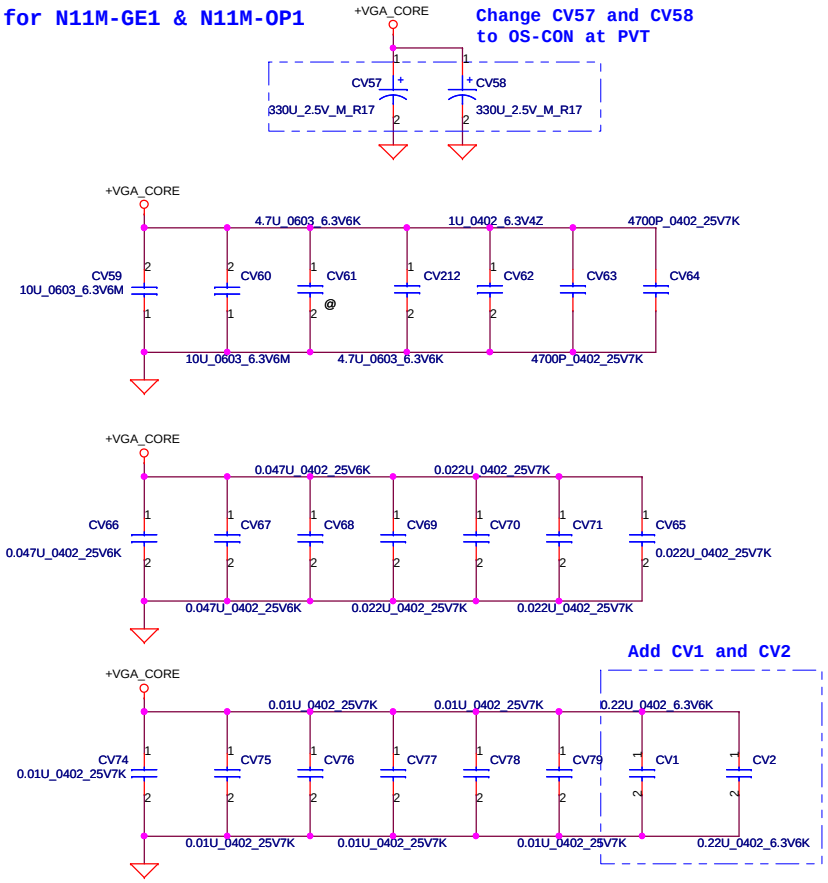
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	575	790	0.95 V
P8	405	324	0.85 V
P12	135	135	0.80 V

N11M-GE1 & N11M-OP1 Performance Mode

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	625	790	1.03 V
P8	405	405	0.85 V
P12	135	135	0.80 V



32A for N11E-GE1-LP
28A for N11P-GE1
16A for N11M-GE1 & N11M-OP1



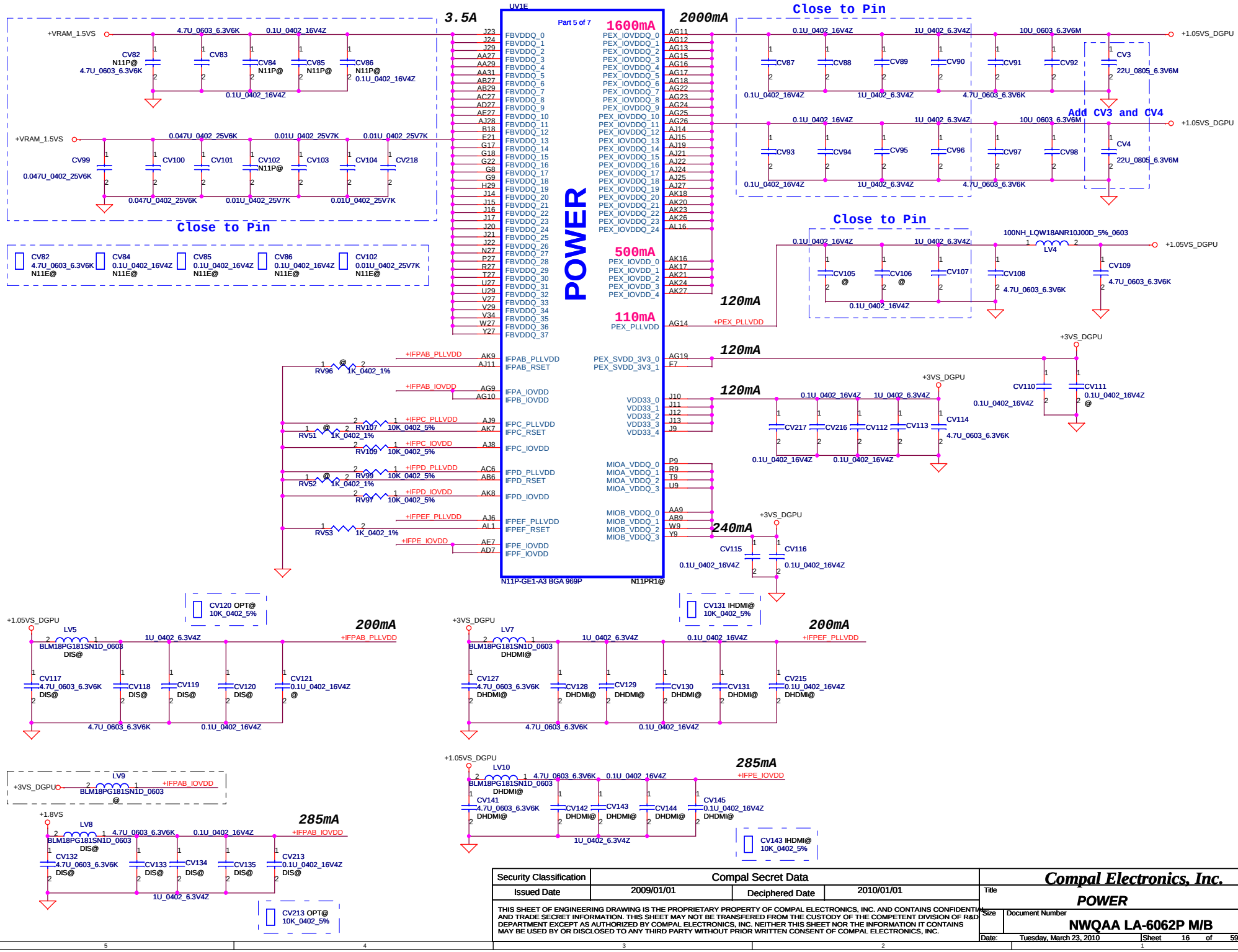
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: VGA CORE

Size | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

Date: Tuesday, March 23, 2010 | Sheet 15 of 59



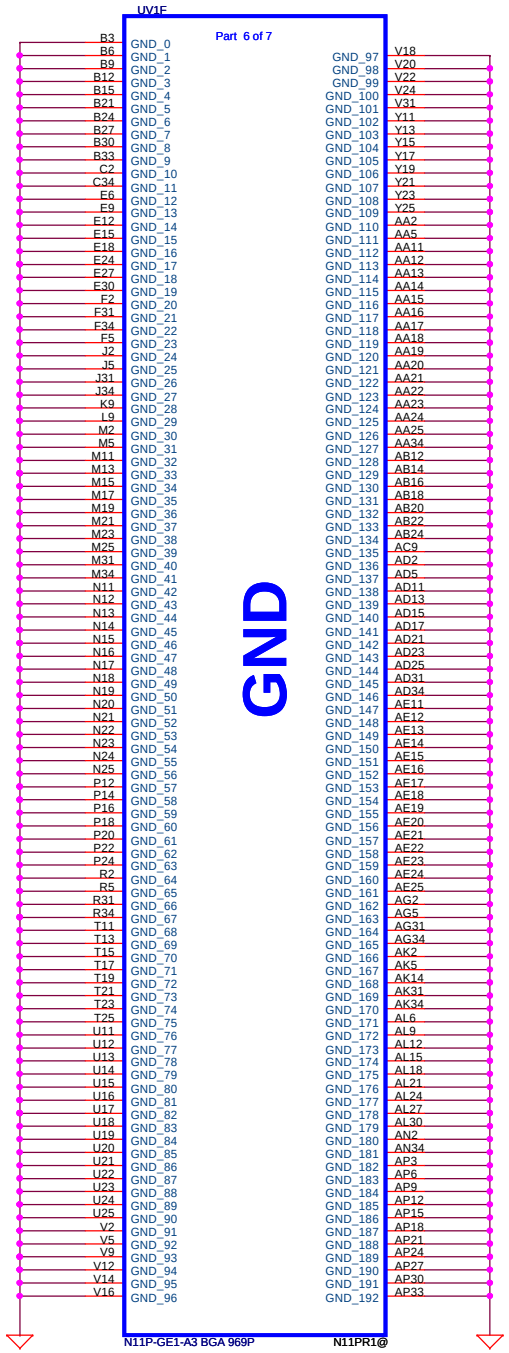
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: **POWER**

Size	Document Number	Rev
	NWQAA LA-6062P M/B	2.0

Date: Tuesday, March 23, 2010 | Sheet 16 of 59



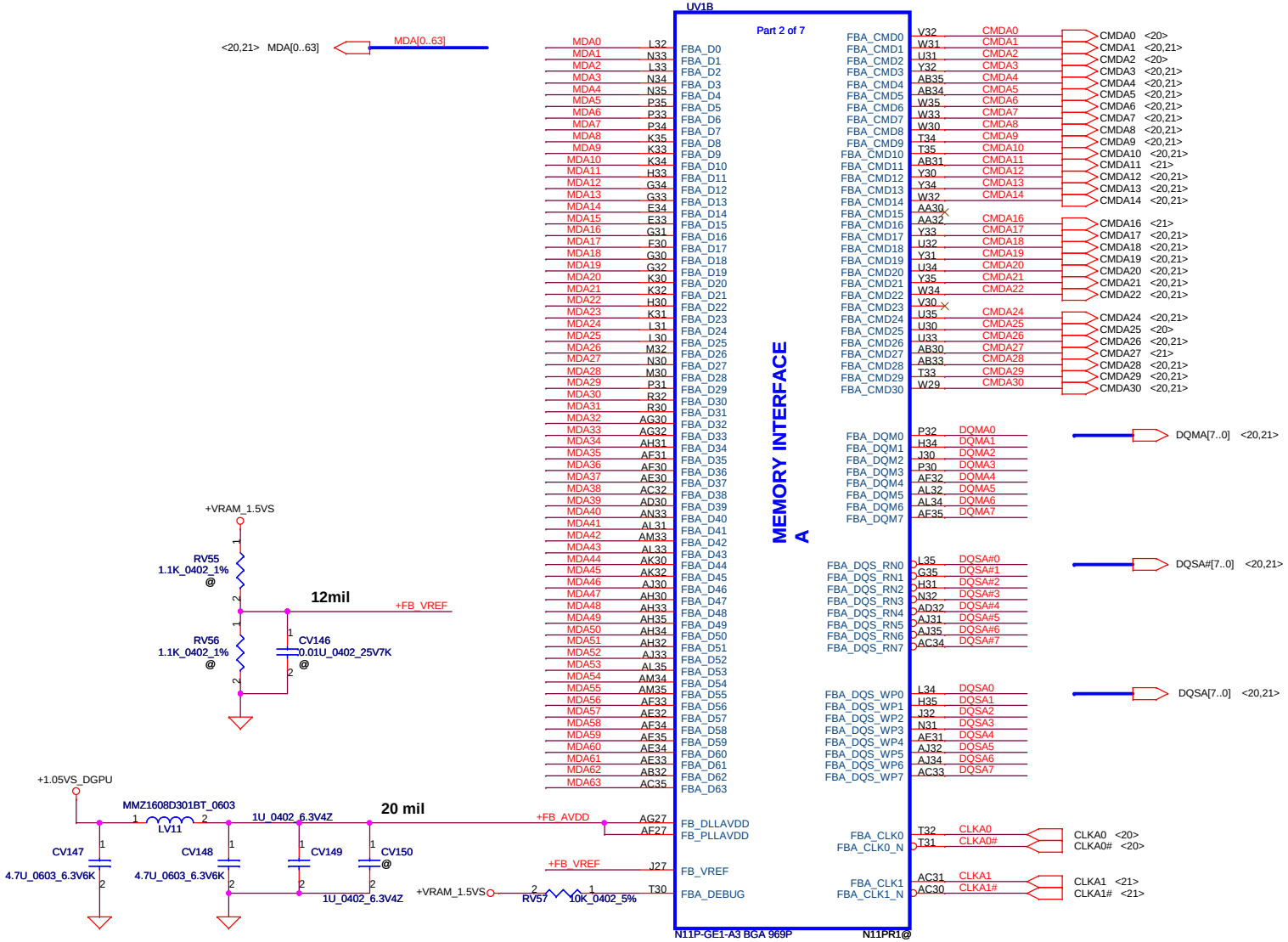
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: **GND**

Size | Document Number: **NWQAA LA-6062P M/B** | Rev: 2.0

Date: Tuesday, March 23, 2010 | Sheet 17 of 59



Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

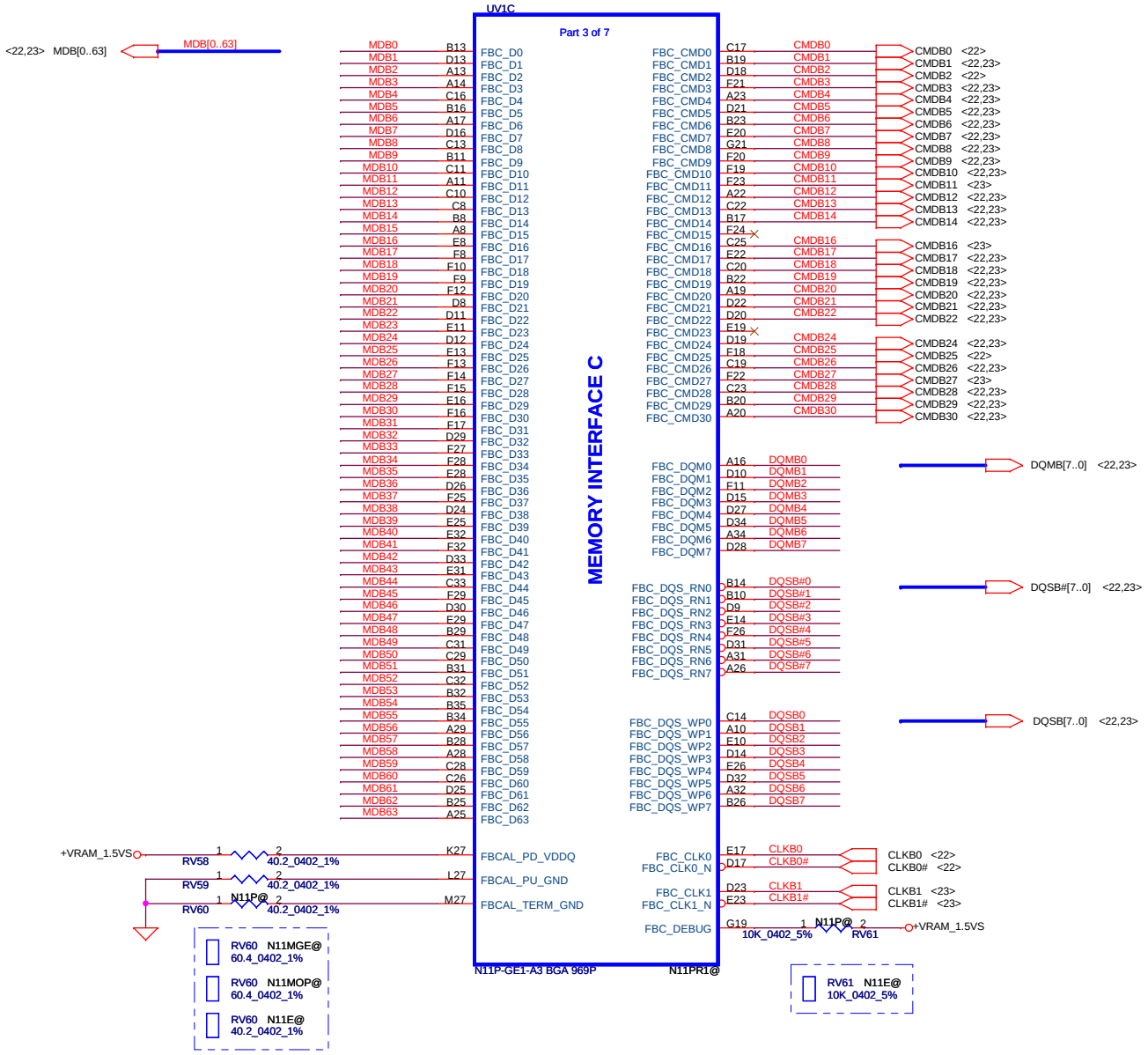
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: MEM Interface A

Size: | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

Date: Wednesday, March 24, 2010 | Sheet 18 of 59



Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: MEM Interface C

Size: C | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

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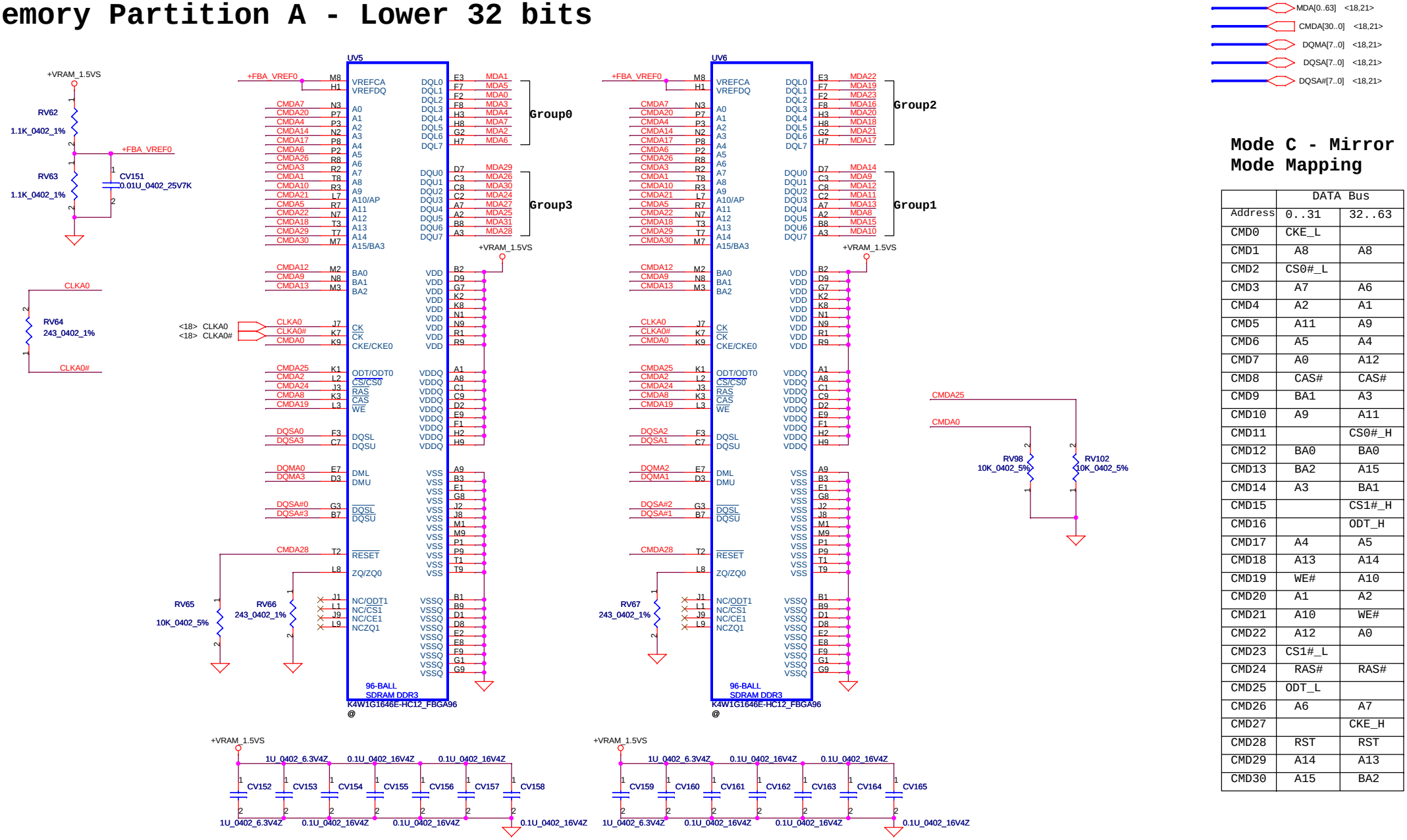
Memory Partition A - Lower 32 bits



Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

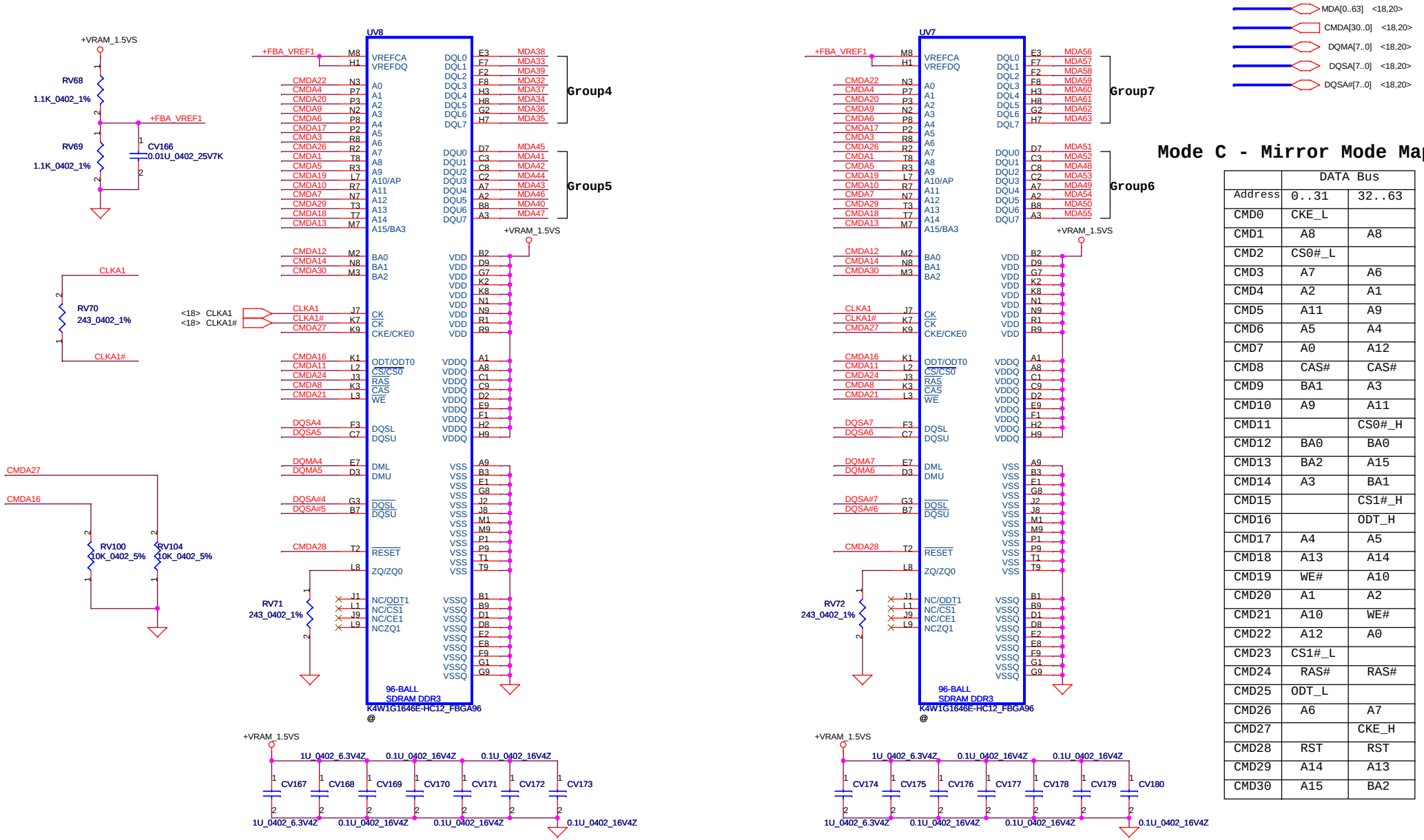
Compal Electronics, Inc.

Title: VRAM A Lower

Size: | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

Date: Wednesday, March 24, 2010 | Sheet 20 of 59

Memory Partition A - Upper 32 bits



Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: VRAM A Upper

Size: | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

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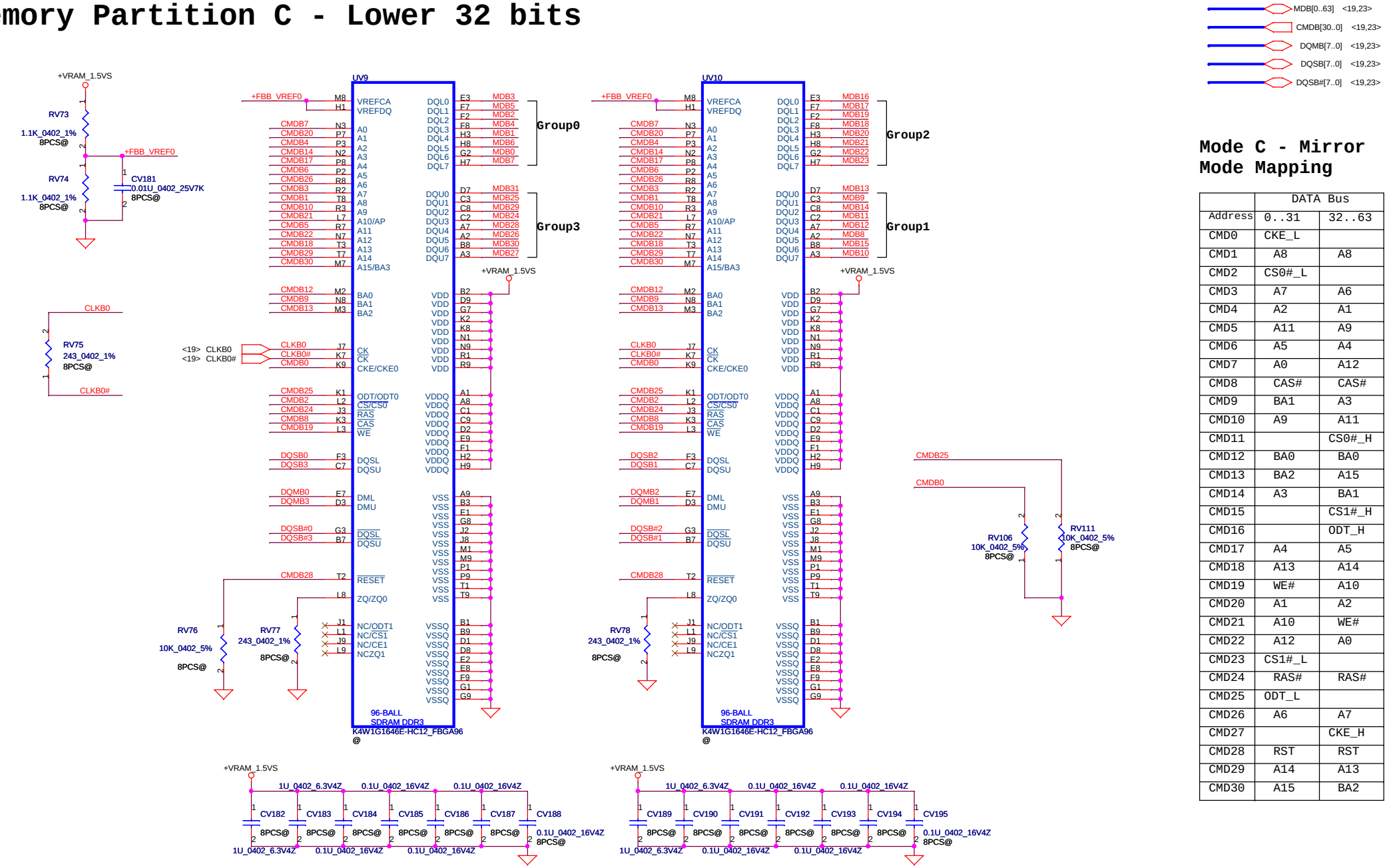
Memory Partition C - Lower 32 bits



Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

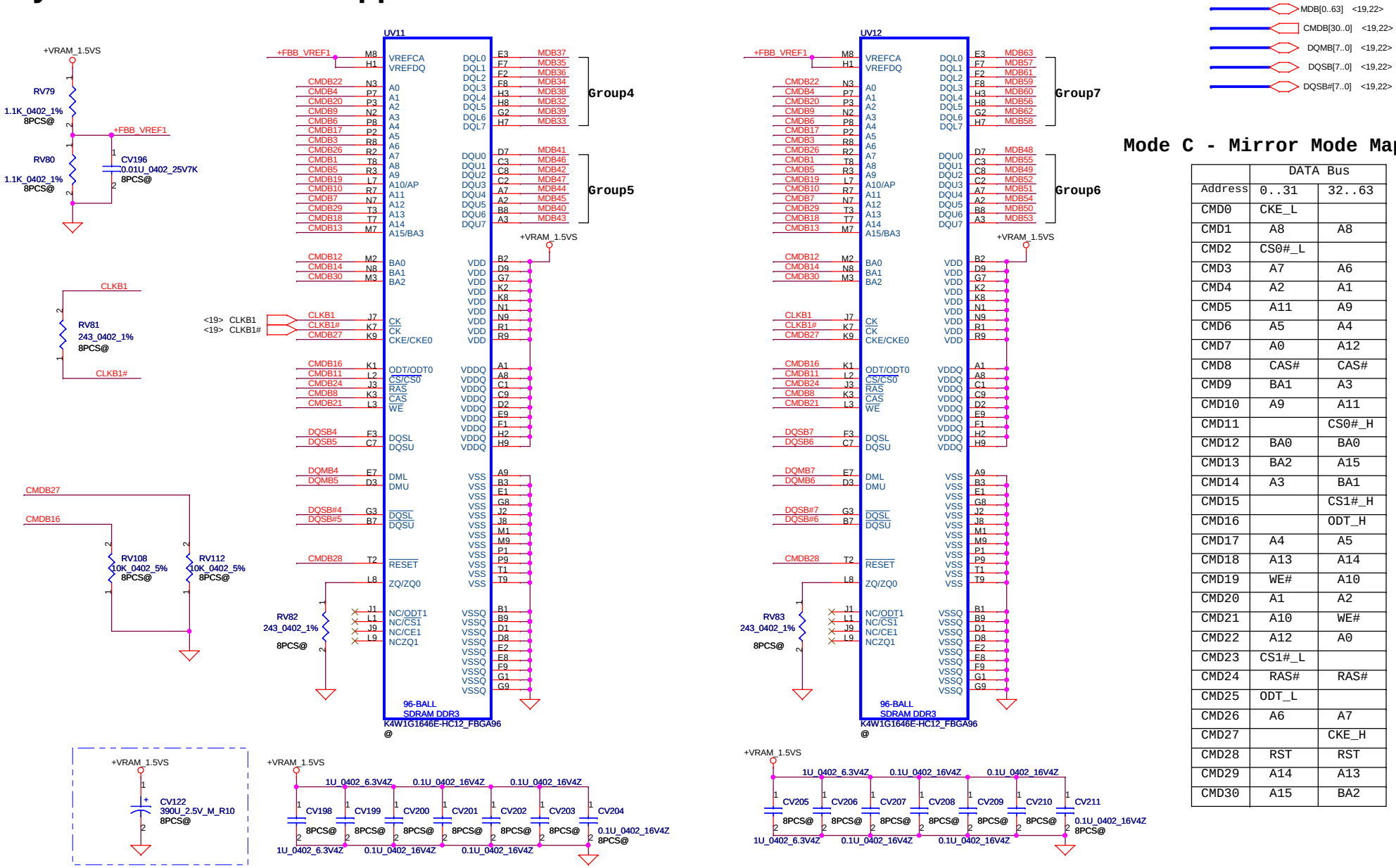
Compal Electronics, Inc.

Title: VRAM C Lower

Size: Custom | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

Date: Wednesday, March 24, 2010 | Sheet 22 of 59

Memory Partition C - Upper 32 bits



Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: VRAM C Upper

Size: Custom | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

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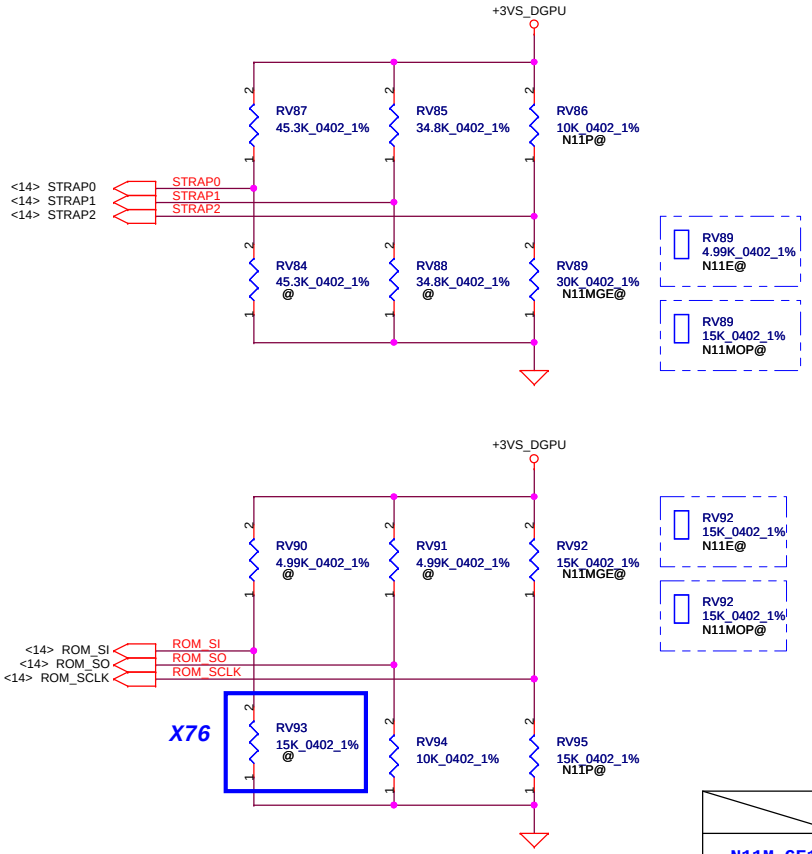


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	DeviceID	ROM_SCLK	STRAP2
N11M-GE1	0xA75	Pull up 15K	Pull down 30K
N11P-GE1	0xA29	Pull down 15K	Pull up 10K
N11M-OP1	0xA72	Pull up 15K	Pull down 15K
N11E-GE1(LP)	0xCB0	Pull up 15K	Pull down 5K

Hynix H5TQ1G63BFR-12C SA000032400	512M	0010	PD 15K	SD034150280
	1G	0010	PD 15K	
Samsung K4W1G1646E-HC12 SA000035700	512M	0011	PD 20K	SD034200280
	1G	0011	PD 20K	

SUB_VENDOR

0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417

0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE

0	256MB (Default)
1	Reserved

USER Straps

User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG

3GIO_PADCFG[3:0]	
1110	Notebook Default

PEX_PLL_EN_TERM

0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG

0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE

0	3D Device
1	VGA Device (Default)

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

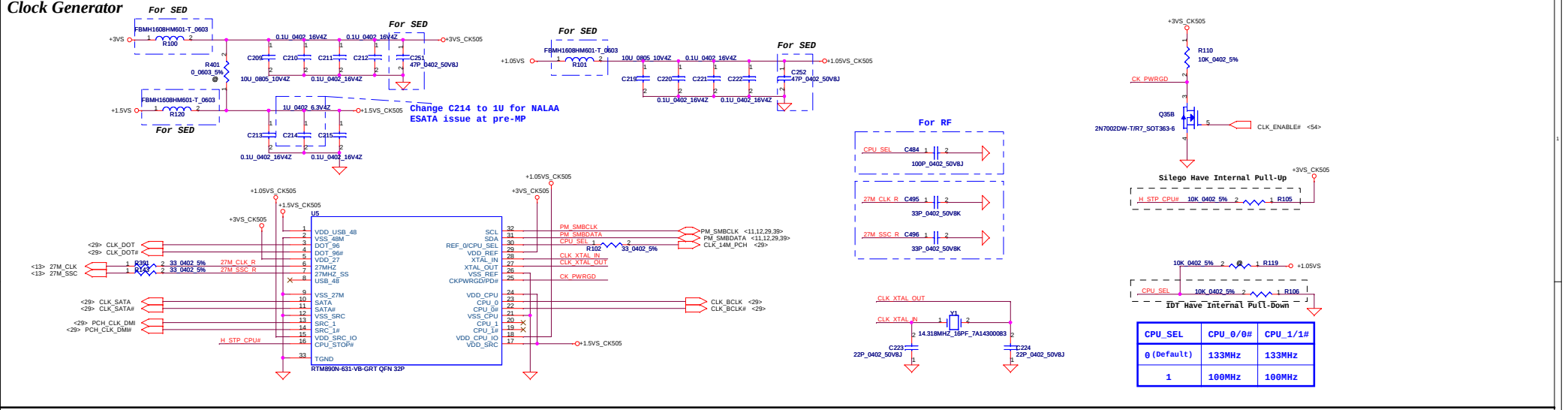
Compal Electronics, Inc.

Title: MSIC

Size: Custom | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

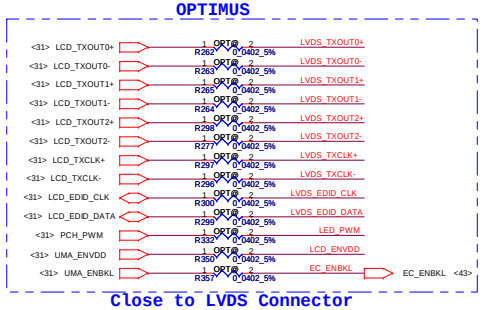
Date: Wednesday, March 24, 2010 | Sheet 24 of 59

Clock Generator



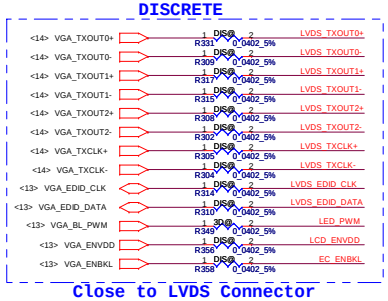
CPU_SEL	CPU_0/0#	CPU_1/1#
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

OPTIMUS



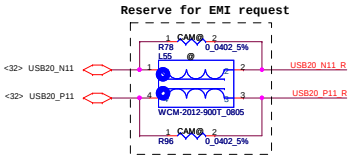
Close to LVDS Connector

DISCRETE

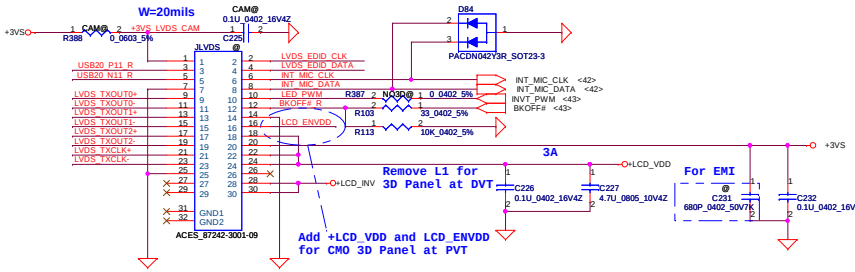


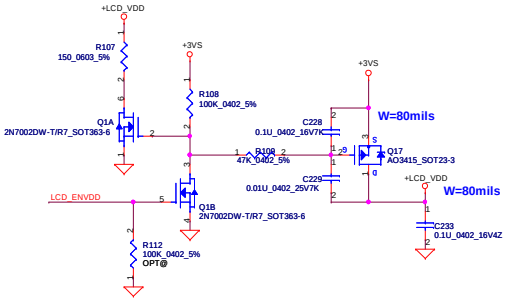
Close to LVDS Connector

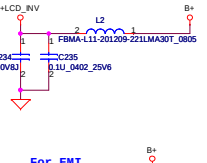
Reserve for EMI request



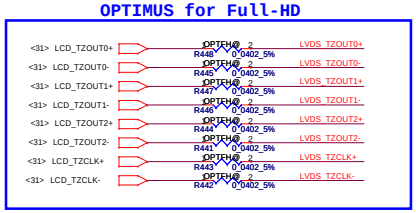
LCD/PANEL BD. Conn.



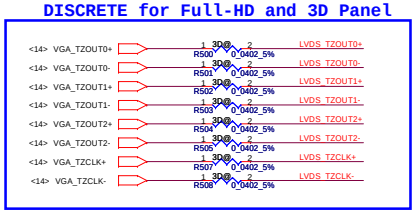




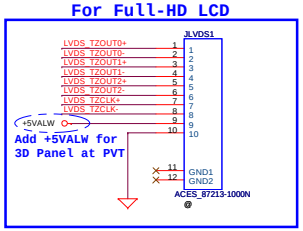
OPTIMUS for Full-HD



DISCRETE for Full-HD and 3D Panel



For Full-HD LCD



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	CCLK GEN/LVDS		
Size: Custom	Document Number: NWQAA LA-6062P M/B		Rev: 2.0
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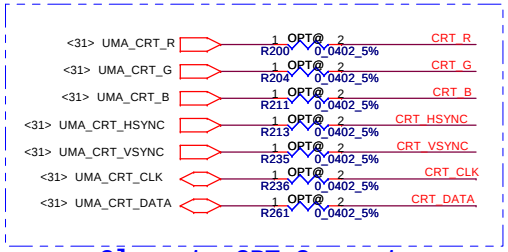
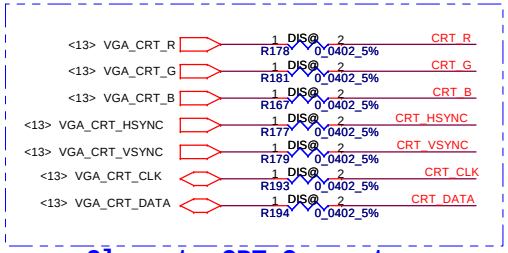
CRT CONNECTOR

OPTIMUS

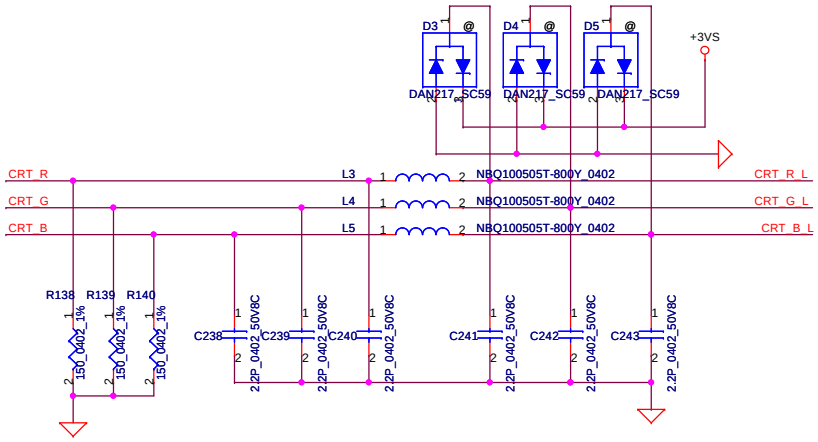


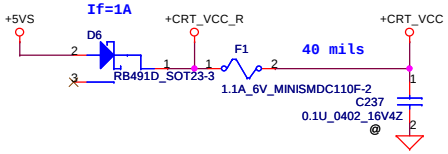
Close to CRT Connector

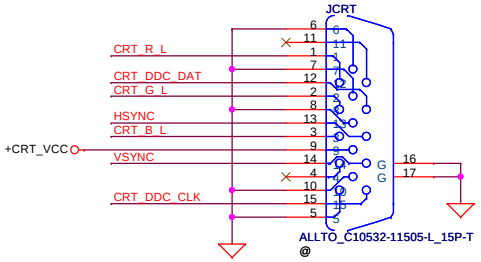
DISCRETE

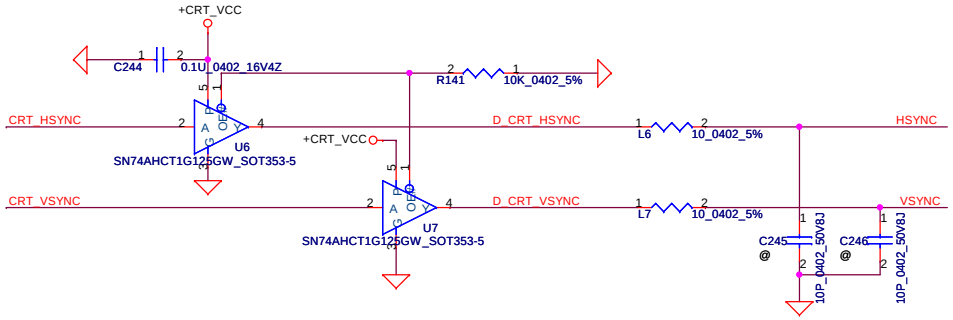


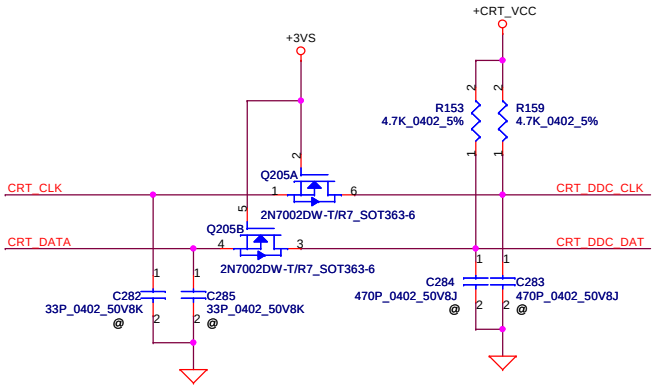
Close to CRT Connector











Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: *CRT*

Size	Document Number	Rev
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HDMI CEC Controller

Address: 0011010X

U16

R5F211A4C33SP-W4_LSSOP20

CEC_FSHUPD (Pin13)
Low= Force to update flash.

Change Q18 and Q19 power to +3VS_DGPU at pre-MP

Add R145 for U9 ESD issue at DVT

For DISCRETE

U18

ASM1442 QFN_48P_7X7

Add R208 for AOC monitor issue at PVT

Add D54 for HDMI CEC issue at pre-MP

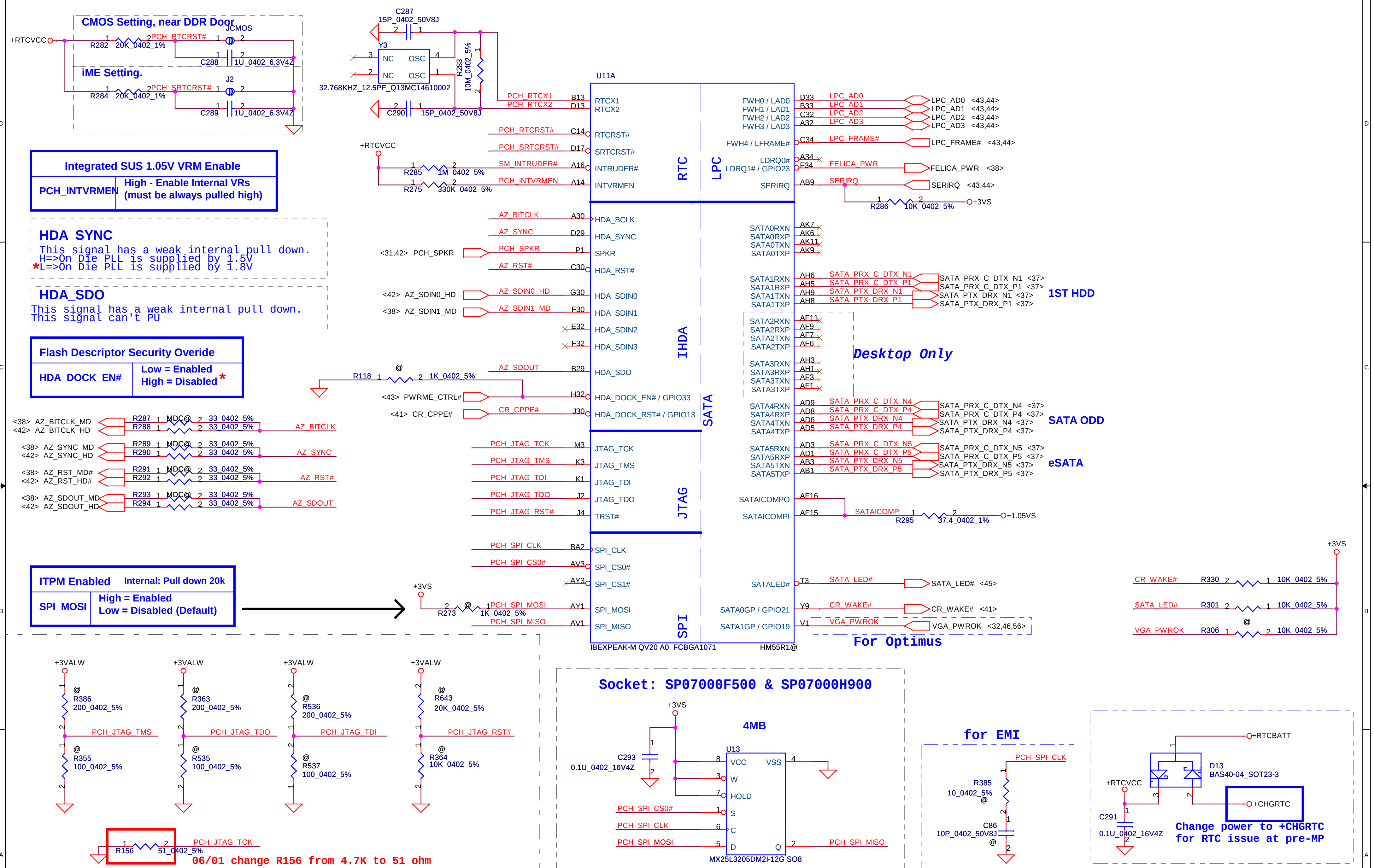
HDMI Connector

JHDMI

TYCO_1939864-1_19P

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title: HDMI Conn./CEC			
Size	Document Number: NWQAA LA-6062P M/B		Rev: 2.0
Date: Wednesday, March 24, 2010	Sheet 27 of 59		



CMOS Setting, near DDR Door
iME Setting.
+RTCVCC
R282 20K_0402_1%
PCH_RTCRST#
JCMOS
C288 1U_0402_6.3V4Z
R284 20K_0402_1%
PCH_SRTCRST#
J2
C289 1U_0402_6.3V4Z
C287 15P_0402_50V8J
Y3
NC OSC
32.768KHZ_12.5PF_Q13MC14610002
C290 15P_0402_50V8J
R283 10M_0402_5%
Integrated SUS 1.05V VRM Enable
PCH_INTVRMEN
High - Enable Internal VRs (must be always pulled high)
HDA_SYNC
This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
*L=>On Die PLL is supplied by 1.8V
HDA_SDO
This signal has a weak internal pull down.
This signal can't PU
Flash Descriptor Security Overide
HDA_DOCK_EN#
Low = Enabled
High = Disabled *
ITPM Enabled Internal: Pull down 20k
SPI_MOSI
High = Enabled
Low = Disabled (Default)
U11A
RTC
LPC
IHDA
SATA
JTAG
SPI
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN# / GPIO33
HDA_DOCK_RST# / GPIO13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
TRST#
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
FWH4 / LFRAME#
LDRQ0#
LDRQ1# / GPIO23
SERIRQ
SATAICOMPO
SATAICOMPI
SATALED#
SATA0GP / GPIO21
SATA1GP / GPIO19
IBEXPEAK-M QV20 A0_FCBGA1071
HM55R1@
LPC_AD0 <43,44>
LPC_AD1 <43,44>
LPC_AD2 <43,44>
LPC_AD3 <43,44>
LPC_FRAME# <43,44>
FELICA_PWR <38>
SERIRQ <43,44>
R286 10K_0402_5%
+3VS
SATA_PRX_C_DTX_N1 <37>
SATA_PRX_C_DTX_P1 <37>
SATA_PTX_DRX_N1 <37>
SATA_PTX_DRX_P1 <37>
1ST HDD
Desktop Only
SATA_PRX_C_DTX_N4 <37>
SATA_PRX_C_DTX_P4 <37>
SATA_PTX_DRX_N4 <37>
SATA_PTX_DRX_P4 <37>
SATA ODD
SATA_PRX_C_DTX_N5 <37>
SATA_PRX_C_DTX_P5 <37>
SATA_PTX_DRX_N5 <37>
SATA_PTX_DRX_P5 <37>
eSATA
R295 37.4_0402_1%
+1.05VS
SATA_LED# <45>
CR_WAKE# <41>
VGA_PWROK <32,46,56>
For Optimus
R330 10K_0402_5%
R301 10K_0402_5%
R306 10K_0402_5%
<31,42> PCH_SPKR
<42> AZ_SDIN0_HD
<38> AZ_SDIN1_MD
<43> PWRME_CTRL#
<41> CR_CPPE#
R118 1K_0402_5%
R285 1M_0402_5%
R275 330K_0402_5%
<38> AZ_BITCLK_MD
<42> AZ_BITCLK_HD
<38> AZ_SYNC_MD
<42> AZ_SYNC_HD
<38> AZ_RST_MD#
<42> AZ_RST_HD#
<38> AZ_SDOUT_MD
<42> AZ_SDOUT_HD
R287 R288 R289 R290 R291 R292 R293 R294 33_0402_5%
R273 1K_0402_5%
+3VALW
R386 200_0402_5%
R355 100_0402_5%
R363 200_0402_5%
R535 100_0402_5%
R536 200_0402_5%
R537 100_0402_5%
R643 20K_0402_5%
R364 10K_0402_5%
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_RST#
Socket: SP07000F500 & SP07000H900
4MB
U13
C293 0.1U_0402_16V4Z
VCC VSS W HOLD S C D Q
MX25L3205DM2I-12G SO8
PCH_SPI_CS0#
PCH_SPI_CLK
PCH_SPI_MOSI
PCH_SPI_MISO
for EMI
R385 10_0402_5%
C86 10P_0402_50V8J
+RTCBATT
D13 BAS40-04_SOT23-3
+RTCVCC
C291 0.1U_0402_16V4Z
+CHGRTC
Change power to +CHGRTC for RTC issue at pre-MP
R156 51_0402_5%
PCH_JTAG_TCK
06/01 change R156 from 4.7K to 51 ohm

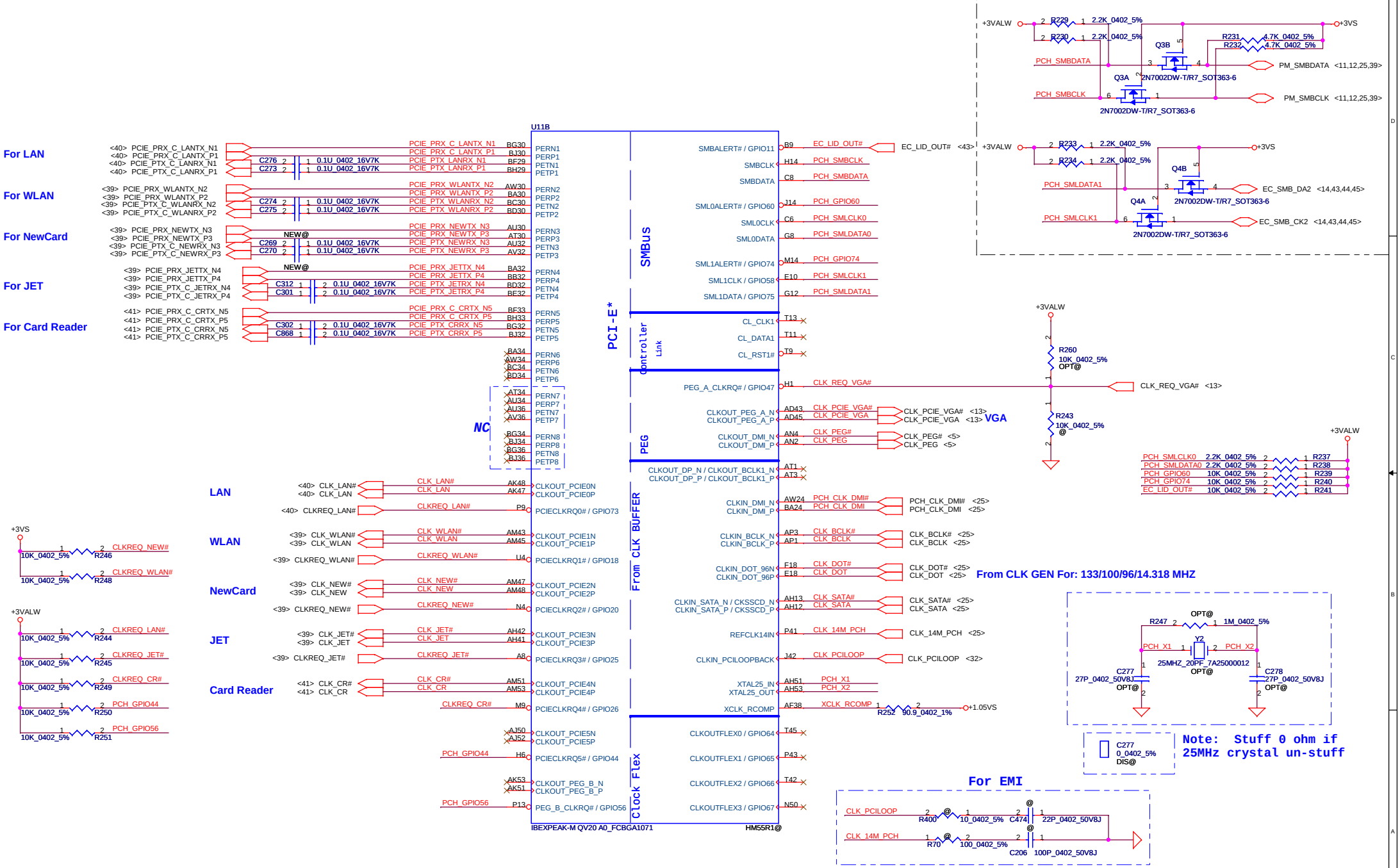
PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
	R535	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R355	200ohm	200ohm	No Install	No Install
	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20Kohm	No Install
	R537	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
	R353	10Kohm	10Kohm	No Install	No Install

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PCH_SPI/SATA/LPC/RTC/HDA**

Size: B | Document Number: **NWQAA LA-6062P M/B** | Rev: 2.0



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

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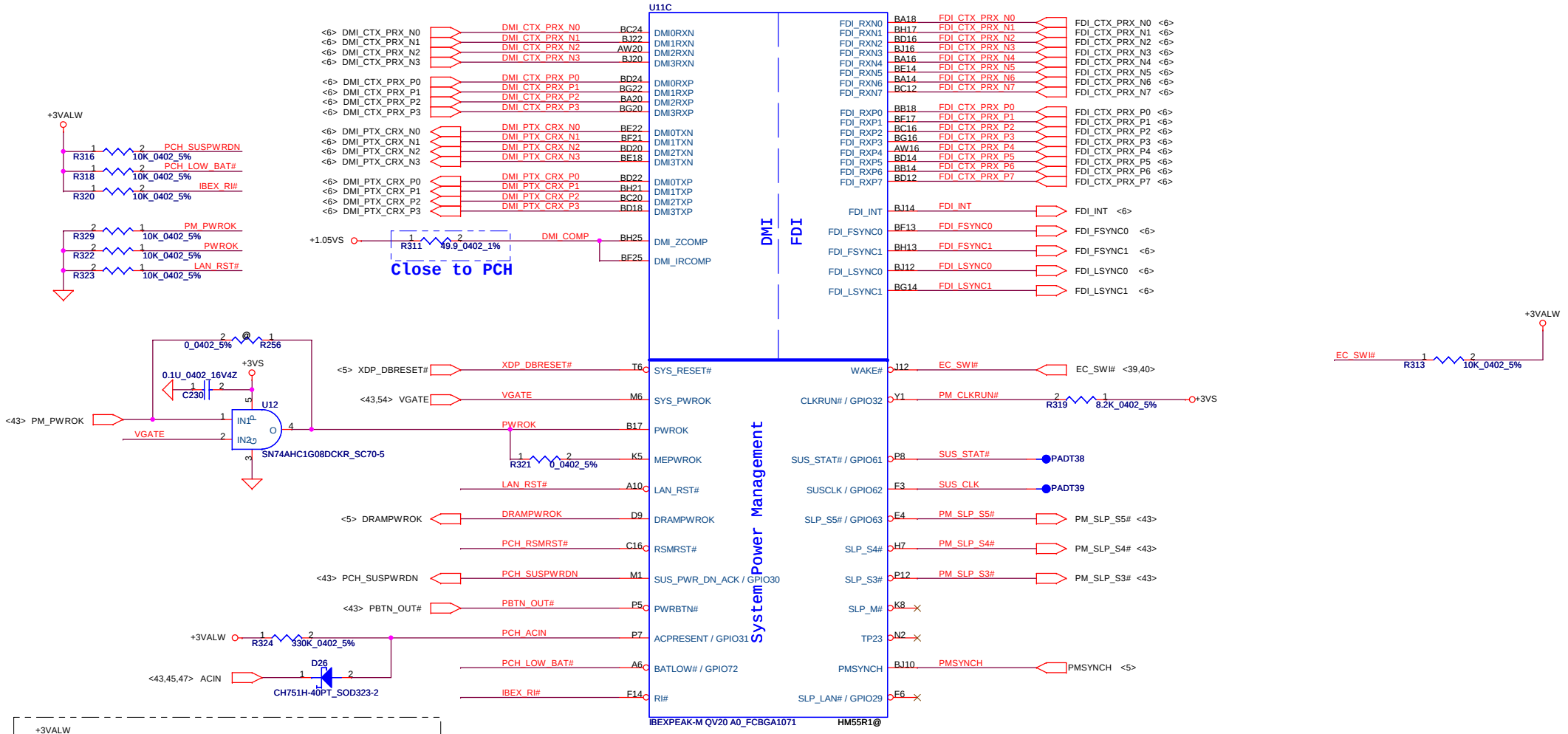
Compal Electronics, Inc.

Title: **PCH_CLK/PCIE/SMBUS**

Size	Document Number	Rev
Custom	NWQAA LA-6062P M/B	2.0

Date: Wednesday, March 24, 2010 | Sheet 29 of 59



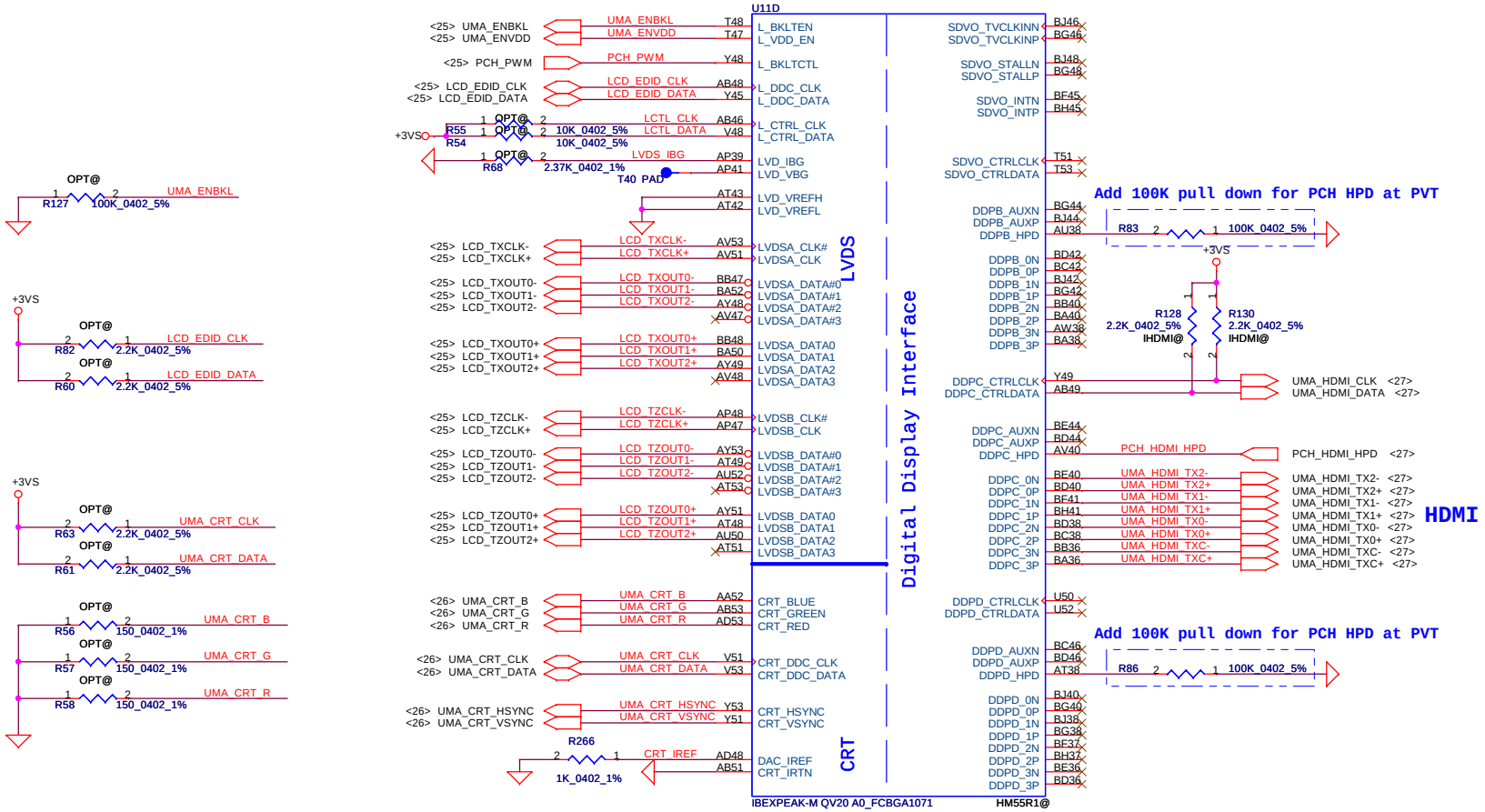
Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

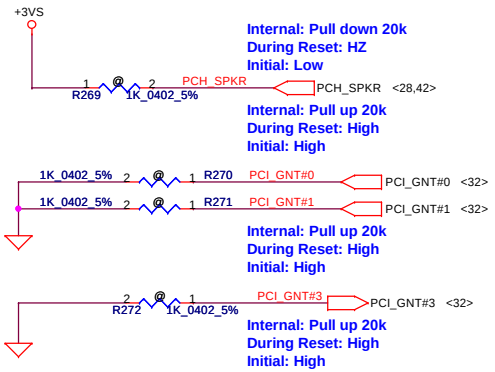
Title: ***PCH_DMI/FDI/PWM***

Size	Document Number	Rev
B	NWQAA LA-6062P M/B	2.0

Date: Wednesday, March 24, 2010 Sheet 30 of 59



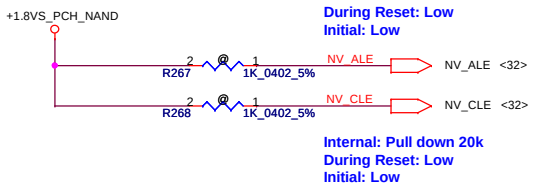
PCH Strap Pin



NO REBOOT Strap	
PCH_SPKR	Low= Disable High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Loaction
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable

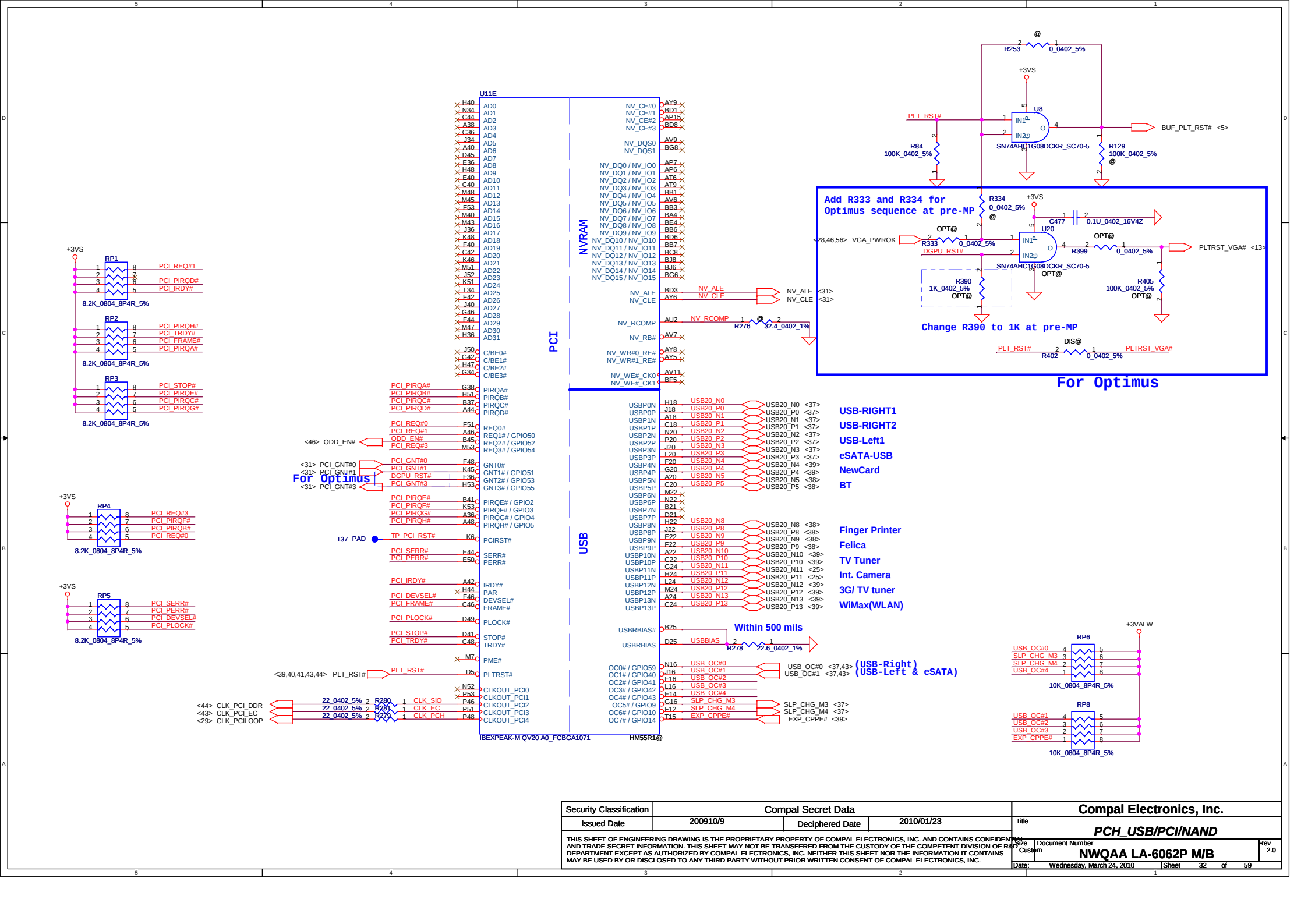


Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.	
Title	PCH_CRT/LVDS/HDMI/STRAP
Size: Custom	Document Number: NWQAA LA-6062P M/B
Rev	2.0
Date: Wednesday, March 24, 2010	Sheet 31 of 59



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

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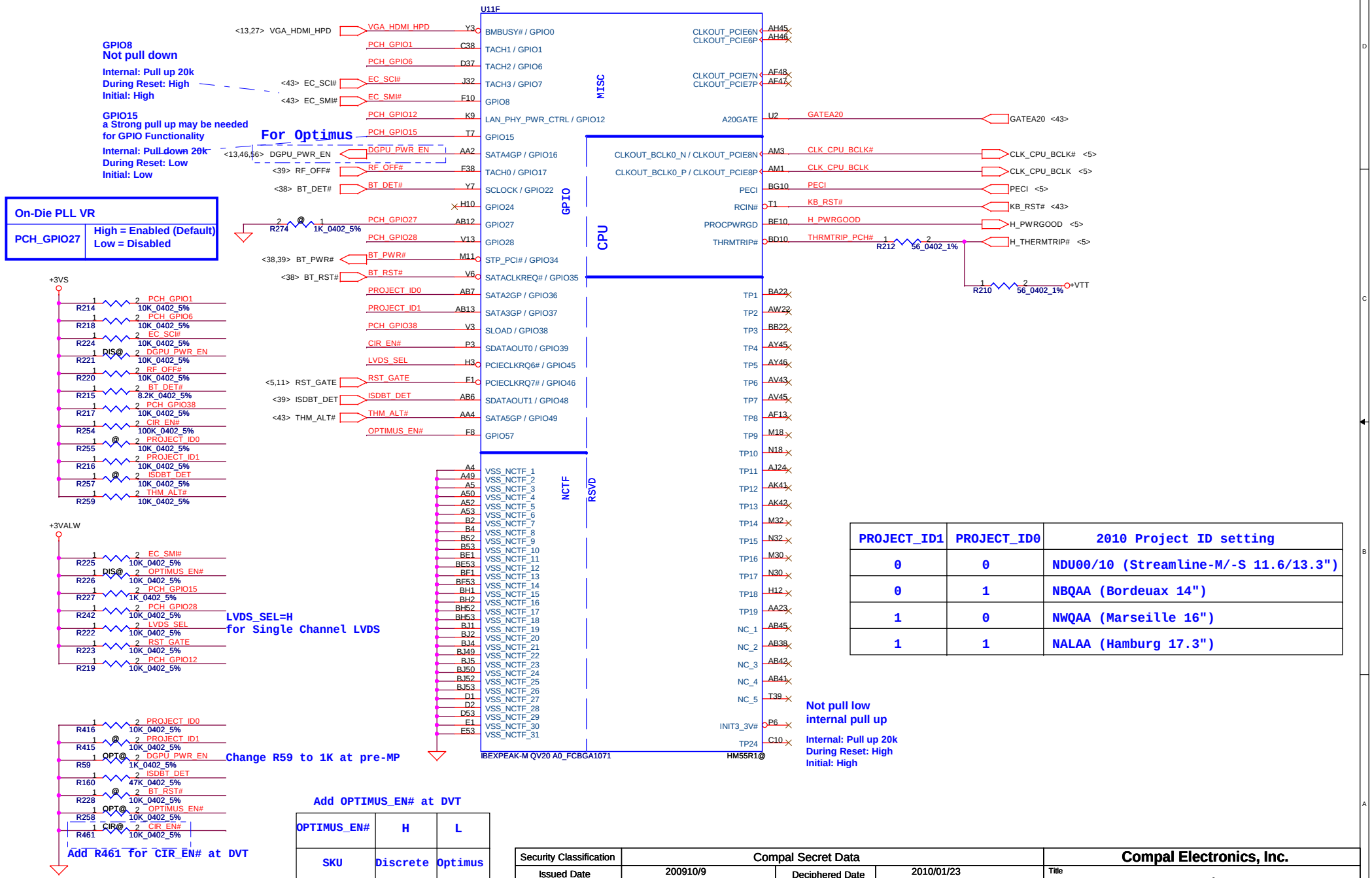
Compal Electronics, Inc.

Title: *PCH_USB/PCI/NAND*

Size: Custom | Document Number: **NWQAA LA-6062P M/B** | Rev: 2.0

Date: Wednesday, March 24, 2010 | Sheet 32 of 59



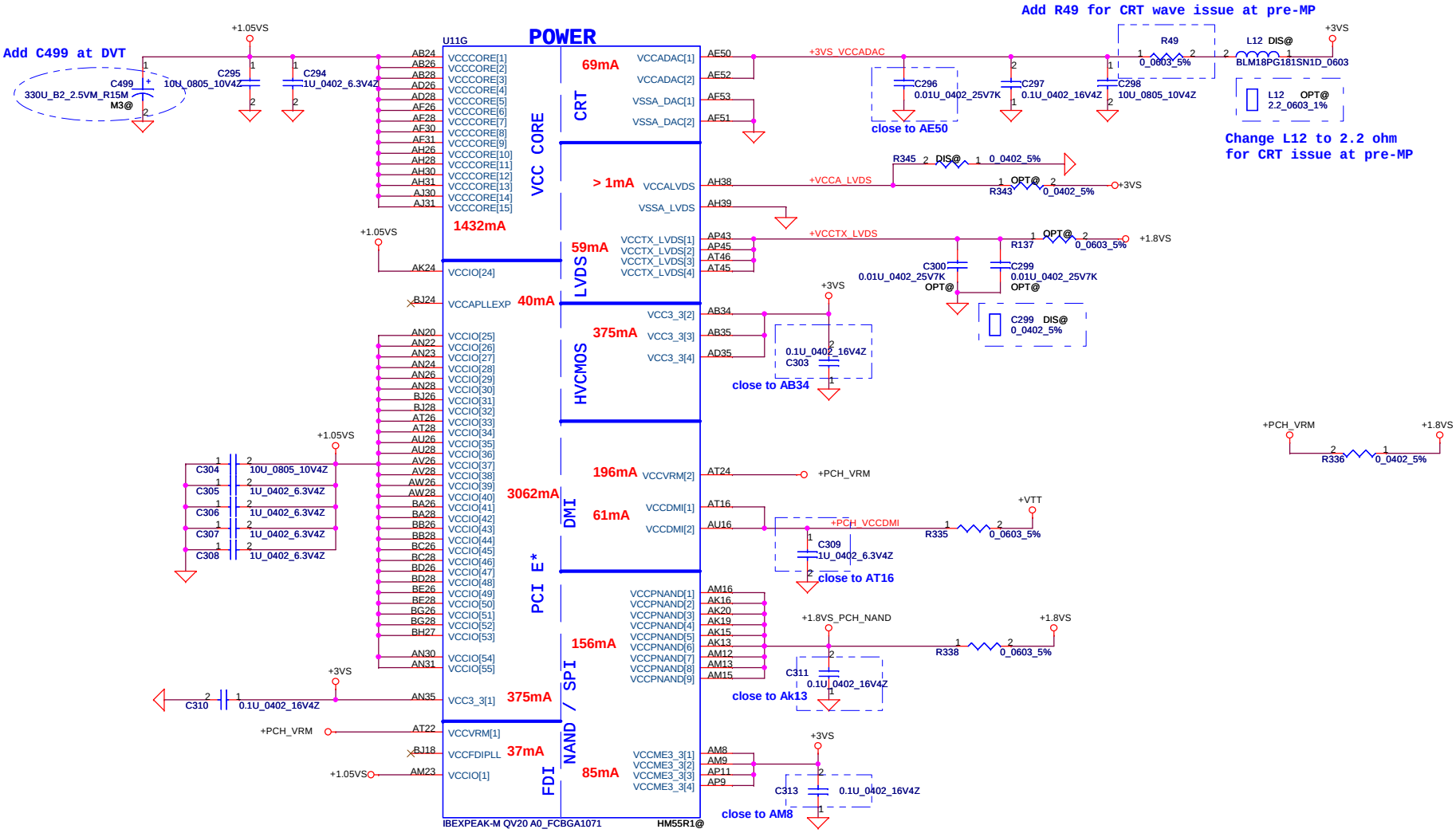
Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: *PCH_CPU/GPIO*

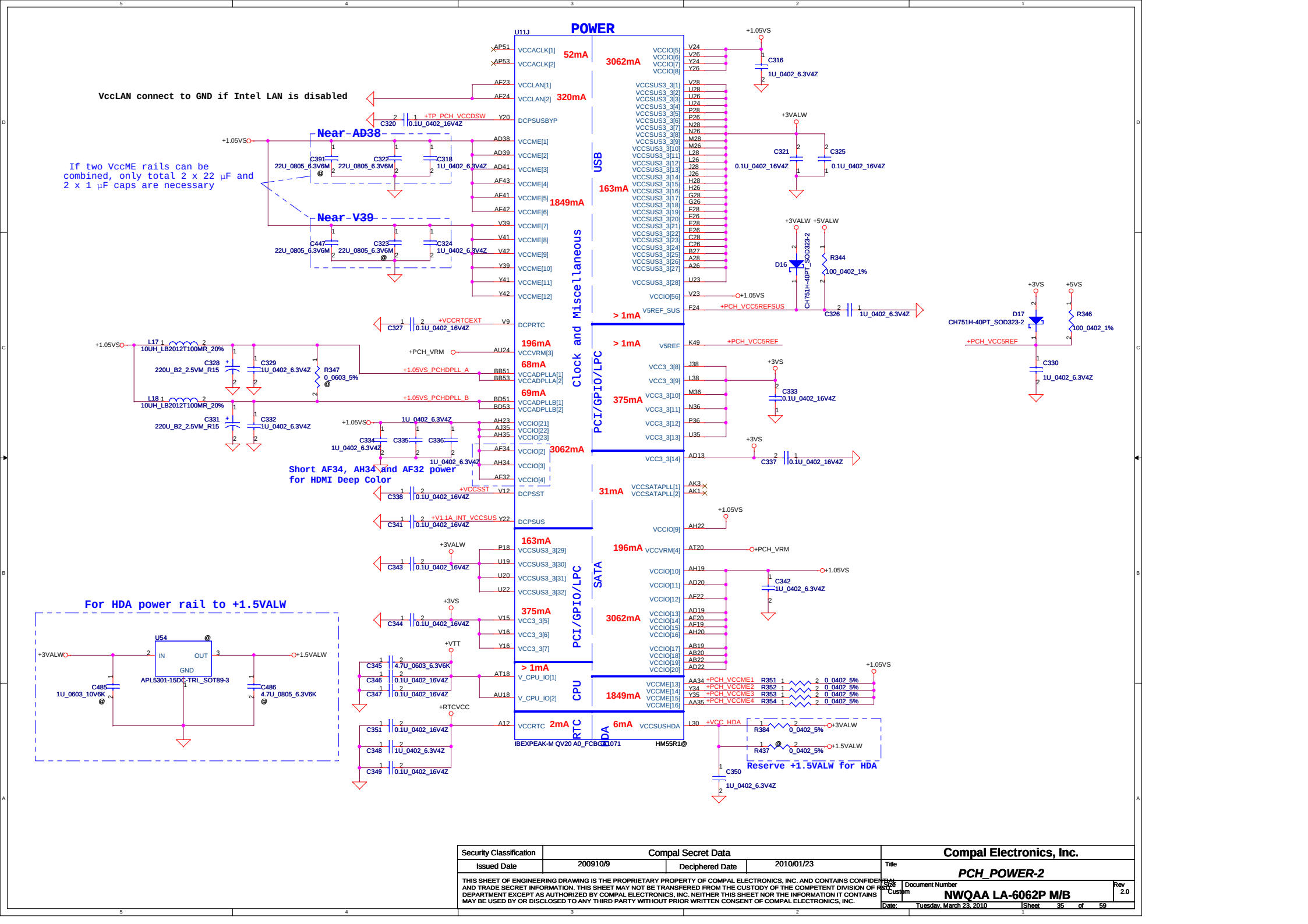
Size: B | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

Date: Wednesday, March 24, 2010 | Sheet 33 of 59



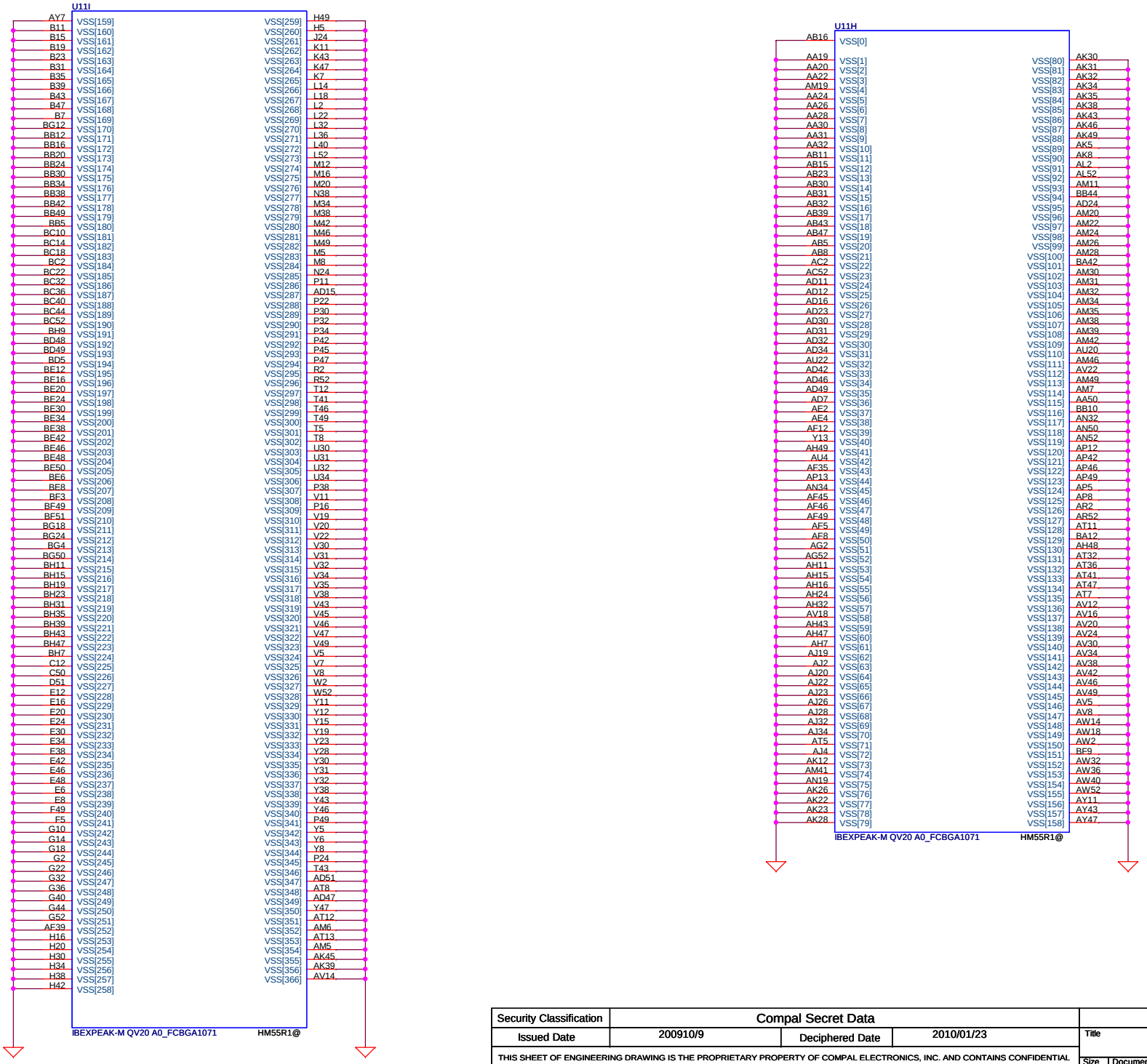
Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.	
Title	PCH_POWER-1
Size B	Document Number NWQAA LA-6062P M/B
Rev	2.0
Date: Tuesday, March 23, 2010	Sheet 34 of 59



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title: PCH_POWER-2			
Size: Custom	Document Number: NWQAA LA-6062P M/B		Rev: 2.0
Date: Tuesday, March 23, 2010	Sheet 35 of 59		



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

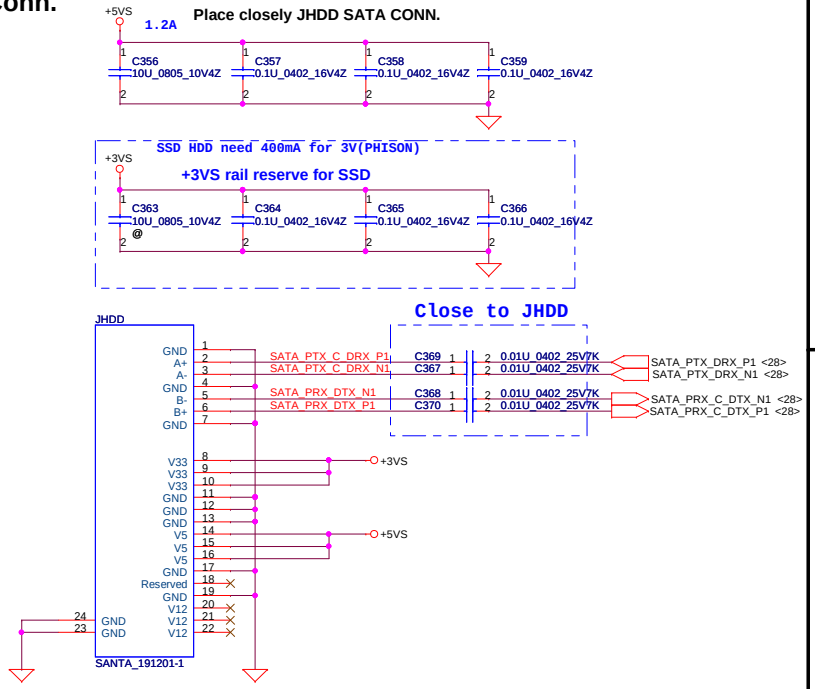
Compal Electronics, Inc.

Title: ***PCH_GND***

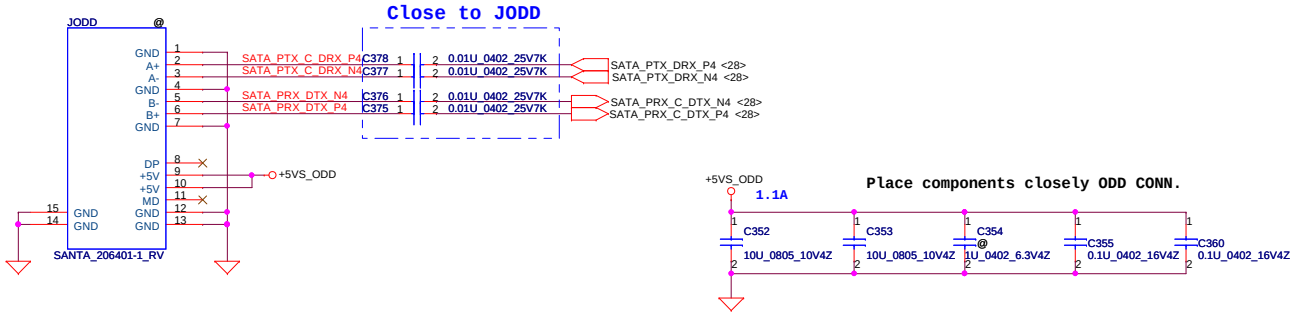
Size	Document Number	Rev
Custom	NWQAA LA-6062P M/B	2.0

Date: Tuesday, March 23, 2010 Sheet 36 of 59

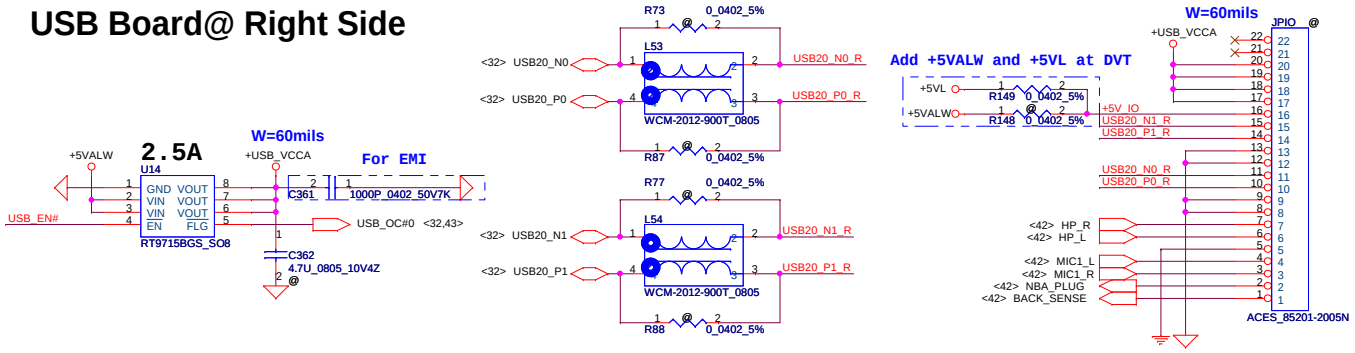
SATA HDD Conn.



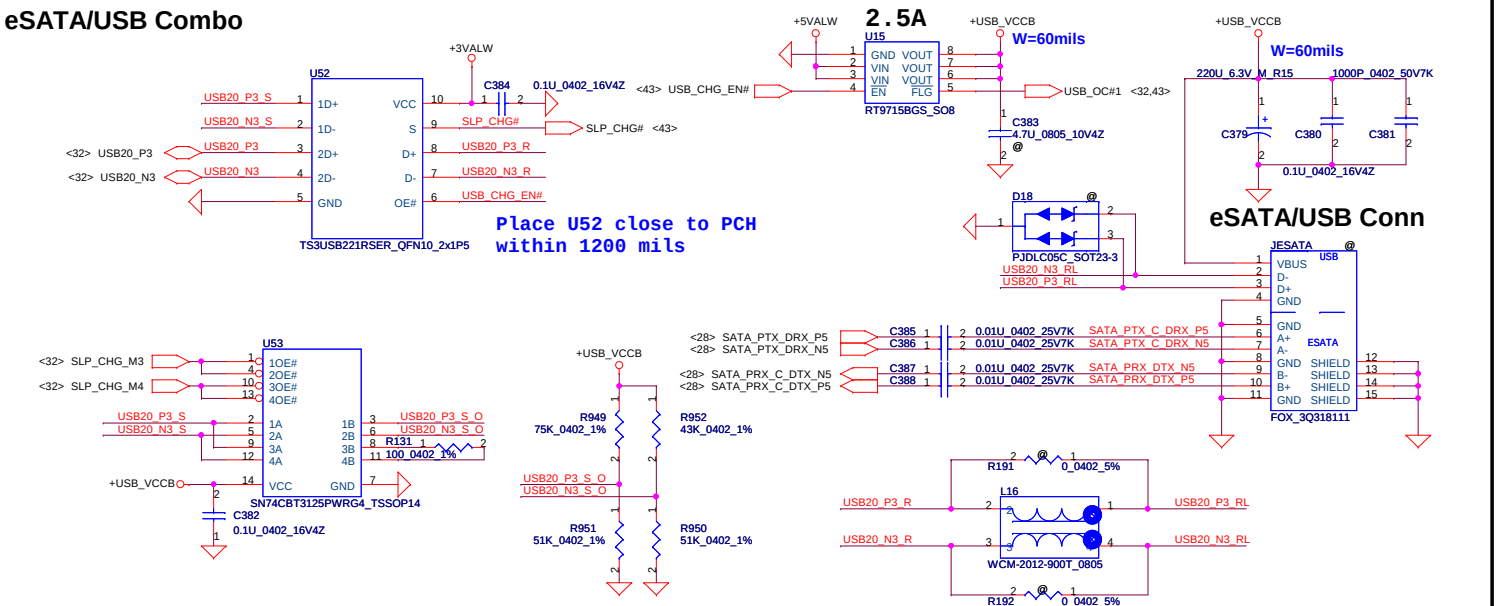
SATA ODD Conn



USB Board@ Right Side



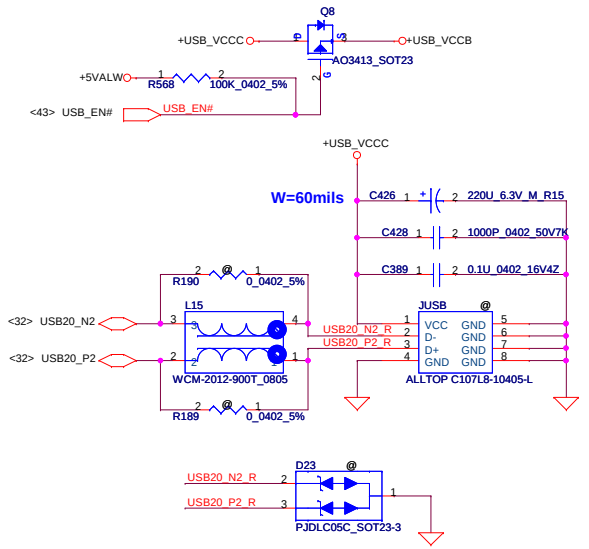
eSATA/USB Combo



SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

USB Board@ Left Side



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

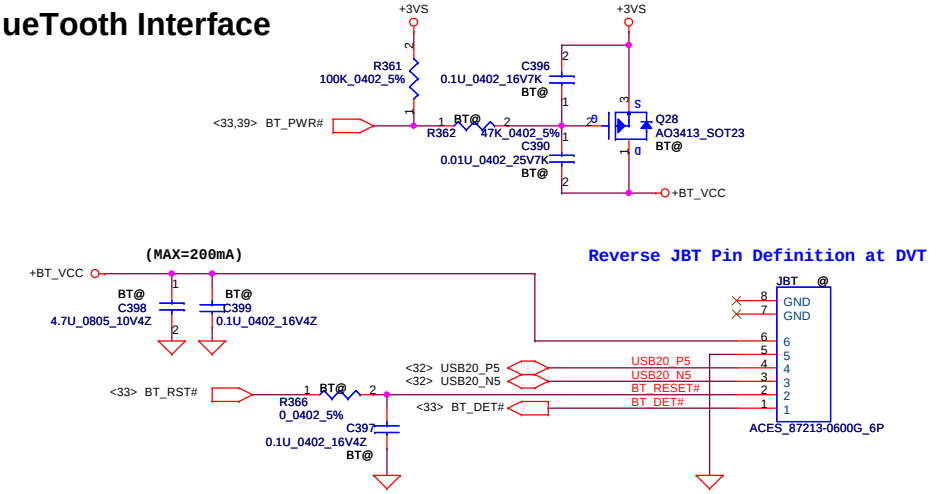
Compal Electronics, Inc.

Title: SATA-HDD/ODD/eSATA/USB

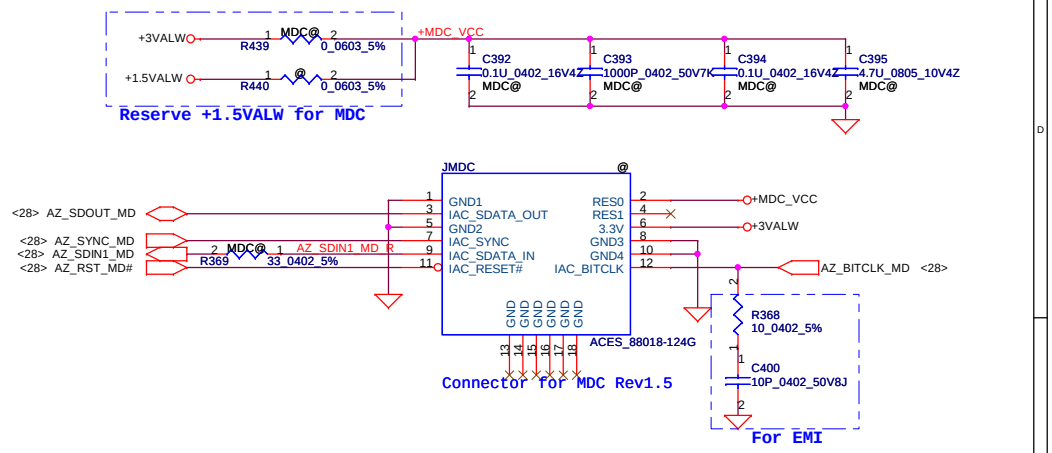
Size | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

Date: Wednesday, March 24, 2010 | Sheet 37 of 59

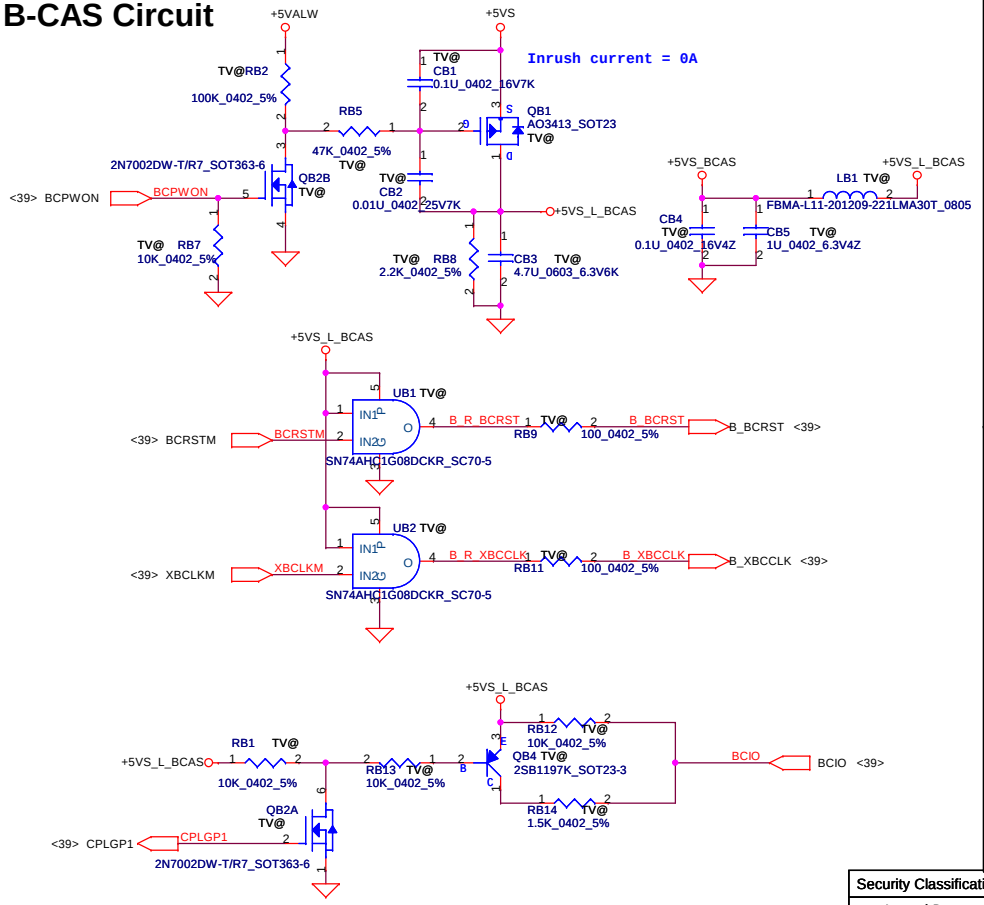
BlueTooth Interface



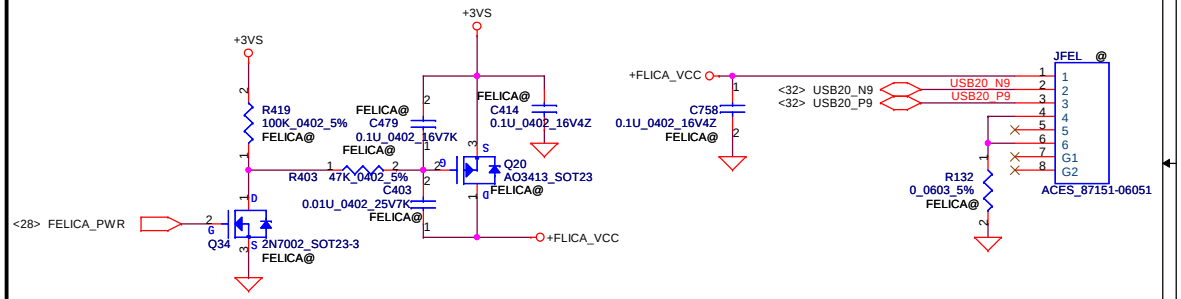
MDC 1.5 Conn.



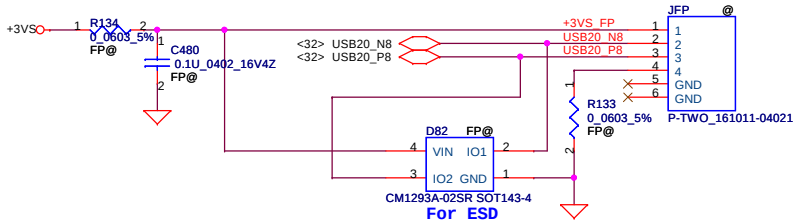
B-CAS Circuit



Felica

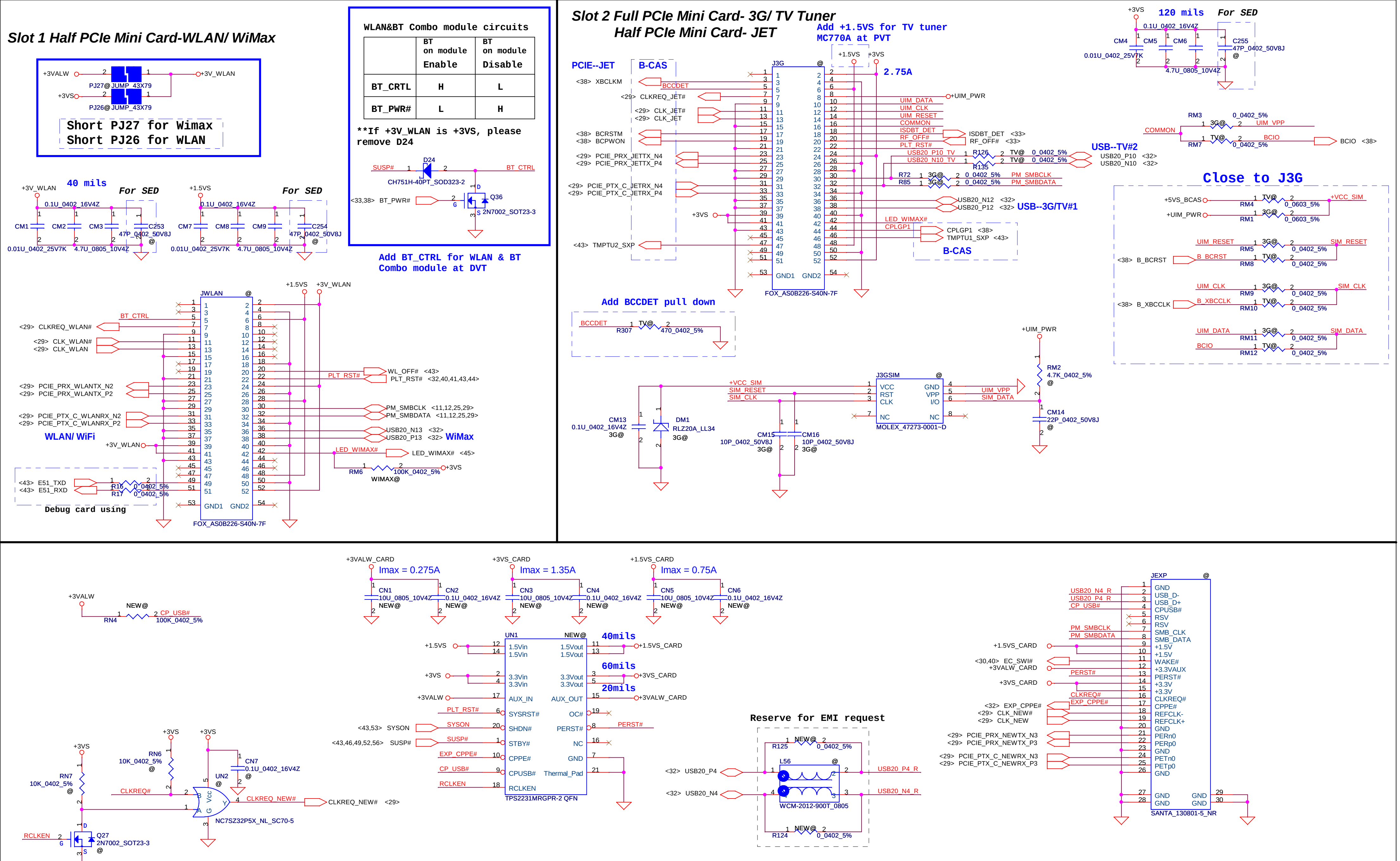


Finger printer



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	BT/FP/B-CAS/Felica/MDC		
Size	Document Number		Rev
	NWQAA LA-6062P M/B		2.0
Date:	Wednesday, March 24, 2010	Sheet	38 of 59



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	200910/9	Deciphered Date	2010/01/23	Title: PCIe-WLAN/JET/3G/TV/NewCard
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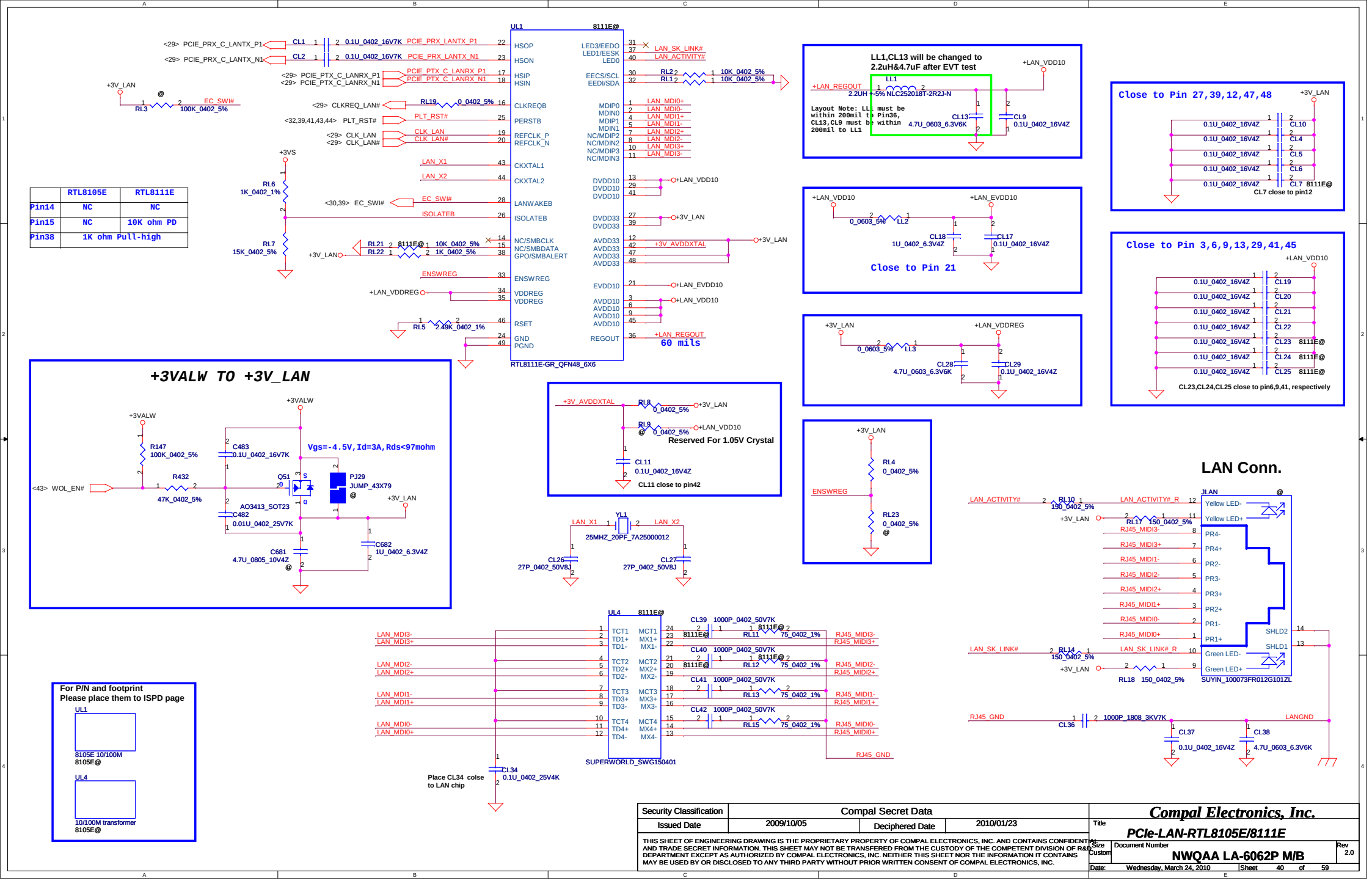
				Date: Wednesday, March 24, 2010 / Sheet 39 of 59



Security Classification	Compal Secret Data		
Issued Date	2009/10/05	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: PCIe-LAN-RTL8105E/8111E

Size: Custom | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

Date: Wednesday, March 24, 2010 | Sheet 40 of 59

JMB389C / JMB385C

5 in 1 Card Reader

D3E mode

Power On Strapping setting

Pin name	Description	
	High	low
MDIO7	on-board★	add-in card
MDIO14	CR_LED high active	CR_LED low active★

CC3 close to pin 5
CC2 close to CC3
CC1 is near CC3
CC4 close to pin 10
place near pin 19,20 and 44
CC12 close to pin 36
CC11 close to pin18
For intenal LDO's usage
CC10 close to pin37
place 6 GND vias on T-pad
Reserved for EMI,close to UC1.42
Reserved for EMI,close to JREAD
Confirm sinking 16mA
CC16 close to pin43
For internal LDO in SD3.0

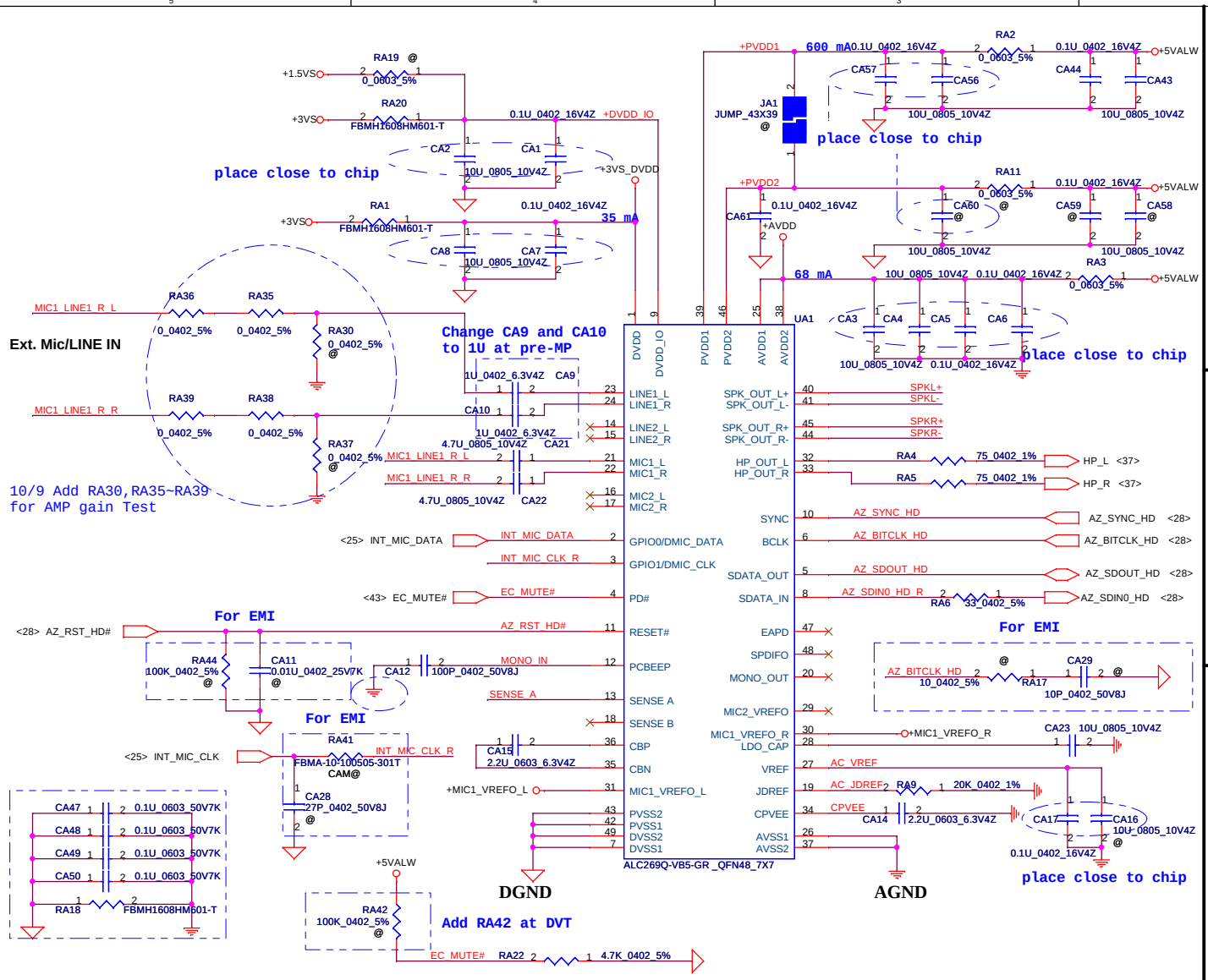
Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

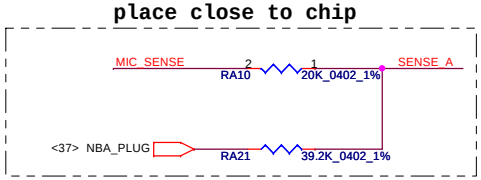
Title: **Card Reader JMB385/389**

Size: Custom | Document Number: **NWQAA LA-6062P M/B** | Rev: 2.0

Date: Wednesday, March 24, 2010 | Sheet 41 of 59



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



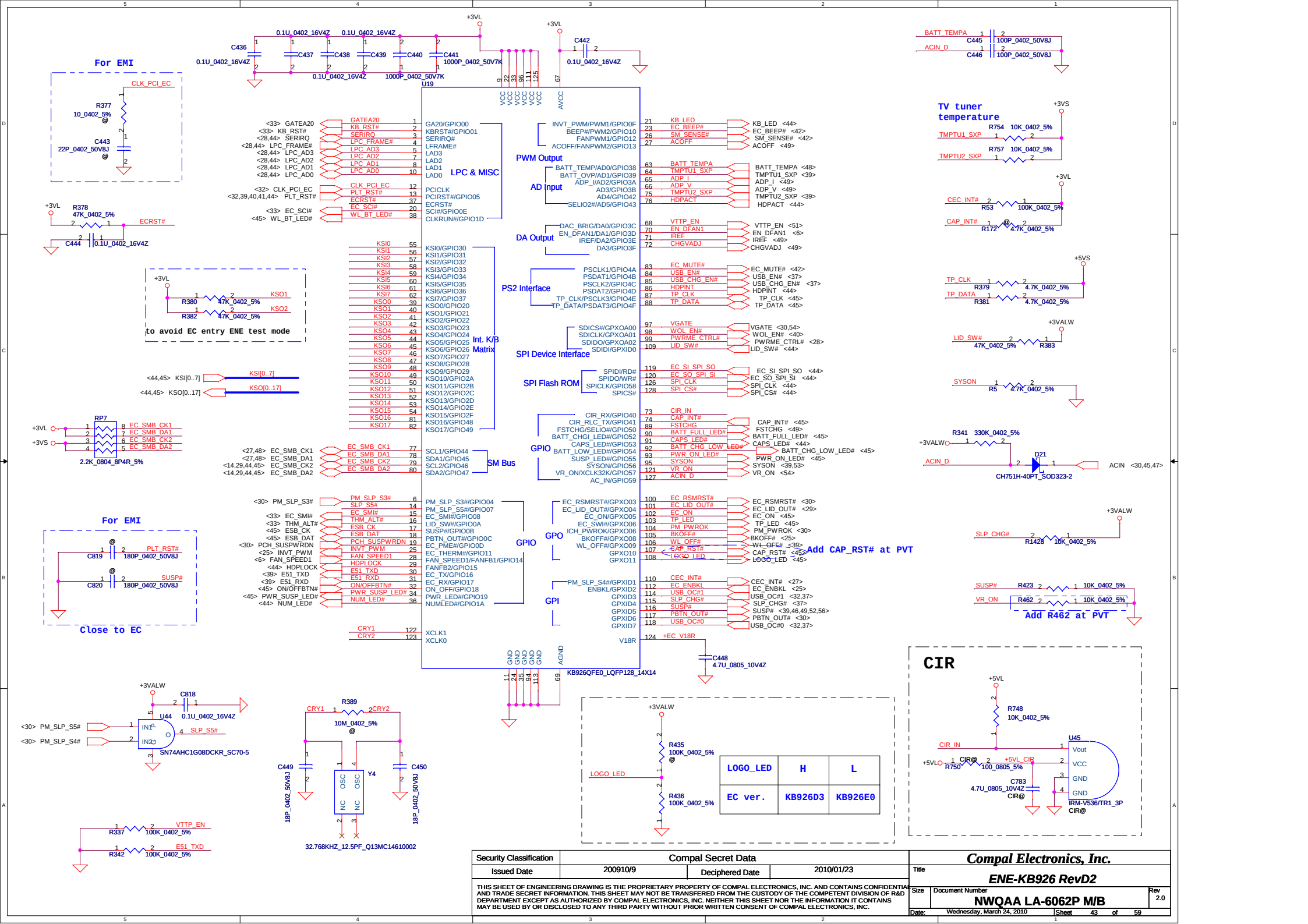
Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: HDA CODEC ALC269

Size: | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

Date: Wednesday, March 24, 2010 | Sheet 42 of 59



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

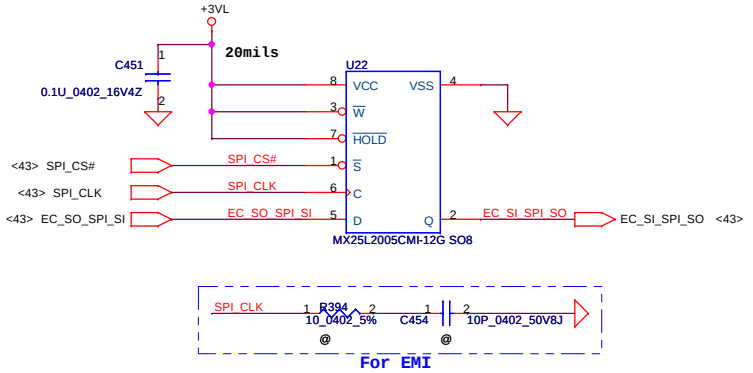
Compal Electronics, Inc.

Title: ENE-KB926 RevD2

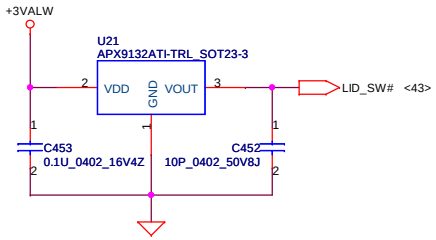
Size | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

Date: Wednesday, March 24, 2010 | Sheet 43 of 59

SPI Flash (256KB)

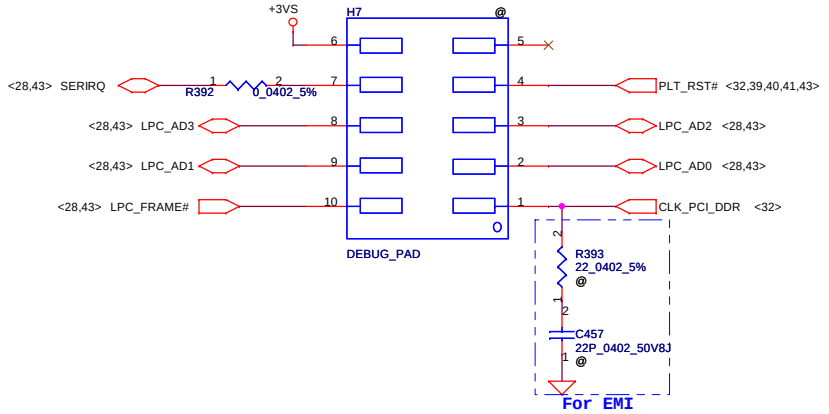


Lid SW

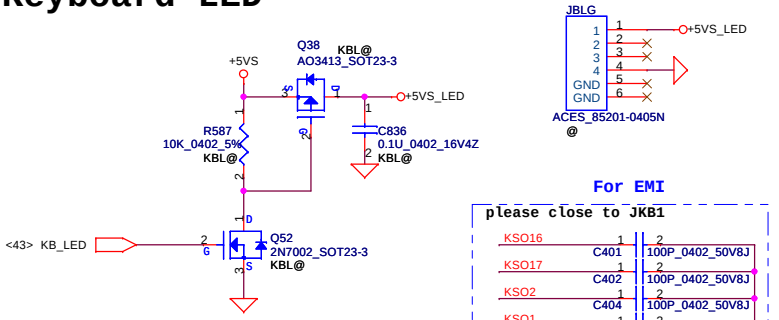


LPC Debug Port

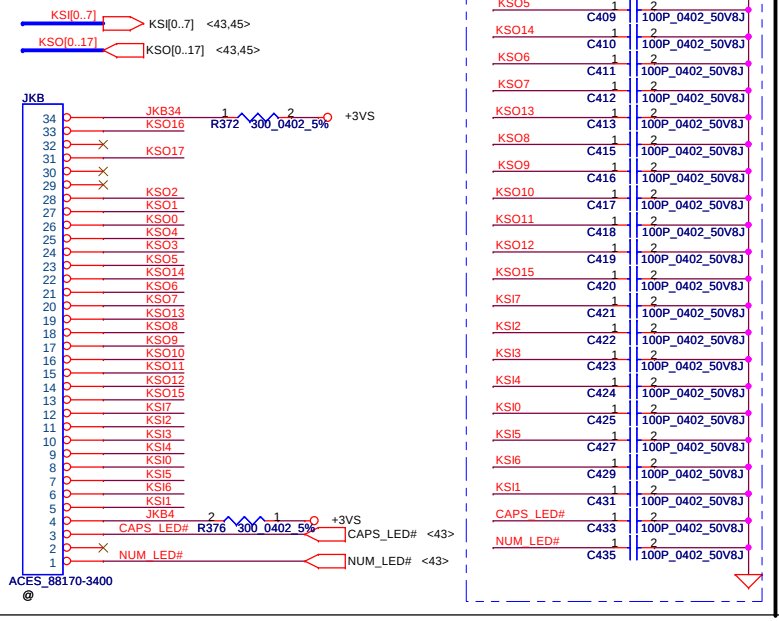
Place the PAD under DDR DIMM.



Keyboard LED

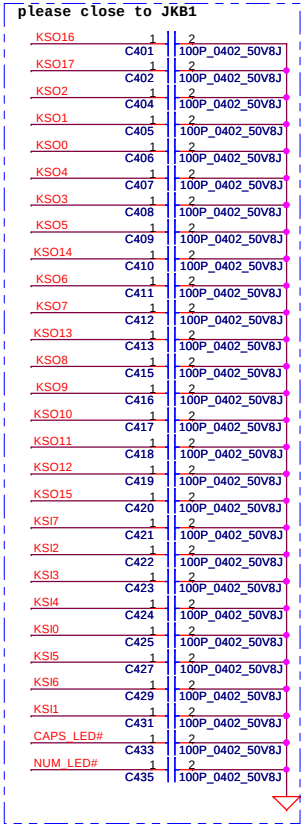


KEYBOARD CONN.

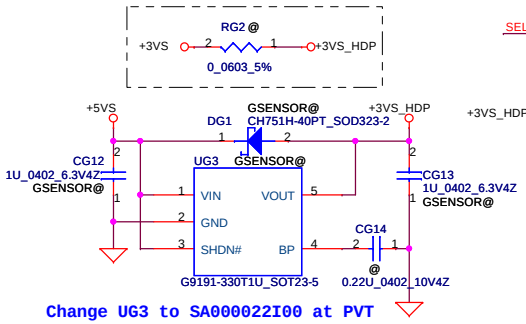


For EMI

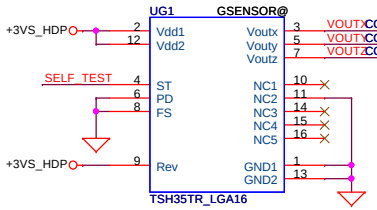
please close to JKB1



G-Sensor

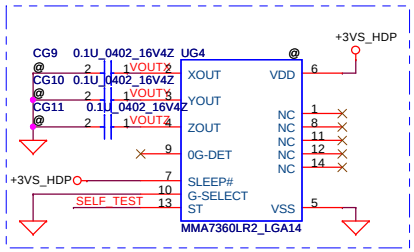


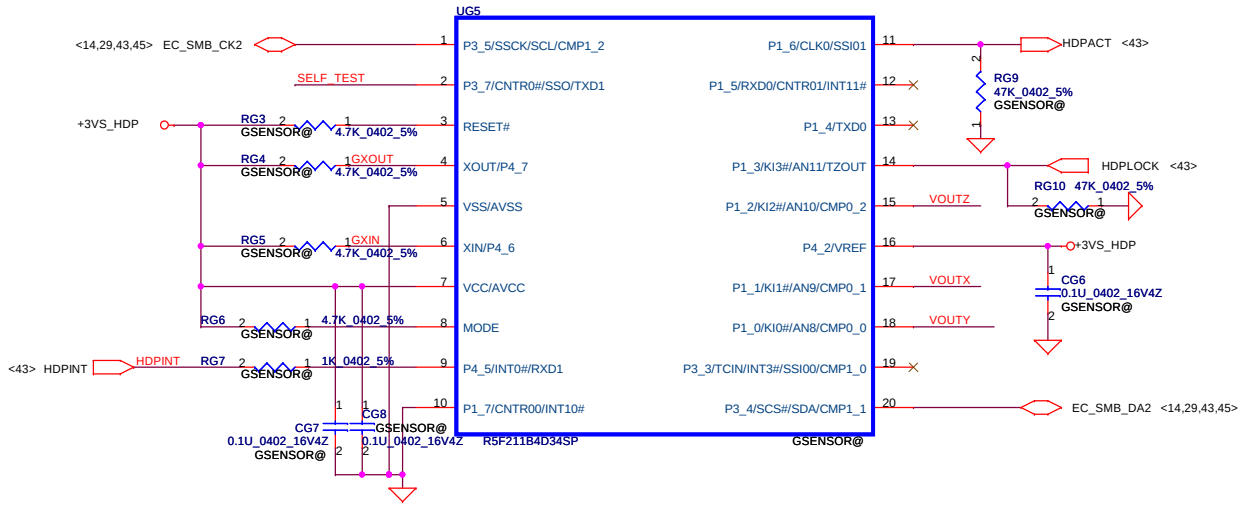
Change UG3 to SA000022I00 at PVT



Place UG1 and UG4 on TOP Layer

Reserve for 2nd Source





Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: SPI ROM/LID/Debug/KB/G-Sen

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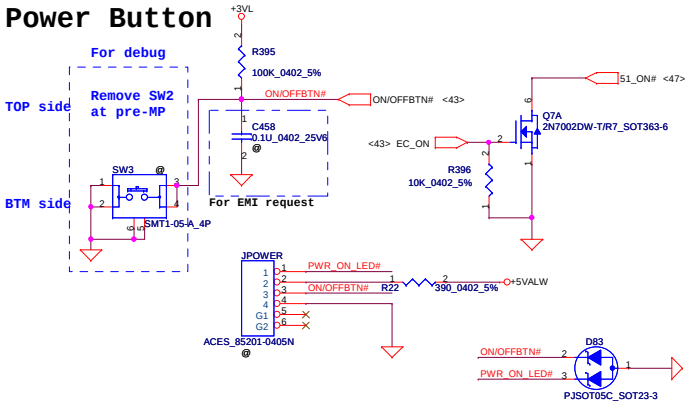
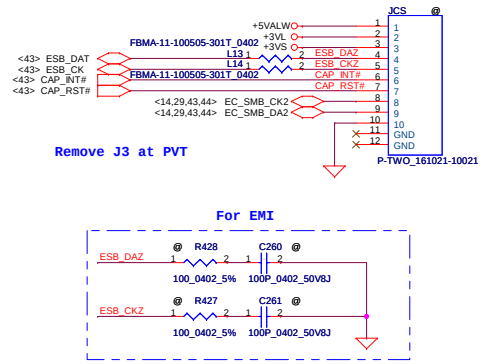
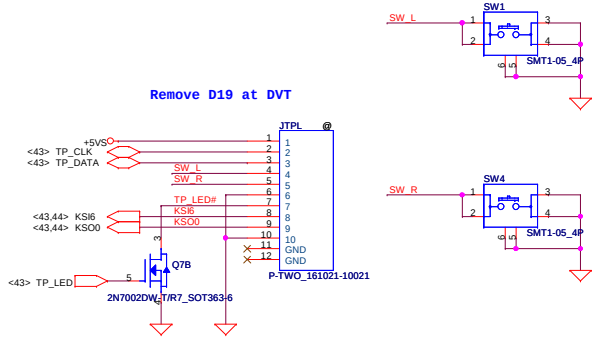
Power Button



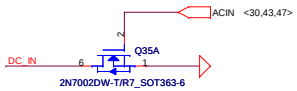
Caps Sensor/Light Sensor Conn.



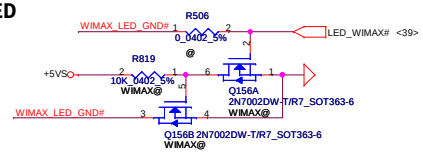
Touchpad & Light Pipe Connector



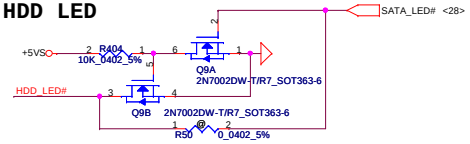
DC-IN LED



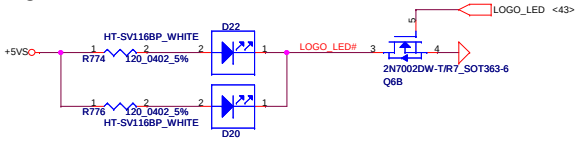
WiMAX LED



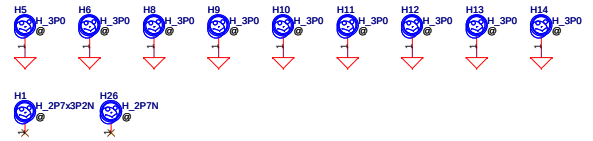
HDD LED



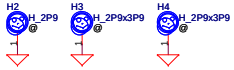
Logo LED



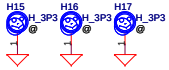
Screw Hole



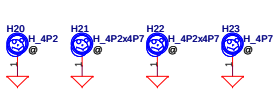
VGA



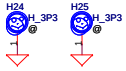
MINI CARD -- 3G



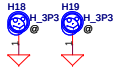
CPU



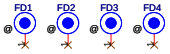
MDC



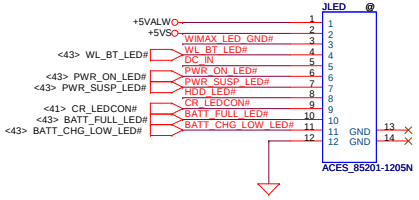
MINI CARD -- WLAN



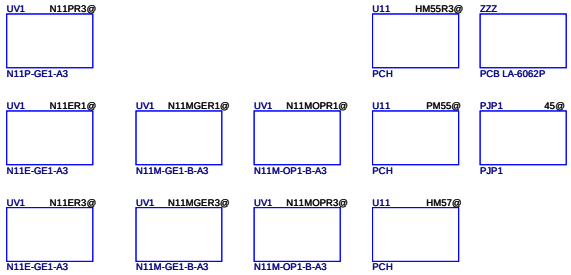
PCB Fedical Mark PAD



LED/B Connector



ISPD



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: PWR/Cap./TP/LED/LP/LS/Screw

Size | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

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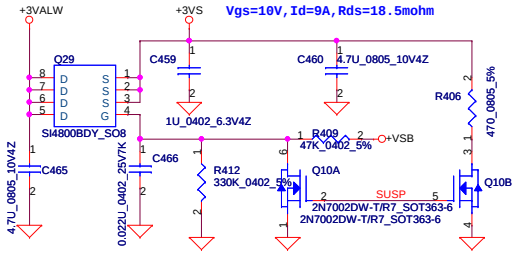
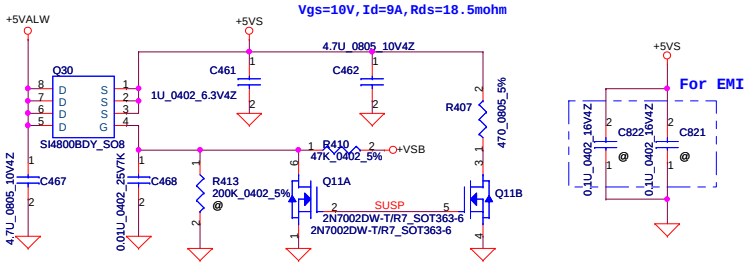
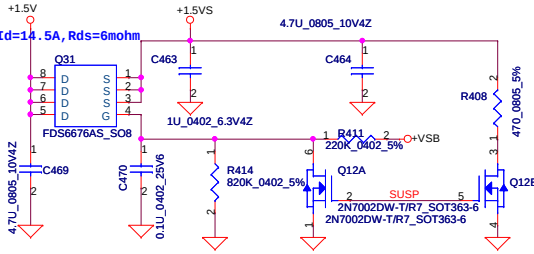
+3VALW TO +3VS



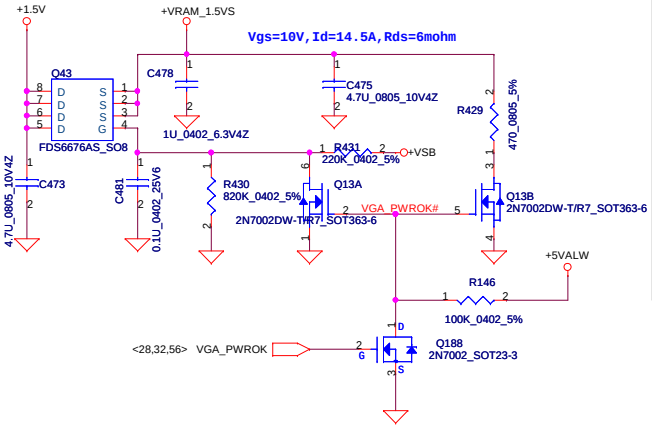
+5VALW TO +5VS



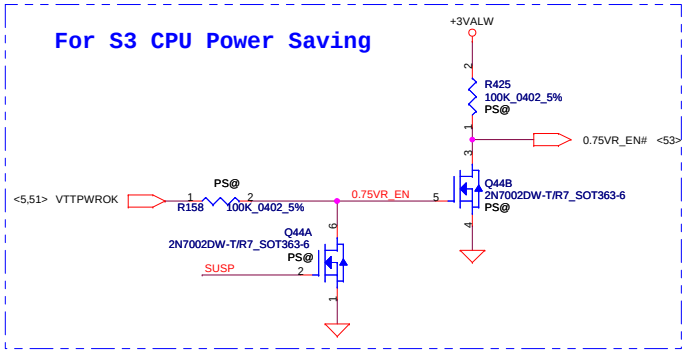
+1.5V to +1.5VS

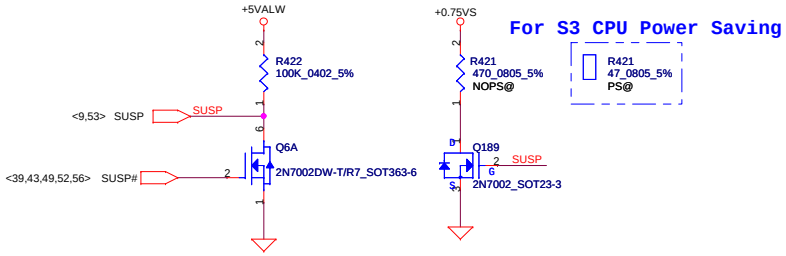


+1.5V to +VRAM_1.5VS

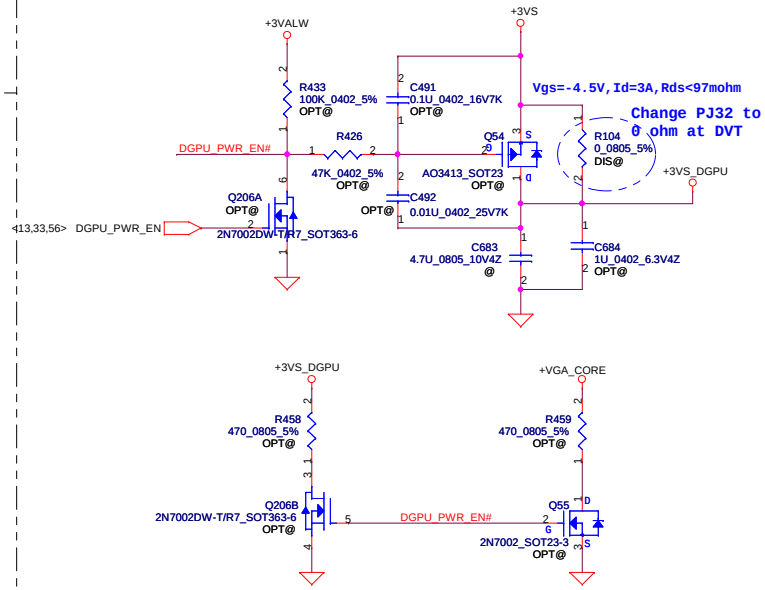


For S3 CPU Power Saving



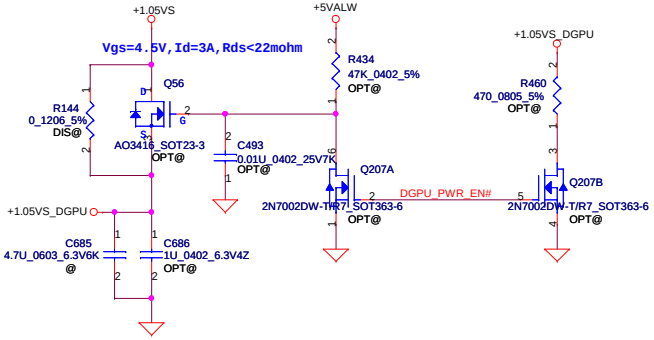


+3VS to +3VS_DGPU

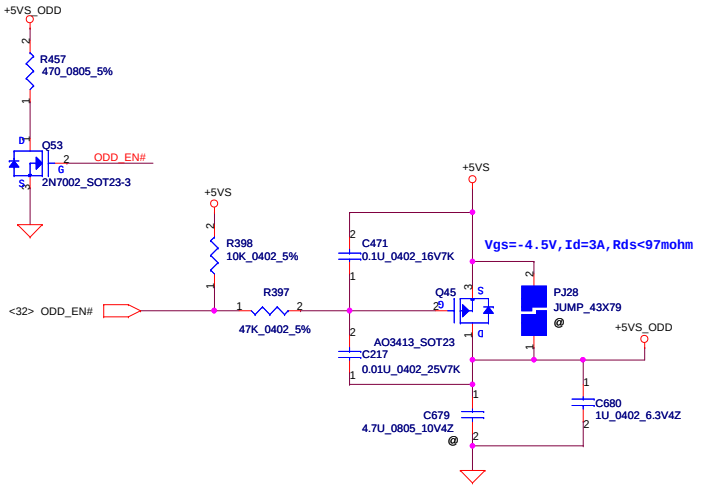


+1.05VS to +1.05VS_DGPU

Change +1.05VS_DGPU circuit
to N-channel MOS at PVT



+5VS TO +5VS_ODD



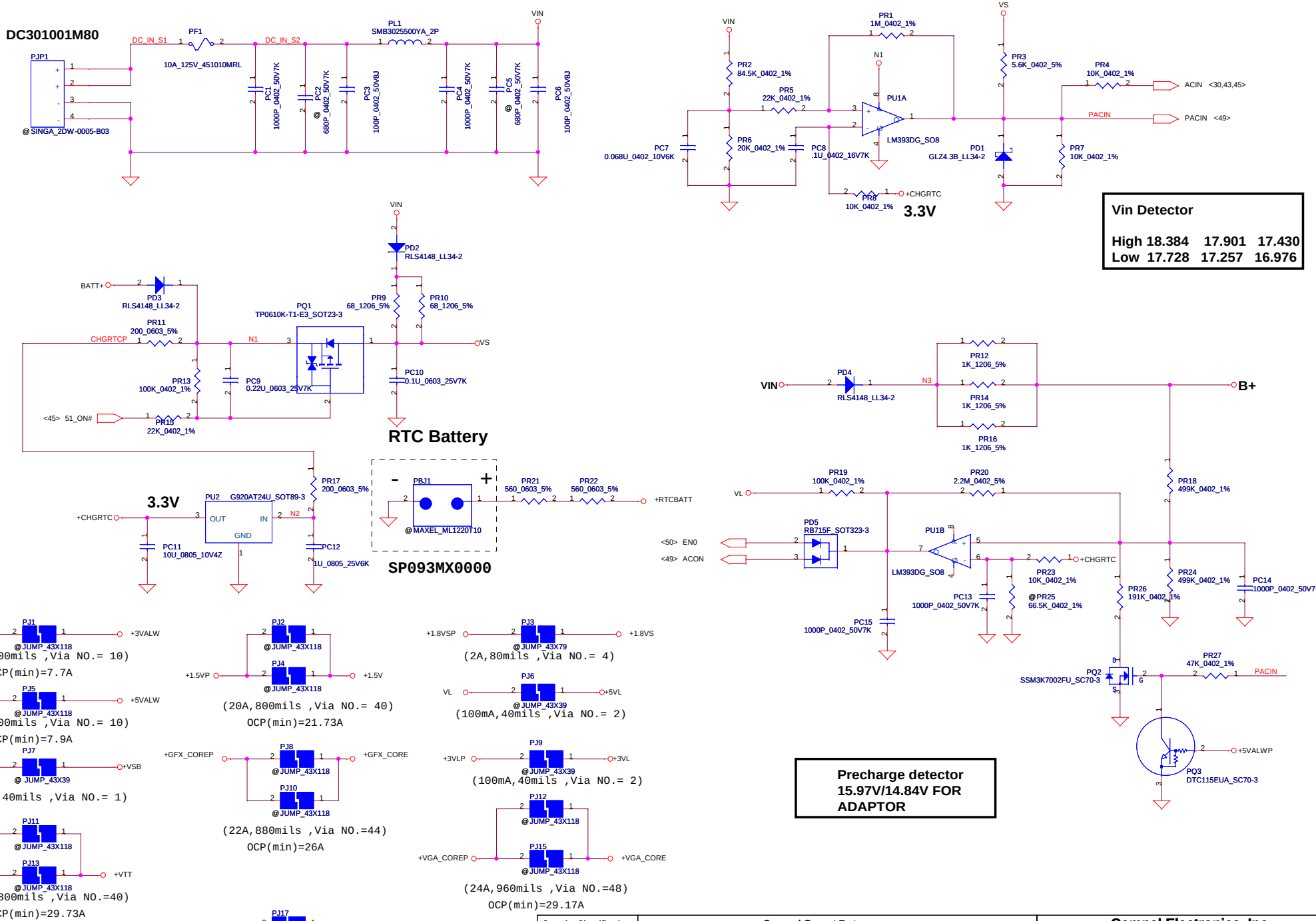
Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: DC-DC INTERFACE

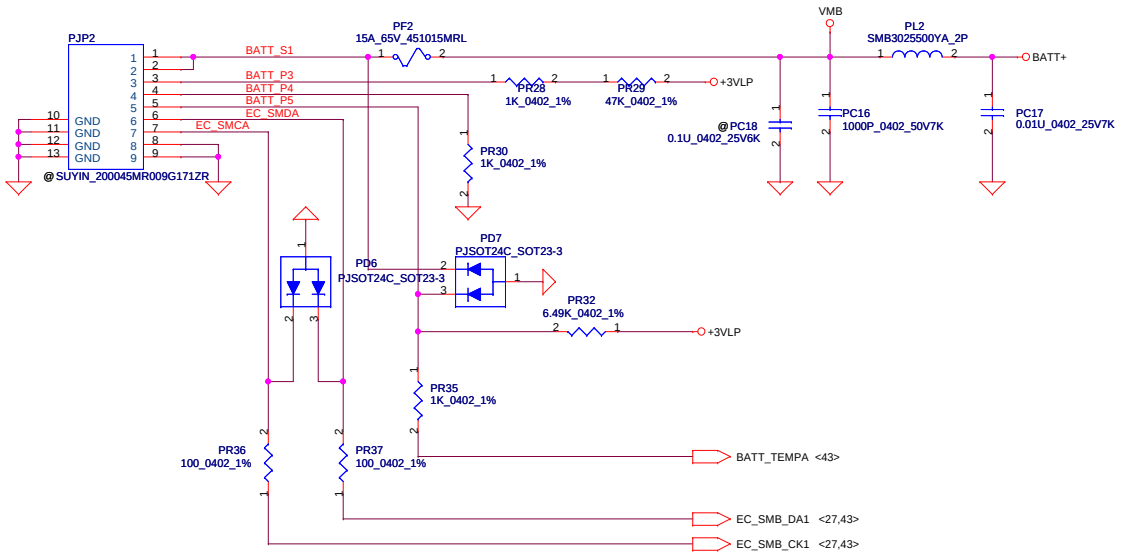
Size | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

Date: Wednesday, March 24, 2010 | Sheet 46 of 59



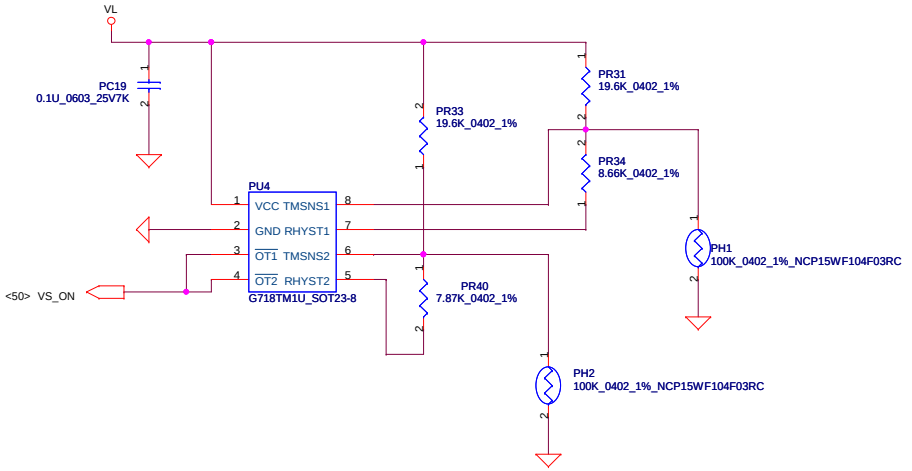
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

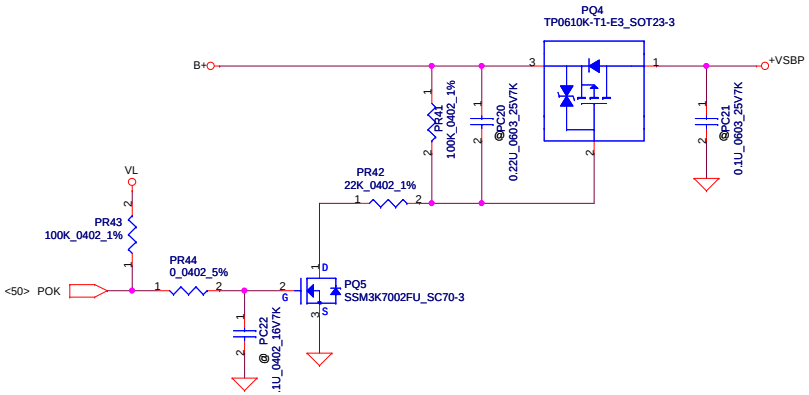
Compal Electronics, Inc.			
Title	DCIN / DETECTOR		
Size	Document Number	NWQAA LA-6062P M/B	Rev 2.0
Date: Wednesday, March 24, 2010	Sheet 47 of 59		



PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C

PH2 near main Battery CONN :
BAT. thermal protection at 95 degree C
Recovery at 48 degree C





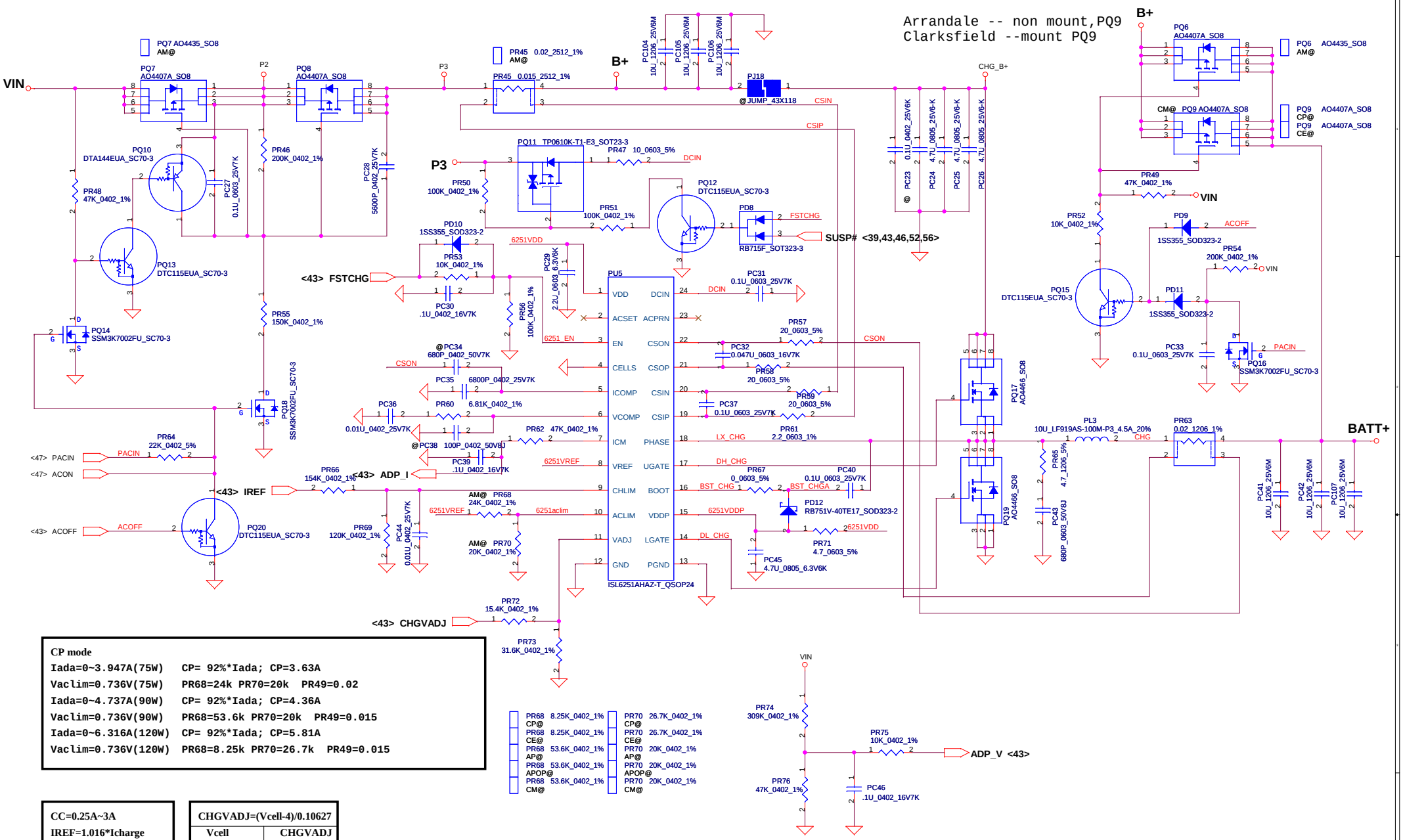
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

Size	Document Number	Rev
	NWQAA LA-6062P M/B	2.0

Date: Wednesday, March 24, 2010 | Sheet 48 of 59



CP mode

```
Iada=0~3.947A(75W)   CP= 92%*Iada; CP=3.63A
Vaclim=0.736V(75W)   PR68=24k PR70=20k  PR49=0.02
Iada=0~4.737A(90W)   CP= 92%*Iada; CP=4.36A
Vaclim=0.736V(90W)   PR68=53.6k PR70=20k  PR49=0.015
Iada=0~6.316A(120W)  CP= 92%*Iada; CP=5.81A
Vaclim=0.736V(120W)  PR68=8.25k PR70=26.7k  PR49=0.015
```

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

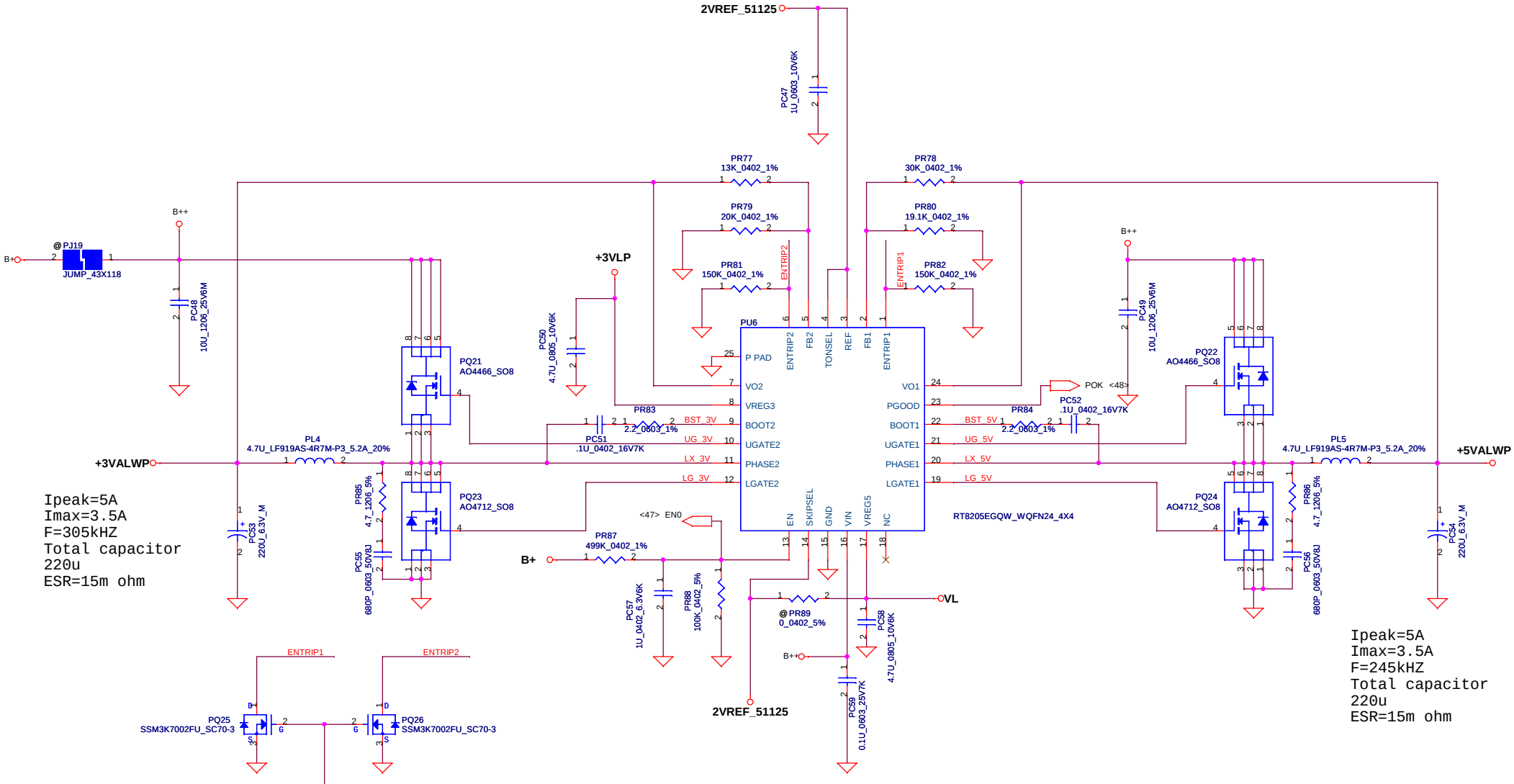
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
	NWQAA LA-6062P M/B	2.0

Date: Wednesday, March 24, 2010 | Sheet 49 of 59



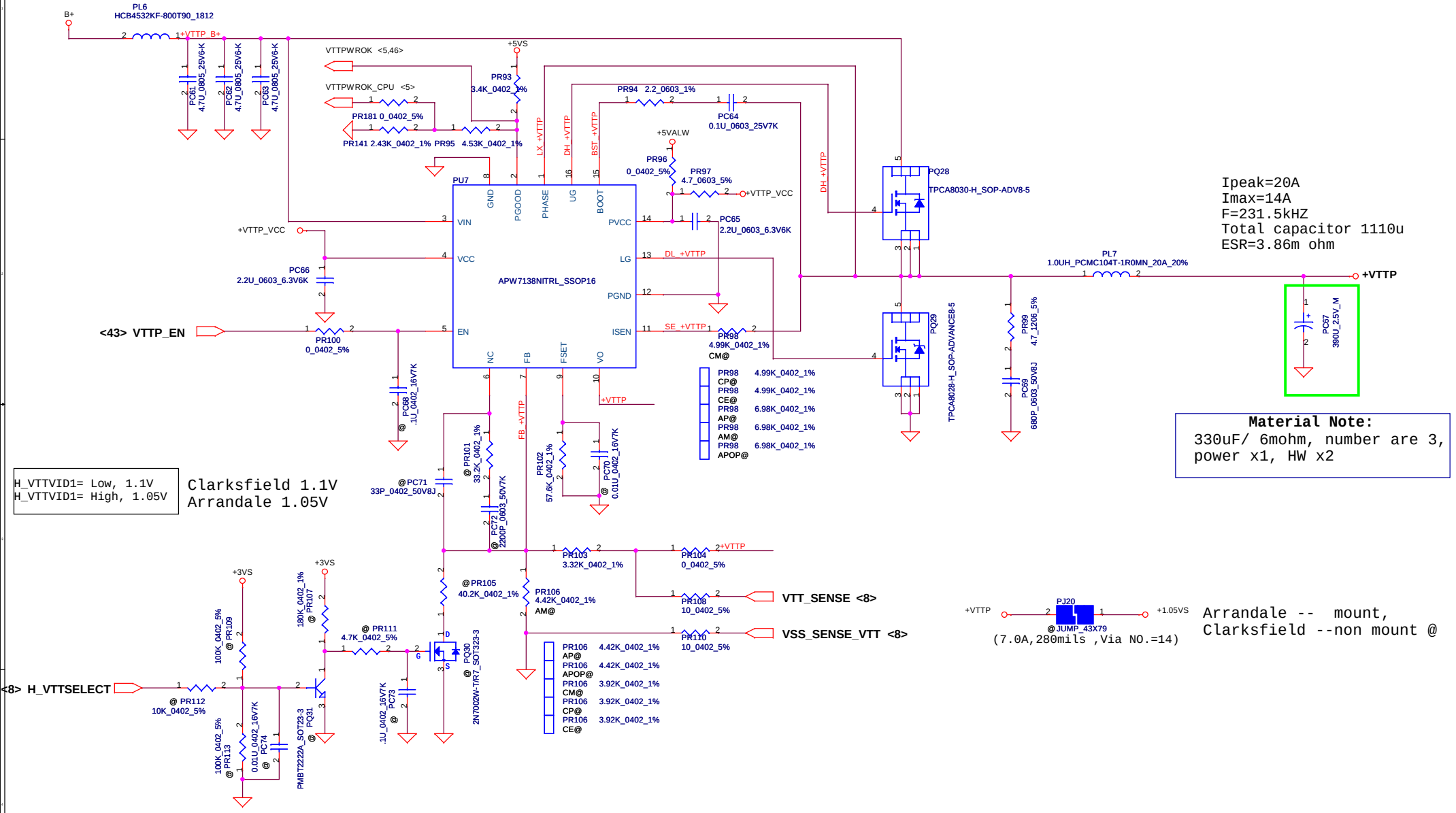
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size | Document Number: NWQAA LA-6062P M/B | Rev: 2.0

Date: Wednesday, March 24, 2010 | Sheet 50 of 59



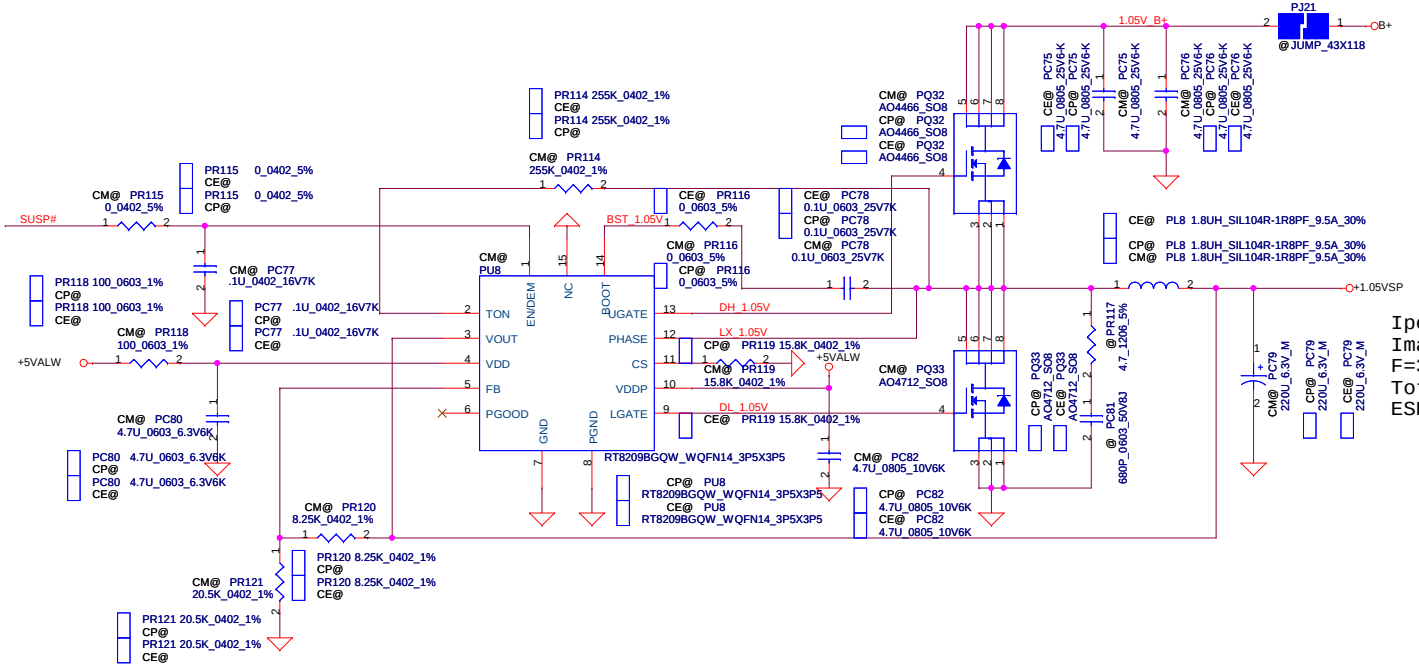
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

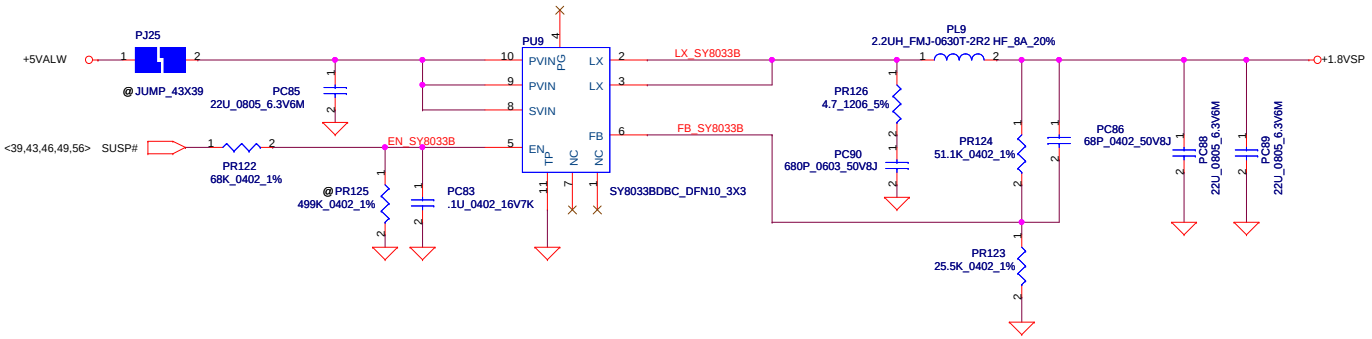
Compal Electronics, Inc.

Title	+VTTP	
Size	Document Number: NWQAA LA-6062P M/B	Rev: 2.0
Date: Wednesday, March 24, 2010	Sheet 51 of 59	

Arrandale -- non mount, @
Clarksfield --mount

Ipeak=7A
Imax=4.9A
F=313kHZ
Total capacitor 550u
ESR=5m ohm





Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **1.05VSP / +1.8VSP**

Size	Document Number	Rev
	NWQAA LA-6062P M/B	2.0

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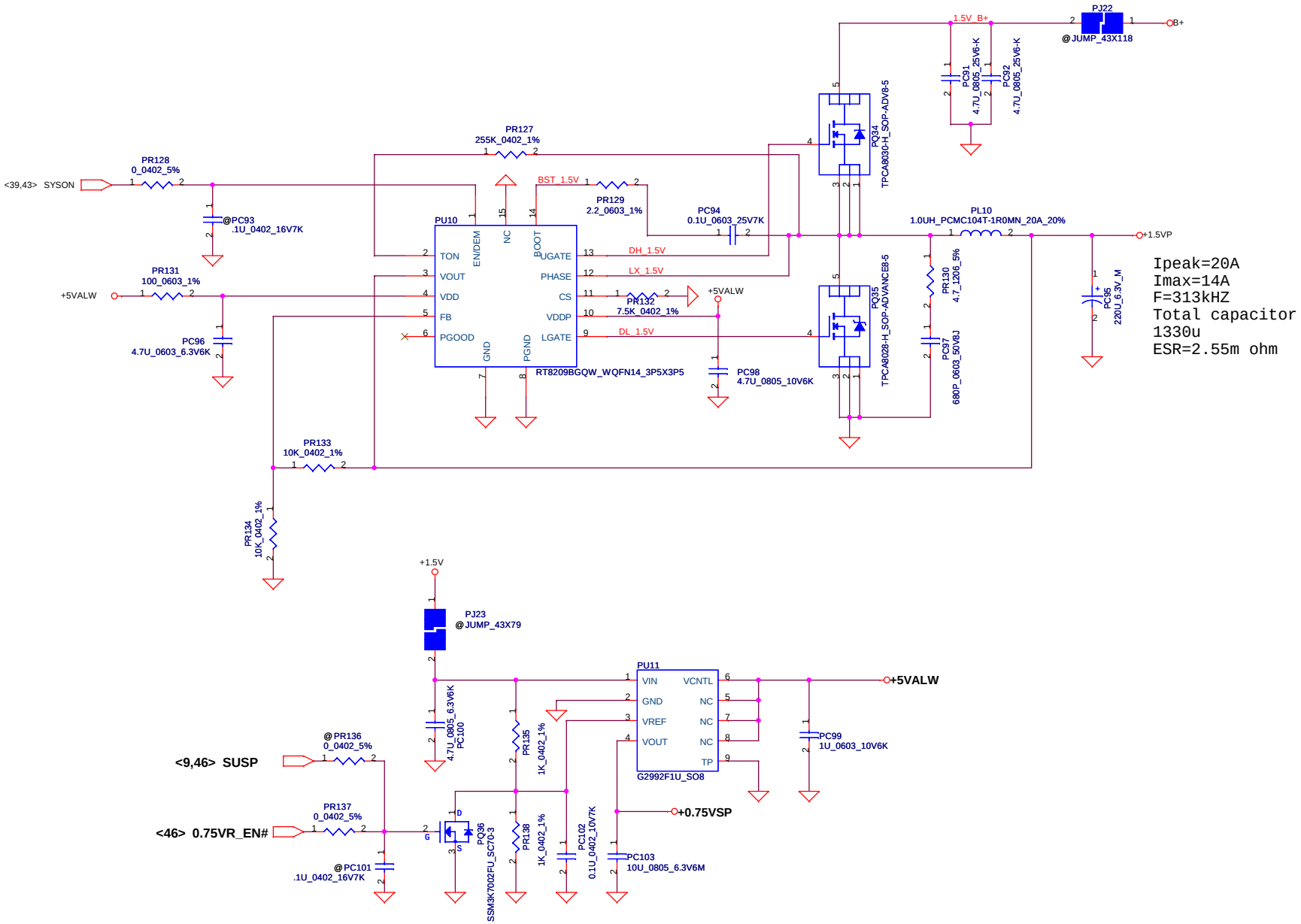
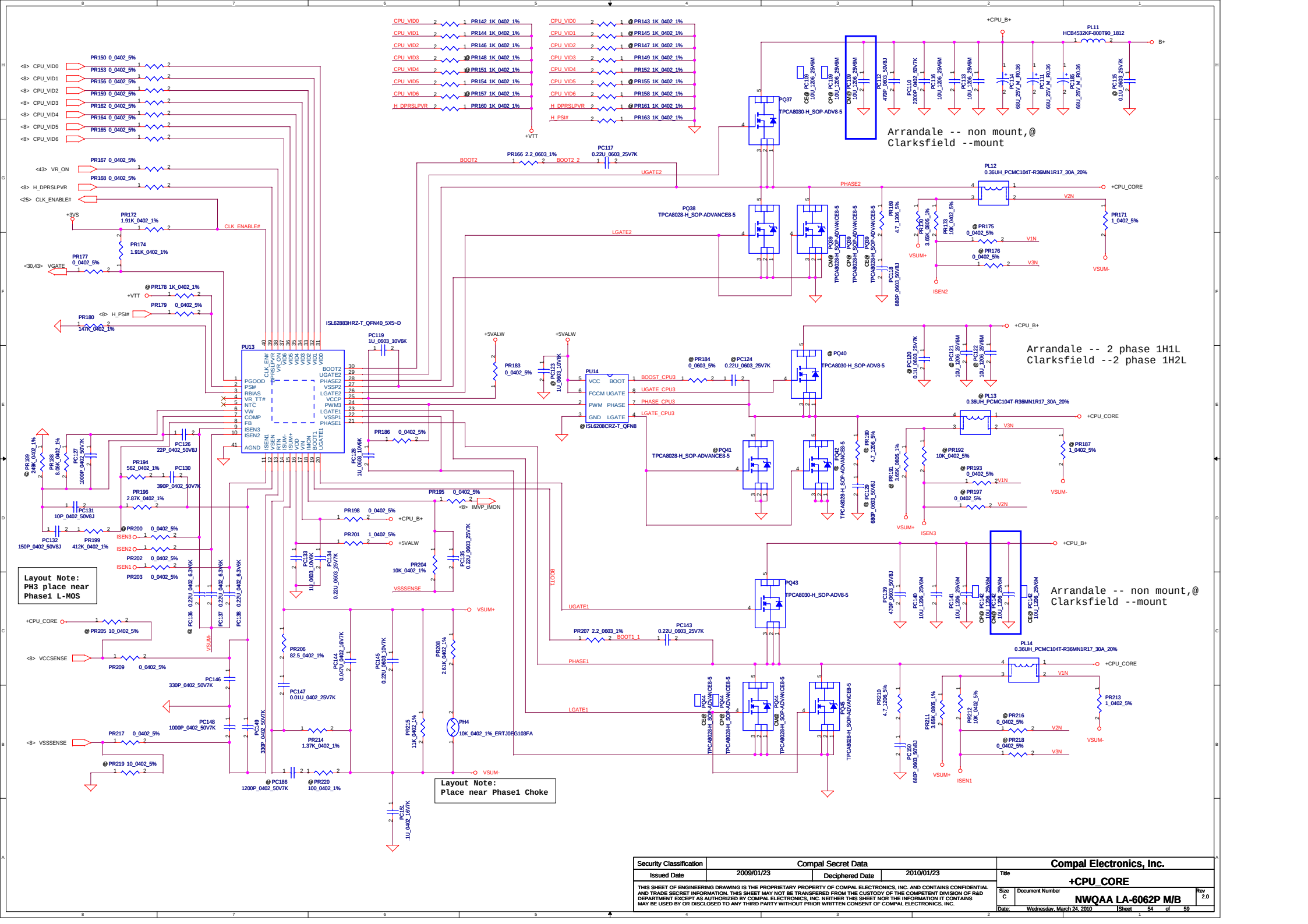


Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title	+1.5VP/0.75VSP	
Size: Custom	Document Number: NWQAA LA-6062P M/B	Rev: 2.0
Date: Wednesday, March 24, 2010	Sheet 53 of 59	



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
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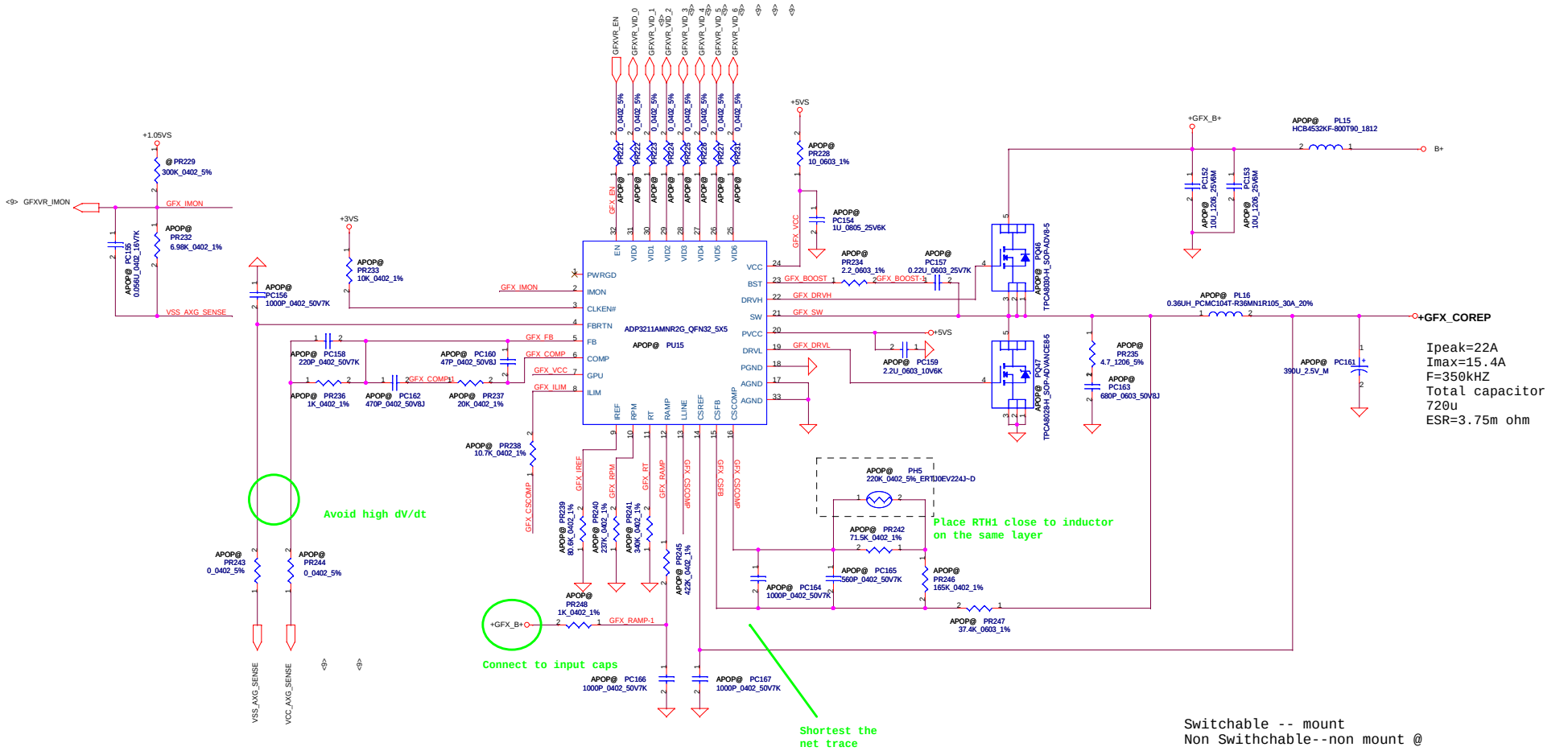

Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.	
Title	+GFX_COREP
Size	Document Number: NWQAA LA-6062P M/B
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Date:	Wednesday, March 24, 2010
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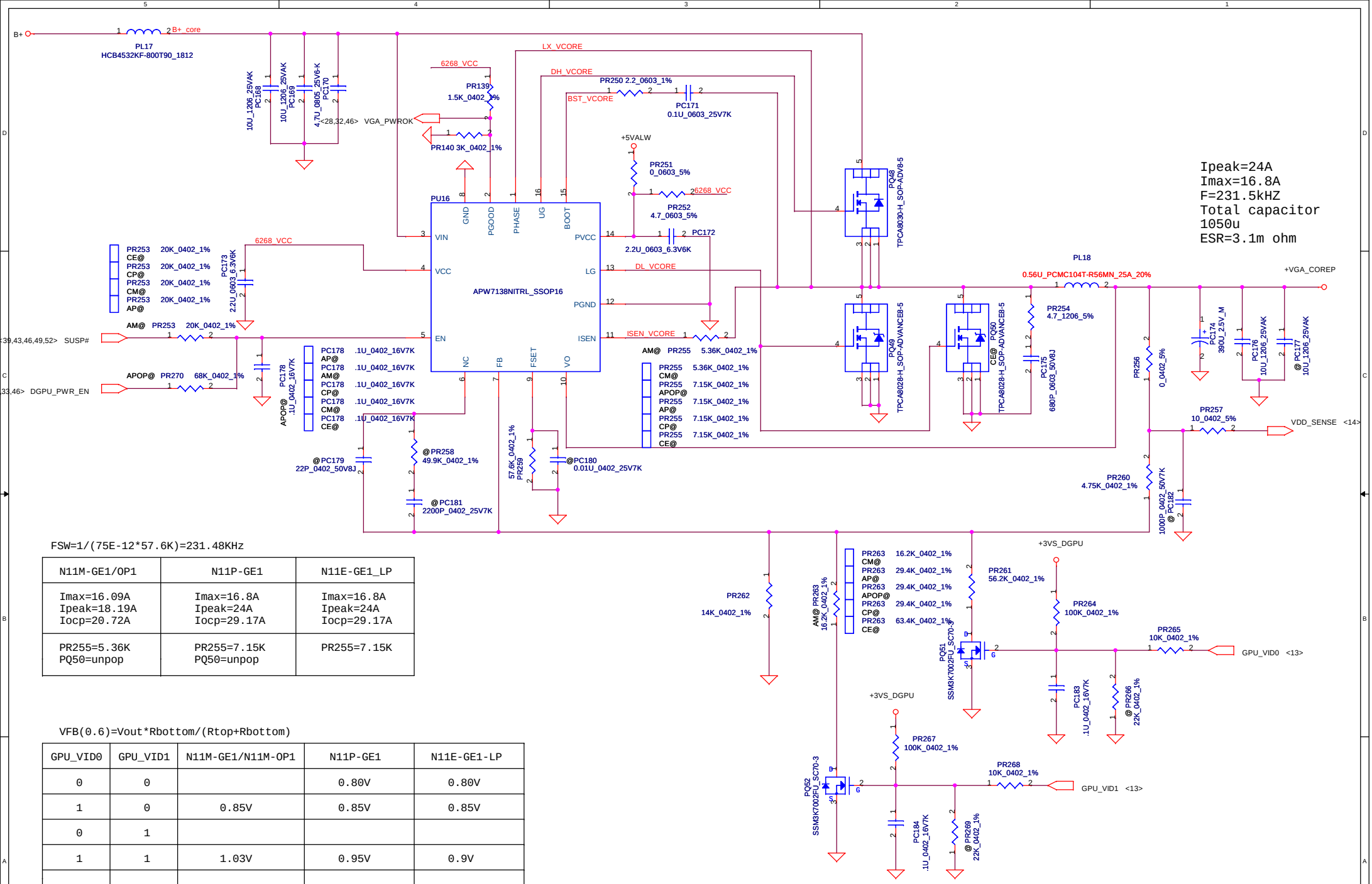

FSW=1/(75E-12*57.6K)=231.48KHz

N11M-GE1/OP1	N11P-GE1	N11E-GE1_LP
Imax=16.09A Ipeak=18.19A Iocp=20.72A	Imax=16.8A Ipeak=24A Iocp=29.17A	Imax=16.8A Ipeak=24A Iocp=29.17A
PR255=5.36K PQ50=unpop	PR255=7.15K PQ50=unpop	PR255=7.15K

VFB(0.6)=Vout*Rbottom/(Rtop+Rbottom)

GPU_VID0	GPU_VID1	N11M-GE1/N11M-OP1	N11P-GE1	N11E-GE1-LP
0	0		0.80V	0.80V
1	0	0.85V	0.85V	0.85V
0	1			
1	1	1.03V	0.95V	0.9V
		PR260 = 4.75K PR262 =14K PR261 =56.2K PR263=16.2K	PR260 = 4.75K PR262 =14K PR261 =56.2K PR263=29.4K	PR260 = 4.75K PR262 =14K PR261 =56.2K PR263=63.4K

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title	+VGA_COREP		
Size: Custom	Document Number: NWQAA LA-6062P M/B		Rev: 2.0
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT		P53-PWR_1.5VP/0.75VSP	Change PR132 18k to 6.19k	Modify 1.5V OCP to 18.09A (2009/11/25)
EVT		P56-PWR_VGA_COREP	Change PR270 0 to 100 Ohm	Adjust RC for Optimus sequence (2009/11/25)
			Change PC178 0.1U to 0.01U	
EVT		P39-PWR_+VTTP	Change PR141 2.26k to 2.43k	Modify VTTPWROK voltage (2009/11/25)
EVT		P39-PWR_+VTTP	Remove PC71 33P, PC72 2200P, PR101 33.2k	APW7138 not use this function (2009/11/25)
EVT		P38-PWR_3VALWP/5VALWP	Change PR92 49.9k to 42.2k	Modify VS divider voltage to drive MOS (2009/11/25)
EVT		P56-PWR_VGA_COREP	Remove PC179 22P, PC181 2200P, PR258 49.9k	APW7138 not use this function (2009/11/25)
EVT		P56-PWR_VGA_COREP	Change PR255 7.15k to 9.09k	Modify VGA 11P OCP to 38.03A (2009/11/25)
EVT		P56-PWR_VGA_COREP	Remove PC177 10U	FAE suggest to remove 1 10U cap for IC on time control (2009/11/25)
EVT		P42-PWR_CPU_CORE	Change PL12,PL14 SH000005680 to SH00000IK00	Use 5% DCR choke (2009/11/25)
EVT		P43-PWR_GM VGA_CORE	Change PH5 SL20000058L to SL200000500	Use Compal PN (2009/11/25)
DVT		P56-PWR_VGA_COREP	Change PR255 9.09k to 7.15k	Modify VGA 11P OCP to 29.17A (2009/12/28)
DVT		P43-PWR_GM VGA_CORE	Change PL16 SH00000HK00 to SH00000IK00	Use same PN choke (2009/12/28)
DVT		P39-PWR_+VTTP	Change PR106 4.42k to 3.92k	Modify VTT voltage to 1.1V for Clarkfield (2009/12/28)
DVT		P42-PWR_CPU_CORE	Change PC114, PC111, PC185 from SF000000F80 to SF000000W00	Cost down (2009/12/28)
DVT		P43-PWR_GM VGA_CORE	Change PC161 to SGA00002680	For DVT budding(thermal issue), it will change to original type for PVT (2009/12/28)
DVT		P56-PWR_VGA_COREP	Change PR253 0 to 20k	For VGA sequence(2009/12/28)
DVT		P56-PWR_VGA_COREP	Change PR270 0 to 20k	For VGA sequence(2009/12/28)
DVT		P52-PWR_1.05VSP/1.8VSP	Add PC83 0.1U and change PR122 0 to 68k	For VGA sequence(2009/12/28)
DVT		P48-PWR_BATTERY CONN / OTP	Add PD6, PD7 ESD diode	For ESD solution(2009/12/28)
DVT		P49-PWR_CHARGER	Add PC104,PC105,PC106 10U	Reserve for EMI solution(2009/12/28)
DVT		P50-PWR_3VALWP/5VALWP	Change PR83,PR84 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
			Add PR85,PR86 4.7 and PC55,PC56 680P	Add snubber(For EMI solution)(2009/12/28)
DVT		P42-PWR_CPU_CORE	Change PR166,PR207 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
			Add PR169,PR210 4.7 and PC118,PC150 680P	Add snubber(For EMI solution)(2009/12/28)
DVT		P55-PWR_GM VGA_CORE	Change PR234 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
			Add PR235 4.7 and PC163 680P	Add snubber(For EMI solution)(2009/12/28)
DVT		P56-PWR_VGA_COREP	Add PR254 4.7 and PC175 680P	Add snubber(For EMI solution)(2009/12/28)
DVT		P48-PWR_BATTERY CONN / OTP	Change PR33 10k,PR31 21k to 19.6k, PR34 9.53k to 8.66k, PR40 47k to 7.87k	Adjust OTP setting point(2009/12/28)
DVT		P42-PWR_CPU_CORE	Add PQ39,PQ44 TPCA8028-H	Use 1H 2L MOS solution for Clarksfield (2009/12/31)
DVT		P42-PWR_CPU_CORE	Add PC109,PC142 10U input cap	For Clarksfield solution (2009/12/31)
DVT		P42-PWR_CPU_CORE	Change PR214 1.2k to 1.37k	Adjust CPO_CORE OCP to 65A (2009/12/31)
DVT		P42-PWR_CPU_CORE	Change PR196 2.43k to 2.87k	Adjust CPU_CORE load line (2009/12/31)
DVT		P42-PWR_CPU_CORE	Change PR204 8.25k to 10k	Adjust resistor for Imon (2009/12/31)
DVT		P39-PWR_+VTTP	Change PR98 4.99k to 6.98k	Adjust VTT_DIS_Arrandale OCP to 29.73A (2009/12/31)
DVT		P53-PWR_1.5VP/0.75VSP	Change PR132 6.19k to 7.5k	Adjust 1.5V OCP to 21.73A(2009/12/31)
DVT		P52-PWR_1.05VSP/1.8VSP	Change PQ33 from FDS6670 to AO4712	Change design rating(2009/12/31)
DVT		P39-PWR_+VTTP	Change PR98 6.98k to 4.99k	Adjust VTT_DIS_Clarksfield OCP to 20.64A (2009/12/31)
DVT		P55-PWR_GM VGA_CORE	Change PR247 34.8k to 37.4k	Adjust GFX load line (2009/12/31)
DVT		P41-PWR_0.75VSP/1.8VSP	Change PC90 SE025681K80 to SE024681J80	Use same PN (2009/12/31)
DVT		P56-PWR_VGA_COREP	Change PR270 20k to 68k, PC178 0.01U to 0.1U	Adjust Optimus sequence (2010/01/06)
PVT		P41-PWR_0.75VSP/1.8VSP	Remove PR136, Add PR137 0 Ohm	For S3 power saving function (2010/02/03)
PVT		P43-PWR_GM VGA_CORE	Change PC161 to SF000002O00	Change to original type for PVT (2010/02/03)
PVT		P49-PWR_CHARGER	Change PC24,PC25,PC26 4.7U to 10U	For EMI solution(ISN test) (2010/02/03)
PVT		P49-PWR_CHARGER	Add PC107 10U	For EMI solution(ISN test) (2010/02/03)
PVT		P49-PWR_CHARGER	Add PC104,PC105,PC106 10U	For EMI solution(ISN test) (2010/02/03)
PVT		P38-PWR_3VALWP/5VALWP	Change PQ27 from SSMK7002 to DTC115EUA	Use low Vth Transistor (2010/02/03)
PVT		P52-PWR_1.05VSP/1.8VSP	Change PR119 10k to 15.8k	Adjust 1.05V OCP to 8.47A (2010/02/03)

NO DATE	PAGE	MODIFICATION LIST	PURPOSE
Pre MP	P52-PWR_1.05VSP/1.8VSP	Change PR123 316k to 25.5k,PR124 402k to 51.1k	Adjust 1.8V voltage divided resistor (2010/03/07)
Pre MP	P52-PWR_1.05VSP/1.8VSP	Change PU9 from MP2121 to SY8033	MP2121 ESD fail (2010/03/07)
Pre MP	P52-PWR_1.05VSP/1.8VSP	Delete PR125 0 Ohm Change PC85 from 0.1U to 22U Delete PC87 10UF, PC84 0.1U	Change for SY8033 solution(2010/03/07)
Pre MP	P52-PWR_1.05VSP/1.8VSP	Change PC86 10U to 68P	Improve 1.8V transient under shoot(2010/03/07)
Pre MP	P49-PWR_CHARGER	Change PC24,PC25,PC26 10U to 4.7U	10U 0805 size price too high(2010/03/07)
Pre MP	P47-PWR_DCIN/DECTOR	Change PC12 from SE033105Z80 to SE000001380	Change PN(2010/03/07)
Pre MP	P49-PWR_CHARGER	Change PR68 from 53.6k to 24k, PR45 from 0.015 to 0.02 Ohm	Change CP from 90W to 75W(For cost down)(2010/03/07)
Pre MP	P49-PWR_CHARGER	Change PQ6,PQ7 from AO4407A to AO4435	Change MOS reting for 75W adapter(For cost down)(2010/03/07)
Pre MP	P56-PWR_VGA_COREP	Add PR264,PR267 100k	Use 100k resistor to pull high +3VS_DGPU(Set initial VID to P0 state)(2010/03/07)

HW PIR (Product Improve Record)

NWQAA LA-6062P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2009/12/30

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/7	37	Add +5VALW and +5VL for JPIO pin5	For BACK_SENSE detect
2	12/7	46	Change PJ32 to R104 and PJ33 to R144	For discrete BOM structure
3	12/7	25	Remove JLVDS pin10 and pin12 for +LCDVDD_R	3D Panel max. current is 1.5A
4	12/8	45	Combine JTOUCH and JLP to JTPL and remove C648	For ME cost down
5	12/8	13	Add QV2, RV110, RV123 and RV124	For CLK_REQ_VGA# level shifter
6	12/14	25	Add C495 and C496	For RF request
7	12/15	33	Add R258	For OPTIMUS_EN#
8	12/15	34	Add C499	For power team request
9	12/17	45	Remove D19	Move D19 to LS-6061P
10	12/18	38	Reverse JBT pin definition	Due to pin reverse
11	12/18	42	Add RA42	For codec EC_MUTE# issue
12	12/21	41	Change JREAD to Push-push type (R015-211-LM-A)	For PRD update
13	12/21	25	Move LED_PWM and BKOFF#_R to JLVDS pin10 and pin12	For avoiding +LCD_INV short issue
14	12/22	44	Change H7 footprint to "DEBUG_PAD-MB-S"	For debug use
15	12/23	39	Add D24 and Q36 for BT_CTRL	For WLAN & BT combo module
16	12/23	33	Add R461	For CIR_EN#
17	12/24	25	Mount C236 and C268	For ESD request
18	12/24	37	Change JPIO footprint and reverse its pin definition	For ME request
19	12/24	27	Add R145	For U9 ESD damage issue
20	12/24	41	Add F3	For connector short issue
21	12/28	42	Change RA41 to SM01000CY00 (FBMA-10-100505-301T)	For EMI request
22	12/28	25	Remove L1	For 3D panel
23	12/29	42	Change RA1, RA18 and RA20 to SM01000B200	For RF request
24	12/29	25	Change C484 to 100P	For RF request
25	1/6	37	Change C426 to SF000001500	For cost down
26	1/12	38	Change R132 BOM from FLICA@ to FELICA@	For Felica issue
27	1/12	11	Change C218 to SF000002O00	For cost down
28	1/12	8	Change C144 to SF000002Z00	For thermal interfere issue

NWQAA LA-6062P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2 TO 0.3
GERBER-OUT DATE: 2010/02/08

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	1/15	42	Add RA43	For sleep & music on battery mode
2	1/15	46	Change +1.05VS_DGPU to N-MOS	For +1.05VS_DGPU drop issue
3	1/21	43	Add R462	Avoid VR_ON floating
4	1/25	44	Change UG3 to SA000022I00	For LDO issue
5	1/25	45	Change SW2 to @	For ME interfere issue
6	1/27	9	Change CV57, CV58 abd C271 to OS-CON	For cost down
7	2/1	25	Add +LCD_VDD to JLVDS pin18	For CMO 3D Panel
8	2/1	27	Add R208	For AOC monitor issue
9	2/1	43	Change U19 to SA00001J5A0	For KB926 E0 version
10	2/1	39	Add +1.5VS for J3G	For TV tuner MC770A
11	2/1	41	Remove F3	For UC1 ES2 sample
12	2/2	43	Add CAP_RST# to EC	For ESD issue
13	2/3	41	Change RC7 to 33 ohm	For EMI request
14	2/4	42	Remove RA40, add RA44 and RA22	For audio issue
15	2/4	14	Reserve VBIOS ROM	For SW request
16	2/5	32	Swap USB port4 and port8	For customer request
17	2/5	13	Reserve 27MHz crystal	For HDMI issue
18	2/9	40	Change LL1 to 2.2U and Cl13 to 4.7U	For Realtek request
19	2/10	41	Change RC7~RC14 to 22 ohm	For O2 request
20	2/10	27	Remove HDMI common mode choke	For cost down

NWQAA LA-6062P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 1.0
GERBER-OUT DATE: 2010/03/15

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/6	32	Change R390 to 1K	For Optimus sequence
2	3/6	33	Change R59 to 1K	For Optimus sequence
3	3/6	27	Change Q18 and Q19 power to +3VS_DGPU	For GPU power rail
4	3/6	41	Add QC2 and RC16	For O2 B0 workaround
5	3/7	28	Change D13.2 power to +CHGRTC	For RTC issue
6	3/8	32	Add R333 and R334	For Optimus sequence
7	3/8	25	Add BOM structure 3D@ and NO3D@	For 3D SKU PWM
8	3/8	13	Change YV1 to SJ100006R00	For cost down
9	3/11	46	Change C685 to 0603 size	For ME height limit
10	3/11	45	Change H15~H19 to H_3P3	For ME request
11	3/15	45	Remove SW2	For ESD request
12	3/15	42	Change CA9 and CA10 to 1U	For cut-off frequency
13	3/16	42	Change MONO_IN to AGND	For high frequency noise issue

NWQAA LA-6062P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0 TO 2.0
GERBER-OUT DATE: 2010/03/19

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/17	41	Change cardreader to JMB385/389	For customer request
2	3/18	34	Add R49	For CRT wave issue
3	3/19	13	Change LV3 to always stuff	For NVIDIA request
4	3/19	34	Change L12 to 2.2 ohm for Optimus SKU	For CRT wave issue
5	3/22	27	Add D54	For HDMI CEC issue
6	3/24	25	Chane C214 to 1U	For NALAA ESATA performance low issue

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